Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 80111

10-5-19 AN

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Third Semester

Electronics and Communication Engineering

EC 8351 — ELECTRONIC CIRCUITS – I

(Common to Electronics and Telecommunication Engineering)

(Regulation 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define Stability Factor.
2. What are the parameters that the operating point depends upon?
3. Why are common emitter amplifiers more popular?
4. What are the benefits of h-parameters?
5. Write two reasons why a hybrid parameter model is used in small signal analysis.
6. Compare the characteristic of small signal amplifier with large signal amplifier.
7. Why are h-parameters not used at high frequencies?
8. What is meant by gain-bandwidth product?
9. Define ripple factor.
10. Summarize the TUF of HWR and FWR.

PART B — (5 × 13 = 65 marks)

11. (a) What is D.C. load line? How will you select the operating point, explain it using common emitter amplifier characteristics as an example?

Or

(b) With neat diagrams, explain two bias compensation techniques and state its advantages and disadvantages.

12. (a) Show the ac equivalent circuit of a CE amplifier with voltage divider bias and derive the expression for current gain, voltage gain, input impedance, output admittance and overall current gain.

Or

(b) Examine the circuit diagram for a differential amplifier using BJT's. Describe its common mode and differential mode operation.

13. (a) Explain the principle of operation of a JFET amplifier? Derive voltage gain, input and output impedance of common source JFET amplifier with a neat circuit diagram of its small signal equivalent circuit.

Or

(b) Demonstrate the working of MOSFET source follower with its small signal equivalent circuit. Derive its voltage gain, current gain and output impedance.

14. (a) Derive the expression for the short circuit current gain of common emitter amplifier at a high frequency. Define alpha cut-off frequency, beta cut-off frequency and transition frequency and derive their values in terms of the circuit parameters.

Or

(b) (i) Derive the expression for input conductance (g_{be}) and output resistance (r_0) for hybrid — π common emitter transistor model. (6)

(ii) Derive the expression for 3dB bandwidth of CE amplifier considering miller effect. (7)

15. (a) (i) Outline the comparison of half wave and full wave rectifier. (7)

(ii) Summarize the comparison of shunt and voltage regulator. (6)

Or

(b) Demonstrate the design and working of regulated dc power supply.

PART C — (1 × 15 = 15 marks)

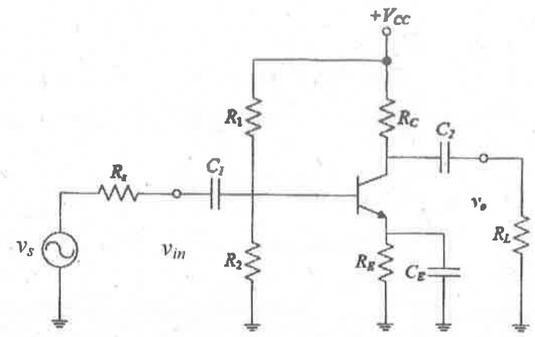
16. (a) Consider the common-emitter BJT amplifier circuit. Assume $V_{CC} = 15, V$ $\beta = 150$, $V_{BE} = 0.7\,V$, $R_E = 1\,k\Omega$, $R_C = 4.7\,k\Omega$, $R_1 = 47\,k\Omega$, $R_2 = 10\,k\Omega$, $R_L = 47\,k\Omega$, Rs = 100 Ω.

(i) Determine the Q-point. (3)

(ii) Sketch the DC load-line. What is the maximum (peak to peak) output voltage swing available in this amplifier? (4)

(iii) Draw the AC equivalent circuit and determine the AC model parameters. (4)

(iv) Find *Rin, Rout, Av, Ai.* (4)



Or

(b) With neat sketch, elaborate the principle, construction and working of different types of switched mode power supply.

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Question Paper Code : 25072

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Third Semester

Electronics and Communication Engineering

EC 8351 — ELECTRONIC CIRCUITS – I

(Common to Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How thermal runaway occurs in a transistor?

2. When does a transistor act as a switch?

3. What is the slope of AC load line?

4. Find CMRR of differential amplifier in dB with differential gain 300 and common mode gain of 0.2.

5. Give the relation between pinch off voltage and drain resistance.

6. How a MOSFET can be used to amplify a time varying voltage?

7. What is the reason for the drop in gain at the low frequency region and at the high frequency region?

8. Define rise time. Give the relationship between bandwidth and rise time.

9. Compare the SMPS with linear power supply.

10. Why capacitor input filter is not suitable for variable loads?

PART B — (5 × 13 = 65 marks)

11. (a) With neat diagrams, explain any two bias compensation techniques and state its advantages and disadvantages.

Or

(b) Explain voltage divider bias method for BJT and derive an expression for stability factors.

12. (a) Examine the circuit diagram for a differential amplifier using BJT's. Describe common mode and differential modes of working.

Or

(b) Analyze the changes in the AC characteristics of a common emitter amplifier when an emitter resistor and an emitter bypass capacitor are incorporated in the design. Explain with necessary equations.

13. (a) Derive voltage gain, input and output impedance of common source JFET amplifier with neat circuit diagram and equivalent circuit.

Or

(b) (i) Bring out the small signal parameters of MOSFET. (7)

(ii) Construct the small signal equivalent circuit for common source NMOS and explain. (6)

14. (a) Derive the expressions for the short circuit current gain of common emitter amplifier at high frequency.

Or

(b) Develop the high frequency equivalent circuit of a MOSFET from its geometry and derive the expression for short circuit current gain in the common source configuration.

15. (a) Discuss the working of centre tapped full wave rectifier with neat diagram. Also derive the expression for the rectification efficiency, ripple factor, transformer utilization factor and peak factor of full wave rectifier.

Or

(b) Elucidate the process and procedure of troubleshooting and fault analysis in electronic circuits.

PART C — (1 × 15 = 15 marks)

16. (a) Draw and explain the characteristics of BiCMOS cascode amplifier and derive the expression for voltage gain. Also discuss graphically the amplification process of a BiCMOS amplifier circuit.

Or

(b) Explain the operation of cascade amplifier and derive voltage gain, overall input resistance, overall current gain and output impedance.

Reg. No. :

Question Paper Code : 90174

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER / DECEMBER 2019

Third Semester

Electronics and Communication Engineering

EC8351 – ELECTRONIC CIRCUITS – I

(Common to Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Mention any two biasing circuits of BJT.
2. Find the operating region of n-channel MOSFET with V_{GS} = 1V, V_t = 0.8 V and V_{DS} = 1.2 V.
3. What is meant by base width modulation ?
4. What is the overall gain of 3-stage cascaded amplifier, having individual gain of amplifier is 20 V/V ?
5. Derive the output resistance of CS amplifier.
6. What are the features of BiCMOS circuits ?
7. List the effect of capacitors that effect frequency response of BJT.
8. Draw the high frequency equivalent circuit of MOSFET.
9. Derive ripple factor of full wave bridge rectifier.
10. Define load regulation of regulators.

PART – B (5×13=65 Marks)

11. a) For the circuit in Fig. 1 draw DC load line and find the Q-point. h_{fe} = 150, V_{cc} = 15 V, R_C = 2100 Ω, R_1 = 566 KΩ, R_2 = 120 KΩ, $V_{BE\text{-}on}$ = 0.7V, I_B = 10 μA.

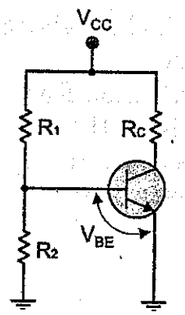

Fig. 1

(OR)

b) For the circuit in Fig. 2, find the drain current and drain to source voltage. MOSFET is operating in saturation region.

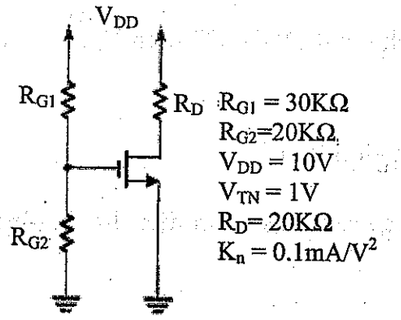

Fig. 2

12. a) Derive gain of common emitter amplifier circuits with R_E bypassed by C_E, draw the small signal equivalent circuit.

(OR)

b) With equivalent circuit, derive the input impedance of Bootstrapped Darlington amplifier.

13. a) Derive gain, input and output impedance of common drain amplifier with neat circuit diagram and equivalent circuit.

(OR)

b) Derive CMRR and explain the operation of differential pair using FET with circuit diagram.

14. a) **Derive f_α and f_β of a frequency response of BJT.**

(OR)

b) **Derive expressions for high frequency analysis of CE and MOSFET CS amplifiers.**

15. a) **Draw the circuit of shunt voltage regulator and explain its operation.**

(OR)

b) **Explain the functional blocks of Switched Mode Power Supply (SMPS).**

PART – C (1×15=15 Marks)

16. a) **For the circuit shown in Fig. 3, identify the amplifier configuration, find the input and output resistance V_{BE} = 0.7V, V_A = 80 V, β = 100.**

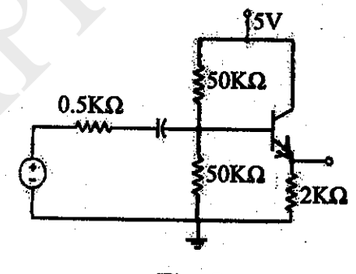

Fig. 3

(OR)

b) **Determine the Unity gain bandwidth, Miller capacitance and cut-off frequency of Common source MOSFET circuit. V_T = 1V, V_{GS} = 3V, K_n = 0.25mA/V², R_L = 10 KΩ, C_{gd} = 0.04pF, c_{gs} = 0.2 pF.**

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