DHANALAKSHMI SRINIVASAN ENGINEERING COLLEGE, PERAMBALUR - 621212

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC6601 - VLSI DESIGN

QUESTION BANK

UNIT I - MOS TRANSISTOR PRINCIPLE

PART – A

1. What is Channel-length modulation? *(Apr/May-17, Apr/may-16)*

The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied $V_{DS,}$ increasing V_{DS} causes the, depletion region at the drain junction to grow, reducing the length of the effective channel.

2. What is Latch – up? How it can be prevented *(Apr/may-16)*

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between V_{DS} and V_{SS} with disastrous results. Careful control during fabrication is necessary to avoid this problem.

- ✓ An increase in substrate doping levels with a consequent drop in the value of Rpsubs.
- ✓ Reducing Rnwell by control of fabrication parameters and ensuring a low contact resistance to VDD.
- ✓ By introducing guard rings.

3. What is body effect in MOSFETs? Or Define body bias effect. *(Nov/Dec-16, Nov/Dec-13)*

The threshold voltage VT is not a constant with respect to the voltage difference between the substrate and the source of the MOS transistor. This effect is called the body effect or substrate bias effect.

4. Define propagation delay of CMOS Inverter. *(Apr/May-17)*

The inverter propagation delay (t_P) is defined as the average of the low-to-high (t_{PLH}) and the high-to low (t_{PHL}) propagation delays: $tp = \frac{t_{PHL} + t_{PLH}}{2}$.

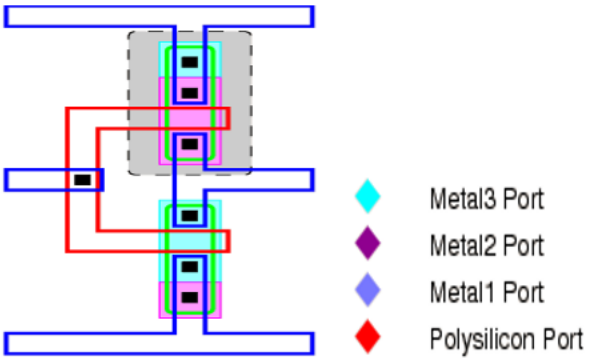
Propagation delays t_{PLH} and t_{PHL} are defined as the times required for output voltage to reach the middle between the low and high logic levels, i.e. 50 % of V_{DD} in our case of CMOS logic.

5. Define the Lambda design rules used for layout? *(May/Jun-13, Apr/may-15)*

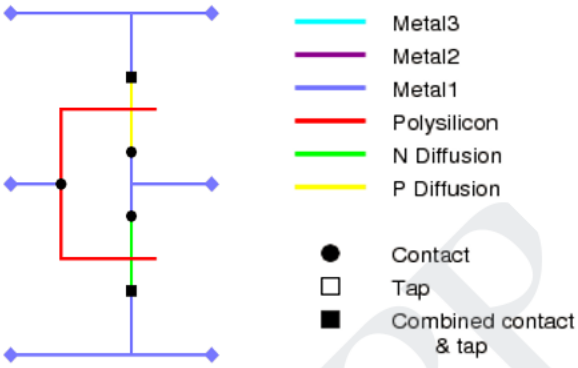
Lambda rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

6. Draw the stick diagram and layout for CMOS Inverter. ***(Nov/Dec-16)***

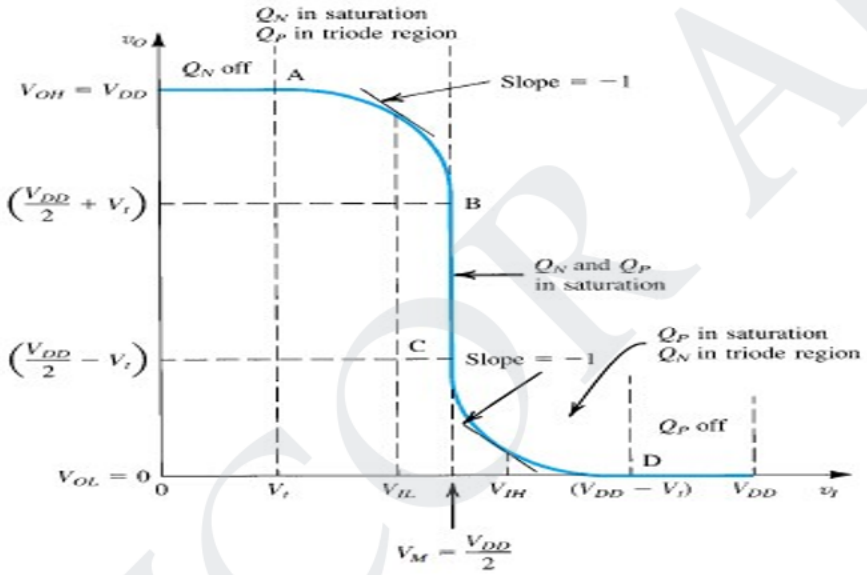
Layout for CMOS Inverter:



Stick diagram for CMOS Inverter:



7. Draw the DC transfer characteristics of CMOS inverter. ***(Apr/may-15, Nov/Dec-13)***



8. What is the need for design rules? ***(Nov/Dec-14)***

Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. Design rules are used to produce workable mask layouts from which the various layers in silicon will be formed or patterned.

9. Define any two layout design rules. ***(Nov/Dec-15, May/Jun-14)***

Micron design rule:

Micron rules specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.

Lambda design rule:

Lambda rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

10. Why nMOS transistor is selected as pull down transistor. *(Nov/Dec-17)*

When high voltage is given at the input nMOS is turned ON. So the output is pulled down to Vss. An NMOS device pulls the output all the way down to GND, while a PMOS lowers the output no further than |VTp| — the PMOS turns off at that point, and stops contributing dis-charge current. NMOS transistors are hence the preferred devices in the PDN.

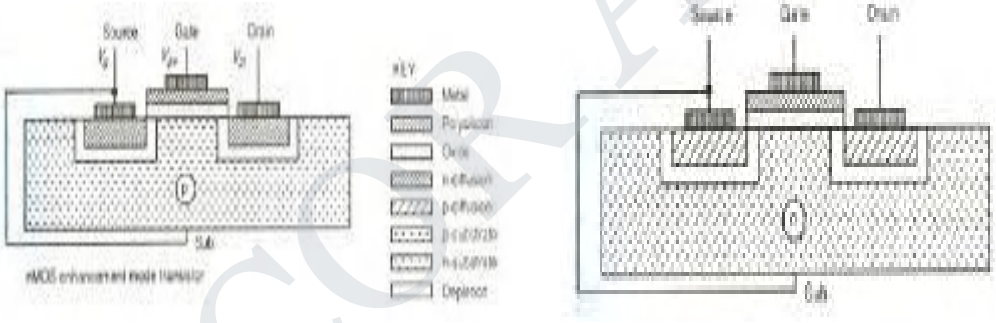
PART –B (Answers as Hint)

1. Describe the equation for source to drain current in the three regions of operation of a MOS transistor and draw the VI characteristics. *(May/Jun-16, Nov/Dec-14, May/Jun-13)*

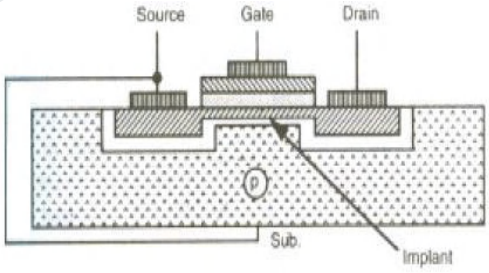
- **<u>Basic MOS Transistors operation: *(4 Marks)*</u>**

We have two types of FETs. They are Enhancement mode and depletion mode transistor. Also we have PMOS and NMOS transistors.

(i) In **Enhancement mode transistor** channel is going to form after giving a proper positive gate voltage. We have NMOS and PMOS enhancement transistors.



(ii) In **Depletion mode transistor** channel will be present by the implant. It can be removed by giving a proper negative gate voltage. We have NMOS and PMOS depletion mode transistors.



- **<u>Three regions of operation of a MOS transistor *(4 Marks)*</u>**

a) Vgs > Vt Vds = 0 Since Vgs > Vt and Vds = 0 the channel is formed but no current flows between drain and source.

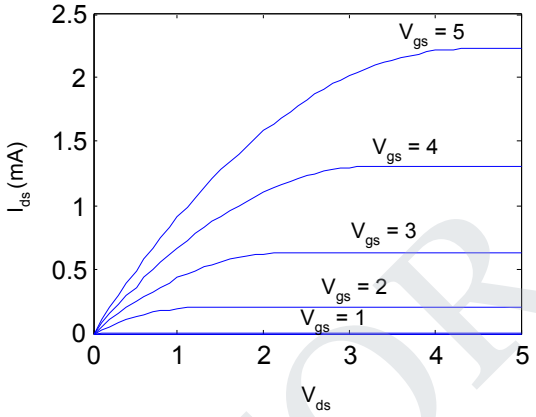
b) Vgs > Vt Vds < Vgs - Vt This region is called the non-saturation Region or linear region where the drain current increases linearly with Vds. When Vds is increased the drain side becomes more reverse biased and the channel starts to pinch. This is called as the pinch off point.

c) Vgs > Vt Vds > Vgs - Vt This region is called Saturation Region where the drain current remains almost constant. Even if the Vds is increased more and more, the increased voltage gets dropped in the depletion region leading to a constant current. The typical threshold voltage for an enhancement mode transistor is given by Vt = 0.2 * Vdd.

- **Derivation: *(6 Marks)***

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{Cutoff} \\ \beta\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{Linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{Saturation} \end{cases}$$

- **Draw the VI characteristics *(2 Marks)***



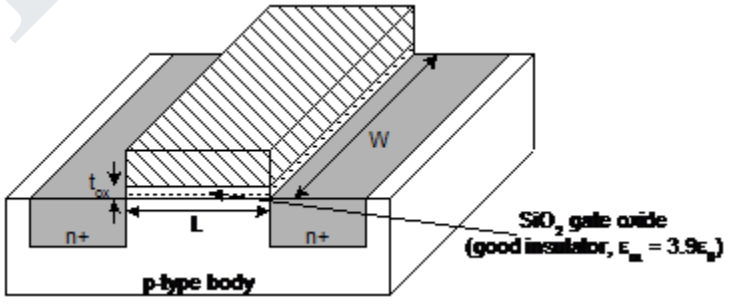
2. Explain in detail of C-V characteristics of MOSFET. *(Nov/Dec-15)*

- **Simple MOS capacitance model *(4 Marks)***

Approximate channel as connected to source

$C_{gs} = e_{ox}WL/t_{ox} = C_{ox}WL = C_{permicron}W$

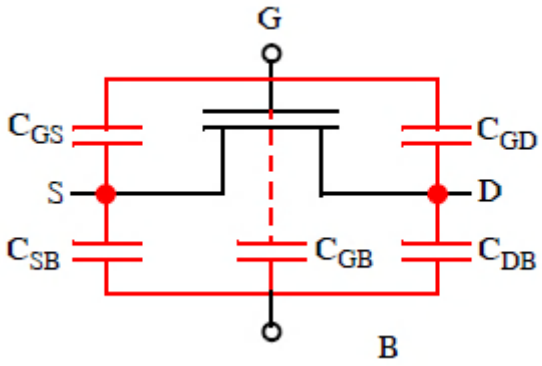
$C_{permicron}$ is typically about 2 fF/mm



- **Detailed MOS capacitance model *(4 Marks)***

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Linear	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

- **MOS device capacitance *(4 Marks)***



$C_{GS} = C_{gs} + C_{gsO}$
$C_{GD} = C_{gd} + C_{gdO}$
$C_{GB} = C_{gb}$
$C_{SB} = C_{Sdiff}$
$C_{DB} = C_{Ddiff}$

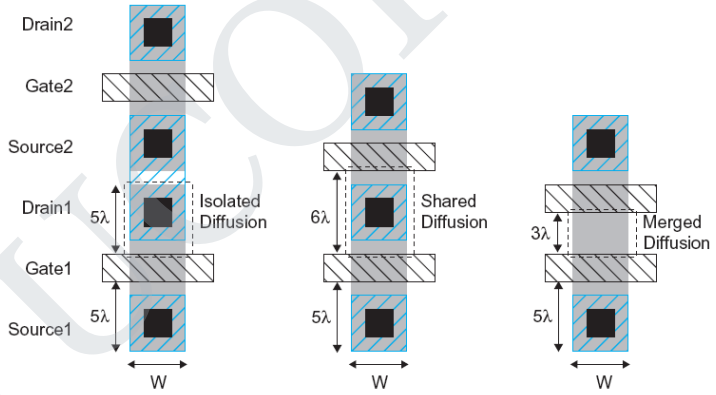
- **Diffusion capacitance *(4 Marks)***

C_{sb}, C_{db}

Undesirable, called *parasitic* capacitance

Capacitance depends on area and perimeter

- ✓ Use small diffusion nodes
- ✓ Comparable to C_g for contacted diff
- ✓ ½ C_g for un contacted
- ✓ Varies with process



3. Discuss the mathematical equations that can be used to model the drain current and diffusion capacitances of MOS transistor. *(Nov/Dec-16)*

- **Drain current derivation: *(8 Marks)***

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{Cutoff} \\ \beta\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{Linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{Saturation} \end{cases}$$

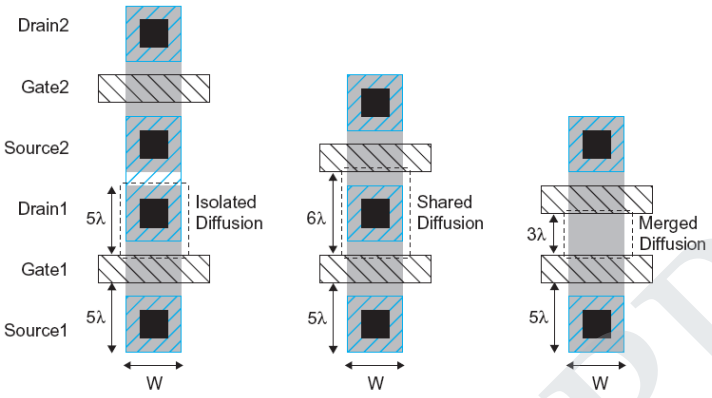
- **Diffusion capacitances of MOS transistor: *(8 Marks)***

C_{sb}, C_{db}

Undesirable, called *parasitic* capacitance

Capacitance depends on area and perimeter

- ✓ Use small diffusion nodes
- ✓ Comparable to C_g for contacted diff
- ✓ ½ C_g for un contacted
- ✓ Varies with process



4. Explain the electrical properties of MOS transistor in detail. *(Nov/Dec-17, Nov/Dec-13)*

- **<u>Ideal IV characteristics *(4 Marks)*</u>**

  Three regions of operation

  - ✓ Cutoff *(1 Mark)*
  - ✓ Linear *(1 Mark)*
  - ✓ Saturation *(1 Mark)*
  - ✓ Equation *(1 Mark)*
- **<u>Non ideal characteristics *(4 Marks)*</u>**
  - High Field Effects *(1 Mark)*
    - ✓ Mobility Degradation
    - ✓ Velocity Saturation
  - Channel Length Modulation*(1 Mark)*
  - Threshold Voltage Effects*(1 Mark)*
    - ✓ Body Effect
    - ✓ Drain-Induced Barrier Lowering
    - ✓ Short Channel Effect
  - Leakage*(1 Mark)*
    - ✓ Subthreshold Leakage
    - ✓ Gate Leakage
    - ✓ Junction Leakage
- **<u>C-V characteristics *(4 Marks)*</u>**
  - ✓ Simple MOS capacitance model *(1 Mark)*
  - ✓ Detailed MOS capacitance model *(4 Mark)*
  - ✓ MOS device capacitance *(4 Mark)*
  - ✓ Diffusion capacitance *(4 Mark)*

5. Explain the need of scaling, scaling principles and fundamental units of CMOS inverter. *(Nov/Dec-17, Apr/May-17)*

- **Need of scaling: *(8 Marks)***

  Definition: *(2 Marks)*

  Proportional adjustment of the dimensions of an electronic device while maintaining the electrical properties of the dev ice, result in a dev ice either *larger* o r *smaller* than the u n -sea led device.

  Factors: *(6 Marks)*

  - ✓ Consider 2 scaling factors, α and β
  - ✓ 1/ β is the scaling factor for VDD and oxide thickness D
  - ✓ 1/ α is scaling factor for all other linear dimensions
  - ✓ We will assume electric field is kept constant

  It is important that you understand how the following parameters are affected by scaling

  - ✓ Gate Area, Gate Capacitance per unit area, Gate Capacitance
  - ✓ Charge in Channel, Channel Resistance
  - ✓ Transistor Delay, Maximum Operating Frequency
  - ✓ Transistor Current, Switching Energy
  - ✓ Power Dissipation Per Gate (Static and Dynamic)
  - ✓ Power Dissipation Per Unit Area
  - ✓ Power - Speed Product

- **Scaling Principles and Fundamental units: *(8 Marks)***

  The Reliability Bathtub Curve, Its Origin and Implications

  - ✓ Key Reliability Functions and Their Use in Reliability Analysis
  - ✓ Defect Screening Techniques and Their Effectiveness
  - ✓ Accelerated Testing and Estimation of Useful Operating Life
  - ✓ Reliability Data Collection and Analysis in Integrated Circuits
  - ✓ Past Technology Scaling Trends
  - ✓ Forward Looking Projections with a Focus on Examining and Understanding of the Impact on VLSI Reliability
  - ✓ Power Density Trends: Operating temperature, activation energies for dominant VLSI failure mechanisms, and reliability impact
  - ✓ Reliability Strategies In Fables Environments

6. Discuss the principle of constant field and lateral scaling. And write the effects of the above scaling methods on the device characteristics. *(May/Jun-16, Nov/Dec-15)*

- **Constant field or Full scaling:*(8 Marks)***

Definition: *(2 Marks)*

All dimensions scaled by same factors keeping the electric field as constant.

Explanation: *(2 Marks)*

- ✓ All the lengths (L G, Z, dOX) and voltages (VDS, VGS, Vth) are scaled by same factor k
- ✓ Electric field unchanged
- ✓ Punch through effect
- ✓ Sol: Increase doping of acceptor by same factor, k (Scaling of Depletion widths)

Effects of scaling: *(4 Marks)*

The effects of constant field scaling on MOS device performance such as gate oxide capacitance per unit area, transconductance, drain current, power dissipation, and power dissipation density are shown from equations (1) – (6).

Gate oxide capacitance per unit area, $C'ox = \varepsilon ox/t'ox$

$= S. \varepsilon ox/tox$

$= S.Cox$ ----------(1)

Transconductance, $k'n = \mu n.C'ox.W'/L' = S. kn$ ----------(2)

Drain current, $I'D (lin) = k'n/2.[2.(V'GS-V'TH).V'DS – V'^2DS]$

$= S. kn/2. 1/S^2.[2.(VGS-VTH).VDS – V^2DS]$

Hence, $I'D (lin) = ID (lin)/S$ ----------(3)

$I'D (sat) = k'n/2. (V'GS-V'TH)^2$

$= S. kn/2. 1/S^2. (VGS-VTH)^2$

Hence, $I'D (sat) = ID (Sat)/S$ ----------(4)

Power dissipation, $P' = I'D . V'DS$

$= 1/S^2 . ID . VDS$

Hence, $P' = P/S^2$ ----------(5)

Power dissipation density, $P'_d = P'/ (W'. L') = P_d$ ----------(6)

- **Lateral scaling or General scaling: *(8 Marks)***

Definition: *(2 Marks)*

Gate length is scaled. It is applied when dimensions and voltages are scaled independently using two variables as S & U.

Explanation: *(2 Marks)*

Effects of scaling: *(4 Marks)*

The effects of constant voltage scaling on MOS device performance such as gate oxide capacitance per unit area, transconductance, drain current, power dissipation, and power dissipation density are shown from equations (7) – (12).

Gate oxide capacitance per unit area, $C'ox = \varepsilon ox/t'ox$

$= S. \varepsilon ox/tox$

$= S.Cox$ ----------(7)

Transconductance, $k'n = \mu n.C'ox.W'/L' = S. kn$ ----------(8)

Drain current, $I'_D (lin) = k'n/2. [2.(V'_{GS}-V'_{TH}).V'_{DS} – V'^2_{DS}]$

$= S. kn/2. [2.(V_{GS}-V_{TH}).V_{DS} – V^2_{DS}]$

Hence, $I'_D (lin) = S. ID (lin)$ ----------(9)

$I'_D (sat) = k'n/2. (V'_{GS}-V'_{TH})^2$

$= S. kn/2. (V_{GS}-V_{TH})^2$

Hence, $I'_D(sat) = S. I_D(Sat)$ ----------(10)

Power dissipation, $P' = I'_D . V'_{DS}$

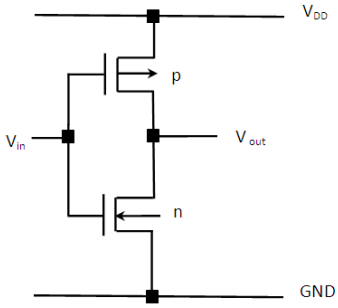
$= S. I_D . V_{DS}$

Hence, $P' = S. P$ ----------(11)

Power dissipation density, $P'd = P'/ (W'. L') = S^3 . Pd$ ----------(12)

7. **Draw and explain the D.C and transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation.** ***(Apr/May-17, May/Jun-16, Apr/May-15, Nov/Dec-15, May/Jun-14, May/Jun-13, Nov/Dec-12)***

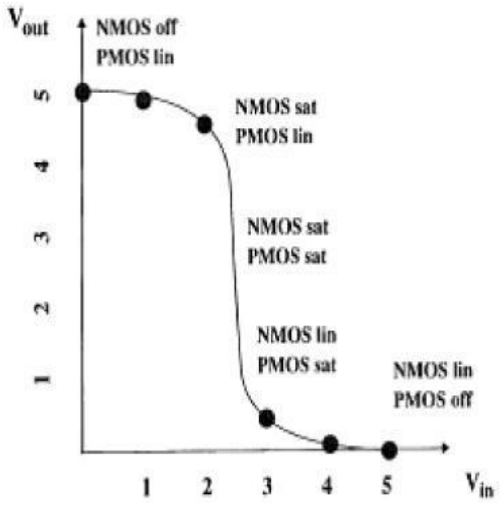
- **CMOS inverter diagram** ***(2 Marks)***

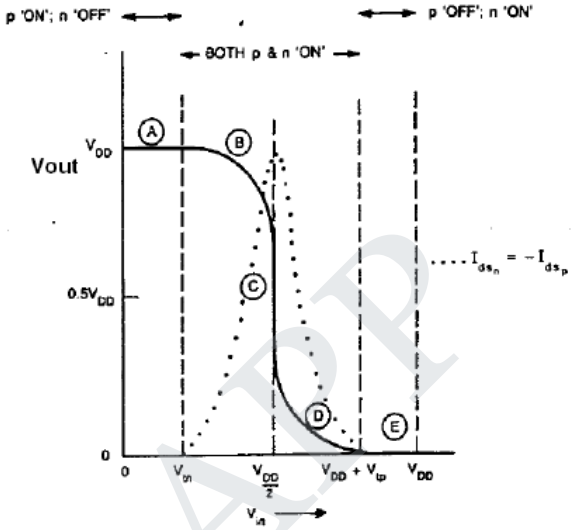


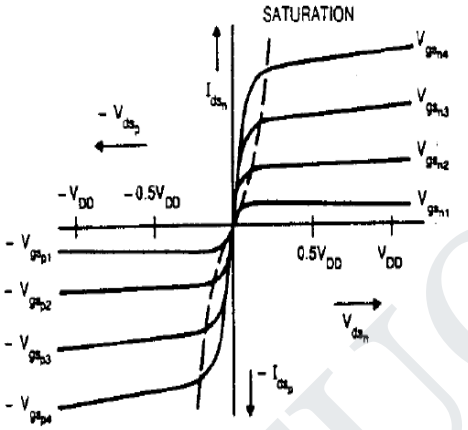
- **Explanation:** ***(6 Marks)***

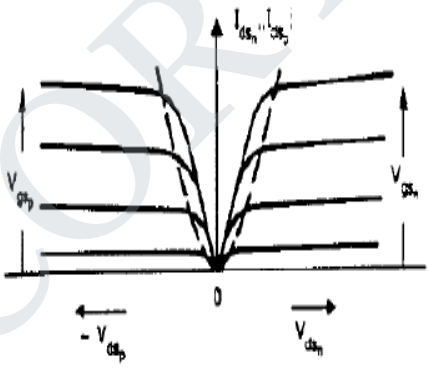
A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal. The operation of the CMOS inverter can be divided into five regions indicated.

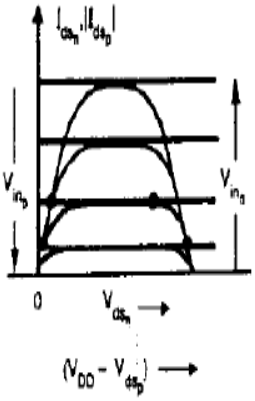
MOSFET	Condition on MOSFET	State of MOSFET
NMOS	Vgs<Vtn	OFF
NMOS	Vgs>Vtn	ON
PMOS	Vsg<Vtp	OFF
PMOS	Vsg>Vtp	ON











- **Regions with formula:** ***(8 Marks)***

Region A: P device is OFF and n device is ON. Vout=VDD.

Region B: PMOS is linear region and NMOS is saturation region.

Region C: Both n and p transistors are in saturation region.

Region D: PMOS is saturation region and NMOS is linear region.

Region E: The output in this region is zero because the P device is OFF and n device is ON.

REGION	CONDITION	p-DEVICE	n-DEVICE	OUTPUT
A	$0 \leq V_{in} \leq V_{tn}$	linear	cut-off	$V_0 = V_{DD}$
B	$V_{tn} \leq V_{in} < \frac{V_{DD}}{2}$	linear	saturated	$*V_0 = (V_{in} + 1) - \sqrt{15 - 6V_{in}}$
C	$V_{in} = \frac{V_{DD}}{2}$	saturated	saturated	$V_0 \neq f(V_{in})$
D	$\frac{V_{DD}}{2} < V_{in} \leq V_{DD} - V_{tp}$	saturated	linear	$*V_0 = (V_{in} - 1) - \sqrt{6V_{in} - 15}$
E	$V_{in} \geq V_{DD} - V_{tp}$	cut-off	linear	$V_0 = 0$

8. (i) Explain in detail about the body effect and its effect in MOS device. ***(May/Jun-16, May/Jun-13)***

- **Definition:** ***(2 Marks)***

  Body effect refers to the change in the transistor threshold voltage (VT) resulting from a voltage difference between the transistor source and body. Because the voltage difference between the source and body affects the VT, the body can be thought of as a second gate that helps determine how the transistor turns on and off.

- **Equations:** ***(6 Marks)***

  V_{sb} affects the charge required to invert the channel

  - Increasing V_s or decreasing V_b increases V_t $\quad V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$

  f_s = *surface potential* at threshold $\quad \phi_s = 2v_T \ln\frac{N_A}{n_i}$

  - Depends on doping level N_A
  - And intrinsic carrier concentration n_i

  γ = *body effect coefficient* $\quad \gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$

  For small source-to-body voltage, treat as linear

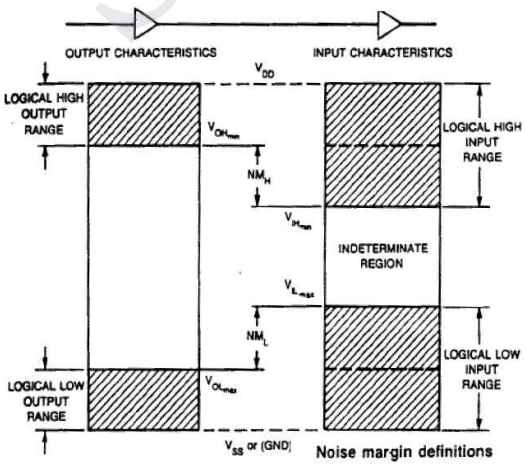
$$V_t = V_{t0} + k_\gamma V_{sb} \qquad k_\gamma = \frac{\gamma}{2\sqrt{\phi_s}} = \frac{\sqrt{\frac{q\varepsilon_{si}N_A}{v_T \ln\frac{N_A}{n_i}}}}{2C_{ox}}$$

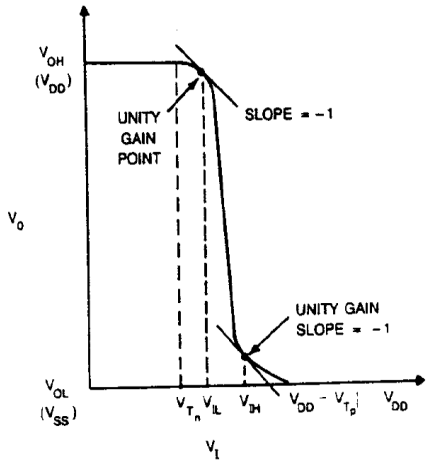
(ii) Derive the noise margins for CMOS inverter. ***(Nov/Dec-16)***

Definition and Types: ***(4 Marks)***

Noise Margin: Noise margin is a parameter related to input output characteristics. It determines the allowable noise voltage on the input so that the output is not affected. We will specify it in terms of two things: LOW noise margin HIGH noise margin.

Diagram and Explanation: ***(6 Marks)***





LOW noise margin: is defined as the difference in magnitude between the maximum Low output voltage of the driving gate and the maximum input Low voltage recognized by the driven gate.
NML=|VILmax – VOLmax|

HIGH noise margin: is defined difference in magnitude between minimum High output voltage of the driving gate and minimum input High voltage recognized by the receiving gate.
NMH=|Vohmin – VIHmin|

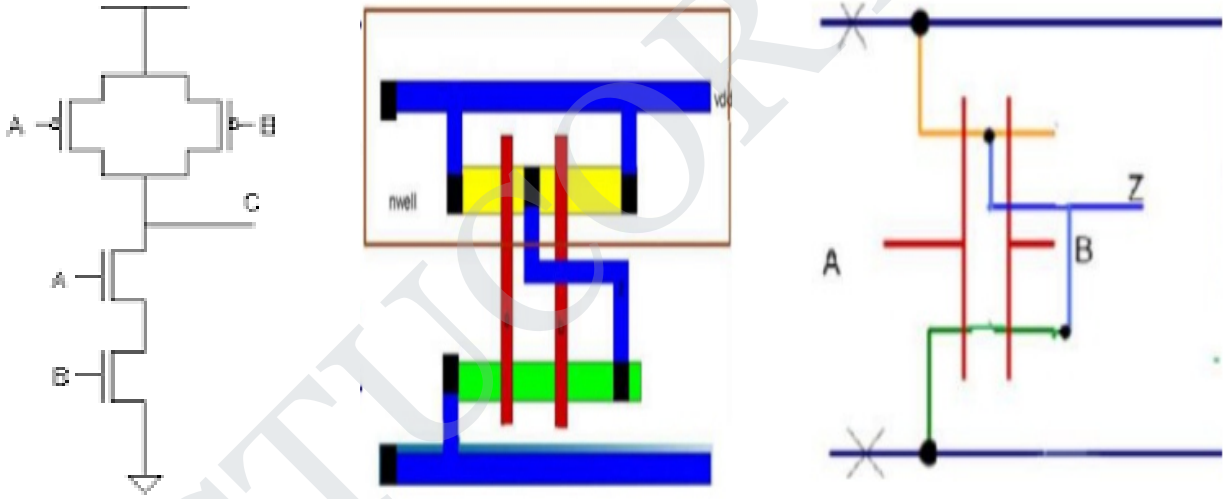
9. **(i) Write the layout design rules and Draw the layout diagram for NAND and NOR gate.** ***(Nov/Dec-17, Apr/May-17)***

- **Design Rules:** ***(4 Marks)***

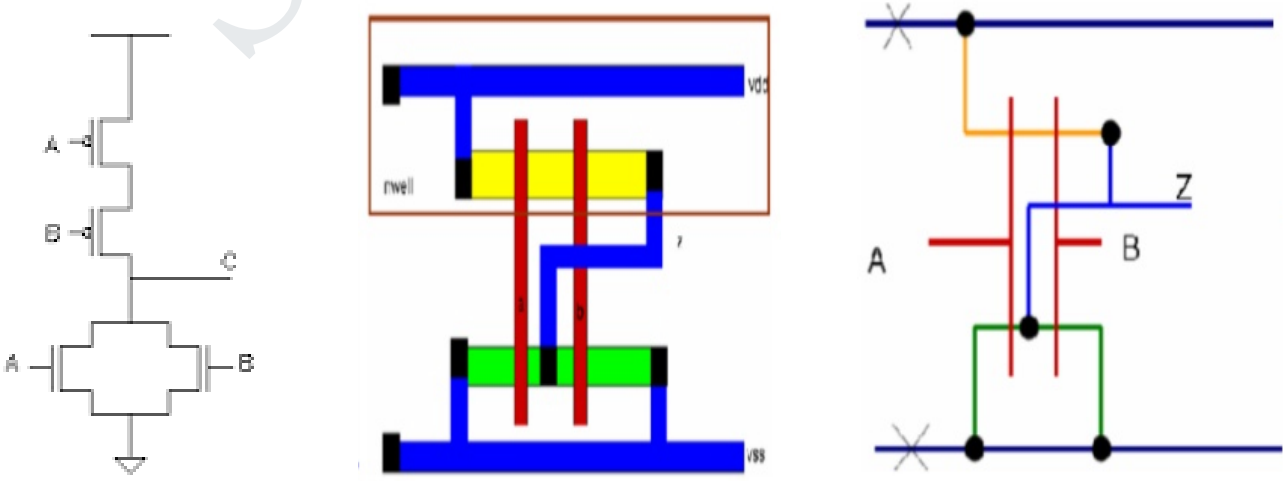
Design rules represent a tolerance that ensures high probability of correct fabrication - rather than a hard boundary between correct and incorrect fabrication.

- ✓ Micron design rule *(1 Mark)*
- ✓ Lambda design rule*(1 Mark)*

- **Layout diagram for NAND gate:** ***(2 Marks)***

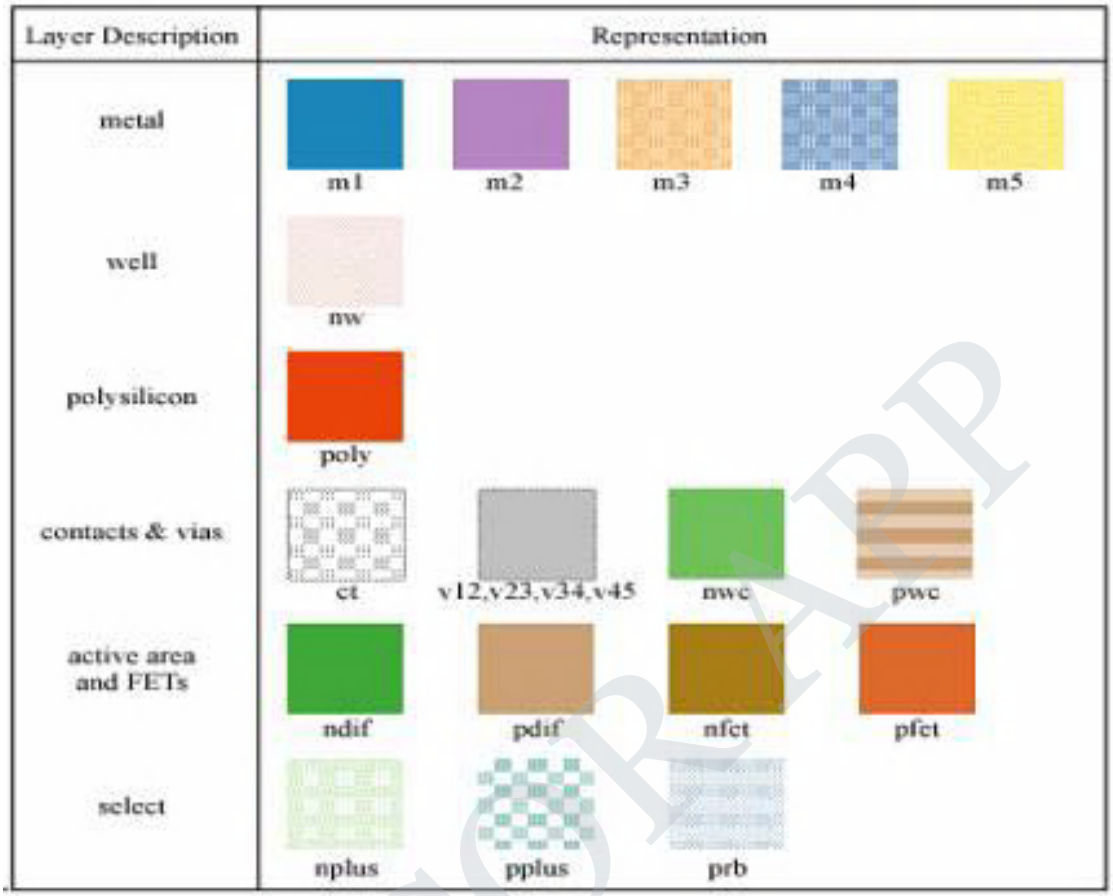


- **Layout diagram for NOR gate:** ***(2 Marks)***

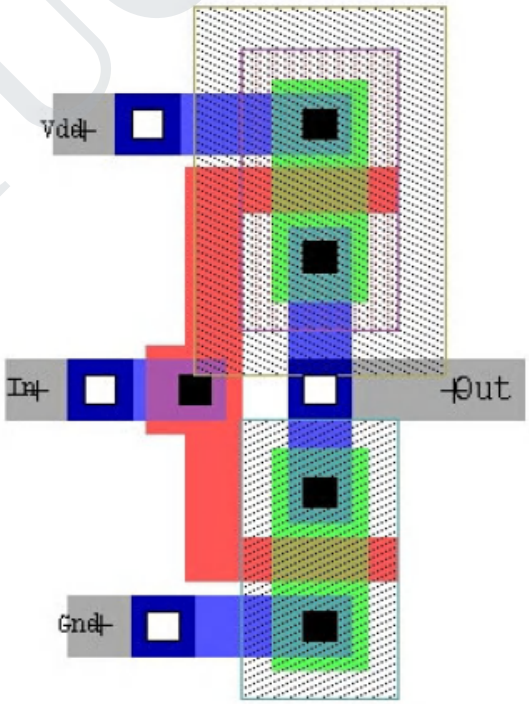


(ii) Discuss in detail with a neat layout, the design rules for a CMOS inverter. *(Nov/Dec-16)*

- **Layout rules: *(4 Marks)***



- **CMOS inverter: *(4 Marks)***

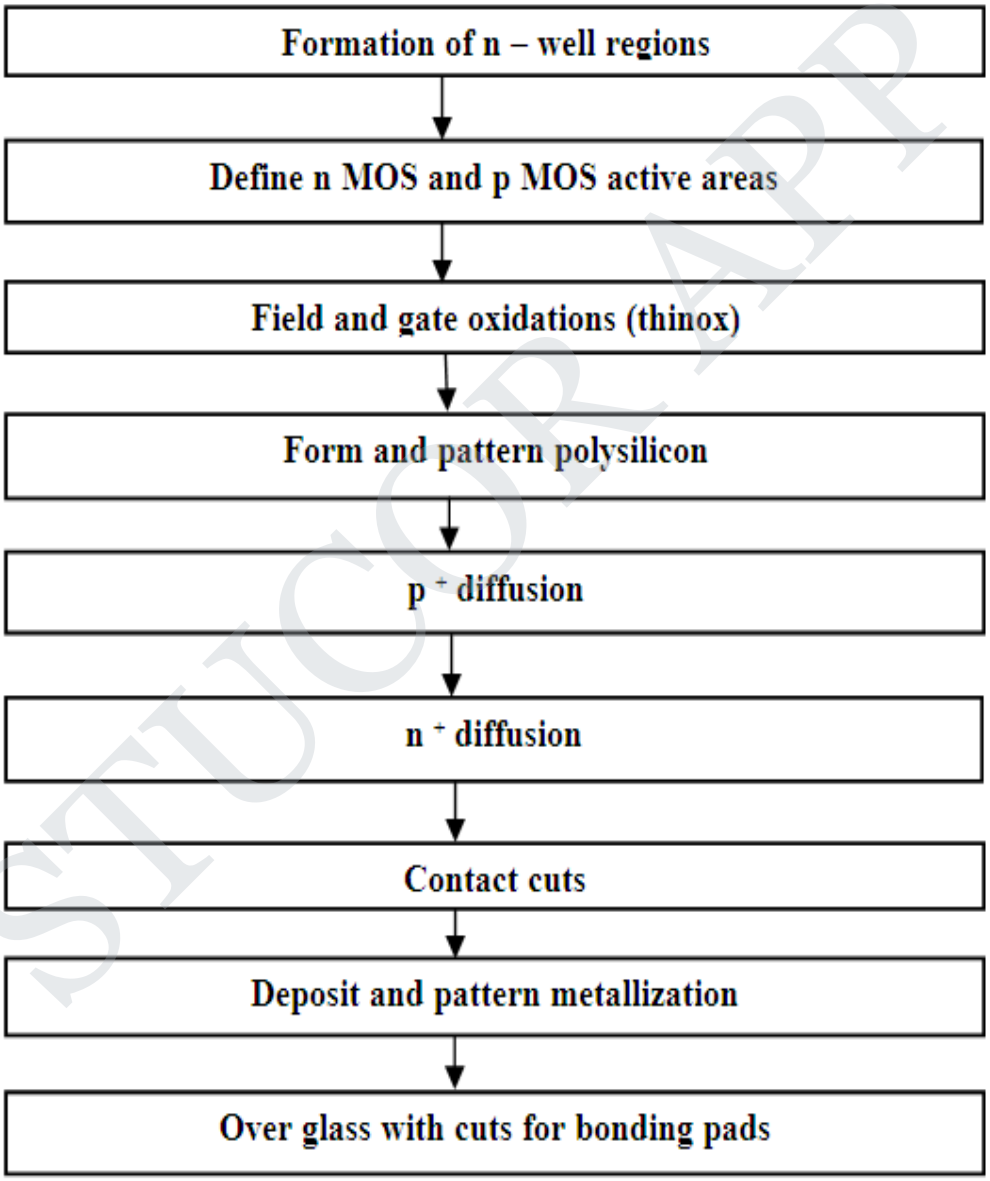


10. Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. ***(Nov/Dec-16, Apr/May-15, Nov/Dec-12)***

- **Definition:** ***(2 Marks)***

The n-well process is that it can be fabricated on the same process line as conventional n MOS. n –well CMOS circuits are also superior to p-well because of the lower substrate bias effects on transistor threshold voltage and inherently lower parasitic capacitances associated with source and drain regions.

- **Explanation of each steps:** ***(14 Marks)***



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC6601 - VLSI DESIGN

QUESTION BANK

UNIT II - COMBINATIONAL LOGIC CIRCUITS

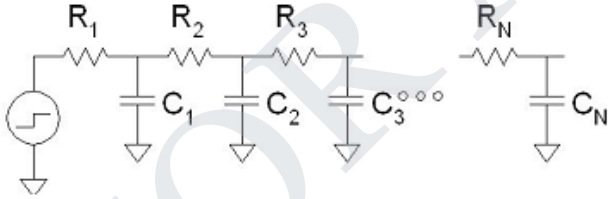
PART –A

1. What is Elmore's Constant? Give Elmore delay expression for propagation delay of an inverter. ***(Nov/Dec-17, Apr/may-17, Apr/may-16)***

It is an analytical method used to estimate the RC delay in a network. Elmore delay model estimates the delay of a RC ladder as the sum over each node in the ladder of the resistance Rn-1 between that node and a supply multiplied by the capacitor on the nodes.

$$t_{pd} \approx \sum_{\text{nodes } i} R_{i\text{-to-source}} C_i$$

$$= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N$$



2. State the advantages of transmission gate. ***(Apr/may-17)***

- Multiplexing element of path selector
- A latch element
- An unlock switch
- Act as a voltage controlled resistor connecting the input and output.

3. Why single phase dynamic logic structure cannot be cascaded? Justify. ***(Apr/may-16)***

The cascading of dynamic logic from one gate to other gives problem. The precharge "1" state of the first gate causes the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, thus there is no recovery from this error.

4. What do you meant by design margin? ***(Apr/may-14)***

The additional performance capability above required standard basic system parameters that may be specified by a system designer to compensate for uncertainties is called design margin. Design margin required as there are three sources of variation- two environmental and one manufacturing.

5. List out the sources of static and dynamic power consumption. Or Define power dissipation. State the types of power dissipation. ***(Nov/Dec-17, Nov/Dec-16, Apr/may-15, Nov/Dec-13)***

- ***Static dissipation*** due to leakage current or other current drawn continuously from the power supply.
- ***Dynamic dissipation*** due to Switching transient current, Charging and discharging of load capacitances.

Types of Power dissipation:

There are three types of power dissipation. They are

- Static power dissipation. P_s= leakage power * supply voltage.
- Dynamic power dissipation. P_d= = $C_L V^2_{dd} f_{clk}$
- Short circuit power dissipation P_{sc}= = $I_{mean} * V_{dd}$

6. Define scaling. What are the advantages of scaling? List different types of scaling. *(Apr/may-15, Nov-Dec-13, Nov/Dec-11)*

Proportional adjustment of the dimensions of an electronic device while maintaining the electrical properties of the device, results in a device either larger or smaller than the unscaled device.

Types:

- ✓ Full scaling (or) constant field scaling
- ✓ Fixed voltage scaling
- ✓ General scaling (or) Lateral scaling

Advantages:

- ✓ Greater device density
- ✓ Higher speed
- ✓ Reduced power consumption
- ✓ Improved performance due to reduced capacitance

7. What are factors that cause static power dissipation in CMOS circuits? *(Nov/Dec-12)*

Power dissipation due to leakage current when the idle is called the static power dissipation. Static power due to

- Sub – threshold conduction through OFF transistors
- Tunneling current through gate oxide
- Leakage through reverse biased diodes
- Contention current in radioed circuits.

8. Write short notes on CMOS transmission gate logic. *(Apr/May-11)*

The circuit constructed with the parallel connection of PMOS and NMOS with shorted drain and source terminals. The gate terminal uses two select signals s and s' when s is high than the transmission gates pass the signal on the input. The main advantage of transmission gate is that it eliminates the threshold voltage drop.

9. What are the methods to reduce dynamic power dissipation?

- Reducing the product of capacitance and its switching frequency.
- Eliminate logic switching that is not necessary for computation.
- Reduce activity factor Reduce supply voltage

10. List various sources of leakage currents?

Various source of leakage currents are listened below:

I1=Reverse-bias p-n junction diode leakage current.

I2=band-to-band tunneling current

I3=Subthreshold leakage current

I4=Gate oxide tunneling current

I5=Gate current due to hot carrier junction

I6=Channel punch through

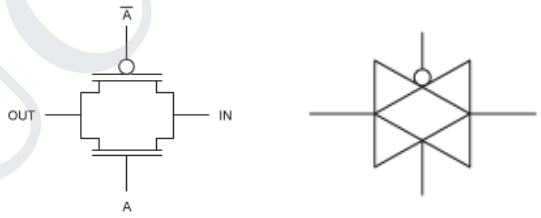
I7=Gate induced drain leakage current

PART – B (Answers as Hint)

1. (i) What is transmission gate? Explain the use of transmission gate. *(Apr/May-17)*

- **Definition: *(4 Marks)***

It is a parallel combination of pmos and nmos transistor with the gates connected to a complementary input. After looking into various issues of pass transistors we will come back to the TGs again.



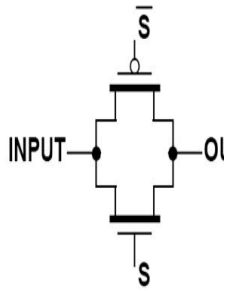
- **Use of transmission gate: *(4 Marks)***
  - ✓ Electronic switch
  - ✓ Analog multiplexer
  - ✓ Logic circuits
  - ✓ Negative voltages

(ii) Discuss in detail the principle & characteristics of CMOS transmission gate. *(Nov/Dec-17, May/Jun-16)*

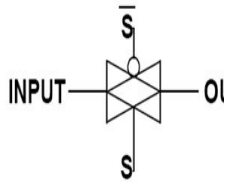
- **Principle: *(4 Marks)***
  - ✓ By combining an nMOS and a pMOS transistor in parallel, we obtain a switch that turns on when a 1 is applied to *g*.

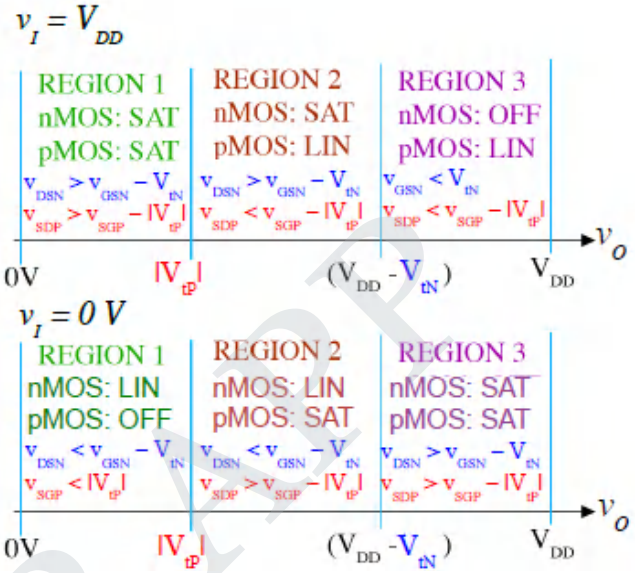
- ✓ In which 0s and 1s are both passed in an acceptable fashion. We term this is a *transmission gate*.
- ✓ In a circuit where only a 0 or a 1 has to be passed, the appropriate transistor (n or p) can be deleted, reverting to a single nMOS or pMOS device.

CMOS TRANSMISSION GATE (SWITCH)

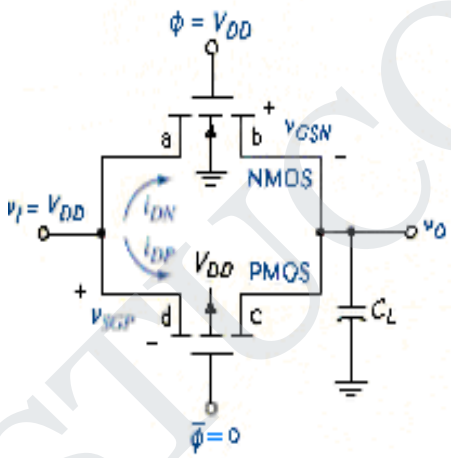


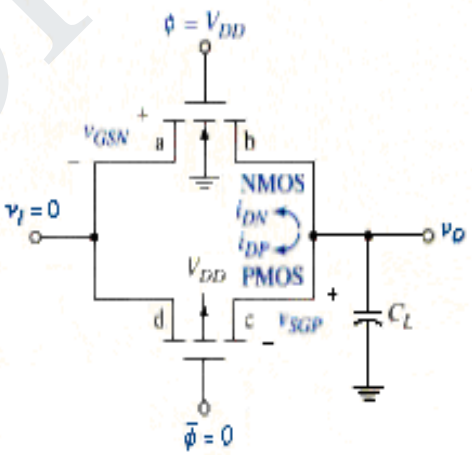
S	nMOS	pMOS	OUTPUT
0	OFF	OFF	Z
1	ON	ON	INPUT

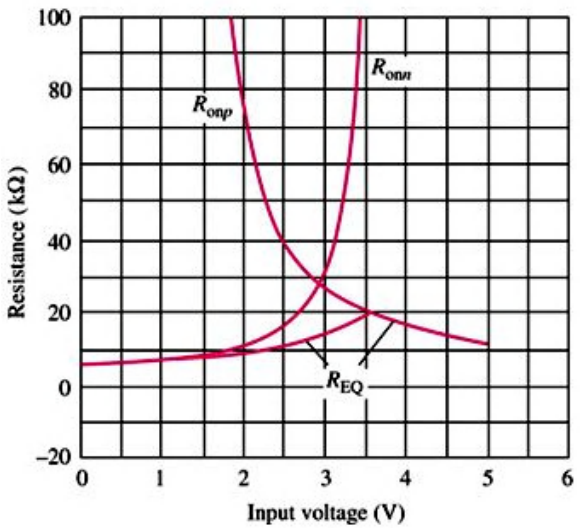




- **Characteristics with operation:** ***(4 Marks)***







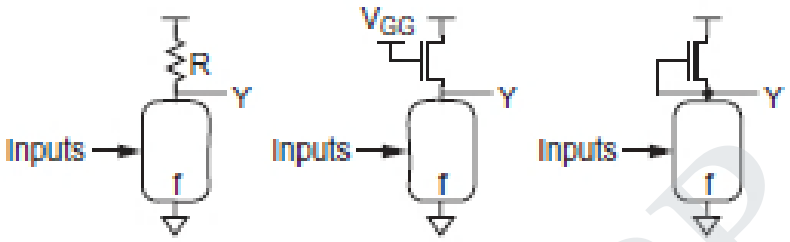
2. Write short notes on (i) Ratioed circuit (ii) dynamic CMOS circuits. *(Nov/Dec-16)*

- **Ratioed circuit: *(8 Marks)***

  Definition: *(2 Marks)*

  - ✓ Alternate method to reduce the number of transistors, cost and extra power dissipation.

  Diagram: *(3 Marks)*



  Explanation: *(3 Marks)*

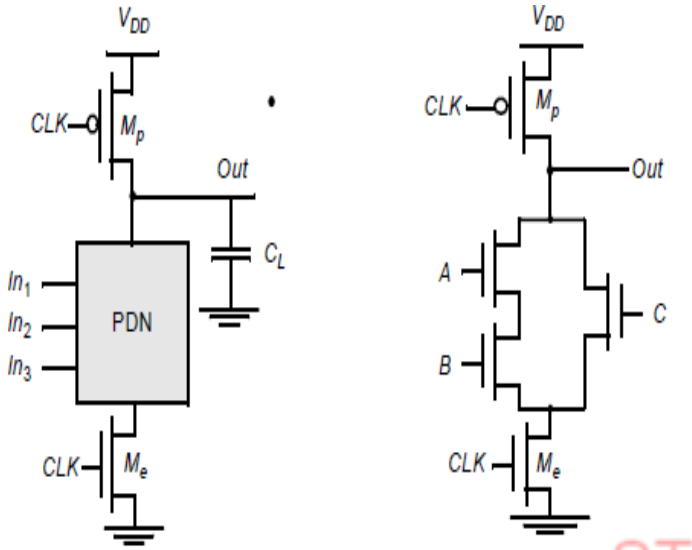
  - ✓ Ratioed circuits depend on the proper size or resistance of devices for correct operation.
  - ✓ The ratioed gate consists of an nMOS pulldown network and some pullup device called the *static load*.
  - ✓ When the pulldown network is OFF, the static load pulls the output to 1.
  - ✓ When the pulldown network turns ON,

- **Dynamic CMOS circuits: *(8 Marks)***

  Definition: *(2 Marks)*

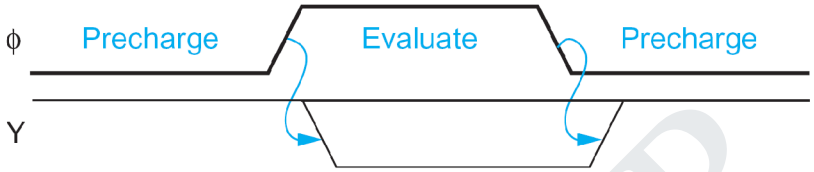
  - ✓ An alternate logic style called *dynamic logic* is presented that obtains a similar result, while avoiding static power consumption.
  - ✓ With the addition of a clock input, it uses a sequence of *precharge* and conditional *evaluation* phases.

  Diagram: *(3 Marks)*



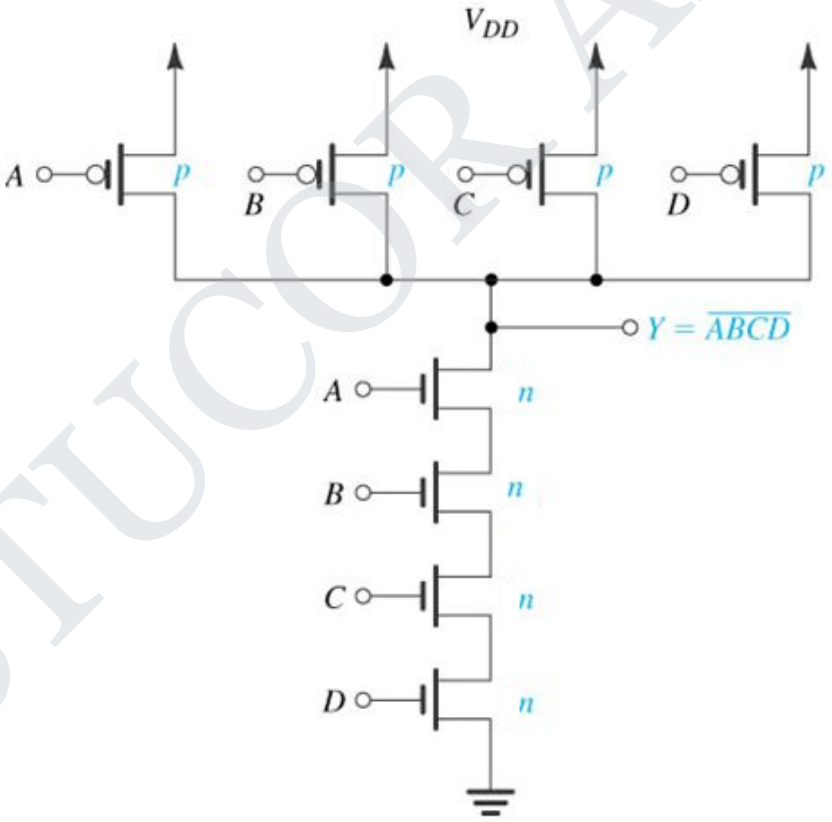
Explanation: ***(3 Marks)***

- ✓ With the addition of a clock input, it uses a sequence of *precharge* and conditional *evaluation* phases.
- ✓ **Precharge:** When *CLK* = 0, *Out* is precharged to *VDD* by the PMOS transistor *Mp.*
- ✓ **Evaluation:** For *CLK* = 1, the precharge transistor *Mp* is off, and the evaluation transistor *Me* is turned on.

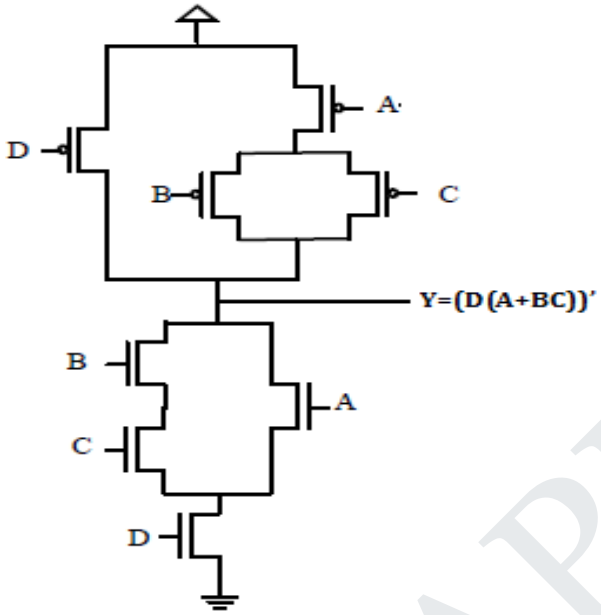


3. Draw the static CMOS logic circuit for the following expression (a) Y=(A.B.C.D)' (b)Y=(D(A+BC))' *(May/Jun-16)*

- **<u>Y=(A.B.C.D)' *(8 Marks)*</u>**

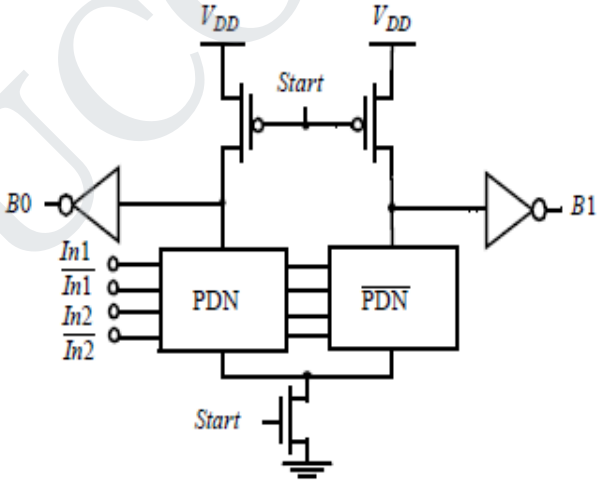


- **(b)Y=(D(A+BC))' *(8 Marks)***



4. (i) Explain about DCVSL logic with suitable example. *(Apr/May-17)*

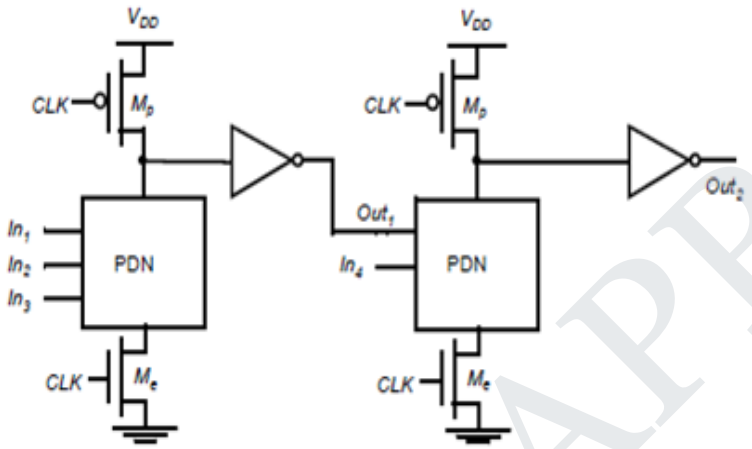
- **Definition: *(2 Marks)***
  - ✓ Differential Cascade Voltage Switch Logic consists of two parts – a complementary NMOS pull down network and PMOS load transistor.
- **Diagram: *(3 Marks)***



- **Explanation: *(3 Marks)***
  - ✓ DCVSL is more expensive in terms of area than a non-redundant circuit due to its dual nature.
  - ✓ It has advantage over static CMOS design in terms of circuit delay, layout area, logic flexibility and power dissipation.
  - ✓ It has self testing property which can provide coverage for stuck-at fault and dynamic faults.

(ii) Explain the domino logic with neat diagram. ***(Nov/Dec-17)***

- **Definition:** ***(2 Marks)***
  - ✓ Differential Cascade Voltage Switch Logic consists of two parts – a complementary NMOS pull down network and PMOS load transistor.
- **Diagram:** ***(3 Marks)***



- **Explanation:** ***(3 Marks)***
  - ✓ They have smaller areas than conventional CMOS logic (as does all Dynamic Logic).
  - ✓ Parasitic capacitances are smaller so that higher operating speeds are possible.
  - ✓ Operation is free of glitches as each gate can make only one transition.
  - ✓ Only non-inverting structures are possible because of the presence of inverting buffer.
  - ✓ Charge distribution may be a problem.

5. Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions. Also explain how it can be reduced. ***(Apr/May-17, May/Jun-16, Nov/Dec-16, Apr/May-15, Nov/Dec-15, May/Jun-14, Nov/Dec-13)***

- **Static power dissipation:** ***(8 Marks)***

  Definition: ***(2 Marks)***
  - ✓ Due to leakage current or other current drawn continuously from the power supply.

  Explanation: ***(3 Marks)***

  Due to leakage current or other current drawn continuously from the power supply.
  - ✓ Sub – threshold conduction through OFF transistors
  - ✓ Tunneling current through gate oxide
  - ✓ Leakage through reverse biased diodes
  - ✓ Contention current in radioed circuits.

$$P_{static} = (I_{sub} + I_{gate} + I_{junct} + I_{contention})V_{DD}$$

  - ✓ Static power dissipation. P_s= leakage power * supply voltage.

Reduction method: ***(3 Marks)***

- ✓ One way to reduce power at the technological level is to reduce the supply voltage.
- ✓ The alternative approach to reducing wasteful activity is applying an asynchronous design methodology.

- **Dynamic power dissipation:** ***(8 Marks)***

Definition: ***(2 Marks)***

- ✓ Due to switching transient current, Charging and discharging of load capacitances.

Explanation: ***(3 Marks)***

Dynamic power: $P_{dynamic} = P_{switching} + P_{shortcircuit}$

- ✓ Switching load capacitances
- ✓ Short-circuit current - Both pMOS and nMOS stacks are partially ON
- ✓ Dynamic power dissipation. $P_d = = C_L V^2_{dd} f_{clk}$

Reduction method: ***(3 Marks)***

Try to minimize

- ✓ Activity factor
- ✓ Capacitance
- ✓ Supply voltage
- ✓ Frequency

$P_{total} = P_{dynamic} + P_{static}$

6. **Derive the expression for the rise time, fall time and propagation delay of CMOS inverter.** ***(Apr/May-15, Nov/Dec-13)***

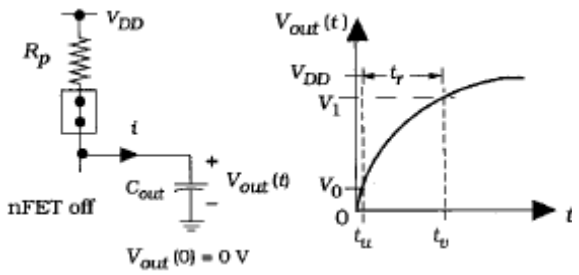
- **Rise time, tr:** ***(6 Marks)***

Definition: ***(2 Marks)***

- ✓ Waveform to rise from 10% to 90% of its steady state value. '
- ✓ Time for output to rise from '0'to '1'

Derivation: ***(4 Marks)***

- ✓ Initial condition, Vout(0) = 0V
- ✓ $i = C_{out}\frac{\partial V_{out}}{\partial t} = \frac{V_{DD} - V_{out}}{R_p}$
- ✓ $V_{out}(t) = V_{DD}[1 - e^{\frac{-t}{\tau_p}}]$
- ✓ $t_r = 2.2\tau_p$



- **Fall time tf:** ***(6 Marks)***

Definition: ***(2 Marks)***

- ✓ Waveform to rise from 90% to 10% of its steady state value. '

✓ Time for output to rise from '1'to '0'

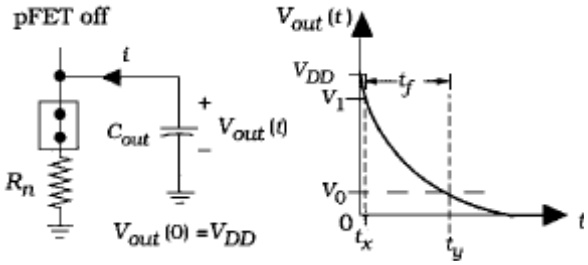
Derivation: ***(4 Marks)***

✓ Initial condition, Vout(0) = 0V

✓ $i = -C_{out}\frac{\partial V_{out}}{\partial t} = \frac{V_{DD} - V_{out}}{R_p}$,

✓ $V_{out}(t) = V_{DD}[e^{\frac{-t}{\tau_n}}]$

✓ $t_f = 2.2\tau_n$

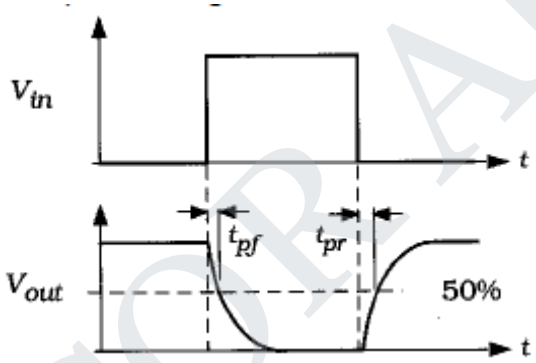


- **Propagation Delay, tp:** ***(4 Marks)***

✓ Measures speed of output reaction to input change

$t_p = 0.35(\tau_n + \tau_p)$

✓ Time difference between input transition (50%) and 50% output level.



7. Define logical effort and read-out why mostly NAND gates are used to realize the combinational circuits rather than NOR gates. ***(Nov/Dec-15)***

- **Definition:** ***(2 Marks)***

Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current. Delay has two components: d = f + p,

Where f: effort delay = gh

g: logical effort

h: electrical effort = C_{out} / C_{in}

p: parasitic delay

- **Logical effort of common gates** ***(2 Marks)***

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		4/3	5/3	6/3	(n+2)/3
NOR		5/3	7/3	9/3	(2n+1)/3
Tristate / mux	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

- **NAND has lesser delay than Nor due to the NAND PMOS: *(4 Marks)***
  - ✓ NAND has lesser delay than NOR due to the NAND PMOS (size 2 and in parallel) when compared to NOR PMOS (size 4 in series).
  - ✓ But the logical effort *g* for NAND is less than that of NOR.
  - ✓ NOR occupies more area.
  - ✓ NAND uses transistors of similar sizes.

8. Derive the final expressions and explain path logical effort, path electrical effort, path effort and path branching effort. *(Nov/dec-14)*

- **Path logical effort: *(4 Marks)***
  - ✓ It is product of logical efforts of all logic gates along the path. $G = \prod g_i$
- **Path electrical effort: *(4 Marks)***
  - ✓ It is ratio of output capacitance to input capacitance. $H = \frac{C_{\text{out-path}}}{C_{\text{in-path}}}$
- ***Path effort*: *(4 Marks)***
  - ✓ The path effort is expressed in terms of the **path logical effort** G (the product of the individual logical efforts of the gates), and the **path electrical effort** H (the ratio of the load of the path to its input capacitance). $F = \prod f_i = \prod g_i h_i$
- **Path branching effort: *(4 Marks)***
  - ✓ Due to fan-out in a logic network, some drive current is directed along the path. $b = \frac{C_{\text{on path}} + C_{\text{off path}}}{C_{\text{on path}}}$

9. Discuss the low power design principles in detail. *(Nov/Dec-17)*

- ✓ To reduce the dynamic power, supply voltage V_{DD} is reduced.
- ✓ The power can be reduces by lowering the effective capacitance.
- ✓ This is achieved by reducing the physical capacitance and switching activity.
- ✓ The transistors with minimum size can be used to reduce the capacitance.
- ✓ Proper layout techniques are used to minimize routing capacitance.
- ✓ Power dissipation due to short-circuit current is minimized
- ✓ The non-active modules can be made to be in standby mode.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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UNIT III - SEQUENTIAL LOGIC CIRCUITS

PART – A

1. Define Pipelining. ***(Apr/May-17, Nov/Dec-16)***

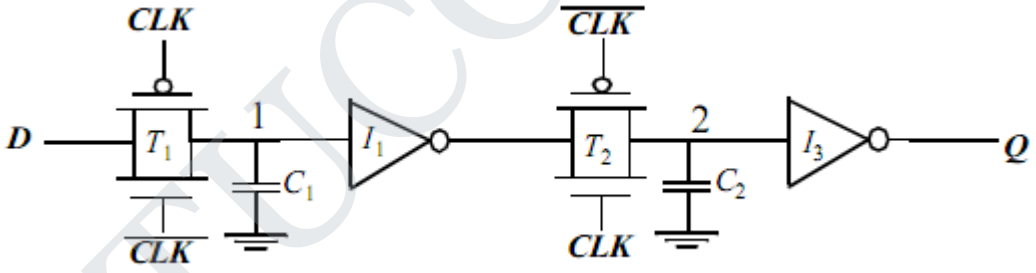
Pipelining is a popular design technique often used to accelerate the operation of the data path in digital processors. The major advantages of pipelining are to reduce glitching in complex logic networks and getting lower energy due to operand isolation.

2. Compare & Contrast synchronous design and asynchronous design. ***(Apr/May-17)***

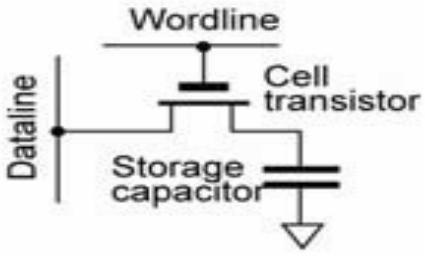
Synchronous Sequential Circuit: Output changes at discrete interval of time. It is a circuit based on an equal state time or a state time defined by external means such as clock. Examples of synchronous sequential circuit are Flip Flops, Synchronous Counter.

Asynchronous Sequential Circuit: Output can be changed at any instant of time by changing the input. It is a circuit whose state time depends solely upon the internal logic circuit delays. Example of asynchronous sequential circuit is Asynchronous Counter.

3. Draw the schematic of dynamic edge-triggered register. ***(Nov/Dec-16)***



4. Design one transistor DRAM cell. ***(Apr/May-15, Nov/Dec-13)***



5. Define clock skew and clock jitter. ***(Nov/Dec-17)***

Clock skew: In reality clocks have some uncertainty in their arrival times that can cut into the time available for useful computation is called clock skew.

Clock jitter: Temporal variations in consecutive edges of the clock signals; modulation + random noise- Cycle-to-cycle (short-term) long term

6. List out the techniques used for low power logic design. ***(Nov/Dec-15, May/Jun-14)***

- To reduce the dynamic power, supply voltage V_{DD} is reduced.
- The transistors with minimum size can be used to reduce the capacitances.
- The power dissipation due to short circuit current is minimized by matching the rise time/fall times of the input and output signals.
- Proper layout techniques are used to minimize routing capacitances.

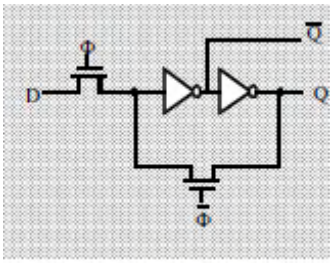
7. Difference between latch and flip-flop. ***(Nov/Dec-15, Nov/Dec-14)***

Sl. No	Latch	Flip-Flop
1	A Latch is Level-Sensitive	A latch stores when the clock level is low and is transparent when the level is high.
2	A FF is edge triggered.	A FF stores when the clock rises and is mostly never transparent.

8. List out the techniques used for low power logic design. ***(Nov/Dec-15, May/Jun-14)***

- To reduce the dynamic power, supply voltage V_{DD} is reduced.
- The transistors with minimum size can be used to reduce the capacitances.
- The power dissipation due to short circuit current is minimized by matching the rise time/fall times of the input and output signals.
- Proper layout techniques are used to minimize routing capacitances.

9. Draw the switch level schematic of multiplexer based nMOS latch using nMOS only pass transistors for multipliers. ***(May/Jun-16)***



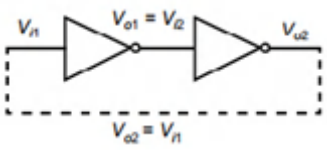
10. What is clocked CMOS registers. ***(May/Jun-16)***

The dynamic latch can also be drawn as a clocked tristate. Such a form is sometimes called *clocked CMOS* (C^2MOS) the output is driven through the nMOS and pMOS working in parallel. C^2MOS is slightly smaller because it eliminates two contacts.

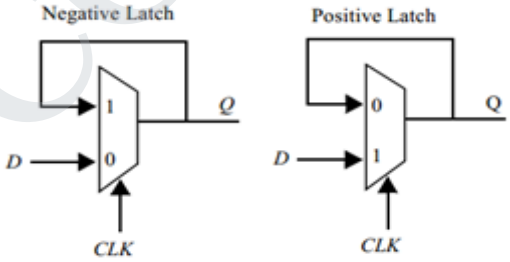
PART – B (Answers as Hint)

1. **Explain the methodology of sequential circuit design of latches and flip-flops.** ***(Nov/Dec-17, Nov/Dec-16, May/Jun-14)***

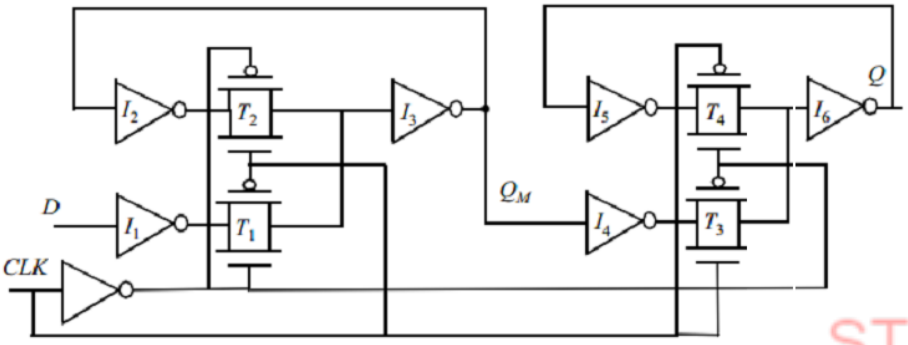
- **Static Latches and registers:** ***(8 Marks)***
- **The Bistability Principle:** ***(2 Marks)***
  - ✓ Static memories use positive feedback to create a bistable circuit — a circuit having two stable states that represent 0 and 1.



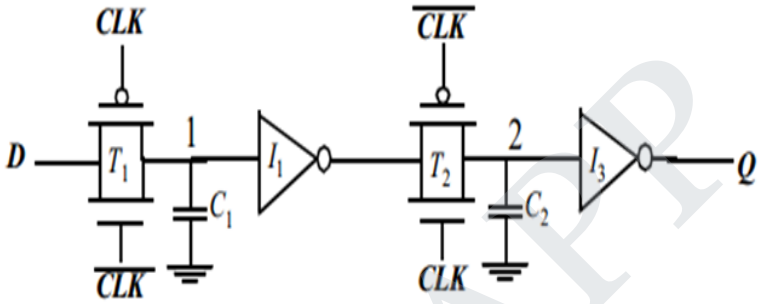
- **Multiplexer Based Latches:** ***(3 Marks)***
  - ✓ Multiplexer based latches can provide similar functionality to the SR latch, but has the important added advantage that the sizing of devices only affects performance and is not critical to the functionality.
  - ✓ **Positive latch:** when CLK=0 D input is passed to output, when CLK=1 input 1 is connected to output of latch.
  - ✓ **Negative latch:** when CLK=0 output is feedback to input, when CLK=1 input 1 D is selected.



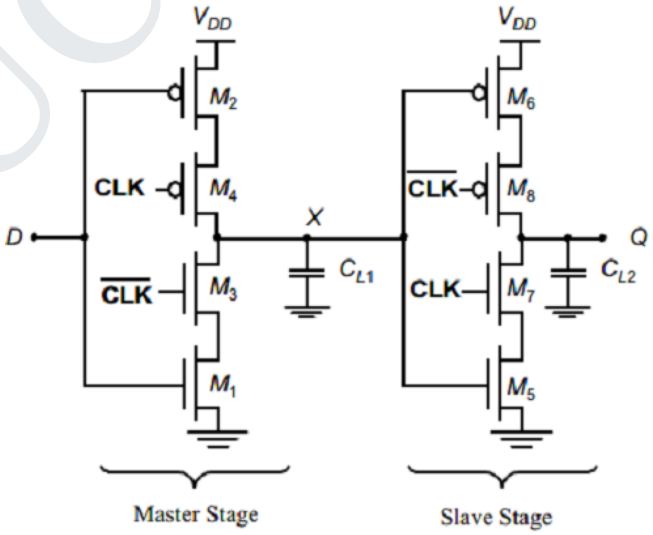
- **Master-Slave Based Edge Triggered Register:** ***(3 Marks)***
  - ✓ When clock is low (CLK = 1), T1 is on and T2 is off, and the D input is sampled onto node QM.
  - ✓ When the clock goes high, the master stage stops sampling the input and goes into a hold mode.



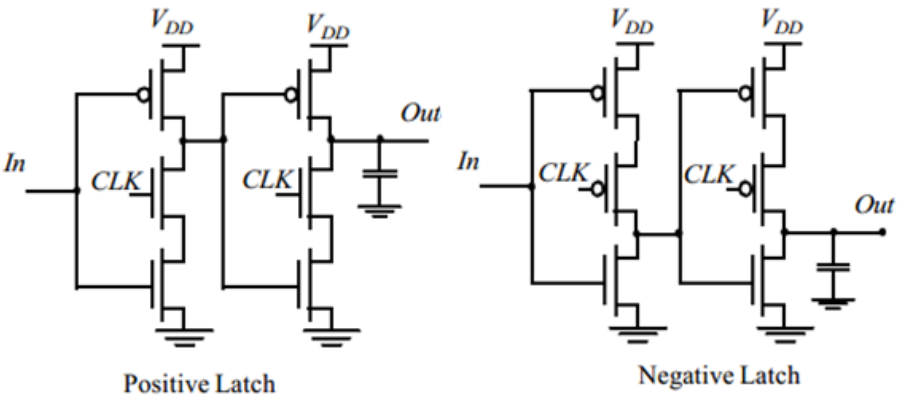
- **Dynamic Latches and registers:** ***(8 Marks)***
- **Dynamic Transmission-Gate Based Edge-triggred Registers:** ***(2 Marks)***
  - ✓ When CLK = 0, the input data is sampled on storage node 1, which has an equivalent capacitance of C1 consisting of the gate capacitance, the junction capacitance and the overlap gate capacitance of T2.
  - ✓ When CLK = 1, the transmission gate T2 turns on, and the value sampled on node 1 right before the rising edge propagates to the output Q.



- **C²MOS Dynamic Register:** ***(3 Marks)***
  - ✓ CLK = 0 (CLK = 1): The first tri-state driver is turned on, and the master stage acts as an inverter sampling the inverted version of D on the internal node X. The master stage is in the evaluation mode. Meanwhile, the slave section is in a high-impedance mode, or in a hold mode.
  - ✓ The roles are reversed when CLK = 1.

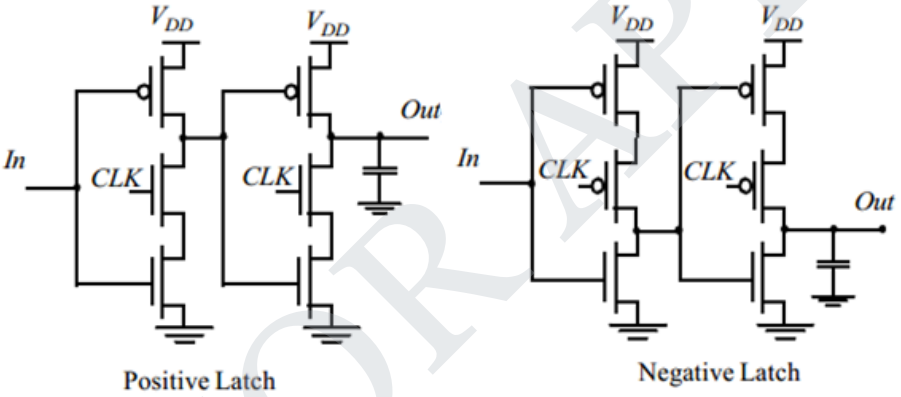


- **True Single-Phase Clocked Register (TSPCR):** ***(3 Marks)***
  - ✓ When CLK is high, the latch is in the transparent mode and corresponds to two cascaded inverters; the latch is non-inverting, and propagates the input to the output.
  - ✓ When CLK = 0, both inverters are disabled, and the latch is in hold-mode.



2. (i) Explain the operation of True Single Phase Clocked Register. ***(Apr/May-17, Nov/Dec-16, Nov/Dec-15)***

- **Diagram:** ***(4 Marks)***



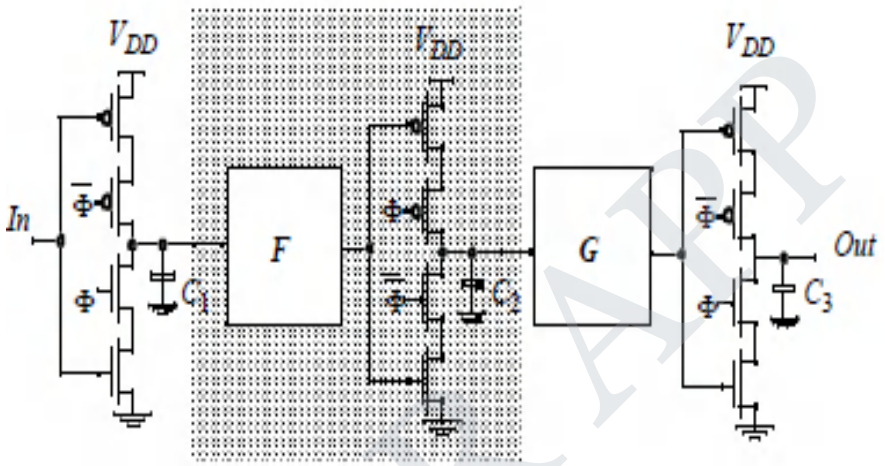
- **Explanation:** ***(4 Marks)***
  - ✓ When CLK is high, the latch is in the transparent mode and corresponds to two cascaded inverters; the latch is non-inverting, and propagates the input to the output.
  - ✓ When CLK = 0, both inverters are disabled, and the latch is in hold-mode.

(ii) Write short notes on NORA-CMOS Latch. ***(Nov/Dec-16)***

- **Explanation:** ***(4 Marks)***
  - ✓ A NORA datapath consists of a chain of alternating CLK and CLK modules.
  - ✓ Logic and latch are clocked in such a way that both are simultaneously in either evaluation, or hold (precharge) mode.
  - ✓ A block that is in evaluation during *CLK = 1 is called a CLK-module, while the inverse is called a CLK-module*
  - ✓ While one class of modules is precharging with its output latch in hold mode, preserving the previous output value, the other class is evaluating.

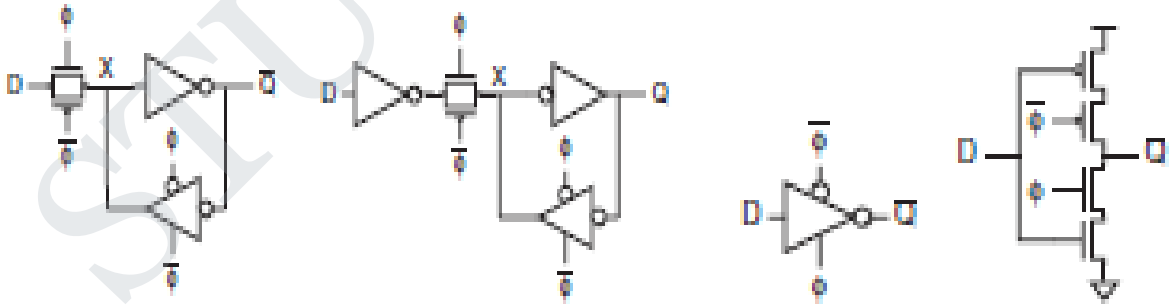
	Φ-block		$\bar{\Phi}$-block	
	Logic	Latch	Logic	Latch
Φ = 0	Precharge	Hold	Evaluate	Evaluate
Φ = 1	Evaluate	Evaluate	Precharge	Hold

- **Diagram:** ***(4 Marks)***



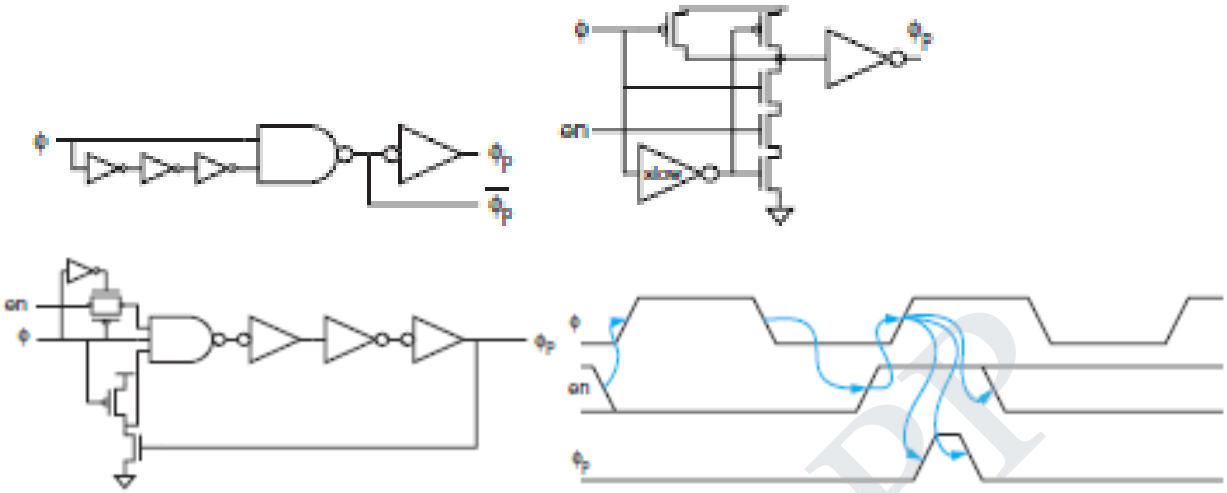
3. **Draw and explain the operation of Conventional, pulsed and resettable latches.** ***(Apr/May-17, Nov/Dec-12)***

- **Conventional latches:** ***(5 Marks)***
- **Diagram:** ***(2 Marks)***

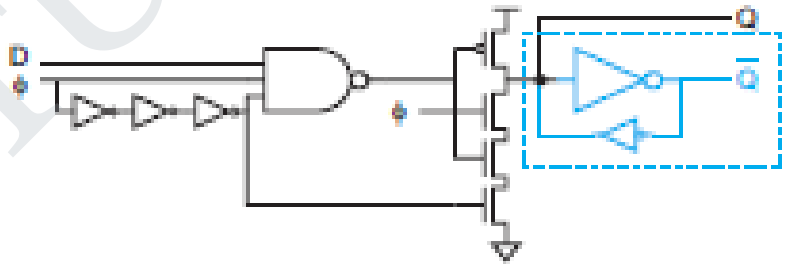


- **Explanation:** ***(3 Marks)***
  - ✓ The conventional form using the inverter and transmission gate is slightly faster because the output is driven through the nMOS and pMOS working in parallel.
  - ✓ When the clock is 1, the input transmission gate is ON, the feedback tristate is OFF, and the latch is transparent.
  - ✓ When the clock is 0, the input transmission gate turns OFF. However, the feedback tristate turns ON, holding *X* at the correct level.

- **Pulsed latches:** ***(5 Marks)***
- **Diagram:** ***(2 Marks)***



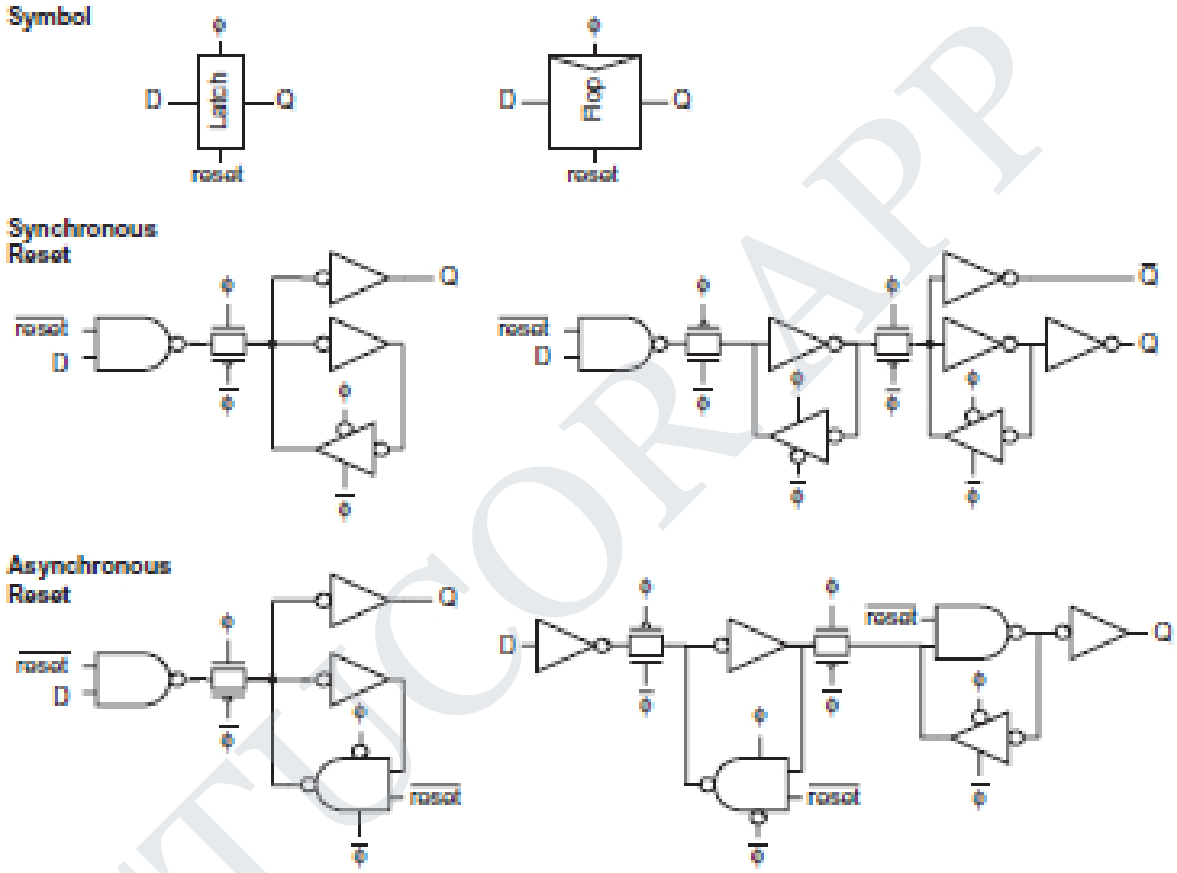
- **Explanation:** ***(3 Marks)***
  - ✓ A pulsed latch can be built from a conventional CMOS transparent latch driven by a brief clock pulse.
  - ✓ The pulsed latch is faster than a regular flip-flop because it involves a single latch rather than two and because it allows time borrowing. It can also consume less energy, although the pulse generator adds to the energy consumption
  - ✓ The drawback is the increased hold time.
  - ✓ The *Partovi pulsed latch* is eliminates the need to distribute the pulse by building the pulse generator into the latch itself



- **Resettable latches** ***(6 Marks)***
- **Explanation:** ***(3 Marks)***
  - ✓ Most practical sequencing elements require a reset signal to enter a known initial state on startup and ensure deterministic behavior.
  - ✓ There are two types of reset: *synchronous* and *asynchronous*
  - ✓ ***Asynchronous:***
    - ✓ Reset forces *Q* low immediately, while synchronous.
    - ✓ Reset is characterized by a propagation delay from reset to output.

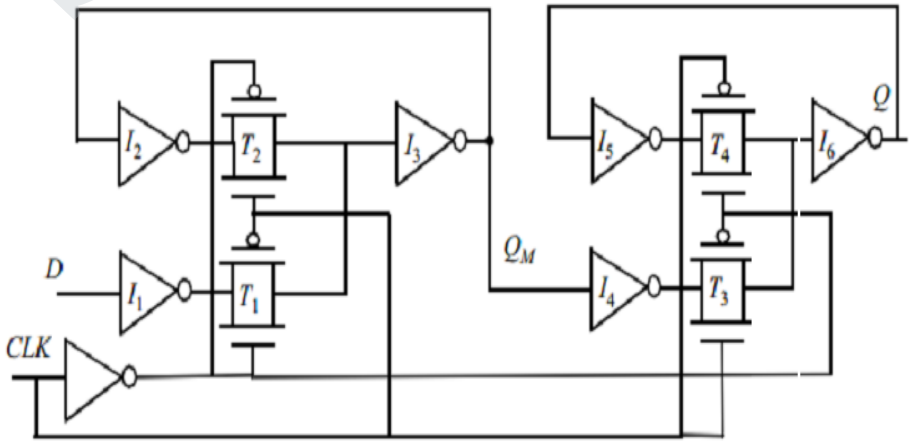
- ✓ Reset requires gating both the data and the feedback to force the reset independent of the clock.
- ✓ ***Synchronous:***
  - ✓ Reset waits for the clock.
  - ✓ Reset signals must be stable for a setup and hold time around the clock edge
  - ✓ Reset simply requires ANDing the input *D* with *reset*.

- **Diagram:** ***(3 Marks)***



4. Explain the operation of master slave based edge triggered register. ***(May/Jun-16)***

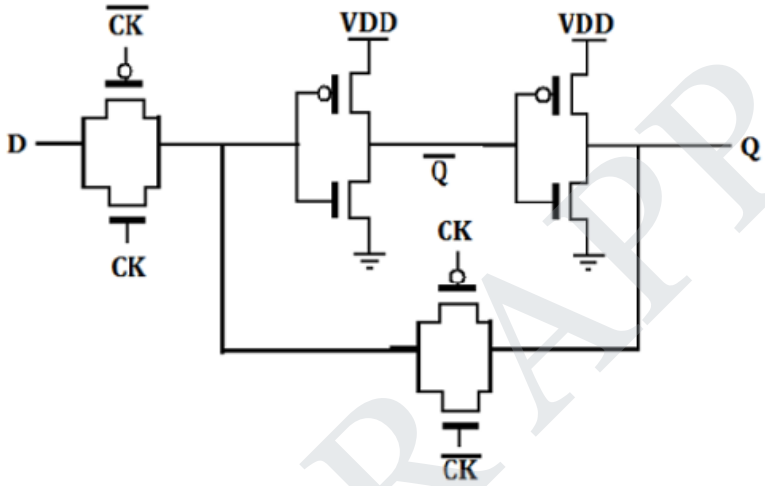
- **<u>Diagram:</u>** ***<u>(8 Marks)</u>***



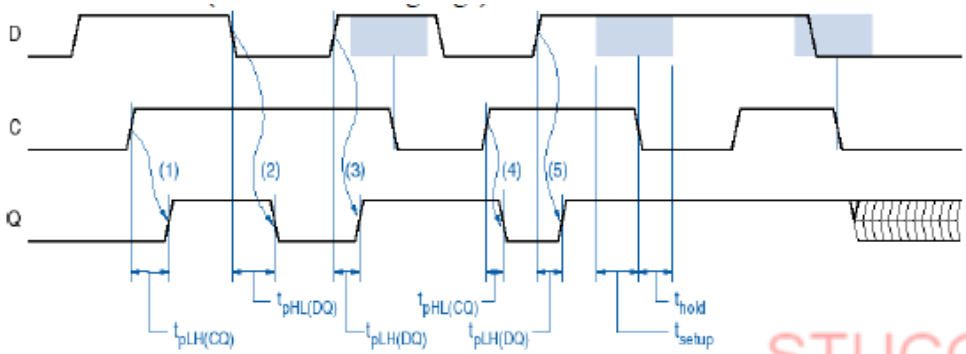
- **Explanation:** ***(8 Marks)***
  - ✓ When clock is low (CLK = 1), T1 is on and T2 is off, and the D input is sampled onto node QM.
  - ✓ When the clock goes high, the master stage stops sampling the input and goes into a hold mode.

5. (i) Design D-Latch using transmission gate. ***(Apr/May-15, Nov/Dec-13)***

- **Diagram:** ***(4 Marks)***

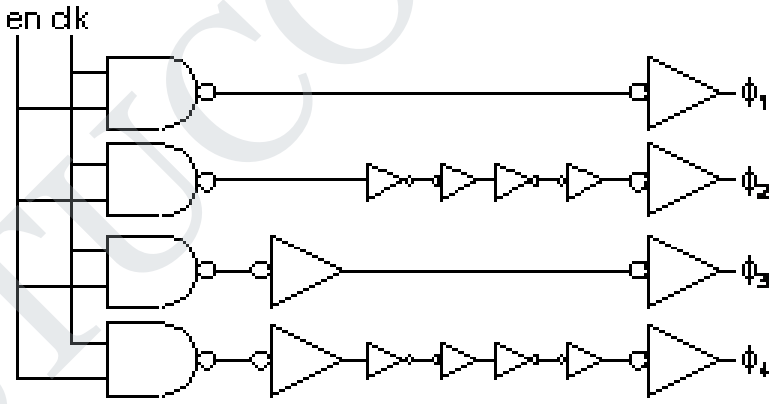


- **Explanation:** ***(4 Marks)***
  - ✓ D latch is implemented with transmission gate (TG).
    - Input TG is activated with CLK, while the latch feedback loop TG is activated with CLK'.
    - Input D is accepted when CLK is high.
    - When CLK goed low, the input is open circuited and the latch is set with the prior data D.
  - ✓ When C = 1, Q follows D
    - Pro p g y( ) a gation dela y (from C or D)
  - ✓ When C = 0, Q remembers D's value at the 1 to 0 transition
    - Setup time (D before C's falling edge)
    - Hold time (D after C's falling edge)



(ii) Explain clock distribution techniques in synchronous design in detail. ***(Nov/Dec-17)***

- **Explanation:** ***(4 Marks)***
  - ✓ On a small chip, the clock distribution network is just a wire
    - ✓ And possibly an inverter for clkb
  - ✓ On practical chips, the RC delay of the wire resistance and gate load is very long
    - ✓ Variations in this delay cause clock to get to different elements at different times
    - ✓ This is called clock skew
  - ✓ Most chips use repeaters to buffer the clock and equalize the delay
    - ✓ Reduces but doesn't eliminate skew
  - ✓ Synchronous systems use a clock to keep operations in sequence
    - ✓ Distinguish *this* from *previous* or *next*
    - ✓ Determine speed at which machine operates
  - ✓ Clock must be distributed to all the sequencing elements
    - ✓ Flip-flops and latches
  - ✓ Also distribute clock to other elements
    - ✓ Domino circuits and memories
- **Diagram:** ***(4 Marks)***



6. Explain the concept of timing issues and pipelining. ***(Nov/Dec-17, Apr/May-17, May/Jun-16, May/Jun-13)***

- **Timing issues:** ***(8 Marks)***

  Explanation: ***(5 Marks)***
  - ✓ The setup time is the interval before the clock where the data must be held stable.
  - ✓ The hold time is the interval after the clock where the data must be held stable.
  - ✓ Hold time can be negative, which means the data can change slightly before the clock edge and still be properly captured.
  - ✓ Most of the current day flip-flops has zero or negative hold time.

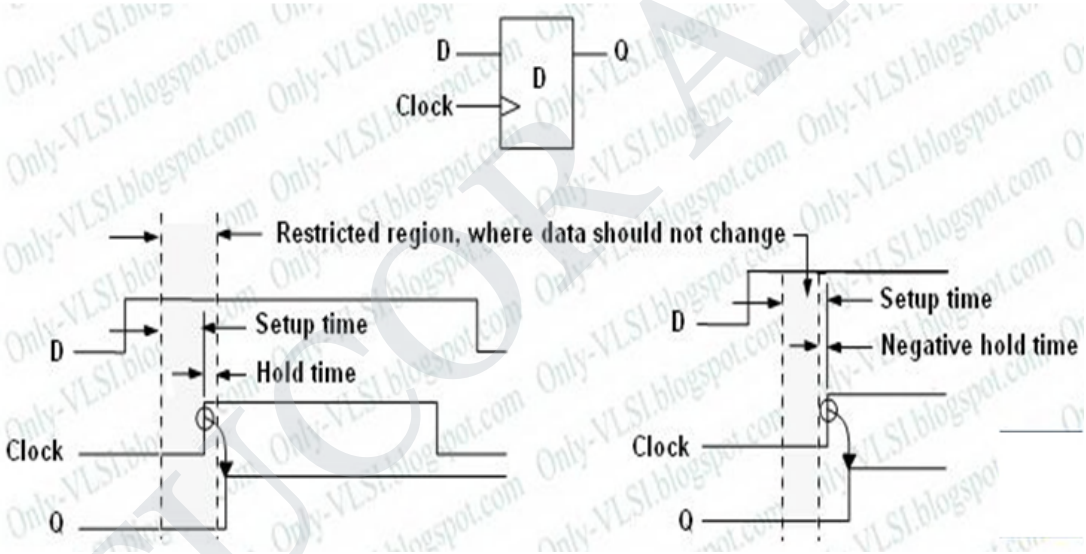
To avoid setup time violations:

- ✓ The combinational logic between the flip-flops should be optimized to get minimum delay.
- ✓ Redesign the flip-flops to get lesser setup time.
- ✓ Tweak launch flip-flop to have better slew at the clock pin, this will make launch flip-flop to be fast there by helping fixing setup violations.
- ✓ Play with clock skew (useful skews).

To avoid hold time violations:

- ✓ By adding delays (using buffers).
- ✓ One can add lockup-latches (in cases where the hold time requirement is very huge, basically to avoid data slip).

Diagram: ***(3 marks)***

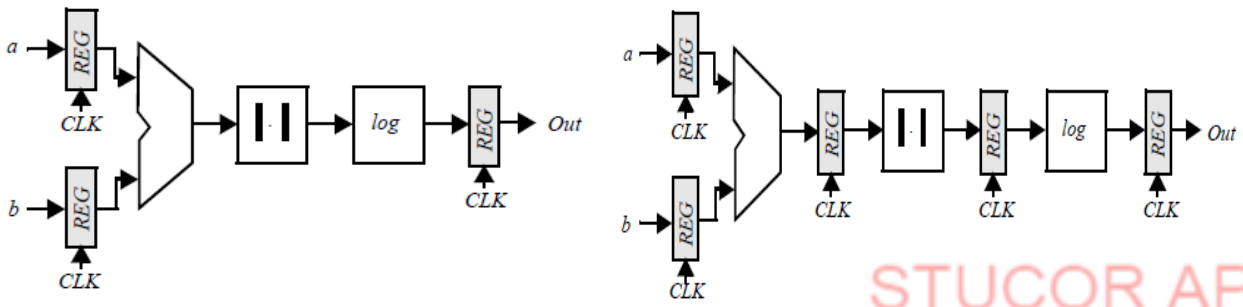


- **<u>Pipelining:</u>** ***<u>(8 Marks)</u>***

Definition: ***(2 Marks)***

- ✓ Pipelining is a popular design technique often used to accelerate the operation of the datapaths in digital processors.
- ✓ Pipelining is a technique to improve the resource utilization, and increase the functional throughput.

Diagram: ***(3 Marks)***



Explanation: ***(3 Marks)***

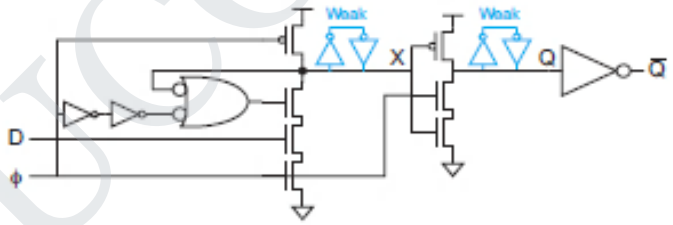
- ✓ The combinational circuit block has been partitioned into three sections, each of which has a smallerp ropagation delay than the original function.
- ✓ Suppose that all logic blocks have approximately the same propagation delay, and that the register overhead is small with respect to the logic delays.
- ✓ This effectively reduces the value of the minimum allowable clock period:

$$T_{min,\text{pipe}} = t_{c\text{-}q} + \max(t_{pd,\text{add}}, t_{pd,\text{abs}}, t_{pd,\text{log}})$$

- ✓ The increased performance comes at the relatively small cost of two additional registers, and an increased latency.
- ✓ The advantage of pipelined operation becomes apparent when examining the minimum clock period of the modified circuit.

7. What are Klass semidynamic flip-flop? Explain with their logic circuits. ***(Nov/Dec-14)***

- ✓ **Definition:** ***(4 Marks)***
  - ✓ The Klass semidynamic flip-flop (SDFF) [Klass99] is a cross between a pulsed latch and a flip-flop.
  - ✓ It is called semidynamic because it combines the dynamic input stage with static operation.
- ✓ **Diagram:** ***(4 Marks)***

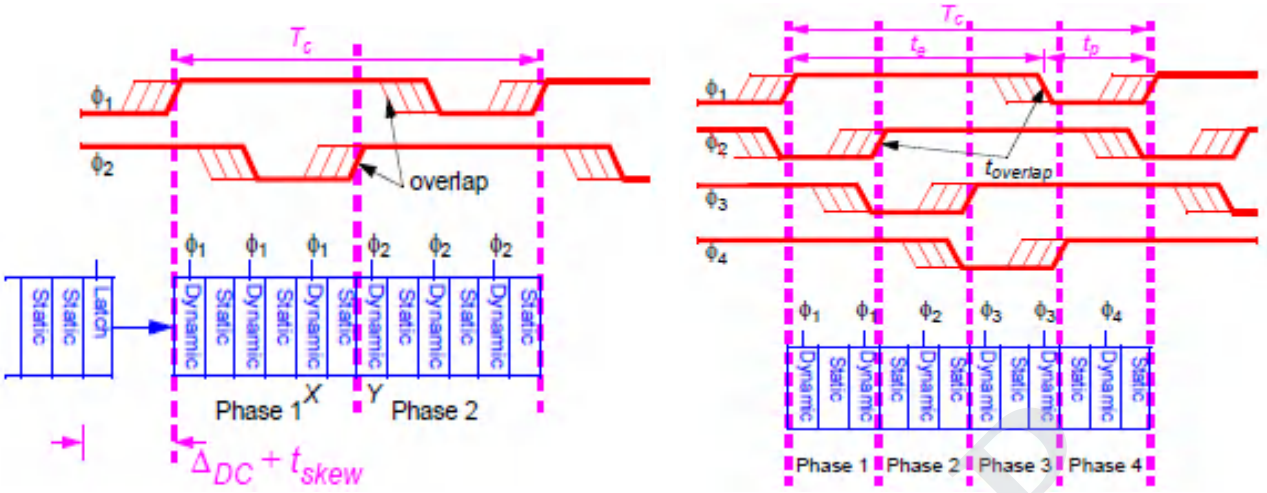


- ✓ **Explanation:** ***(8 Marks)***
  - ✓ It uses a dynamic NAND gate in place of the static NAND.
  - ✓ If *D* is 0, *X* remains high and the top nMOS transistor turns OFF.
  - ✓ If *D* is 1 and *X* starts to fall low, the transistor remains ON to finish the transition.

8. Discuss on skew tolerant Domino circuits. ***(Nov/Dec-14)***

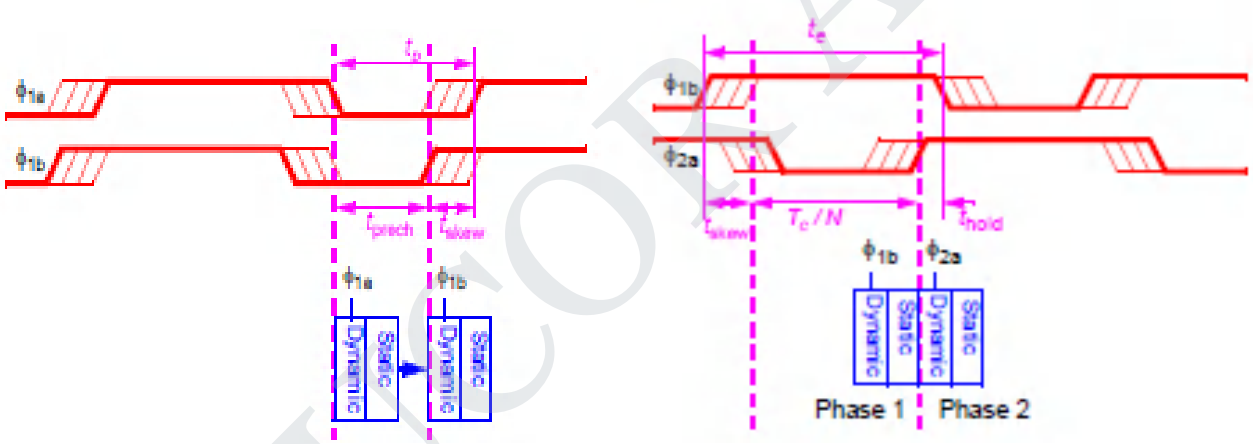
- ✓ **Explanation:** ***(8 Marks)***
  - ✓ If inputs are all dual rail, then as long as the clock arrives before the data, The gate will wait and fire when the data arrives
  - ✓ If the next gate fires before the current gate precharges, there is no need for a latch.
  - ✓ Divide logic into N phases of T/N duration each.
  - ✓ We can remove latches within domino pipeline
  - ✓ Eliminate all sequencing overhead within the domino pipeline

- ✓ Still budget skew and setup at static / domino interface



- ✓ **Calculation with diagram:** ***(8 Marks)***
  - ✓ Precharge Time (tp): Precharge must complete before second gate reenters evaluation

    tp = tprech + tskew



  - ✓ Evaluation Time (te): First phase begins evaluation early Must not precharge until some hold time t_{hold} after second phase evaluates

    $Te=Tc/N + t_{hold} + t_{skew}$

  - ✓ Skew Tolerance : We've found the best duty cycle
    - ✓ Precharge: tp = tprech + tskew
    - ✓ Evaluation: $Te=Tc/N + t_{hold} + t_{skew}$
  - ✓ Solve for the maximum tolerable skew tskew-max=([(N-1)/N]Tc - tprech – thold)/2
  - ✓ Observations
    - ✓ Skew tolerance increases with N
    - ✓ Precharge and hold time cut into skew tolerance
    - ✓ In the limit of large N and long cycles, skew tolerance ~ 1/2 cycle

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC6601 - VLSI DESIGN

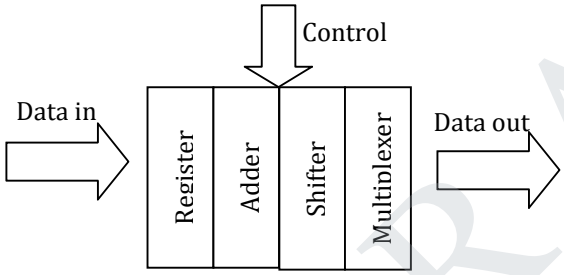
QUESTION BANK

UNIT IV - DESIGNING ARITHMETIC BUILDING BLOCK

PART – A

1. What is meant by bit-sliced data path organization and what are the advantages of data path operators? *(May/Jun-16)*

A **data path** is a collection of functional units, such as arithmetic logic units or multipliers that perform data processing operations, registers, and buses. Along with the control unit it composes the central processing unit (CPU).



Advantages:

To implement the logic function using n-identical circuits Data may be arranged to flow in one direction, while any control signals are introduced in an orthogonal direction to the data flow.

2. List out the components of data path. *(Apr/May-17)*

- Register
- Adder
- Shifter
- Multiplexer

3. Give the applications of high speed adders. *(Nov/Dec-17, Apr/May-17)*

Addition is one of the essential operations in Digital Signal Processing (DSP) applications which include Fast Fourier Transform (FFT), Digital filters, multipliers etc. With the advancements in technology, research is still going on to design a adder that performs addition in flash of time. One of such high speed adder is carry save adder (CSA).

4. Determine propagation delay of n-bit carry select adder. *(May/Jun-16)*

$t_p = t_{setup} + M\, t_{carry} + (N/M)t_{mux} + t_{sum}$

5. Why barrel shifter very useful in the designing of arithmetic circuits? *(Nov/Dec-16)*

A common usage of a barrel shifter is in the hardware implementation of floating-point arithmetic. For a floating-point add or subtract operation, the significant of the two numbers must be aligned, which

requires shifting the smaller number to the right, increasing its exponent, until it matches the exponent of the larger number. This is done by subtracting the exponents and using the barrel shifter to shift the smaller number to the right by the difference, in one cycle. If a simple shifter were used, shifting by n bit positions would require n clock cycles.

6. Write the principle of any one fast multiplier*? (Nov/Dec-16)*

The Wallace tree has three steps:

- Multiply each bit of one of the arguments, by each bit of the other, yielding n2 results.
- Reduce the number of partial products to two by layers of full and half adders.
- Group the wires in two numbers, and add them with a conventional adder.

7. Why we go to Booth's algorithm?

Booth algorithm is a method that will reduce the number of multiplicand multiples. For a given number of ranges to be represented, a higher representation radix leads to fewer digits.

8. What is latency? *(Nov/Dec-17)*

Latency refers to time interval or delay when a system component is waiting for another system component to do something. This duration of time is called latency.

9. Define accumulator.

An accumulator is a register in which intermediate arithmetic and logic results are stored. Without a register like an accumulator, it would be necessary to write the result of each calculation (addition, multiplication, shift, etc.) To main memory, perhaps only to be read right back again for use in the next operation.

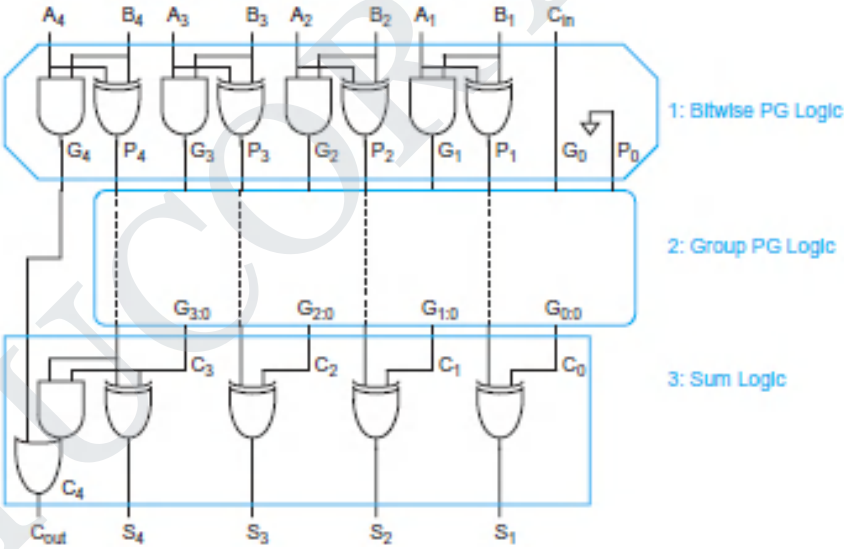
10. How CLA differ from RCA.

Sl. No	CLA	RCA
1.	The carry look ahead adder (CLA) solves the carry delay problem by calculating the carry signals in advance, based on the input signals.	In the ripple carry adder, the output is known after the carry generated by the previous stage is produced.
2.	It is based on the fact that a carry signal will be generated in two cases: (1) when both bits ai and bi are 1, or (2) when one of the two bits is and the carry-in is 1	Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay.

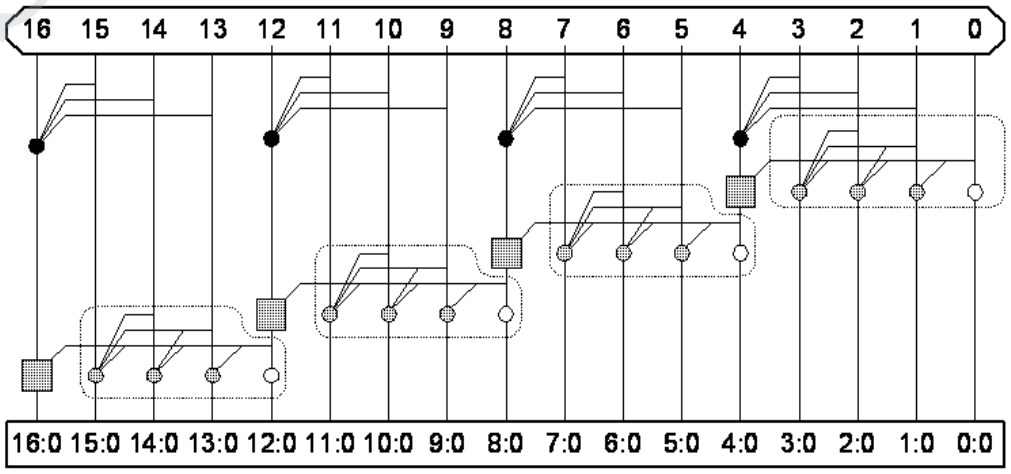
PART – B (Answer as Hints)

1. Explain the concept of carry look ahead adder with neat diagram. *(Nov/Dec-17, Apr/May-17)*

- **Explanation: *(10 Marks)***
  - ✓ To improve the speed of addition operation, carry propagation delay of adders is important.
  - ✓ Carry look ahead adder reduces circuit de3aly in ripple carry adder by calculation carry generation Cg, carry propagation, Cp.
  - ✓ Carry-look ahead adder computes $G_{i:0}$ for many bits in parallel.
  - ✓ Hence, addition can be reduced to a three-step process:
    - Computing bitwise generate and propagate signals using $G_i=A_i.B_i$, $P_i=A_i \oplus B_i$
    - Combining PG signals to determine group generates $G_{i-1:0}$ for all $N \geq i \geq 1$ using $G_i=C_i+P_iG_{i-1}$
    - Calculating the sums using $S_i=P_i \oplus G_{i-1:0}$
  - ✓ Some of the hardware can be shared in the bitwise PG logic.

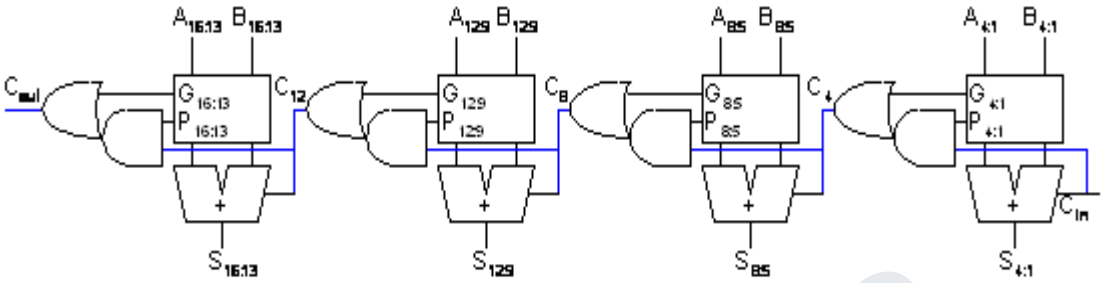


  - ✓ Uses higher-valency cells with more than two inputs.



- **Diagram:** ***(6 Marks)***
  - ✓ In general, a CLA using k groups of n bits each has a delay of

$$t_{CLA} = t_{pg} + t_{pg(n)} + [(n-1)+(k-1)]t_{AO} + t_{xor}$$



2. Design 16 bit carry bypass and carry select adder and discuss their features. ***(May/Jun-16)***

- **Carry bypass adder:** ***(8 Marks)***

  Explanation: ***(4 Marks)***
  - ✓ Carry-ripple is slow through all N stages
  - ✓ Carry-skip allows carry to skip over groups of n bits
    - Decision based on n-bit propagate signal

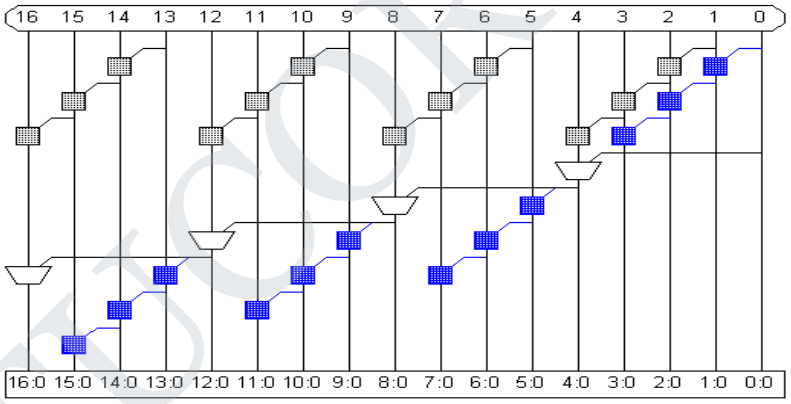
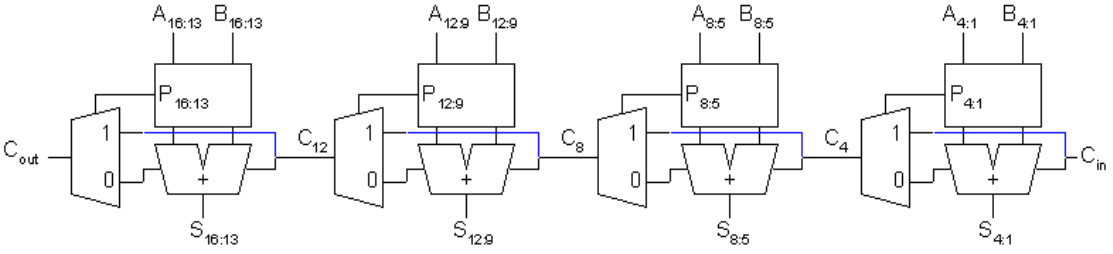


  Diagram: ***(4 Marks)***
  - ✓ It involves the initial PG logic producing a carry out of bit 1, three AND-OR gates rippling it to bit 4, three multiplexers bypassing it to C12, 3 AND-OR gates rippling through bit 15, and a final XOR to produce S16.
  - ✓ In general, an N-bit carry-skip adder using k n-bit groups (N = n × k) has a delay of

$$T_{skip} = t_{pg} + 2[(n-1)+(k-1)]t_{AO} + t_{xor}$$



- **Carry select adder:** ***(8 Marks)***

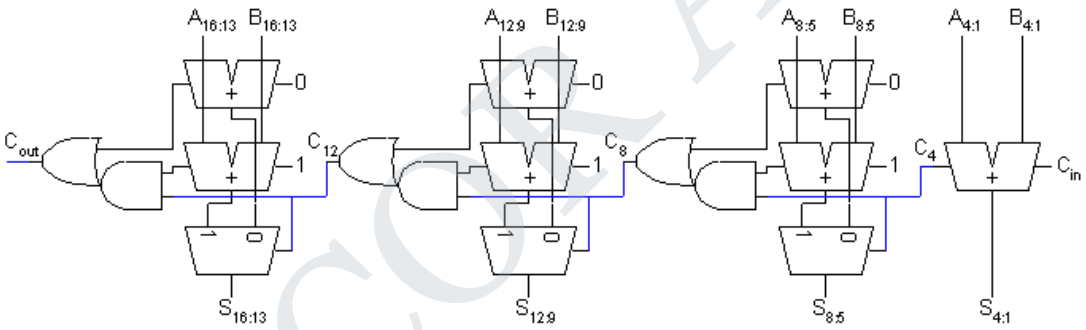
Explanation: ***(4 Marks)***

- ✓ Trick for critical paths dependent on late input X
  - Precompute two possible outputs for X = 0, 1
  - Select proper output when X arrives
- ✓ Carry-select adder precomputes n-bit sums
  - For both possible carries into n-bit group

Diagram: ***(4 Marks)***

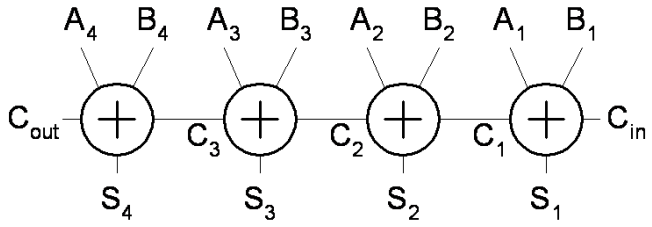
- ✓ One adder calculates the sums assuming a carry-in of 0 while the other calculates the sums assuming a carry-in of 1.
- ✓ The actual carry triggers a multiplexer that chooses the appropriate sum. The critical path delay is

$$T_{select} = t_{pg} + [n+(k-2)]t_{AO} + tmux$$

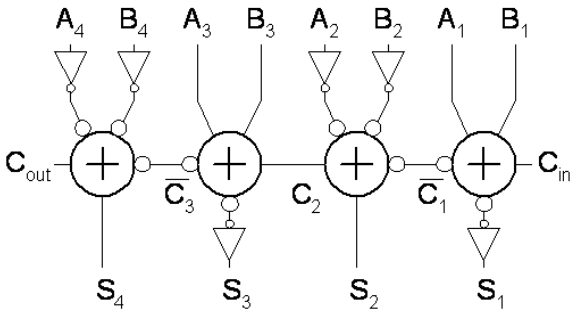


3. Explain the operation of a basic 4 bit adder, Describe the different approaches of improving the speed of the adder. ***(Nov/Dec-17, Nov/Dec-16)***

- **Explanation of basic 4 bit adder:** ***(4 Marks)***
  - ✓ Simplest design: cascade full adders
    - Critical path goes from C_{in} to C_{out}
    - Design full adder to have fast carry delay



  - ✓ Critical path passes through majority gate
    - Built from minority + inverter
    - Eliminate inverter and use inverting full adder



- **High speed adders: *(12 Marks)***
  - ✓ Carry select adder: *(4 Marks)*
  - ✓ Carry bypass adder: *(4 Marks)*
  - ✓ carry look ahead adder *(4 Marks)*

4. Explain the structure of booth multiplier with a suitable example and list its advantages. *(Apr/May-17, Nov/Dec-16)*

- **Explanation: *(12 Marks)***

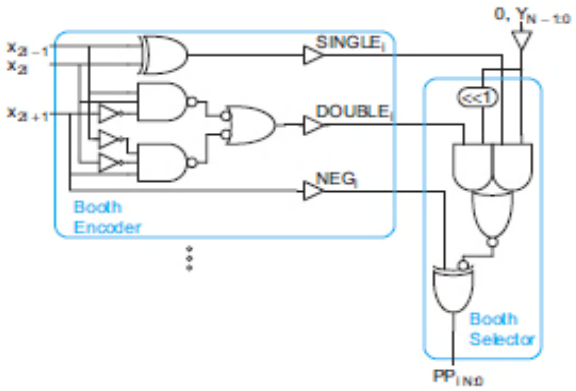
Definition: *(2 Marks)*

- ✓ Booth encoding was originally proposed to accelerate serial multiplication.
- ✓ Modified Booth encoding allows higher radix parallel operation without generating the hard 3Y multiple by instead using negative partial products.

Inputs			Partial Product	Booth Selects		
x_{2i+1}	x_{2i}	x_{2i-1}	PP_i	$SINGLE_i$	$DOUBLE_i$	NEG_i
0	0	0	0	0	0	0
0	0	1	Y	1	0	0
0	1	0	Y	1	0	0
0	1	1	$2Y$	0	1	0
1	0	0	$-2Y$	0	1	1
1	0	1	$-Y$	1	0	1
1	1	0	$-Y$	1	0	1
1	1	1	$-0 (= 0)$	0	0	1

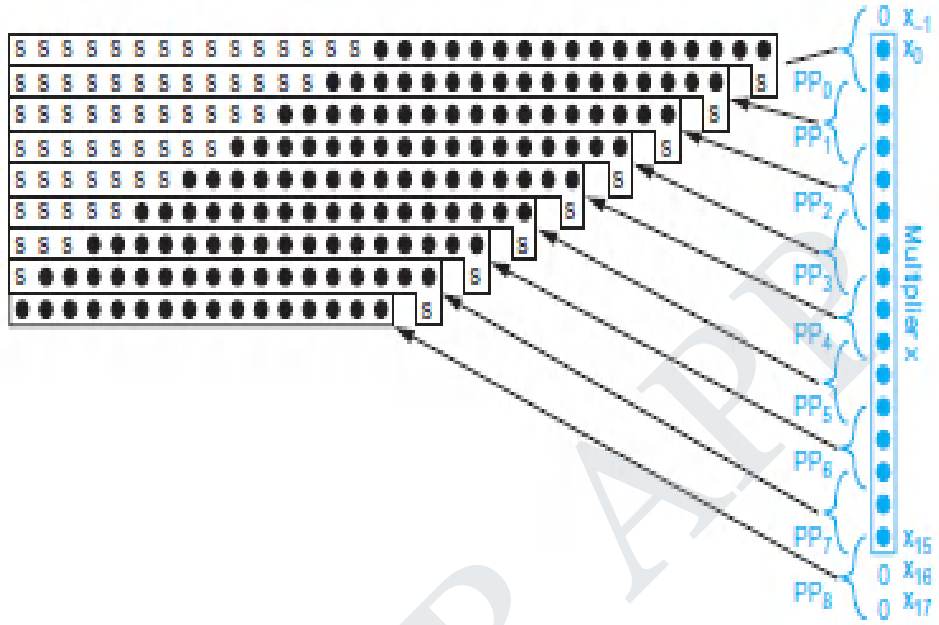
Booth Hardware: *(2 Marks)*

- ✓ Booth encoder generates control lines for each PP
  - Booth selectors choose PP bits



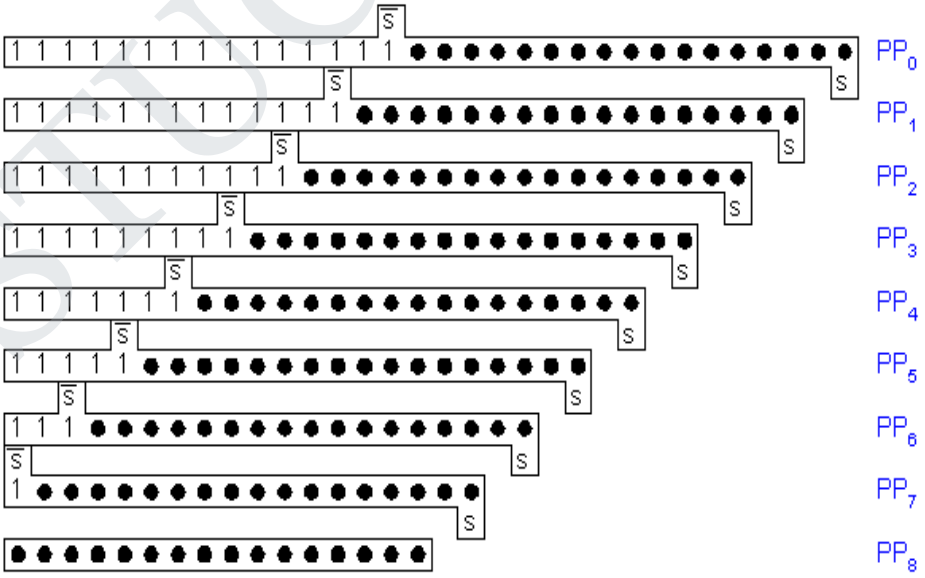
Sign Extension: ***(4 Marks)***

- ✓ Partial products can be negative
  - Require sign extension, which is cumbersome
  - High fanout on most significant bit



Simplified Sign Ext.: ***(4 Marks)***

- ✓ Sign bits are either all 0's or all 1's
  - Note that all 0's is all 1's + 1 in proper column
  - Use this to reduce loading on MSB



Advanced Multiplication: ***(4 Marks)***

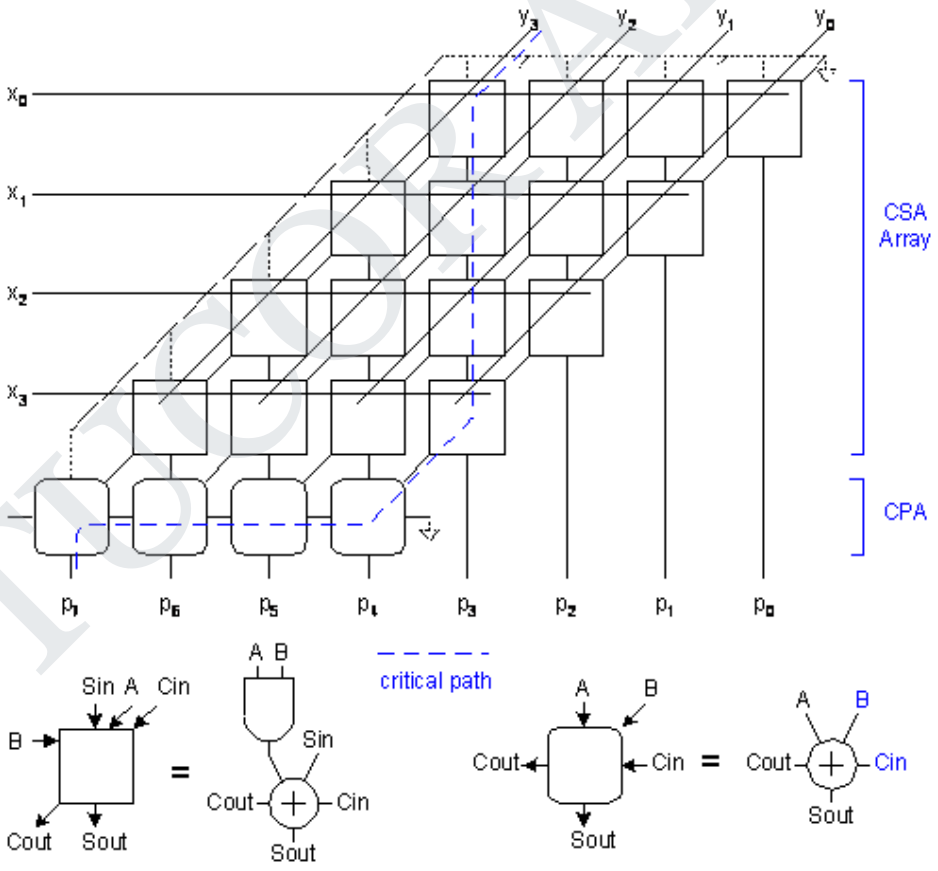
- ✓ Signed vs. unsigned inputs
- ✓ Higher radix Booth encoding
- ✓ Array vs. tree CSA networks

5. Design a 4x4 array multiplier and write down the equation for delay. *(May/Jun-16)*

- **Explanation: *(10 Marks)***

4 X 4 array multiplier: *(5 Marks)*

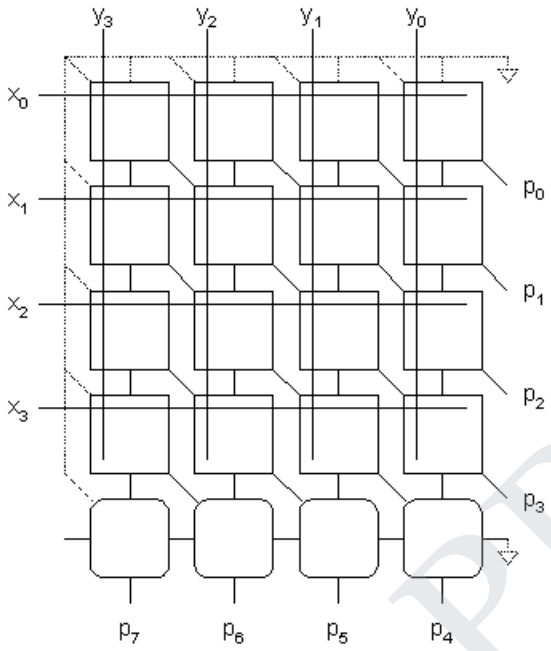
- ✓ Fast multipliers use carry-save adders to sum the partial products.
- ✓ Each cell contains a 2-input AND gate that forms a partial product and a full adder (CSA) to add the partial product into the running sum.
- ✓ The first row converts the first partial product into carry-save redundant form. Each later row uses the CSA to add the corresponding partial product to the carry-save redundant result of the previous row and generate a carry-save redundant result.
- ✓ The least significant N output bits are available as sum outputs directly from CSAs.
- ✓ The array is regular in structure and uses a single type of cell, so it is easy to design and lay out.



- ✓ Total Number of logic units in n-bit × m bit Array Multiplier • n × m two-input ANDs and (m – 1) units of n-bit adders

Rectangular Array: *(5 Marks)*

- ✓ Squash array to fit rectangular floorplan.



- **Delay calculation:** ***(6 Marks)***
  - ✓ Total Delay in n-bit × m bit Array Multiplier
    - Delay due to ANDs in partial products at all level is just one unit AND gate delay.
    - But delay at levels 1 to (m – 1) units of n-bit adders = (m – 1) × delay of one-unit 16-bit adder
    - The delay in adders is very large if ripple carry adders are used.
    - The delay in adders reduced by using carry-look ahead adders.
  - ✓ ***Advantages:***
    - A multiplication method in which an array of identical cells generates new partial product and accumulation of it at the same time
    - We can use pipelines at each level
    - The delay is logarithmically proportional to the bit size of multiplicand and multiplier if we use the high speed array multiplier circuit

6. **Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multiplier.** ***(Nov/Dec-17)***

- **Explanation:** ***(10 Marks)***

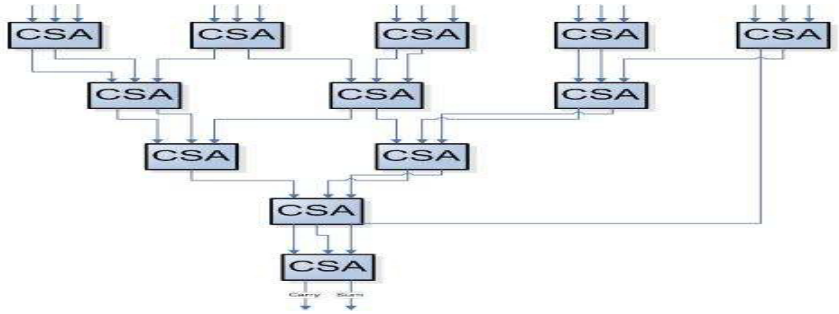
  5 X 4 array multiplier: ***(5 Marks)***
  - ✓ Each cell contains a 2-input AND gate that forms a partial product and a full adder (CSA) to add the partial product into the running sum.
  - ✓ The least significant N output bits are available as sum outputs directly from CSAs.
  - ✓ The array is regular in structure and uses a single type of cell, so it is easy to design and layout.

- **Design*: (5 Marks)***

		B4	B3	B2	B1	B0
			X	A2	A1	A0
		A0B4	A0B3	A0B2	A0B1	A0B0
	A1B4	A1B3	A1B2	A1B1	A1B0	
A1B4	A1B3	A1B2	A1B1	A1B0		
P6	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**

  - ✓ It requires 2 Half adders, 5 Full adders.
  - ✓ So it needs more area. Difficult to design.

- **<u>Wallace multiplier: *(6 Marks)*</u>**
  - ✓ A Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers.
  - ✓ The Wallace tree has three steps:
    - Multiply each bit of one of the arguments, by each bit of the other, yielding n2 results.
    - Reduce the number of partial products to two by layers of full and half adders.
    - Group the wires in two numbers, and add them with a conventional adder.
  - ✓ The second phase works as follows. As long as there are three or more wires with the same weight add a following layer:
    - Take any three wires with the same weights and input them into a full adder. The result will be an output wire of the same weight and an output wire with a higher weight for each three input wires.
    - If there are two wires of the same weight left, input them into a half adder.
    - If there is just one wire left, connect it to the next layer.
  - ✓ The conventional Wallace tree algorithm reduces the propagation by incorporating 3:2 compressors.
  - ✓ However Wallace tree algorithm can also reduce the propagation using higher order compressor. The below fig explains the steps of Wallace tree multiplier.



7. Discuss the details about speed and area trade off. *(Apr/May-17)*

- ✓ Speed, area and power can be trade off through the choice of the supply voltages, transistor threshold and device sizes.
- ✓ Some design techniques are implemented at design time.
- ✓ Transistor width s and lengths can be fixed at the time of design.
- ✓ A reduction in supply voltage results in power savings and thus is the most attractive approach.
- ✓ Reduced supply evenly lowers the power dissipation of all the logic gates.
- ✓ In this approach, non –critical path having timing slack is supplied with low voltage without affecting the system performance.
- ✓ Important design concepts:
  - To select right structure before starting an circuit optimization.
  - Determine the critical timing path through the circuit.
  - Circuit size is not only determined by the number and size of the transistors.
  - An obscure optimization can sometimes help to get a better result.
  - Power and speed can be traded off through a choice of circuit sizing, supply voltages and transistor threshold.

DHANALAKSHMI SRINIVASAN ENGINEERING COLLEGE, PERAMBALUR - 621212

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC6601 - VLSI DESIGN

QUESTION BANK

UNIT V - IMPLEMENTATION STRATEGIES

PART – A

1. What is meant by CBIC? *(Apr/May-17)*

A Cell Based ASIC or Cell Based IC is known as CBIC. It uses predesigned logic cells like AND gate, OR gate, multiplexers & flip-flops.

2. Name the elements in a Configurable Logic Block. *(Apr/May-17)*

- Configurable switch matrix with 4 or 6 inputs
- Some selection circuitry (MUX, etc.)
- Flip-flop

3. What are feed-through cells? State their uses. *(May/June-16)*

Feed through is a piece of metal used to pass a signal through a cell or to a piece in a cell. The connection between the rows of standard cell is made by feed through.

4. State the features of full custom design. *(May/June-16)*

In a Full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

5. What is standard cell based ASIC design. *(Nov/Dec-16)*

A cell-based ASIC (CBIC) uses predesigned logic cells known as standard cells. The standard cell areas also called fle4xible blocks in a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnect in a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

6. What is an antifuse? State its merits and demerits. *(Nov/Dec-16)*

An antifuse is normally high resistance (>100MΩ). on application of appropriate programming voltages, the antifuse is changed permanently to a low-resistance structure(200-500Ω) .

7. Write the various ways of routing procedures. *(Nov/Dec-17)*

- Global routing architecture
- Detailed routing architecture
- FPGA interconnect routing.

8. Differentiate between channeled and channel less gate array.

SL. No	Channeled Gate Array	Channel less Gate Array
1	Only the interconnect is customized	Only the top few mask layers are customized
2	The interconnect uses predefined spaces between rows of base cells	No predefined areas are set aside for routing between cells.
3	Routing is done using the spaces	Routing is done using the area of transistors
4	Logic density is less	Logic density is higher

9. Give the different types of ASIC and give the steps in ASIC design flow.

Types of ASIC:

- Full custom ASICs
- Semicustom ASICs - Standard cell based ASICs, Gate-array based ASICs
- Programmable ASICs - Programmable Logic Device (PLD), Field Programmable Gate Array (FPGA).

Steps in ASIC design flow:

- Design entry
- Logic synthesis system partitioning
- Prelayout simulation
- Floor planning
- Placement
- Routing
- Extraction
- Post layout simulation

10. What is FPGA and VLSI? *(Nov/Dec-17)*

VLSI:

Very-large-scale integration (**VLSI**) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip.

FPGA:

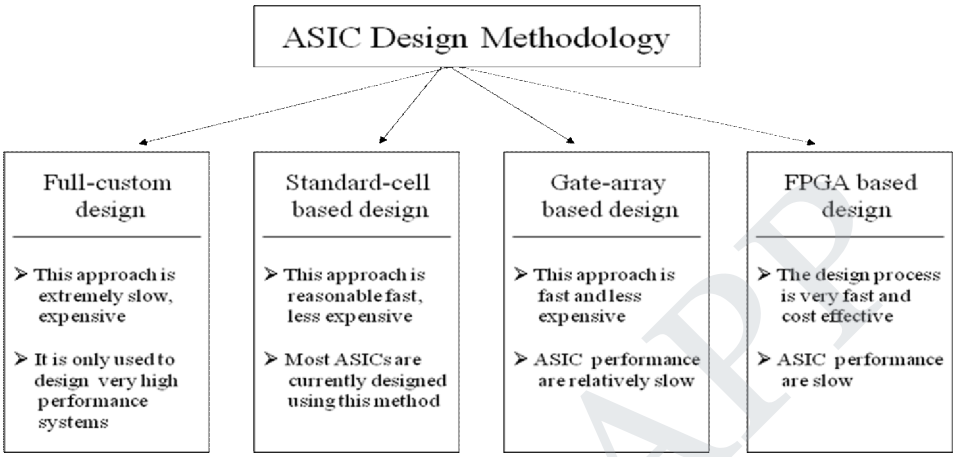
A Field Programmable Gate Array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGA can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of up to about 20,000 equivalent gates.

PART – B (Answers as Hint)

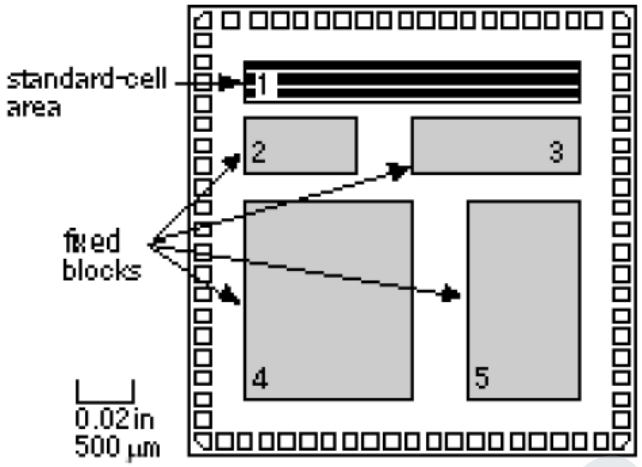
1. **Explain about different types of ASIC with neat diagram.** ***(Nov/Dec-17, Apr/May-17, May/Jun-16, Nov/Dec-16)***

- **Types:** ***(4 Marks)***

ASIC – Application Specific Integrated Circuits

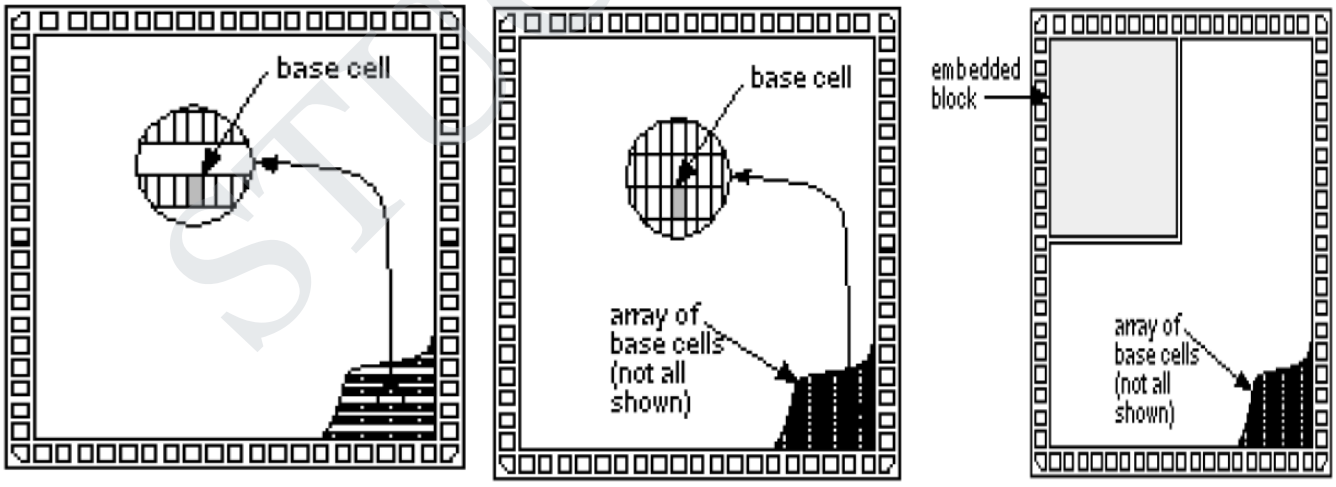


- **A full-custom IC:** ***(4 Marks)***
  - ✓ It includes some logic cells that are customized and all mask layers that are customized. A microprocessor is an example of a full-custom IC.
  - ✓ Full-custom ICs are the most expensive to manufacture and to design.
  - ✓ The manufacturing lead time is typically eight weeks.
- **A Semi-custom IC:** ***(8 Marks)***
  - ✓ Standard-cell–based ASICs: *(4 Marks)*
    - A **cell-based ASIC** (cell-based IC, or **CBIC**) uses predesigned logic cells (AND gates, OR gates, multiplexers, and flipflops, for example) known as **standard cells.**
    - The advantage of CBICs is that designers save time, money, and reduce risk by using a predesigned, pretested, and pre characterized standard-cell library.
    - Standard cells are designed to fit together like bricks in a wall.
    - The microcontroller block may be a fixed-size megacell, you might generate the memory using a memory compiler, and the custom logic and memory controller will be built from flexible standard-cell blocks, shaped to fit in the empty spaces on the chip.
    - The important features of this type of ASIC are as follows:
      - All mask layers are customized transistors and interconnect.
      - Custom blocks can be embedded.
      - Manufacturing lead time is about eight weeks



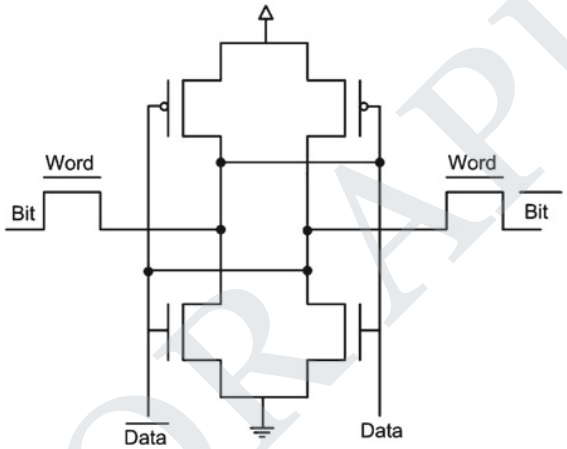
✓ Gate-array–based ASICs: *(4 Marks)*

- In a gate array (sometimes abbreviated to GA) or gate-array–based ASIC the transistors are predefined on the silicon wafer.
- Only the top few layers of metal, which defines interconnect between transistors, are defined by the designer using custom masks.
- To distinguish this type of gate array from other types of gate array, it is often called a masked gate array (MGA).
- There are the following different types of MGA or gate-array–based ASICs:
    - Channeled gate arrays.
    - Channelless gate arrays.
    - Structured gate arrays.

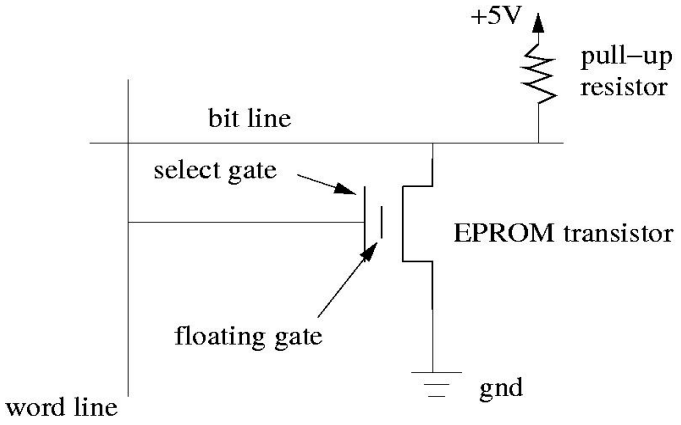


2. Discuss different types of programming technology used in FPGA design. *(Nov/Dec-16)*

- **SRAM-Based Programming Technology: *(6 Marks)***
  - ✓ Static memory cells are the basic cells used for SRAM-based FPGAs.
  - ✓ In an SRAM-based FPGA, SRAM cells are mainly used for following purposes:
    - To program the routing interconnect of FPGAs which are generally steered by small multiplexors.
    - To program Configurable Logic Blocks (CLBs) that is used to implement logic functions.
    - Further SRAM cells are volatile in nature and external devices are required to permanently.

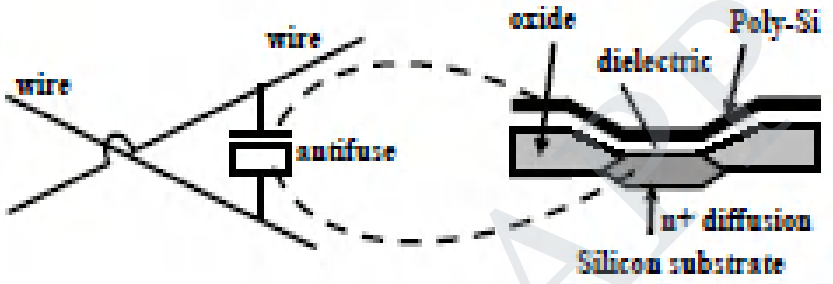


- **Flash Programming Technology: *(5 Marks)***
  - ✓ Flash-based programming technology offers several advantages.
  - ✓ Flash-based programming technology is also more area efficient than SRAM-based programming technology.
  - ✓ Flash-based programming technology has its own disadvantages also.
  - ✓ Unlike SRAM-based programming technology, flash based devices can not be reconfigured/reprogrammed an infinite number of times.
  - ✓ Also, flash-based technology uses non-standard CMOS process.



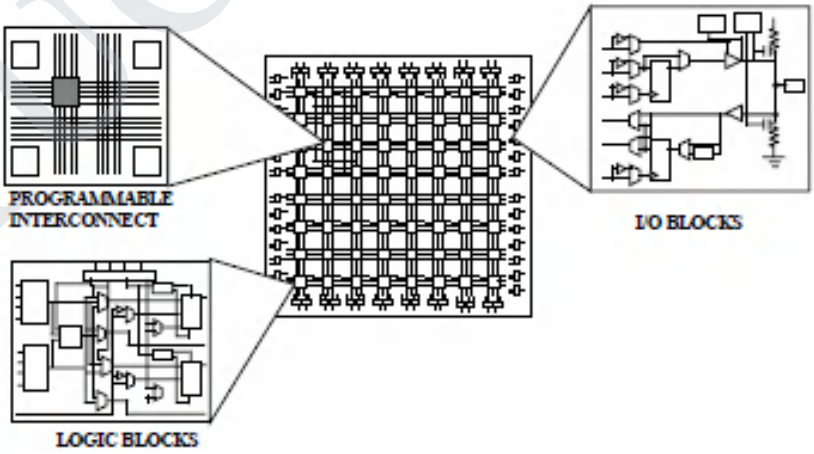
EPROM Programming Technology

- **Anti-fuse Programming Technology: *(5 Marks)***
  - ✓ The primary advantage of anti-fuse programming technology is its low area.
  - ✓ Also this technology has lower on resistance and parasitic capacitance than other two programming technologies.
  - ✓ Further, this technology is non-volatile in nature.
  - ✓ Also, anti-fuse programming technology based devices can not be reprogrammed.
  - ✓ Ideally, one would like to have a programming technology which is reprogrammable, non-volatile, and that uses a standard CMOS process.

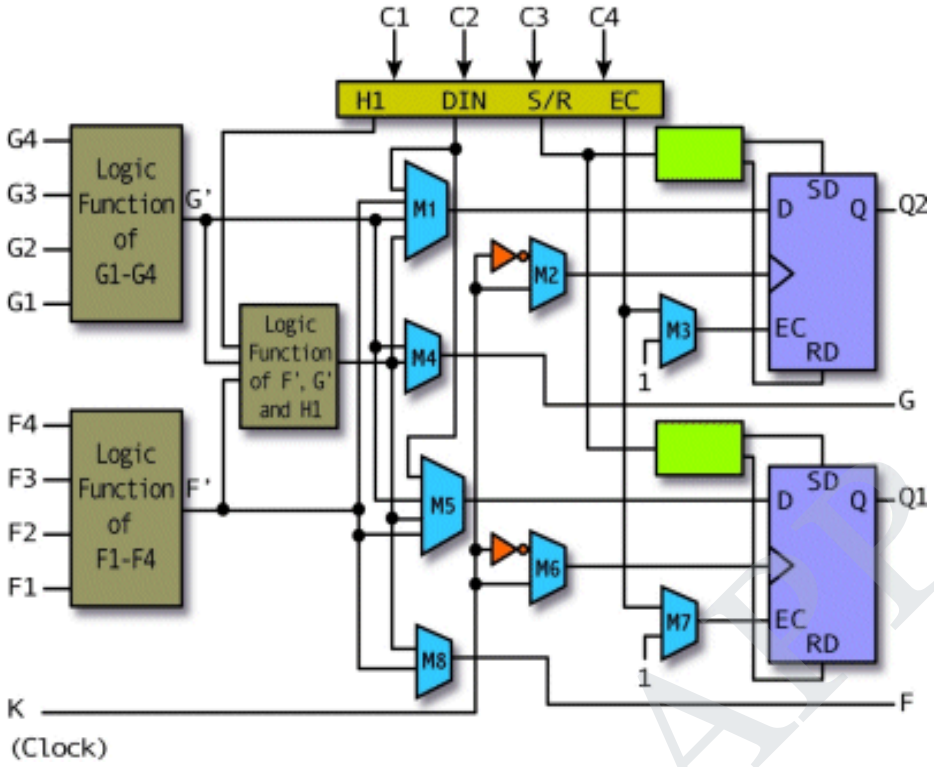


3. Explain about building block architecture of FPGA. *(Nov/Dec-17, Apr/May-17, May/Jun-16)*

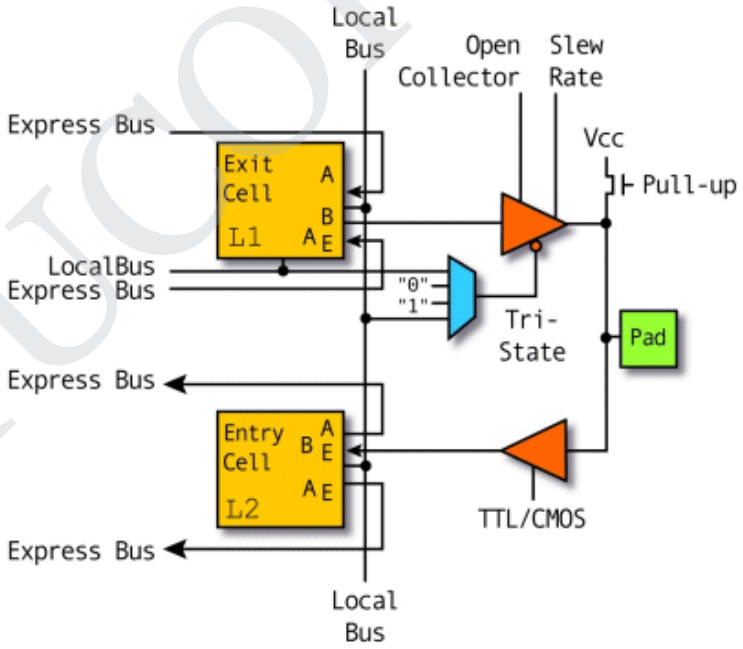
- **FPGA Architecture: *(4 Marks)***
  - ✓ The FPGA architecture consists of three types of configurable elements
    - IOBs – a perimeter of input/output blocks
    - CLBs- a core array of configurable logic blocks
    - Programmable interconnection



- **CLBs: *(4 Marks)***
  - ✓ The CLB contains RAM memory cells and can be programmed to realize any function of five variables or any two functions of four variables.
  - ✓ In the above fig each trapezoidal block represents a multiplexer, which can be programmed to select one of its inputs.
  - ✓ Three different modes of operation for this block: (i)FG mode,(ii)F mode,(iii)FGM mode

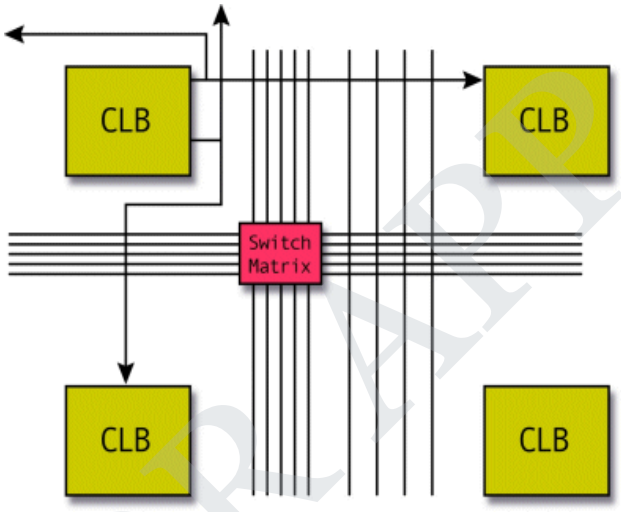


- **IOBs:** ***(4 Marks)***
  - ✓ I/O blocks n special logic blocks at periphery of device for external connections.



- **Programmable Interconnect:** ***(4 Marks)***
  - ✓ The programmable interconnections between the configurable logic blocks and I/O blocks can be made in several ways
    - ***General purpose interconnects:***
      - In general purposes interconnect system, the signals between CLBs or between CLBs and IOBs can be routed through switch matrices as they travel along the horizontal and vertical lines.

- ***Direct interconnect:***
    - Direct interconnection of adjacent CLBs is possible.
    - Long lines are provided to connect CLBs that are far apart.
    - All the interconnections are programmed by storing bits in internal configuration memory cells within the LCA.
    - Long lines provide for high fan-out, low-skew distribution of signals that must travel a relatively long distance.



- ***Vertical & Horizontal Long Line interconnect:***
    - There are four vertical long lines between each pair of adjacent columns of CLBs, and two of these can be used for clocks.
    - There are two horizontal long lines between each pair of adjacent rows of CLBs. The long line spans the entire length or width of the interconnection area.

4. Write short notes on routing procedures involved in FPGA interconnect. *(Apr/May-17)*

- **<u>Global routing:</u> *<u>(8 Marks)</u>***
    - ✓ The global router performs a coarse route to determine, for each connection, the minimum distance path through routing channels that it has to go through.
    - ✓ If the net to be routed has more than two terminals the global router will break the net into a set of two-terminal5 connections and route each set independently.
    - ✓ The global router considers for each connection multiple ways of routing it and chooses the one that passes through the least congested routing channels.
    - ✓ The principal objective of the global router, balancing the usage of the routing channels, is achieved.
    - ✓ Once all connections have been coarse routed, the solution is optimized by ripping up and rerouting each connection a small number of times.
    - ✓ After that, the final solution is passed to the detailed router

- **Detail routing:** ***(8 Marks)***
  - ✓ Detail routing algorithms construct a directed graph from the routing resources to represent the available connection between wires, C blocks, S blocks and logic blocks within the FPGA.
  - ✓ The paths are labeled according to a cost function that takes into account the usage of each wire segment and the distance of the interconnecting points.
  - ✓ The distance is estimated by calculating the wire length in the bounding box of the interconnecting points.
  - ✓ This is done to avoid subsequent iterations of ripping out and re-routing if the solution lies on the near outside of the bounding box.