SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

QUESTION BANK

SUBJECT : EC8095 VLSI Design

SEM / YEAR: VI / III

UNIT I - INTRODUCTION TO MOS TRANSISTOR			
MOS Transistor, CMOS logic, Inverter, Pass Transistor, Transmission gate, Layout Design Rules, Gate Layouts, Stick Diagrams, Long-Channel I-V Charters tics, C-V Charters tics, Non ideal I-V Effects, DC Transfer characteristics, RC Delay Model, Elmore Delay, Linear Delay Model, Logical effort, Parasitic Delay, Delay in Logic Gate, Scaling.			
PART - A			
Q. No	**Questions**	**BTL**	**Competence**
1.	Write the functions of gate terminal.	BTL 1	Remembering
2.	Compare nMOS and pMOS transistor.	BTL 4	Analyzing
3.	What is gate-to-body capacitance?	BTL 1	Remembering
4.	Summarize the flow of current between the source and drain.	BTL 2	Understanding
5.	Draw the 3-input NOR gate using CMOS Logic with truth table.	BTL 3	Applying
6.	Evaluate the structure of MOS.	BTL 5	Evaluating
7.	Illustrate the transmission gate or pass gate with neat sketch.	BTL 3	Applying
8.	Point out the set of design rules for layouts with two metal layers.	BTL 4	Analyzing
9.	What is stick diagram? Sketch the stick diagram for 3 input NAND gate.	BTL 3	Applying
10.	Name the different operating modes of transistor and its current?	BTL 1	Remembering
11.	Explain the equation for describing the channel length modulation effect in nMOS transistor.	BTL 2	Understanding
12.	Mention the Non ideal I-V effects of MOS transistor.	BTL 1	Remembering
13.	Discuss the relationships between voltages for the three regions of operation of a CMOS inverter.	BTL 2	Understanding
14.	Why pMOS transistors are wider than nMOS transistors.	BTL 1	Remembering
15.	Design a RC ladder for Elmore delay with its propagation delay time, $t_{pd.}$	BTL 6	Creating
16.	Define body effect and write the threshold equation including the body effect.	BTL 1	Remembering
17.	Describe the Logical effort of a gate.	BTL 2	Understanding
18.	Analyze Parasitic delay of a gate.	BTL 4	Analyzing

19.	Compare constant field scaling and constant voltage scaling.	BTL 5	Evaluating
20.	Formulate the various critical parameters of Transistor scaling.	BTL 6	Creating
	PART – B		
1.	Explain the structure and working of nMOS and pMOS transistor. (13)	BTL 4	Analyzing
2.	Summarize the following using CMOS logic: (i) Inverter with truth table, (6) (ii) NAND Gate with truth table. (7)	BTL 2	Understanding
3.	Illustrate with necessary diagrams (i) Ideal I-V characteristics of MOS transistors, (6) (ii) C-V characteristics of MOS transistors. (7)	BTL 3	Applying
4.	Analyze the characteristics and working of the following with neat diagram, (i) Pass transistors, (6) (ii) Transmission gate. (7)	BTL 4	Analyzing
5.	(i) Describe in detail about Layout design rules. (7) (ii) Draw the stick diagram and layout diagram for the CMOS gate computing. $Y = \overline{(A+B+C) \bullet D}$. (6)	BTL 1	Remembering
6.	Discuss in detail about the velocity saturation and channel length modulation. (13)	BTL 2	Understanding
7.	Write short notes on: (i) Body Effect, (4) (ii) Subthreshold Condition, (4) (iii) Junction Leakage. (5)	BTL 1	Remembering
8.	Interpret the DC transfer characteristics of CMOS inverter. (13)	BTL 3	Applying
9.	Describe the following with necessary equations. (i) Detailed MOS gate capacitance model, (7) (ii) Detailed MOS diffusion capacitance model. (6)	BTL 2	Understanding
10.	Demonstrate the RC Delay model and Elmore delay model. (13)	BTL 3	Applying
11.	(i) State logical effort and draw the logic gates for different transistor widths. (6) (ii) Define parasitic delay and compare the parasitic delay of common gates for various inputs. (7)	BTL 1	Remembering
12.	Write short notes on: (i) Transistor scaling, (7) (ii) Interconnect scaling. (6)	BTL 1	Remembering
13.	Design a CMOS inverter and formulate the beta ratio effects and noise margin. (13)	BTL 6	Creating
14.	Evaluate Multistage Logic Networks with delay and formulate the expression with an example. (13)	BTL 5	Evaluating
	PART – C		

1.	Explain the Non ideal I-V effects of MOS transistors. (15)	BTL 5	Evaluating
2.	Evaluate the DC transfer characteristics of CMOS inverter. (15)	BTL 5	Evaluating
3.	Design a CMOS compound gate computing and sketch a stick diagram. $F = \overline{(A+B)\bullet(C+D)}$ and write the layout procedure. (15)	BTL 6	Creating
4.	Generalize the following delay models: (i) RC delay model, (5) (ii) Linear delay model, (5) (iii) Parasitic delay. (5)	BTL 6	Creating

UNIT II – COMBINATIONAL LOGIC CIRCUITS			
Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass Transistor Logic, Transmission Gates, Domino, Dual Rail Domino, CPL, DCVSPG, DPL, Circuit Pitfalls. **Power:** Dynamic Power, Static Power, Low Power Architecture.			
PART – A			
Q. No	**Questions**	**BTL**	**Competence**
1.	Write about static CMOS circuits.	BTL 1	Remembering
2.	What is meant by bubble pushing?	BTL 1	Remembering
3.	Generalize the skewed gates and calculate the logical effort for HI-skew inverter.	BTL 3	Applying
4.	Summarize the Multiple threshold voltages for CMOS.	BTL 2	Understanding
5.	Analyse the pseudo-nMOS logic gates.	BTL 4	Analyzing
6.	Construct the symmetric 2-input NOR gate with its truth table.	BTL 6	Creating
7.	Illustrate the Source follower Pull-up logic.	BTL 4	Analyzing
8.	Describe the precharge and evaluation modes of dynamic gates with its timing diagram.	BTL 1	Remembering
9.	Draw the footed and unfooted Inverter, NAND2 and NOR2.	BTL 1	Remembering
10.	Compare the static CMOS, Pseudo-nMOS and dynamic inverters.	BTL 4	Analyzing
11.	Evaluate the Multiple Output Domino Logic (MODL).	BTL 5	Evaluating
12.	Design a circuit to compute F=AB+CD using NANDs and NORs.	BTL 6	Creating
13.	Define Keeper circuit.	BTL 1	Remembering
14.	Discuss the Dual-rail Domino Logic.	BTL 2	Understanding
15.	Show that CMOS gates are very power-efficient.	BTL 3	Applying
16.	Estimate the power dissipation in CMOS circuits.	BTL 2	Understanding
17.	Explain static dissipation in CMOS inverter.	BTL 2	Understanding
18.	Mention the methods used for dynamic power reduction.	BTL 1	Remembering
19.	Interpret the average dynamic power dissipation.	BTL 3	Applying
20.	Justify that CPL is an improvement of CVSL.	BTL 5	Evaluating

PART – B			
1.	Analyse the following static CMOS logic. (i) Bubble pushing, (4) (ii) Compound gates, (4) (iii) Skewed gates. (5)	BTL 4	Analyzing
2.	Illustrate the following circuits in detail. (i) Pseudo-nMOS, (8) (ii) Ganged CMOS. (5)	BTL 2	Understanding
3.	(i) Explain in detail about Cascode voltage switch logic. (8) (ii) Infer the modes of operation in dynamic circuits. (5)	BTL 4	Analyzing
4.	Write short notes on (i) Domino logic, (7) (ii) Dual-rail Domino Logic. (6)	BTL 1	Remembering
5.	Draw the 2-input multiplexers using the following circuit techniques. (i) static CMOS, (3) (ii) Pseudo-nMOS, (3) (iii) CVSL, (3) (iv) Dual-rail Domino. (4)	BTL 1	Remembering
6.	Summarize the following. (i) Pass transistor logic, (7) (ii) Complementary pass transistor logic. (6)	BTL 2	Understanding
7.	Evaluate the design of Differential Cascode Voltage Switch with Pass Gate (DCVSPG). (13)	BTL 5	Evaluating
8.	Describe in detail about the following. (i) Keepers, (5) (ii) Multiple-Output Domino Logic (MODL), (4) (iii) NP and Zipper Domino. (4)	BTL 1	Remembering
9.	Illustrate the Cascode Voltage Switch Logic with neat diagram. (13)	BTL 3	Applying
10.	Classify the types of power dissipation and manipulate each in detail. (13)	BTL 3	Applying
11.	(i) Define Multiple Threshold voltages. (3) (ii) Examine the P/N Ratios for logic gates. (10)	BTL 1	Remembering
12.	Manipulate the various Ratioed circuits for CMOS circuits. (13)	BTL 3	Applying
13.	Discuss the structure and working of CMOS with transmission gates. (13)	BTL 2	Understanding
14.	Construct the various low-power reduction techniques. (13)	BTL 6	Creating
PART – C			
1.	Summarize the following. (i) Input ordering delay effect, (5) (ii) Asymmetric gates, (5) (iii) P/N ratios. (5)	BTL 5	Evaluating

2.	Evaluate the following Dynamic circuits. (i) Domino logic, (5) (ii) Dual-rail Domino logic, (5) (iii) Keepers. (5)	BTL 5	Evaluating
3.	Design the Ratioed circuits and its types with neat diagram. (15)	BTL 6	Creating
4.	Formulate the following power dissipation in CMOS circuits. (i) Static dissipation, (7) (ii) Dynamic dissipation. (8)	BTL 6	Creating

UNIT III - SEQUENTIAL CIRCUIT DESIGN			
Static latches and Registers, Dynamic latches and Registers, Pulse Registers, Sense Amplifier Based Register, Pipelining, Schmitt Trigger, Monostable Sequential Circuits, Astable Sequential Circuits. **Timing Issues:** Timing Classification Of Digital System, Synchronous Design.			
PART - A			
Q. No	**Questions**	**BTL**	**Competence**
1.	Define bistability principle.	BTL 1	Remembering
2.	Name the approaches used to accomplish the bistable circuit.	BTL 1	Remembering
3.	Show the mode of operation of low voltage static latches.	BTL 3	Applying
4.	Summarize the timing properties of Master-slave registers.	BTL 2	Understanding
5.	Analyse the working of dynamic positive edge-triggered register when clk=0.	BTL 4	Analyzing
6.	Draw the Multiplexer-based nMOS latch.	BTL 1	Remembering
7.	Describe the operation of C^2MOS register.	BTL 2	Understanding
8.	Evaluate the True Single-Phase Clocked Register (TSPCR).	BTL 5	Evaluating
9.	What is the role of transistor sizing in TSPC Edge-Triggered Register?	BTL 1	Remembering
10.	Mention the advantages of pipelined operation.	BTL 1	Remembering
11.	Discuss the sense-amplifier based registers.	BTL 2	Understanding
12.	Sketch the circuit of latch-based pipeline using C^2MOS latches.	BTL 4	Analyzing
13.	Explain the operation modes for NORA logic style.	BTL 4	Analyzing
14.	List out the timing parameters of the sequential circuit in synchronous design.	BTL 1	Remembering
15.	Deduce the properties of Schmitt trigger.	BTL 5	Evaluating
16.	Design a voltage-controlled oscillator based on current-starved inverters.	BTL 6	Creating
17.	Examine the uses of Schmitt trigger.	BTL 3	Applying
18.	Estimate the use of address transition detection (ATD) circuit.	BTL 2	Understanding
14.	Develop the positive and negative clock skew scenarios.	BTL 6	Creating
20.	Classify the transition of signals at predetermined periods.	BTL 3	Applying
PART-B			
1.	State and explain the Bistability principle and its two different approaches. (13)	BTL 1	Remembering

2.	Discuss in detail: (i) Master-Slave Edge-Triggered Register, (7) (ii) Timing properties of Multiplexer-Based Master-Slave registers. (6)	BTL 2	Understanding
3.	Write short notes on: (i) Multiplexer-Based Latches, (7) (ii) Low-Voltage Static Latches. (6)	BTL 1	Remembering
4.	Explain the C^2MOS Register with CLK-$\overline{CLK}$ clocking approach. (13)	BTL 4	Analyzing
5.	Evaluate the True Single-Phase Clocked Register (TSPCR) and TSPC Edge-Triggered register. (13)	BTL 5	Evaluating
6.	Illustrative the following Alternative Register styles. (i) Pulse Registers, (7) (ii) Sense-Amplifier-Based Registers. (6)	BTL 3	Applying
7.	Classify the various Pipeling techniques and explain in detail. (13)	BTL 3	Applying
8.	Summarize the following. (i) Latch versus Register based pipeline, (6) (ii) NORA-CMOS logic style for pipelined structures. (7)	BTL 2	Understanding
9.	(i) Define Schmitt trigger and its properties. (4) (ii) Describe Schmitt trigger and its CMOS implementation with neat diagram. (9)	BTL 1	Remembering
10.	Construct the clock-distribution techniques dealing with clock skew and jitter. (13)	BTL 6	Creating
11.	Describe in detail: (i) Synchronous interconnect, (3) (ii) Mesochronous interconnect, (3) (iii) Plesiochronous interconnect, (3) (iv) Asynchronous interconnect. (4)	BTL 1	Remembering
12.	Examine the Monostable Sequential circuits and Astable circuits with neat an example. (13)	BTL 2	Understanding
13.	Analyze the basics of synchronous timing, clock skew, clock jitter and combined impact of skew and jitter. (13)	BTL 4	Analyzing
14.	Manipulate the various sources of skew and jitter. (13)	BTL 3	Applying
	PART-C		
1.	Evaluate the Master-Slave Edge-Triggered register with its timing properties and Non-ideal clock signals. (15)	BTL5	Evaluating
2.	Summarize the following: (i) Dynamic transmission-gate edge-triggered registers, (5) (ii) C^2MOS-A clock-skew insensitive approach, (5) (iii) True single-phase clocked register. (5)	BTL5	Evaluating
3.	Formulate the following Nonbistable sequential circuits (i)) The Schmitt Trigger, (5) (ii) Monostable Sequential Circuits, (5) (iii) Astable Circuits. (5)	BTL 6	Creating
4.	Design the clock distribution strategies for three generations of the digital alpha microprocessors. (15)	BTL 6	Creating

UNIT IV - DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM

Arithmetic Building Blocks: Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed tradeoffs, Case Study: Design as a tradeoff.
Designing Memory and Array structures: Memory Architectures and Building Blocks, Memory Core, Memory Peripheral Circuitry.

PART-A

Q. No	Questions	BTL	Competence
1.	Obtain the critical path delay of 4 bit ripple carry adder and draw the circuit.	BTL 6	Creating
2.	Summarize about carry propagation delay. Mention its effect in circuits.	BTL 2	Understanding
3.	List out the components of Data path.	BTL 1	Remembering
4.	Why is barrel Shifters very useful in the designing of arithmetic circuits?	BTL 2	Understanding
5.	Interpret a partial product selection table using modified 3-bit booth's recoding multiplication.	BTL 5	Evaluating
6.	What is one time programmable memories?	BTL 1	Remembering
7.	Draw the structure of 6- transistor SRAM cell.	BTL 3	Applying
8.	List the advantages and disadvantages of full adder design using static CMOS.	BTL 1	Remembering
9.	Analyze the concept of Dynamic voltage scaling and list its advantages.	BTL 4	Analyzing
10.	Define Clock gating.	BTL 1	Remembering
11.	Create a schematic for Sleep transistors used on both supply and ground.	BTL 6	Creating
12.	Examine the need of VTCMOS.	BTL 4	Analyzing
13.	Give the applications of CAM.	BTL 2	Understanding
14.	Explain the inverting property of full adder.	BTL 4	Analyzing
15.	How to design a column multiplexer with separate decoder circuit?	BTL 3	Applying
16.	Write the full adders output in terms of propagate and generate.	BTL 1	Remembering
17.	Classify Power optimization techniques for latency and throughput constrained design.	BTL 3	Applying
18.	Write the charge-share equation for DRAM.	BTL1	Remembering
19.	Sketch a sense amplifiers CMOS circuit.	BTL2	Understanding
20.	Elaborate the Concept of large SRAMs.	BTL 5	Evaluating
	PART-B		
1.	(i) Describe ripple carry adder and derive the expression for worst case delay. (10) (ii) Write a note on Carry Bypass adders. (3)	BTL 1	Remembering
2.	Examine the concept of carry look ahead adder and discuss its types. (13)	BTL 4	Analyzing
3.	Outline the operation of a basic 4 bit adder. Describe the different approaches of improving the speed of the adder. (13)	BTL 1	Remembering
4.	Illustrate the concepts of faster decoder and sum-addressed decoder circuit. (13)	BTL 3	Applying
5.	Define SRAM memory cell operation and summarize short note on (i) Read operation, (7)	BTL 1	Remembering

	(ii) Write operation. (6)		
6.	Demonstrate the bitline conditioning circuitry with necessary circuit diagram. (13)	BTL3	Applying
7.	Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multiplier. (13)	BTL 6	Creating
8.	Summarize the Multi-ported SRAM and Register file CMOS logic circuit. (13)	BTL2	Understanding
9.	Evaluate the architecture of large memory array with subarray memory Circuitry. (13)	BTL5	Evaluating
10.	Give a note on linear carry select adder. (13)	BTL 2	Understanding
11.	Examine the operation of : (i) Static CMOS adders. (7) (ii) Mirror adder (6)	BTL 4	Analyzing
12.	Analyse the operation of booth multiplication with suitable examples. Justify how booth algorithms speed up the multiplication process. (13)	BTL 4	Analyzing
13.	Discuss the data paths in digital processor architectures. (13)	BTL 2	Understanding
14.	Write detailed note about any two multiplier circuit. (13)	BTL 1	Remembering
	PART-C		
1.	(i) Construct 4 X 4 array type multiplier and find its critical path delay. (8) (ii) Implement a 4 input and 4 output barrel shift adder using NMOS logic. (7)	BTL5	Evaluating
2.	Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multiplier. (15)	BTL6	Creating
3.	Explain a Modified Booth algorithm with a suitable example. (15)	BTL5	Evaluating
4.	Discuss detail about the DRAM sub array and open bitlines architecture. (15)	BTL6	Creating

UNIT V - IMPLEMENTATION STRATEGIES AND TESTING			
FPGA Building Block Architectures, FPGA Interconnect Routing Procedures. Design for Testability: Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan.			
PART-A			
Q. No	**Questions**	**BT Level**	**Competence**
1.	What is fault model?	BTL 1	Remembering
2.	Point out the common techniques of ad hoc testing.	BTL 4	Analyzing
3.	List out the different approaches of Design for testability.	BTL 1	Remembering
4.	Narrate about stuck-at faults and state their uses.	BTL 3	Remembering
5.	Classify the types of stuck-at faults.	BTL 3	Applying
6.	Give a note on short circuit and open circuit faults.	BTL 2	Understanding
7.	State the features of boundary scan method.	BTL 1	Remembering
8.	Differentiate between observability and controllability.	BTL 4	Analyzing
9.	Describe about ATPG design scan?	BTL 1	Remembering

10.	Define Fuse based FPGA.	BTL 1	Remembering
11.	Name the two different types of routing in FPGA.	BTL 2	Understanding
12.	Develop a PRSG logic circuit for BIST test.	BTL 6	Creating
13.	Draw the block diagram of test data register..	BTL 6	Creating
14.	Compare serial and parallel scan in ad hoc testing.	BTL 4	Analyzing
15.	Summarize the functions of Programmable Interconnect Points in FPGA.	BTL 5	Evaluating
16.	Give an example circuit for delay fault CMOS logic circuit.	BTL 2	Understanding
17.	Determine the power supply of CMOS logic circuit using IDDQ fault test.	BTL 5	Evaluating
18.	Illustrate the Test Access Port connection details.	BTL 3	Applying
19.	Outline the steps for CMOS circuit IDDQ test.	BTL 2	Understanding
20.	Write the various ways of routing procedure.	BTL 1	Remembering
	PART-B		
1.	(i) Explain the manufacturing test principle with an example of digital logic circuits. (8) (ii) Give a short note on stuck-at faults model. (5)	BTL1	Remembering
2.	Describe the various types of ad hoc testing techniques with neat diagram. (13)	BTL 2	Understanding
3.	(i) List out the common testing technique for ad hoc test. (8) (ii) Outline the need of Observability for integrated circuits. (5)	BTL 1	Remembering
4.	Illustrate the concepts of short circuit and open circuit fault. (13)	BTL 3	Applying
5.	Explain the architecture of parallel scan testing method. (13)	BTL 4	Analyzing
6.	Examine the boundary scan architectures and explain how to test the circuit board level and system level. (13)	BTL 4	Analyzing
7.	Identify and Explain the BIST block structure along its components. (13)	BTL 1	Remembering
8.	(i) Discuss the types of FPGA routing techniques. (7) (ii) Demonstrate the basic types of programmable elements of FPGA. (6)	BTL 2	Understanding
9.	Elaborate the small finite state machine of TAP architecture. (13)	BTL 6	Creating
10.	(i) Compare two types of Ad hoc scanning methods. (10) (ii) Point out the Test access port signals. (3)	BTL 4	Analyzing
11.	Draw and explain the building blocks of FPGA. (13)	BTL 2	Understanding
12.	Draw the block diagram of BILBO\BIST and explain each unit operation. (13)	BTL 3	Applying
13.	Summarize the steps involved in design for manufacturability to increase the yield of optimized circuit. (13)	BTL 5	Evaluating
14.	Write short notes on (i) TAP controller (6) (ii) Instruction register (7)	BTL 1	Remembering
	PART-C		
1.	With neat sketch explain the CLB, IOB and programmable interconnects of an FPGA device. (15)	BTL 5	Evaluating
2.	Draw and explain the building blocks of FPGA with different fusing technologies. (15)	BTL 6	Creating

3.	(i) Explain about building block architecture of TAP. (10) (ii) Write short notes on routing procedures involved in FPGA interconnect. (5)	BTL 5	Evaluating
4.	Discuss in detail about different types of scan design method and explain with neat diagram. (15)	BTL 6	Creating