EC8252- ELECTRONIC DEVICES

I YEAR / II SEMESTER B.E. (ME)

UNIT – I

SEMICONDUCTOR DIODE

COMPILED BY

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DEPARTMENT OF MEDICAL ELECTRONICS

SENGUNTHAR COLLEGE OF ENGINEERING – TIRUCHENGODE

CREDIT POINT

ANNA UNIVERSITY, CHENNAI

AFFILIATED INSTITUTIONS

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B.E. MEDICAL ELECTRONICS

SEMESTER II

S.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	HS8251	Technical English – II	4	0	0	4
2.	MA8251	Engineering Mathematics – II	4	0	0	4
3.	PH8253	Physics for Electronics Engineering	3	0	0	3
4.	BM8251	Engineering Mechanics for biomedical Engineers	3	0	0	3
5.	EC8251	Circuit Analysis	4	0	0	4
6.	**EC8252**	**Electronic Devices**	**3**	**0**	**0**	**3**
PRACTICAL						
7.	GE8261	Engineering Practices Laboratory	0	0	4	2
8.	EC8261	Circuits and Devices Laboratory	0	0	3	2
TOTAL			**21**	**0**	**8**	**25**

SYLLABUS

EC8252 ELECTRONIC DEVICES L T P C

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UNIT I SEMICONDUCTOR DIODE 9

PN junction diode, Current equations, Energy Band diagram, Diffusion and drift current densities, **forward and reverse bias characteristics, Transition and Diffusion Capacitances, Switching Characteristics, Breakdown in PN Junction Diodes.**

UNIT II BIPOLAR JUNCTION TRANSISTORS 9

NPN -PNP -Operations-Early effect-Current equations – Input and Output characteristics of CE, CB, CC - Hybrid -π model - h-parameter model, Ebers Moll Model- Gummel Poon-model, Multi Emitter Transistor.

UNIT III FIELD EFFECT TRANSISTORS 9

JFETs – Drain and Transfer characteristics,-Current equations-Pinch off voltage and its significance- MOSFET- Characteristics- Threshold voltage -Channel length modulation, D-MOSFET, E-MOSFET- Characteristics – Comparison of MOSFET with JFET.

UNIT IV SPECIAL SEMICONDUCTOR DEVICES 9

Metal-Semiconductor Junction- MESFET, FINFET, PINFET, CNTFET, DUAL GATE MOSFET, Schottky barrier diode-Zener diode-Varactor diode –Tunnel diode- Gallium Arsenide device, LASER diode, LDR.

UNIT V POWER DEVICES AND DISPLAY DEVICES 9

UJT, SCR, Diac, Triac, Power BJT- Power MOSFET- DMOS-VMOS. LED, LCD, Photo transistor, Opto Coupler, Solar cell, CCD.

TOTAL : 45 PERIODS

TEXT BOOKS:

1. Donald A Neaman, —Semiconductor Physics and Devices||, Fourth Edition, Tata Mc GrawHill Inc. 2012.
2. Salivahanan. S, Suresh Kumar. N, Vallavaraj.A, —Electronic Devices and circuits||, Third Edition, Tata McGraw- Hill, 2008.

REFERENCES:

1. R.S.Sedha, — A Text Book of Applied Electronics|| S.Chand Publications, 2006.
2. Yang, —Fundamentals of Semiconductor devices||, McGraw Hill International Edition, 1978. 3. Robert Boylestad and Louis Nashelsky, —Electron Devices and Circuit Theory|| Pearson Prentice Hall, 10th edition, July 2008. Instrumentation", CRC Press, 2004.

UNIT – I

SEMICONDUCTOR DIODE

- **PN junction diode**
- **Current equations**, Energy Band diagram
- Diffusion and drift current densities
- **forward and reverse bias characteristics**
- **Transition and Diffusion Capacitances**
- **Switching Characteristics**
- **Breakdown in PN Junction Diodes**

LIST OF IMPORTANT QUESTIONS

UNIT I - SEMICONDUCTOR DIODE

PART- A

1. **What is meant by avalanche breakdown? (N/D-19)**
2. **Give the expression for diffusion current density (N/D-19)**
3. **Determine the total forward bias current density in a PN junction diode under an applied forward bias voltage of 0.65 V at 300K. Assume Js=4.155 x 10^{-11} A/Cm^2 (A/M-2019)**
4. **Define Diffusion capacitance (A/M-2019)**
5. **Write down equation for diode current. (A/M 2018)**
6. **State the relationship between diffusion capacitance and diode current in a PN diode (A/M 2018) .**
7. **State the difference between diffusion current and drift current?(N/D-2017)**
8. **Calculate the built in potential barrier in a pn junction diode having following specification: T= 300K, Na = 10^{18} cm^{-3} , Nd = 10^{15} cm^{-3} and n_i= 1.5 x 10^{10} $cm^{-3.}$ (N/D-2017)**
9. **Define Peak Inverse Voltage (PIV). (A/M-2017)**
10. **Find the voltage at which the reverse current in a germanium PN junction diode attains a value of 90% of its saturation value at room temperature. (A/M – 2017)**

PART-B

1. The phosphorous (donor) concentration in a region of a silicon crystal varies linearly from a concentration of $n_0 = 10^{14}$ cm^{-3} at x=0 mm to a concentration of $n_1 = 10^{17}$ cm^{-3} at x=1 mm. The diffusion constant for electrons is Dn = 22.5 cm^2/s, the diffusion constant for holes is D_p = 5.2 cm^2/s, and the temperature is 300 K. What is the diffusion current density in the positive x-direction? (N/D-2019)

2. Explain the theory of PN junction diode and derive its diode current equation. (OR) Explain the operation of PN junction under zero voltage applied bias condition and derive the expression for built in potential barrier. (OR) Explain the basic structure of the PN junction. (OR) Describe about V – I Characteristics of PN junction diode. (OR) With neat diagram describe the Characteristics of forward and reverse biased PN junction diode. (OR) Derive the current equation of diode. (OR) Derive an expression for PN junction diode forward and reverse currents with suitable diagram. (OR) Explain the theory of PN junction diode when forward and reverse biased derive its diode current equation. (OR) From the basic concepts, derive the expression for the ideal PN junction current. (M/J 2014) (N/D 2014) (A/M 2015) (N/D 2015) (A/M 2016) (N/D 2016) (A/M 2017) (N/D 2017) (A/M 2018) (A/M-2019) (N/D-2019)

3. Derive the transition and diffusion capacitance in PN diode. (N/D-2019) (OR)

(i)Derive the expression of the Space Charge or Transition capacitance of PN diode under reverse bias with a neat diagram.

(ii)Derive the expression for diffusion capacitance of PN junction diode.

4. Explain and derive current components and switching characteristics of diode. (OR) Write short notes on switching characteristics of diode. (OR) Discuss about the switching characteristics of PN junction diode with suitable diagram (M/J 2014) (N/D 2014) (N/D 2015) (A/M 2017) (N/D 2017) (A/M-2019)

5. Explain about breakdown mechanism in PN junction diode. (A/M-2019)

PART – A

1. What is meant by avalanche breakdown? (N/D-19)

As Voltage approaches the breakdown voltage V_{BD} (Reverse breakdown voltage), the value of M (carrier multiplication factor) will become infinite and there is a rapid increase in carrier density and a corresponding increase in current. Because of the cumulative increase in carrier density after each collision, the process is known as **avalanche breakdown.**

2. Give the expression for diffusion current density (OR) Define diffusion current and drift current? (N/D-14) (A/M-15) (M/J-16) (N/D-19)

DIFFUSION CURRENT:

- In a semiconductor material, the charge carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers.
- Thus the movement of charge carriers takes place resulting in a current called diffusion current.

Diffusion current density due to holes is $J_p = - q D_p \frac{dp}{dx}$ A/cm²

Diffusion current density due to electrons is $J_n = q D_n \frac{dn}{dx}$ A/cm²

D_n & D_p ⇨ Diffusion coefficients

$\frac{dn}{dx}$ & $\frac{dp}{dx}$ ⇨ concentration gradients for electrons and holes.

DRIFT CURRENT:

- When an electric field is applied across the semiconductor material, the holes move towards the negative terminal of the battery and electrons move towards the positive terminal.
- This combined effect of movement of the charge carriers constitutes a current known as the drift current.
- The equation for drift current density due to electrons is $J_n = qn\mu E$ A/cm²
- The equation for drift current density due to holes is $J_p = qp\mu E$ A/cm²

Where n ⇨ No.of free electrons

p ⇨ No.of holes

μ ⇨ Mobility of electrons in cm²/V-s

μ ⇨ Mobility of holes in cm²/V-s

E ⇨ Applied electric field intensity in V/cm

q ⇨ Charge of an electron (1.6x10ˆ-19 coulomb)

3. Determine the total forward bias current density in a PN junction diode under an applied forward bias voltage of 0.65 V at 300K. Assume Js=4.155 x 10^{-11} A/Cm^2 (A/M-2019)

4. Define Diffusion capacitance (A/M-2019) , What is diffusion or storage capacitance?

- The capacitance that exists in a forward biased junction is called a diffusion or storage capacitance (C_D) due to diffusion of minority carriers on both sides of the junctions.
- As a result the holes in the N-region and electrons in the P-region are separated by a very thin depletion layer which leads to capacitance. It can be expressed as

Diffusion capacitance (C_D) = τ I / η V_T

τ ⇨ Mean life time for holes and electrons

I ⇨ Diode forward current

V_T ⇨ Thermal voltage (kT/q)

η ⇨ A constant (or) Emission coefficient(1 for germanium diode and 2 for silicon diode)

5. Write down equation for diode current. (A/M 2018)

Diode current equation is

$I=I_0 [e^{v/\eta V_T}-1]$ Amps

I= Diode current

I_0=Diode Reverse saturation current in amps

V= External Voltage Applied

V_T= voltage equivalent of temperature in volts (Thermal voltage) (V_T = kT/q)

At room Temp T=300K, V_T= 26mv

η= A constant (or) Emission coefficient (1 for germanium diode and 2 for silicon diode

6. State the relationship between diffusion capacitance and diode current in a PN diode (A/M 2018)

Diffusion capacitance

- The capacitance that exists in a forward biased junction is called a diffusion or storage capacitance (C_D) due to diffusion of minority carriers on both sides of the junctions.
- As a result the holes in the N-region and electrons in the P-region are separated by a very thin depletion layer which leads to capacitance. It can be expressed as

Diffusion capacitance (C_D) = $C_D = \frac{\tau I}{\eta V_T}$

τ ⇨ Mean life time for holes and electrons

I⇨ Diode forward current

V_T ⇨ Thermal voltage (kT/q)

η ⇨ A constant (or) Emission coefficient(1 for germanium diode and 2 for silicon diode)

Diode current

The current in a p-n diode is due to carrier recombination or generation somewhere within the p-n diode structure.

Diode current equation is

$I=I_0 [e^{v/\eta V_T}-1]$ Amps

I= Diode current

I_0=Diode Reverse saturation current in amps

V= External Voltage Applied

V_T= voltage equivalent of temperature in volts (Thermal voltage) (V_T = kT/q)

At room Temp T=300K, V_T= 26mv

η= A constant (or) Emission coefficient (1 for germanium diode and 2 for silicon diode.

7. State the difference between diffusion current and drift current? (N/D-2017)

DRIFT CURRENT	DIFFUSION CURRENT
It is developed due to potential gradient	It is developed due to charge concentration gradient.
This phenomenon is found both in metals and semiconductors	It is found only in semiconductors.

Drift current density due to electrons is Jn = qnμ E A/cm² Drift current density due to holes is Jp = qpμ E A/cm²	Diffusion current density due to electrons is Jn= q Dn dn/dx A/cm². Diffusion current density due to holes is Jp= - q Dp dp/dx A/cm²

8. Calculate the built in potential barrier in a pn junction diode having following specification: T= 300K, Na = 10^{18} cm^{-3} , Nd = 10^{15} cm^{-3} and n_i= 1.5 x 10^{10} $cm^{-3.}$ (N/D-2017)

9. Define Peak Inverse Voltage (PIV). (A/M-2017)

- It is the maximum reverse voltage that can be applied to the PN junction.
- If the voltage across the junction exceeds PIV, under reverse bias condition, the junction gets damaged due to excessive heat.

10. Find the voltage at which the reverse current in a germanium PN junction diode attains a value of 90% of its saturation value at room temperature. (A/M – 2017)

Solution:

We know that the current of a PN junction diode is

$$I = I_o\left(e^{\frac{V}{V_T}} - 1\right)$$

Therefore, $$-0.90\, I_o = I_o\left(e^{\frac{V}{V_T}} - 1\right)$$

where $$V_T = \frac{T}{11,600} = 26 \text{ mV}$$

$$-0.9 = e^{\frac{V}{0.026}} - 1$$

$$0.1 = e^{\frac{V}{0.026}}$$

Therefore, $$V = -0.06 \text{ V}$$

11. What is barrier potential? (N/D 2016)

Due to immobile positive charges on n side and negative charges on p side, there exists an electric field across the junction. This creates potential difference across the junction which is called **barrier potential, junction potential, built-in potential** or **cut-in voltage of p-n junction.**

12. Define mass action law? (M/J-2014) (N/D 2016)

- Under thermal equilibrium for any semiconductor, the product of the number of holes and the number of electrons is constant and is independent of the amount of donor and acceptor impurity doping.
- This relation is known as Mass action law and is given by,

$$n \cdot p = n_i^2$$

Where n is the number of free electrons per unit volume

P is the number of holes per unit volume

n_i is the intrinsic concentration

13. Define storage time. (A/M-2016)

- When the diode is switched from forward biased to reverse biased, the minority charge carriers remain stored and decrease slowly to zero.
- This time for which minority charge carriers remain stored is called storage time.

14. List some applications of PN diode. (N/D 2015)

- Rectifiers in DC power supplies
- Switch in digital logic circuits used in computers
- Clamping network used as DC restorer in TV receivers and voltage multipliers.
- Clipping circuits used as wave shaping circuits used in computers, radars, radio and TV receivers
- Demodulation (detector) circuits

15. Consider a gallium arsenide sample at T=300K with doping concentration of N_a=0 and N_D=10^{16} cm^{-3} and μ_n = 8500. Calculate the drift current density if the applied electric field is E=10V/cm. (N/D - 2015)

Ans. :

$$N_d = 10^{16}\ cm^{-3},\ \mu_n = 8500,\ E = 10\ V/cm$$

$$J = N_d \mu_n qE$$

$$= 10^{16} \times 8500 \times 1.6 \times 10^{-19} \times 10$$

$$\therefore \quad J = 136\ A/cm^2$$

16. Consider a Si PN junction at T=300K so that n_i=1.5x10^{10} cm^{-3}. The n type doping is 1x10^{16} cm^{-3} and a forward bias of 0.60V is applied to the PN junction. Calculate the minority hole concentration at the edge of the space charge region. (A/M -2015)

Ans. : The hole concentration at the edge of the space charge region is,

$$p_n = p_{n0}\, e^{V / V_T}$$

$$p_{n0} = \frac{n_i^2}{N_D} = \frac{(1.5\times10^{16})^2}{1\times10^{22}}$$

$$p_n = 2.25 \times 10^{10}\, e^{0.6 / 0.0259}$$

$$= 2.588 \times 10^{20} / m^3$$

Note that $n_i = 1.5 \times 10^{10} / cm^3 = 1.5 \times 10^{16} / m^3$

17. Sketch the forward bias characteristics of a PN junction diode? (A/M-2015)

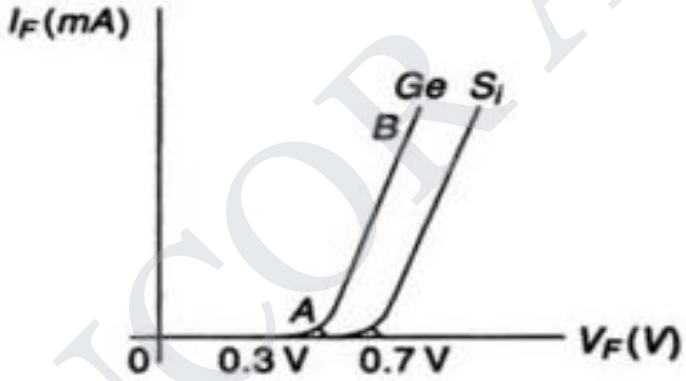


Fig. 4.10 *V–I* characteristics of a diode under forward bias condition

18. Consider a Si PN junction at T=300K with doping concentration of $N_a=10^{16}$ cm^{-3} and $N_D=10^{15}$ cm^{-3}. Assume that $n_i=1.5x10^{10}$ cm^{-3}. Calculate width of space charge region in a PN junction, when a reverse bias voltage V_R=5V is applied. (N/D 2014)

Sol. : $T = 300\,°K$, $N_A = 10^{16}\ /\ cm^3$, $N_D = 10^{15}\ /\ cm^3$
$n_i = 1.5\times10^{10}\ /\ cm^3$, $V_R = 5\,V$, $\varepsilon_r = 11.7$ for Si,
$q = 1.6\times10^{-19}$

$$V_J = V_T\ ln\left[\frac{N_A N_D}{n_i^2}\right]$$

$$= 26\times10^{-3}\ ln\left[\frac{10^{16}\times10^6\times10^{15}\times10^6}{\left(1.5\times10^{10}\times10^6\right)^2}\right]$$

$$= 0.637\ V$$

$$\therefore\quad V_B = V_J + V_R = 5 + 0.637 = 5.637\ V$$

$$\therefore\quad W = \sqrt{\frac{2\varepsilon_0\ \varepsilon_r\ (V_J + V_R)}{q}\left[\frac{N_A + N_D}{N_A N_D}\right]}$$

$$= 2.833\ \mu m$$

Note that $N_A = 10^{16}/cm^3 = 10^{16}\times10^6/m^3 = 10^{22}/m^3$

19. What is the principle operation of a PN junction diode in reverse bias condition? (M/J-2014)

- Under reverse bias condition, the holes in P type and the electrons in N type regions move to the negative and positive terminals of the battery respectively.
- Hence the width of the depletion region is increased, which prevents the flow of majority carriers through the junction.
- When the applied voltage is slowly increased, the minority carriers (electrons) in P region and the minority carriers (holes) in N region make a small amount of current flow through the junction. This current is called “Reverse saturation current”.

20. What is recovery time? Give its types.

- The total time required by a diode to switch from ON to OFF state which is addition of storage time and transition time is called as reverse recovery time of a diode.
- i.e. $t_{rr}. = t_s + t_t$.
- For commercial switching type diodes the reverse recovery time, t_{rr}, ranges from less than 1 ns up to as high as 1 µs.

21. What is depletion (or) transition (or) space charge capacitance?

Under reverse bias condition, the majority carriers move away from the junction. Thereby uncovering more immobile charges.

- Hence the width of the space-charge layer at the junction increases with reverse voltage. This may be considered a capacitive effect.
- This capacitance which is due to depletion layer is known as depletion capacitance or transition capacitance can be expressed as $C_T = dQ/dV$

Where dQ⇨ increase in charge caused by a change in voltage dV

The values of C_T ranges from 5 to 200PF.

22. Distinguish between avalanche break down and Zener break down.

ZENER BREAKDOWN	AVALANCHE BREAKDOWN
Breakdown occurs due to heavily doped junction and applied strong electric field	Breakdown occurs due to avalanche multiplication between thermally generated ions.
Doping level is high	Doping level is low
Breakdown occurs at lower voltage	Breakdown occurs at higher voltage
The breakdown voltage decreases with increase in the junction temperature.	The breakdown voltage increases with increase in the junction temperature.

23. A silicon diode has a saturation current of 7.5μA at room temperature 300^0K. Calculate the saturation current at 400^0K.

Given

$T_1 = 300°K$, $T_2 = 400°K$, $I_{01} = 7.5\ \mu A$,

$\Delta T = T_2 - T_1 = 100$

$I_{02} = (2^{\frac{\Delta T}{10}})\ I_{01} = (2^{\frac{100}{10}}) \times 7.5 = 7680\ \mu A = 7.68\ mA$

24. Define Diode Resistance. (Or) What is meant by Static resistance and Dynamic resistance of Diode?

Diode resistance is the resistance which a diode offers in a circuit.

DC OR STATIC RESISTANCE (R_f)

- The static resistance of a diode is the ratio of voltage to current in the forward bias characteristics of the PN junction diode. It is denoted by R. As the static resistance varies widely with V and I, it is not a useful parameter.

$$R_F = V_F / I_F$$

AC OR DYNAMIC RESISTANCE: (r_f)

- The dynamic resistance of a diode is defined as the reciprocal of the slope of the volt – ampere characteristics.

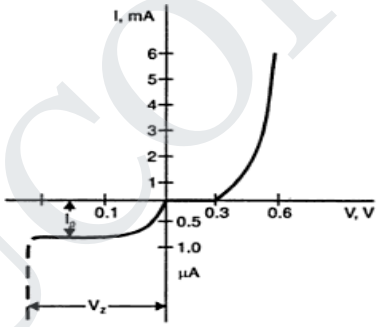
r = Change in voltage / Resulting change in current

= ΔV / ΔI

The dynamic resistance varies inversely with current rf= ŋ Vt / I.

25. What is meant by PN Junction diode? Draw the VI characteristics of diode.

- A PN junction diode is formed by suitably joining a P-type semiconductor and a N-type semiconductor. It is shown in the figure.
- The P-type semiconductor has more holes and fewer electrons. The N-type semiconductor has more electrons and fewer holes



26. What is a free electron? What are holes?

Free electron: An electron which is removed from the force of attraction of nucleus is called a free electron. (OR) any electron that is not attached to an ion, atom, or molecule and is free to move under the influence of an applied electric or magnetic field

Holes:

- When a valence electron drift from the valence band to conduction band by breaking a covalent band, a vacancy is created in the broken covalent bond. Such a vacancy is called a hole.

27. Differentiate N-type and P-type semi conductors?

N type semiconductor	P type semiconductor
It is formed by adding a small amount of pentavalent impurities such as arsenic, antimony or phosphorous to a semiconductor (Si or Ge) material.	It is formed by adding a small amount of trivalent impurities such as aluminium or boron to a semiconductor (Si or Ge) material.
The added impurities are called donar impurities because they will donate electrons.	The added impurities are called acceptor impurities because they will accept electrons
The electrons are majority carriers and holes are minority carriers.	The holes are majority carriers and electrons are minority carriers.

28. What is depletion layer?

- A PN junction diode is formed by suitably joining a P-type semiconductor and a N-type semiconductor.
- The P-type semiconductor has more holes and fewer electrons. The N-type semiconductor has more electrons and fewer holes. Therefore at the junction, the electrons in the N-side have a tendency to move towards the P-side. Similarly the holes on the P-side have a tendency to move towards the N-side.
- According to that, the electrons and holes recombine with each other, to form a region at the junction. It is called “Depletion Region”.

29. What is avalanche effect?

- During reverse biased condition, due to multiplication of minority carriers by collision, reverse current increases to a large extent which destroys the PN junction. This effect is called avalanche effect.

30. Define forward recovery time and reverse recovery Time?

- The forward recovery time can be defined as the time required to reach 10 to 90% of its diode voltage.

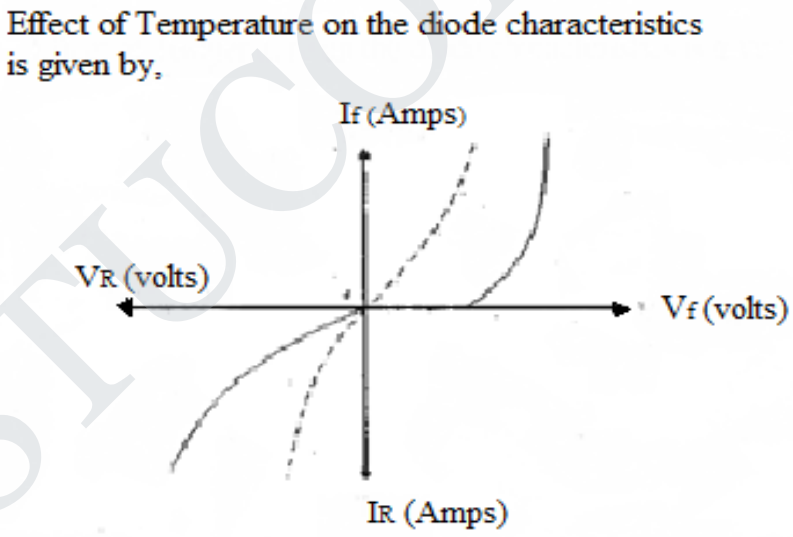
- The reverse recovery time is defined as the time interval from the instant of current reversal from forward to reverse condition until the diode has recovered to a specified extent either in terms of diode current or in terms of diode resistance

31. What is zener breakdown?

- Zener Breakdown takes place when both sides of the junction are very heavily doped and consequently the depletion layer is think When a small reverse bias voltage is applied a very strong electric field is set up across the thin depletion layer.
- This electric field is enough to break the covalent bonds. So the large number of free charge carriers are produced which constitute the zener current. The process is known as zener breakdown.

32. What is the effect of Temperature on PN Junction diode?

- The rise in temperature increases the generation of electron hole pairs in semiconductors and increase their conductivity.
- As a result, the current through the PN junction diode increases with temperature as given by the diode current equation Effect of Temperature on the diode characteristics is given by,



33. Define Knee voltage (or) cut in voltage (or) Threshold voltage of a diode.

- It is the forward voltage at which the current through the junction starts to increase rapidly. Its value is 0.7V for Si and 0.3V for Ge.

34. Calculate the diffusion capacitance for a silicon diode with a 15 mA forward current, if the charge carrier transit time is 70nsec.

(For silicon $\eta = 2$

At room temp

$T = 300K$, $V_T = 26mV$)

Given :

Forward current (I) = 15mA

Transit time (τ) = 70nS

Solution :

Diffusion capacitance $C_D = \frac{\tau I}{\eta V_T}$

$$C_D = \frac{70 \times 10^{-9} \times 15 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 20.192 \text{ nF}$$

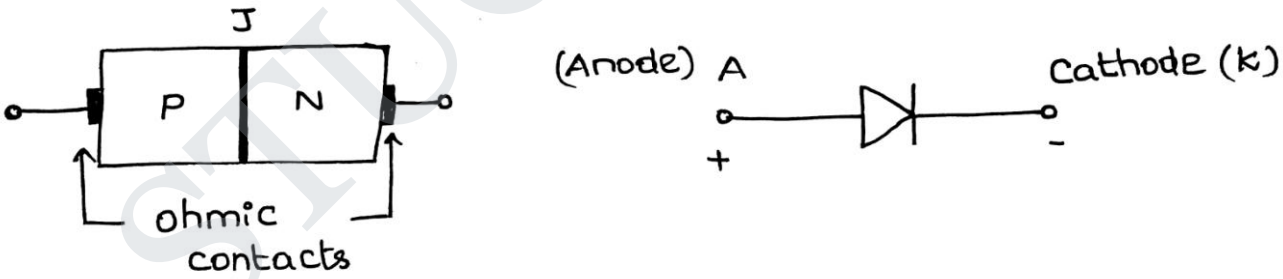
PART – B

1. The phosphorous (donor) concentration in a region of a silicon crystal varies linearly from a concentration of $n_0 = 10^{14}$ cm^{-3} at x=0 mm to a concentration of $n_1 = 10^{17}$ cm^{-3} at x=1 mm. The diffusion constant for electrons is Dn = 22.5 cm^2/s, the diffusion constant for holes is D_p = 5.2 cm^2/s, and the temperature is 300 K. What is the diffusion current density in the positive x-direction? (N/D-2019)

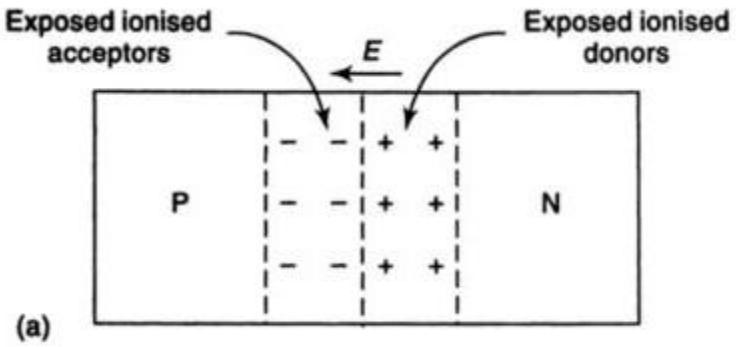
2. Explain the theory of PN junction diode and derive its diode current equation. (OR) Explain the operation of PN junction under zero voltage applied bias condition and derive the expression for built in potential barrier. (OR) Explain the basic structure of the PN junction. (OR) Describe about V – I Characteristics of PN junction diode. (OR) With neat diagram describe the Characteristics of forward and reverse biased PN junction diode. (OR) Derive the current equation of diode. (OR) Derive an expression for PN junction diode forward and reverse currents with suitable diagram. (OR) Explain the theory of PN junction diode when forward and reverse biased derive its diode current equation. (OR) From the basic concepts, derive the expression for the ideal PN junction current. (M/J 2014) (N/D 2014) (A/M 2015) (N/D 2015) (A/M 2016) (N/D 2016) (A/M 2017) (N/D 2017)(A/M 2018) (A/M-2019) (N/D-2019)

PN JUNCTION DIODE (SEMICONDUCTOR DIODE):

- A PN junction diode is formed by suitably joining a P-type semiconductor and a N-type semiconductor. It is shown in the figure.
- The P-type semiconductor has more holes and fewer electrons. The N-type semiconductor has more electrons and fewer holes. Therefore at the junction, the electrons in the N-side have a tendency to move towards the P-side. Similarly the holes on the P-side have a tendency to move towards the N-side.



- According to that, the electrons and holes recombine with each other, to form a region at the junction. It is called “Depletion Region”.
- When the free electrons move from N-type to P-type, the donor ions become positively charged. Similarly when the holes move from P-type to N-type, the acceptor ions become negatively charged. These two charges, on either side make a potential across the depletion region called “Barrier Potential”.



WORKING OF A PN JUNCTION DIODE:

- The conduction of any diodes depends on their biasing. There are two types of biasing:
  (i)Forward biasing (ii) Reverse biasing

(i)FORWARD BIASING:

- In forward biasing, the positive terminal of the battery is connected to the P-type and the negative terminal of the battery is connected to the N-type materials of the diode.
- Under forward biased condition, the applied positive potential repels the holes in P-type region. The negative potential repels the electrons in N-type region. Now the electrons in N-type region and the holes in the P-type region move towards the junction. This reduces the width of the depletion region and also barrier potential.

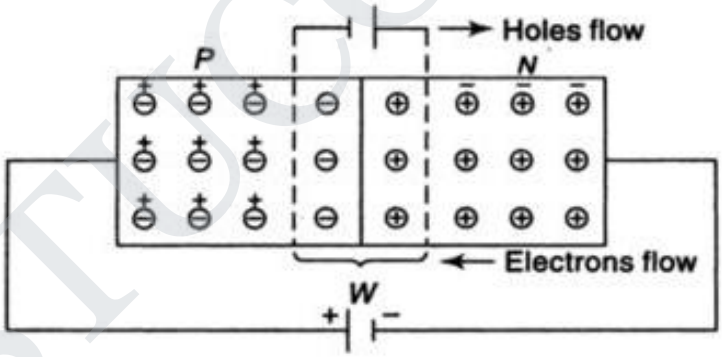


Fig. 4.9 PN junction under forward bias

- If the applied potential is greater than barrier potential, the majority carriers on both regions move towards the junction. It makes current flow through the junction. The amount of current flow depends upon the magnitude of applied potential.
- When the applied potential is less than cut-in or threshold voltage, the current flow is very low. The cut-in voltage is generally 0.3V for Ge and 0.7V foe Si diodes respectively.

- At the cut-in voltage, the applied potential overcomes the barrier potential, increases the current rapidly.

V—I CHARACTERISTICS

- Under forward bias condition, the V—I characteristics of a PN unction diode are shown in Fig. As the forward voltage (V_F) is increased, for $V_F < V_O$, the forward current I_F is almost zero (region OA) because the potential barrier prevents the holes from P-region and electrons from N-region to flow across the depletion region in the opposite direction.

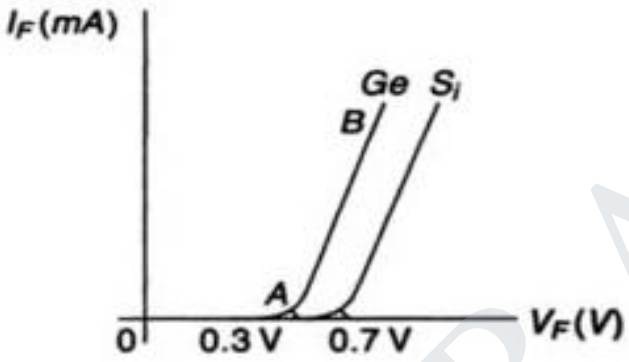


Fig. 4.10 *V–I* characteristics of a diode under forward bias condition

- For $V_F > V_O$, the potential barrier at the junction completely disappears and hence, the holes cross the junction from P-type to N-type and the electrons cross the junction in the opposite direction, resulting in relatively large current flow in the external circuit.

(ii)REVERSE BIASING:

- In reverse biasing, the positive terminal of the battery is connected to the N-type and the negative terminal of the battery is connected to the P-type materials of the diode.
- Under reverse bias condition, the holes in P type and the electrons in N type regions move to the negative and positive terminals of the battery respectively.
- Hence the width of the depletion region is increased, which prevents the flow of majority carriers through the junction.
- Therefore theoretically no current should flow in the external circuit.
- When the applied voltage is slowly increased, the minority carriers (electrons) in P region and the minority carriers (holes) in N region make a small amount of current flow through the junction. This current is called “Reverse saturation current”.

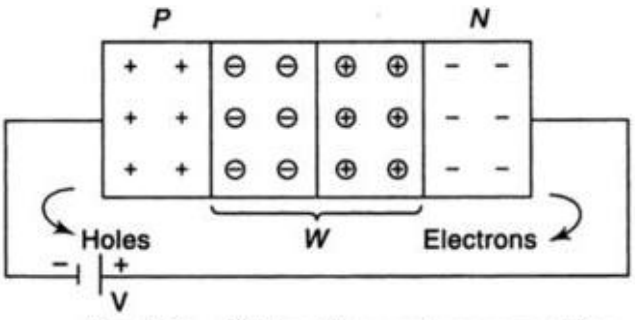


Fig. 4.11 PN junction under reverse bias

V—I CHARACTERISTICS

- But in practice, a very small current of the order of a few microamperes flows under reverse bias as shown in Fig.
- Electrons forming covalent bonds of the semiconductor atoms in the P- and N-type regions may absorb sufficient energy from heat and light to cause breaking of some covalent bonds. Hence VA VF electron—hole pairs are continually produced in both the regions.

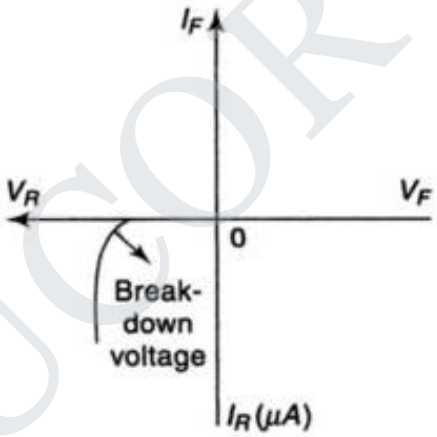


Fig. 4.12 *V–I* characteristics under reverse bias.

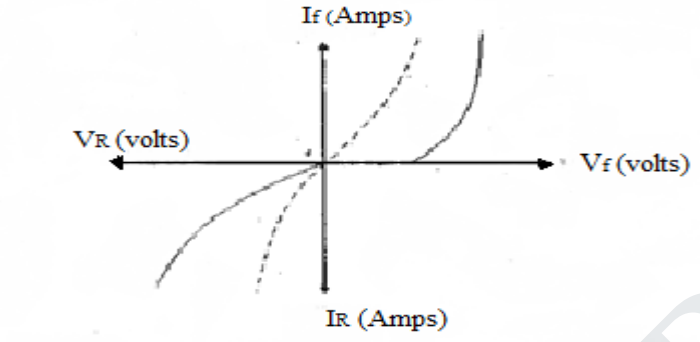
- When the applied reverse voltage is further increased, breakdown occurs in the junction. Now large reverse current flows through the junction. The minimum voltage that needs to breakdown occurs in the junction is called “Breakdown Voltage”.

TEMPERATURE EFFECT OF PN DIODE:

- The rise in temperature increases the generation of electron hole pairs in semiconductors and increase their conductivity.
- As a result, the current through the PN junction diode increases with temperature as given by the diode current equation Effect of Temperature on the diode characteristics is given by,

$I=I_0 [e^{v/\eta V_T}-1]$ Amps

Effect of Temperature on the diode characteristics is given by,



I= Diode current

I_0=Diode Reverse saturation current in amps

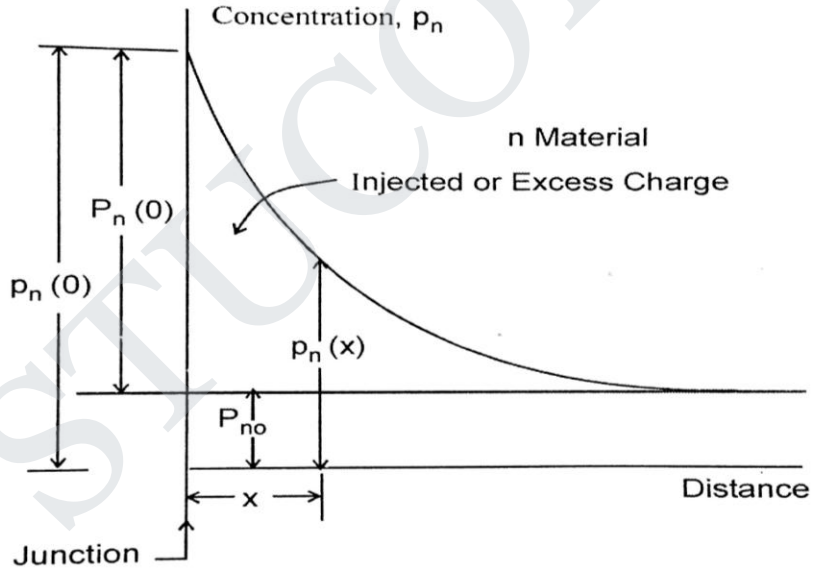
V= External Voltage Applied

V_T= voltage equivalent of temperature in volts (Thermal voltage) ($V_T = kT/q$)

At room Temp T=300K, V_T= 26mv

η= A constant (or) Emission coefficient(1 for germanium diode and 2 for silicon diode)

PN DIODE CURRENT EQUATIONS:



. 1.15: Defining the several components of hole concentration in the *n* side of a forward-biased diode. The diagram is not drawn to scale since $p = (0) >> p_{no}$

The expression for the total current as a function of applied voltage can be derived assuming that the width of the depletion region is zero.

When a forward bias is applied to a diode, holes are injected from the P-side into the N-side. Due to this, the concentration of holes in the N-side (p_n) is increased from its thermal equilibrium value (p_{no}) and injected hole concentration [$p_n(x)$] decreases exponentially with respect to distance (x) as shown in Figure 1.15

$$P_n(x) = p_n - p_{no} = P_n(0)\ e^{-x/Lp}$$

where L_p is the diffusion length for holes in the N-material

$$P_n(x) = p_{no} + P_n(0)\ e^{-x/Lp} \qquad \ldots (1)$$

Injected hole concentration at $x = 0$ is:

$$P_n(0) = p_n(0) - p_{no} \qquad \ldots (2)$$

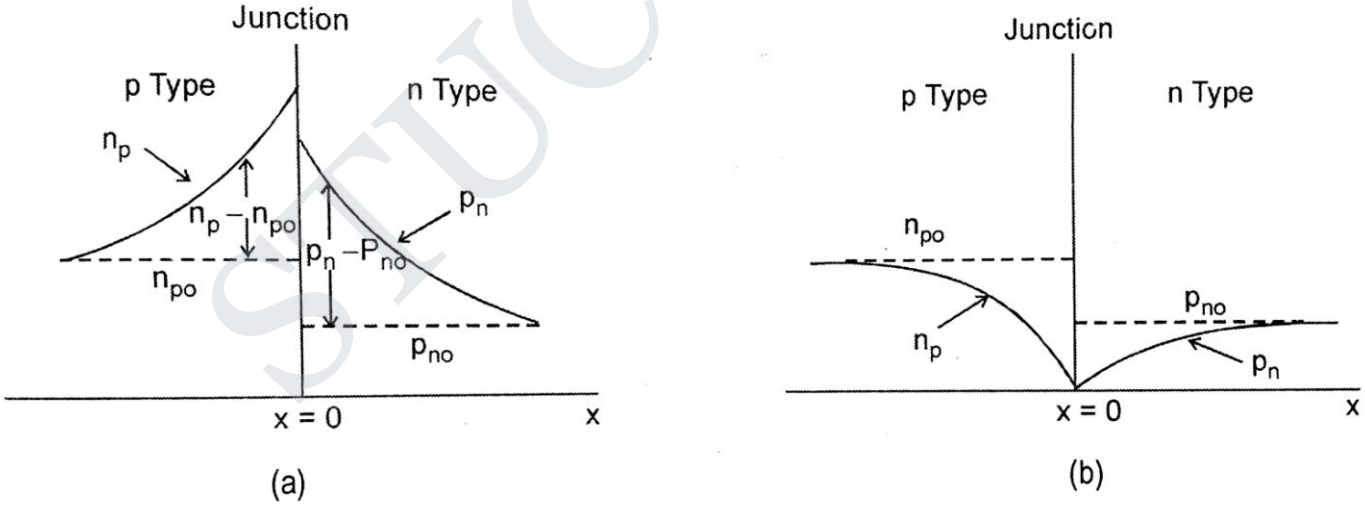


Fig. 1.16: Minority-carrier density distribution as a function of the distance x from a junction. (a) A forward-biased junction; (b) A reverse-biased junction

These several components of hole concentration in the N-side of a forward biased diode are shown in Figure 1.15, in which the density $p_n(x)$ dereases exponentially with distance (x).

Let p_p and p_n be the hole concentration at the edges of the space charge in the P- and N-sides, respectively. Let $V_B(= V_0 - V)$ be the effective barrier potential across the depletion layer. Then,

$$p_p = P_n e^{V_B / V_T} \quad \ldots (3)$$

where V_T is the volt-equivalent of temperature.

This is the Boltzmann's relation of kinetic gas theory. This equation is valid as long as the hole current is small compared with diffusion or drift current. This condition is called **low level injection**.

Under open circuit condition (i.e., V = 0), $p_p = p_{po}$, $p_n = p_{no}$ and $V_B = V_0$. Equation (3) can be written as:

$$p_{p0} = p_{no} e^{V_0 / V_T} \quad \ldots (4)$$

Under forward bias condition let V be the applied voltage, then the effective barrier voltage:

$$V_B = V_0 - V$$

The hole concentration throughout the p-side is constant and equal to the thermal equilibrium value ($p_p = p_{po}$). The hole concentration varies exponentially with distance into the N-side.

At $x = 0$, $p_n = p_n(0)$

Equation (3) can be changed into:

$$p_{p0} = p_n(0)\, e^{(V_0 - V)/V_T} \quad \ldots (5)$$

Comparing Equations (4) and (5),

$$p_n(0) = p_{n0}\, e^{V/V_T}$$

This boundary condition is called the **law of the junction**, substituting this into Equation (2), we get

$$P_n(0) = p_{n0}\left(e^{V/V_T} - 1\right) \qquad \ldots (6)$$

The diffusion hole current in the N-side is:

$$I_{pn}(x) = -A\, e D_p \frac{dp_n(x)}{dx}$$

$$= -A\, e D_p \frac{d}{dx}\left[p_{n0} + P_n(0)\, e^{-x/L_p}\right]$$

$$= \frac{A\, e D_p P_n(0)}{L_p} e^{-x/L_p}$$

From this equation, it is evident that the injected hole current decreases exponentially with distance.

The hole current crossing the junction into the N-side with $x = 0$ is:

$$I_{pn}(0) = \frac{A\, e D_p P_n(0)}{L_p} = \frac{A\, e D_p p_{no}}{L_p}\left(e^{V/V_T} - 1\right)$$

The electron current crossing the junction into the P-side with $x = 0$ is:

$$I_{np}(0) = \frac{A\, e D_n N_p(0)}{L_n} = \frac{A\, e D_n n_{p0}}{L_n}\left(e^{V/V_T} - 1\right)$$

The total diode current,

$$I = I_{pn}(0) + I_{np}(0) = I_0\left(e^{V/V_T} - 1\right)$$

where $I_0 = \dfrac{A\, e D_p p_{no}}{L_p} + \dfrac{A\, e D_n n_{po}}{L_n}$ = reverse saturation current.

If the carrier generation and recombination in the space-charge region are considered, the general equation of the diode current is given by:

$$I = I_0 \left[e^{(V/\eta V_T)} - 1 \right]$$

where V = external voltage applied to the diode, and η = *a* constant, 1 for germanium and 2 for silicon.

I = diode current

I_0 = reverse saturation current

$V_T = KT/q = T/11600$, volt-equivalent temperature.

where K = Boltzmann's constant (1.38×10^{-23} J/K)

q = Charge of an electron (1.602×10^{-19} C)

T = temperature of the divide junction (K) = (°C + 273°).

At room temperature, T = 300 K, V_T = 26 *m*V.

Substituting this value in the current equation, we get

$$I = I_0 \left[e^{(40V/\eta)} - 1 \right]$$

Therefore, for germanium diode,

$$I = I_0 \left[e^{40\,V} - 1 \right].$$

Since η = 1 for germanium.

For silicon diode,

$$I = I_0 \left[e^{20\,V} - 1 \right].$$

since η = 2 for silicon.

When the diode is reverse biased, its current equation may be obtained by changing the sign of the applied voltage V. Thus, the diode current with reverse bias is:

$$I = I_0 \left[e^{(-V/\eta V_T)} - 1 \right]$$

If $V >> V_T$, then the term $e^{(-V/\eta V_T)} << 1$, therefore

$$I \approx -I_0$$

termed as reverse saturation current, which is valid as long as the external voltage is below the breakdown value.

3. Derive the transition and diffusion capacitance in PN diode. (N/D-2019) (OR)

(i)Derive the expression of the Space Charge or Transition capacitance of PN diode under reverse bias with a neat diagram.

(ii)Derive the expression for diffusion capacitance of PN junction diode.

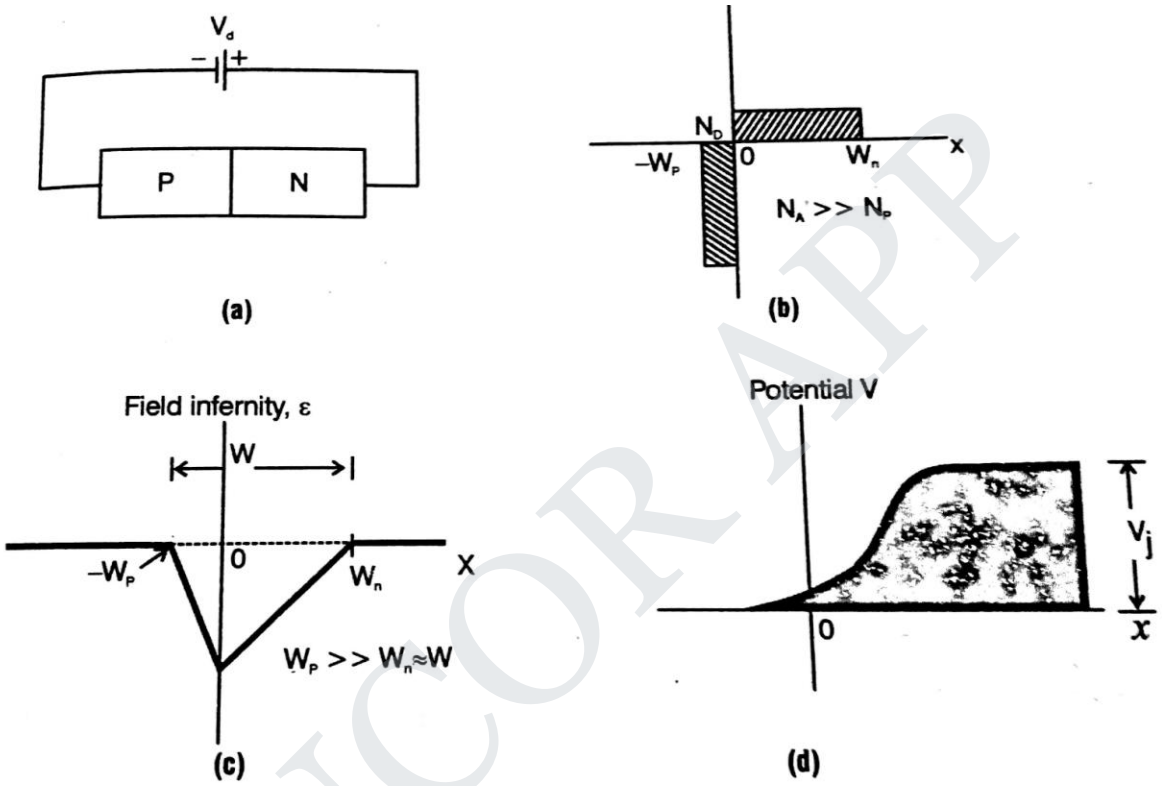
SPACE-CHARGE CAPACITANCE:

Under reverse bias condition, the majority carriers move away from the junction. There by uncovering more immobile charges.

- Hence the width of the space-charge layer at the junction increases with reverse voltage. This may be considered a capacitive effect.
- This capacitance which is due to depletion layer is known as depletion capacitance or transition capacitance can be expressed as $C_T = \frac{dQ}{dV}$. The values of C_T ranges from 5 to 200PF.

  Where $\frac{dQ}{dV}$ change in charge due to change in voltage
- C_T is also referred to as transition-region, space-charge, barrier or depletion-region capacitance.
- Step-graded junction: In this junction there is an abrupt change from acceptor ions on one side to donor ions on the other side. Such a junction is formed by placing trivalent indium against N-type germanium and heating the combination to a high temperature, for a short time some of the indium dissolves into the germanium, the N-type germanium is changed into P-type at the junction.

- Such a step-graded junction is called an alloy or fusion junction. It is not necessary for the abrupt junction to be symmetrical, that is the doping concentration at either side of the junction is dissimilar. Consider a PN junction diode Which is asymmetrically doped at the junction as shown in Fig.



(a)A reverse biased PN step graded function, (b)The charge density, (c)The field infinity, (d)The potential variation with distance x.

Let the net charges in the device to be zero. Then

$$eN_aW_p = eN_DW_n$$

Where,

N_A = acceptor impurity density

N_D = donor impurity density

W_d and Wn = Depletion region width of P and N region

q = charge of electron or hole

If $N_A >> N_d$ then $W_p << W_n W$. The relationship between potential and charge density is given by poission's equation.

$$\frac{d^2v}{dx^2} = \frac{-\rho}{\varepsilon} = \frac{-qN_D}{\varepsilon}$$

The electric field intensity n the depletion region is obtained by integrating equation once and substituting boundary conditions

$$E = \frac{-dv}{dx} \qquad \left[\frac{dv}{dx} = -\int \frac{P}{\varepsilon} dx\right]$$

$$E = \int_{x^0}^{x} \frac{\rho}{\varepsilon} dx$$

$$\frac{dv}{dx} = 0, x = W_n \approx W$$

$$E = -\frac{dv}{dx} = \frac{\rho}{\varepsilon} x + c \text{ at x= W, E=0}$$

$$C = -\frac{\rho}{\varepsilon} W$$

$$= \frac{\rho}{\varepsilon} x - \frac{\rho}{\varepsilon} W$$

$$= \frac{\rho}{\varepsilon} (x - W)$$

$$E = \frac{qN_D}{\varepsilon}(x - W)$$

We have

$$V = -\int E \cdot dx$$

$$= -\int \left(\frac{\rho}{\varepsilon} x + C\right) dx$$

$$= -\left(\frac{\rho}{\varepsilon} \cdot \frac{x^2}{2} + cx + D\right)$$

$$= -\left(\frac{qN_D x^2}{2\varepsilon} + cx + D\right)$$

The total potential at x=0 can be assumed to be zero. That is v=0, then D=0

$$V = -\left(\frac{qN_D x^2}{2\varepsilon} - \frac{qN_D}{\varepsilon} Wx\right)$$

$$= \frac{-qN_D}{\varepsilon}\left(\frac{x^2}{2} - Wx\right)$$

$$\therefore \; V = \frac{-qN_D}{2\varepsilon}\left(x^2 - 2Wx\right)$$

At x=W, V=V_j = junction or barrier potential, then

$$V_j = \frac{-qN_D}{2\varepsilon}\left(x^2 - 2Wx\right)\Big|_{x=W}$$

$$\therefore \; V_j = \frac{qN_D W^2}{2\varepsilon}$$

$$\therefore \; V = \frac{-qN_D}{2\varepsilon}\left(x^2 - 2Wx\right)$$

At x=W, V=V_j = junction or barrier potential, then

$$V_j = \frac{-qN_D}{2\varepsilon}\left(x^2 - 2Wx\right)\Big|_{x=W}$$

$$\therefore \; V_j = \frac{qN_D W^2}{2\varepsilon} \qquad \text{.....(3)}$$

If V_d is the external diode voltage and V_o is barrier potential then $V_j = V_o - V_d$

From equation (3) we can observe that the thickness of the depletion layer increases with applied reverse voltage.

W varies as $V_j^{1/2} = (V_o - V_d)^{1/2}$

If A is the area of the junction, the charge in the distance W is

$$Q = qN_D W_A \qquad \text{.....(4)}$$

The transition capacitance C_T is given by

$$C_T = \frac{dQ}{dv}$$

From equation (4)

$$\frac{dQ}{dv} = qN_D A \frac{dW}{dv}$$

Differentiating equation (3) with respect to V_j we get

$$1 = \frac{qN_D}{2\varepsilon} \cdot 2W \frac{dW}{dv_j}$$

$$\frac{dW}{dv_j} = \frac{\varepsilon}{qN_D W}$$

Now, $$\frac{dQ}{dv} = qN_D \cdot A \cdot \frac{\varepsilon}{qN_D W} = \frac{\varepsilon A}{W}$$

$$\therefore \boxed{C_T = \frac{\varepsilon A}{W}} \qquad \text{.....(5)}$$

The equation (5) gives the transition capacitance which is exactly same as the equation of capacitance for parallel plate capacitor.

LINEARLY GRADED JUNCTION

The charge density varies linearly with the applied voltage.

Linear graded junction is formed by melting Germanium and its type is changed during the drawing process by adding first p-type and then *n*-type impurities. The charge density becomes absolutely zero at edge distances $\frac{W}{2}$ and $-\frac{W}{2}$ and varies linearly with distance.

Net charge density, $\rho = q\,kx$, for $-\frac{W}{2} < x < +\frac{W}{2}$ ...(1)

Where k - proportionality constant

Using Poisson's equation

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\varepsilon} = -\frac{q\,k\,x}{\varepsilon} \qquad ...(2)$$

Where V - potential at a distance 'x' from the junction

Integrating (2)

$$\frac{dV}{dx} = \frac{-q\,k}{\varepsilon}\,\frac{x^2}{2} + C_1 \qquad ...(3)$$

at $x = \pm\frac{W}{2}, E = -\frac{dV}{dx} = 0$ ...(4)

Substitute (4) in (3)

$$\Rightarrow 0 = -\frac{q\,k}{2\,\varepsilon}\left(\frac{W^2}{4}\right) + C_1 \Rightarrow C_1 = \frac{q\,k\,W^2}{8\,\varepsilon} \qquad ...(5)$$

Substitute (5) in (3)

$$\frac{dV}{dx} = -\frac{qk}{\varepsilon}\,\frac{x^2}{2} + \frac{q\,kW^2}{8\,\varepsilon}$$

$$= -\frac{q\,k}{\varepsilon}\left[\frac{x^2}{2} - \frac{W^2}{8}\right] \qquad ...(6)$$

Integrating (6)

$$\int dV = -\frac{q\,k}{\varepsilon}\int\left[\frac{x^2}{2} - \frac{W^2}{8}\right]dx$$

$$V = -\frac{q\,k}{\varepsilon}\left[\frac{x^3}{6} - \frac{W^2\,x}{8} + C_2\right]$$

V- 0 at $x = 0 \Rightarrow C_2 = 0$

Thus $$V = -\frac{q\,k}{2\,\varepsilon}\left[\frac{x^3}{3} - \frac{W^2 x}{4}\right]$$

The total potential V_J across the junction from $-\frac{W}{2}$ to $\frac{W}{2}$ is given by

$$\therefore V_J = V \text{ at } x = \frac{W}{2}$$

$$V_J = -V \text{ at } x = -\frac{W}{2}$$

$$V_J = -\frac{q\,k}{2\,\varepsilon}\left[\frac{W^3}{24} - \frac{W^3}{8}\right] + \frac{q\,k}{2\,\varepsilon}\left[-\frac{W^3}{24} + \frac{W^3}{8}\right]$$

$$= \frac{q\,k}{2\,\varepsilon}\left[-\frac{W^3}{24} + \frac{W^3}{8} - \frac{W^3}{24} + \frac{W^3}{8}\right]$$

$$= \frac{q\,k}{2\,\varepsilon}\left(\frac{-2W^3 + 3\,W^3 + 3\,W^3}{24}\right)$$

$$V_J = \frac{q\,k\,W^3}{12\,\varepsilon} \qquad \ldots(7)$$

$$V_J \propto W^3$$

$\Rightarrow W$ varies as $V_J^{1/3}$

The total charge on one side of the layer is

$$Q_T = \frac{1}{2}\left(\frac{W}{2}\right)\left(\frac{q\,k\,W}{2}\right)A = \frac{q\,k\,W^2\,A}{8}$$

$$C_T = \frac{dQ}{dV} = \frac{d}{dV}\left|\frac{q\,k\,W^2\,A}{8}\right|$$

$$= \frac{A\,q\,k}{8}(2\,W)\left|\frac{dW}{dV}\right|$$

$$C_T = \frac{A\,q\,k\,W}{4}\left|\frac{dW}{dV}\right| \qquad \ldots(8)$$

From (7)

$$V_J = \frac{q\,k\,W^3}{12\,\varepsilon}$$

$$\frac{dV}{dW} = \frac{q\,k}{12\,\varepsilon} \cdot 3\,W^2$$

$$\Rightarrow \frac{dW}{dV} = \frac{4\,\varepsilon}{q\,k\,W^2} \qquad \ldots(9)$$

Substitute (9) in (8)

$$C_T = \frac{A\,q\,k\,W}{4}\left(\frac{4\,\varepsilon}{q\,k\,W^2}\right)$$

$$\boxed{C_T = \frac{\varepsilon\,A}{W}}$$

(ii)Derive the expression for diffusion capacitance of PN junction diode.

- The capacitance that exists in a forward biased junction is called a diffusion or storage capacitance (C_D) due to diffusion of minority carriers on both sides of the junctions.
- As a result the holes in the N-region and electrons in the P-region are separated by a very thin depletion layer which leads to capacitance. It can be expressed as

Diffusion capacitance (C_D) = $C_D = \frac{\tau I}{\eta V_T}$

τ ⇨ Mean life time for holes and electrons

I⇨ Diode forward current

V_T ⇨ Thermal voltage (kT/q)

η ⇨ A constant (or) Emission coefficient(1 for germanium diode and 2 for silicon diode)

$$C_D = \frac{dQ}{dv} \qquad \text{.....(1)}$$

Where dQ is change in charge due to minority carriers and dv is change in voltage across diode.

If τ is mean life time of holes and electrons, then

$$dQ = \tau dI \qquad \text{.....(2)}$$

Substituting equation (2) in equation (1) results

$$C_D = \tau \frac{dI}{dv}$$

$= \tau g$ [g – diode incremental conductance]

$$= \frac{\tau}{r} \quad [r\text{– diode incremental resistance } g = \frac{1}{r}] \qquad \text{.....(3)}$$

Since the diode resistance $r = \frac{\eta V_T}{I}$ .....(4)

Substituting equation (4) in equation (3) we get,

$$C_D = \frac{\tau}{\frac{\eta V_T}{I}}$$

$$\therefore \boxed{C_D = \frac{\tau I}{\eta V_T}} \quad \text{.....(5)}$$

From equation (5) we can observe that the diffusion capacitance is proportional to the current I.

4. Explain and derive current components and switching characteristics of diode. (OR) Write short notes on switching characteristics of diode. (OR) Discuss about the switching characteristics of PN junction diode with suitable diagram (M/J 2014) (N/D 2014) (N/D 2015) (A/M 2017) (N/D 2017) (A/M-2019)

CURRENT COMPONENTS

When a forward bias is applied to a diode, holes are injected into the *n* side and electrons into the *p* side. The number of these injected minority carriers falls off exponentially with distance from the junction. Since the diffusion current of minority carriers is proportional to the concentration gradient, this current also varies exponentially with distance. There are two minority currents, I_{pn} and I_{np} as shown in Figure 1.14

The symbol $I_{pn}(x)$ represents the hole current in the *n*-material, and $I_{np}(x)$ indicates the electron current in the *p* side as a function of *x*.

Electrons crossing the junction at $x = 0$ from right to left constitute a current in the same direction as holes crossing the junction from left to right. Hence the total current I at $x = 0$ is

$$I = I_{pn}(0) + I_{np}(0) \quad \text{... (1)}$$

Since the current is the same throughout a series circuit, I is independent of *x*, and is indicated as a horizontal line in Figure 1.14. Similarly, in the *p* side, there must be second component of current I_{PP} which, when added to I_{pn}, gives the total current I. Hence this hole current in the *p* side I_{PP} (a majority carrier current) is given by:

$$I_{PP}(x) = I - I_{np}(x) \quad \text{... (2)}$$

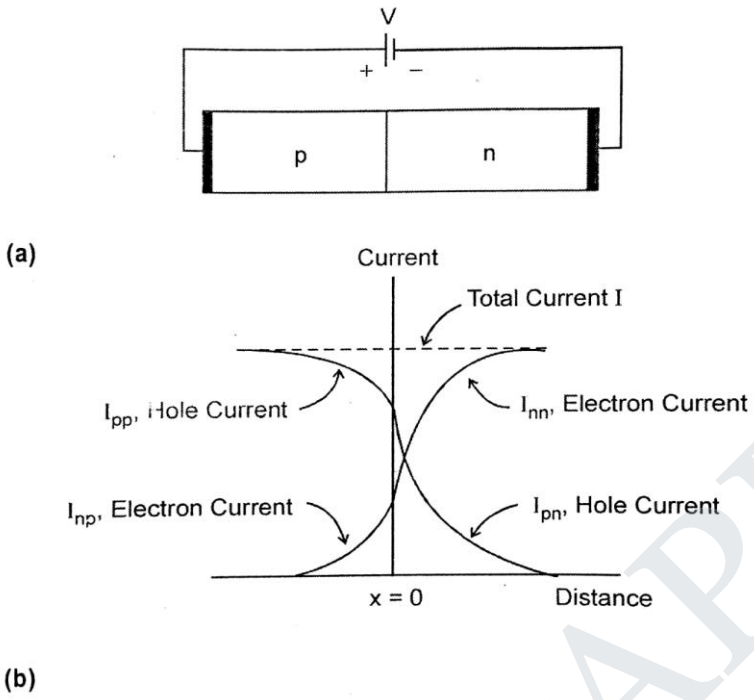


Fig. 1.14: The hole- and electron-current components vs. distance in a *p-n* junction diode.

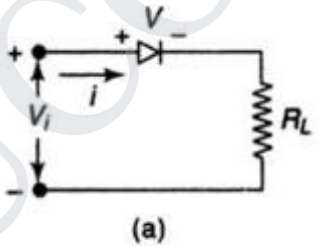
This current is plotted as a function of distance in Figure 1.14, as is also the corresponding electron current I_{nn} in the *n* material. This Figure is drawn for an unsymmetrically doped diode, so that $I_{pn} \neq I_{np}$.

Deep into the *p* side the current is a drift current I_{pp} of holes sustained by the small electric field in the semiconductor. As the holes approach the junction, some of them recombine with the electrons, which are injected into the *p* side from the *n* side. Hence, part of the current I_{pp} becomes a negative current equal in magnitude to the diffusion current I_{np}. The current I_{pp} thus decreases forward the junction. Similar remarks can be made with respect to current I_{nn}. Hence, in a forward-biased *pn* diode, the current enters the *p* side as a hole current and leaves the *n* side as an electron current of the same magnitude.

The current in a *pn* diode is made up of both positive and negative carriers of electricity. The total current is constant throughout the device, but the proportion due to holes and that due to electrons varies with distance, as indicated in Figure 1.14.

SWITCHING CHARACTERISTICS:

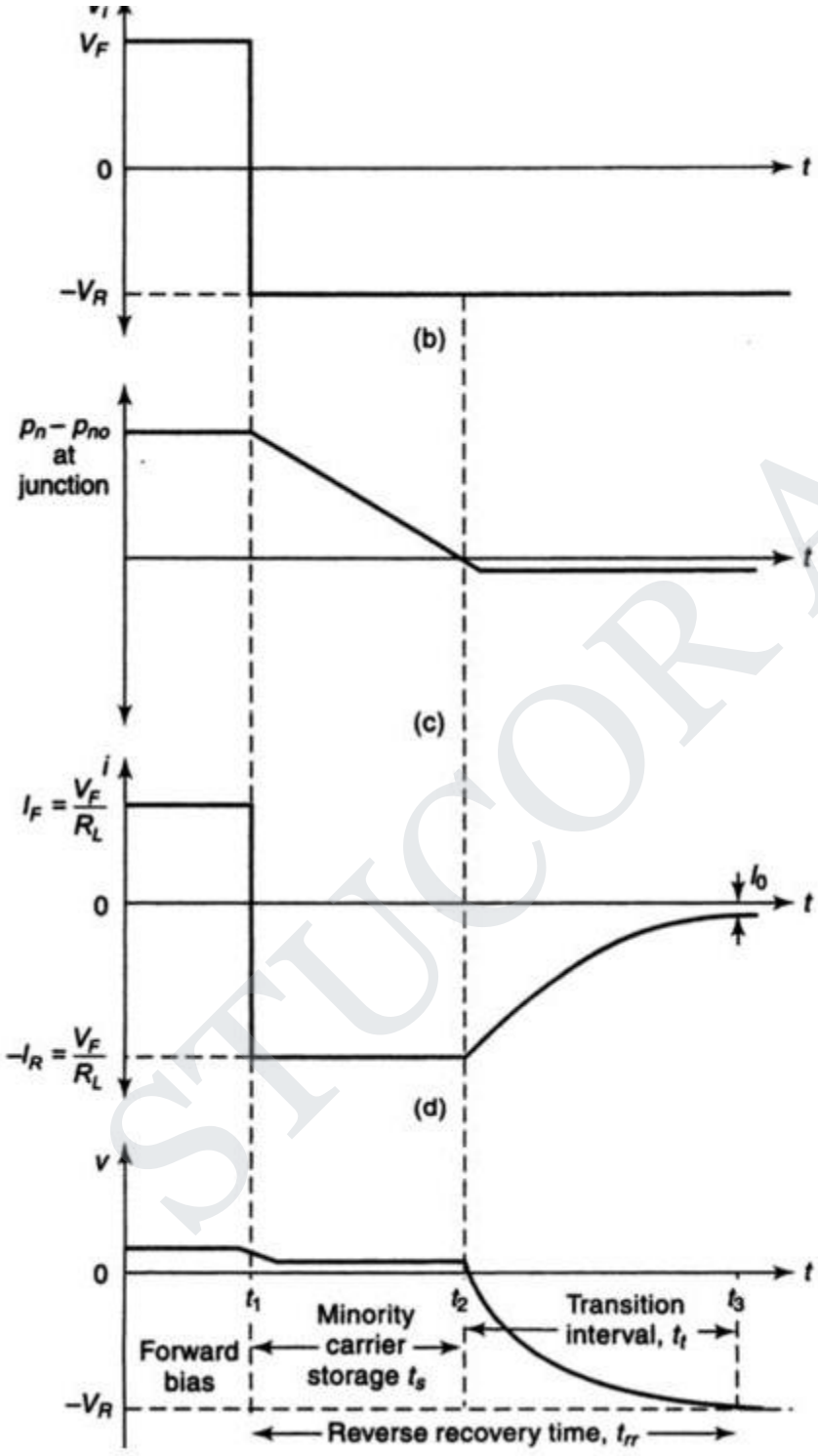
- Diodes are often used in a switching mode. When the applied bias voltage to the PN diode is suddenly reversed in the opposite direction, the diode response reaches a steady state after an interval of time, called the **recovery time**.
- The **forward recovery time**, t_{fr}, is defined as the time required for forward voltage or current to reach a specified value (time interval between the instant of 10% diode voltage to the instant this voltage reaches within 10% of its final value) after switching diode from its reverse- to forward-biased state.
- When the PN junction diode is forward biased, the minority electron concentration in the P-region is approximately linear. If the junction is suddenly reverse biased, at t_1, then because of this stored electronic charge, the reverse current (I_R) is initially of the same magnitude as the forward current (I_F).
- The diode will continue to conduct until the injected or excess minority carrier density ($p — p_0$) or ($n — n_0$.) has dropped to zero.
- However, as the stored electrons are removed into the N-region and the contact, the available charge quickly drops to an equilibrium level and a steady current eventually flows corresponding to the reverse bias voltage as shown in Fig. (c).



(a)

- As shown in Fig. (b), the applied voltage V_i, = V_F for the time up to t_1, is in the direction to forward-bias the diode. The resistance R_L is large so that the drop across R_L. is large when compared to the drop across the diode.
- Then the current is I = V_F/ R_L.= I_F Then, at time t = t_1. the input voltage is suddenly reversed to the value of - V_R. Due to the reasons explained above, the current does not become zero and has the value I = V_R/ R_L.= - I_R until the time t = t_2
- At t = t_2, when the excess minority carriers have reached the equilibrium state, the magnitude of the diode current starts to decrease, as shown in Fig. (d).

- During the time interval from t_1 to t_2, the injected minority carriers have remained stored and hence this time interval is called the **storage time** (t_S).



- After the instant t= t_2, the diode gradually recovers and ultimately reaches the steady state. The time interval between t_2, and the instant t_3 when the diode has recovered nominally, is called the **transition time, t_t.**
- The recovery is said to have completed (i) when even the minority carriers remote from the junction have diffused to the junction and crossed it, and (ii) when the junction transition capacitance, C_T, across the reverse-biased junction has got charged through the external resistor R_L to the voltage $-V_R$.
- The **reverse recovery time** (or turn-off time) of a diode, t_{rr}, is the interval from the current reversal at t = t_1 until the diode has recovered to a specified extent in terms either of the diode current or of the diode resistance, i.e. t_{rr}. = t_s + t_t.
- For commercial switching type diodes the reverse recovery time, t_{rr}, ranges from less than 1 ns up to as high as 1 µs. This switching time obviously limits the maximum operating frequency of the device. The t_{rr}. can be reduced by shortening the length of the P-region in a PN junction diode. The stored charge and, consequently, the switching time can also be reduced by introduction of gold impurities into the junction diode by diffusion.
- The gold dopant, sometimes called a life time killer, increases the recombination rate and removes the stored minority carriers. This technique is used to produce diodes and other active devices for high speed applications.

5. Explain about breakdown mechanism in PN junction diode. (A/M-2019)

BREAKDOWN IN PN JUNCTION DIODES:

- The diode equation predicts that, under reverse bias conditions, a small constant current, the saturation current, I_o flows due to minority carriers, which is independent of the magnitude of the bias voltage.
- But this prediction is not entirely true in practical diodes. There is a gradual increase of reverse current with increasing bias due to the ohmic leakage currents around the surface of the junction. Also, there is a sudden increase in reverse current due to some sort of breakdown, when the reverse bias voltage approaches a particular value called breakdown voltage, V_{BD}, as shown in Fig.
- Once breakdown occurs, the diode is no longer blocking current and the diode current can be controlled only by the resistance of the external circuit.

- The breakdown occurs due to avalanche effect in which thermally generated minority carriers cross the depletion region and acquire sufficient kinetic energy from the applied potential to produce new carriers by removing valence electrons from their bonds.

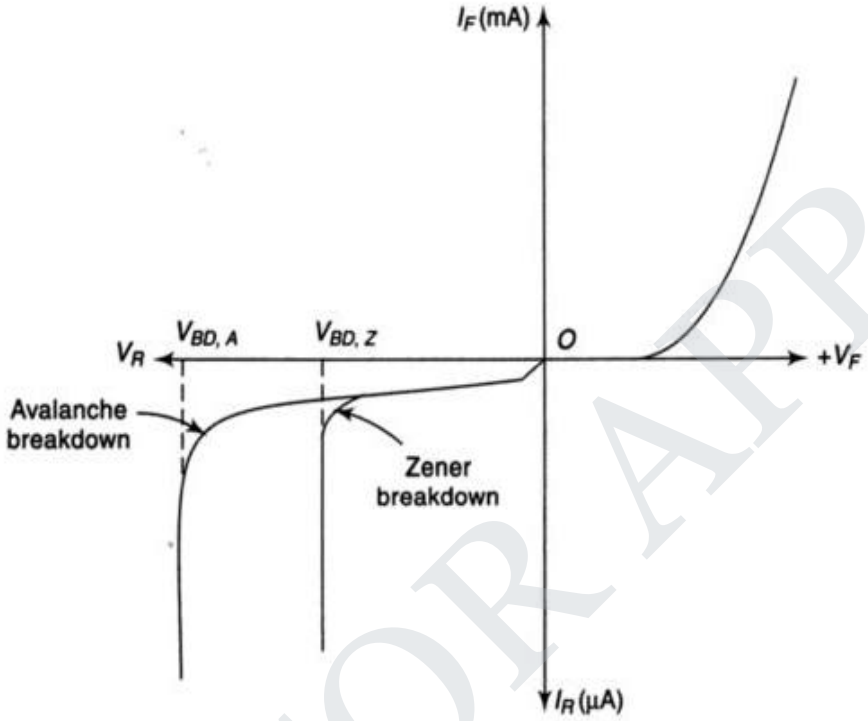


Fig. 4.17 Breakdown in PN junction diodes

- These new carriers will in turn collide with other atoms and will increase the number of electrons and holes available for conduction. This multiplication effect of free carriers may be represented by the following equation: M = $\frac{1}{1-(V/VBD)}$ n

where M = carrier multiplication factor, which is the ratio of the total number of electrons leaving the depletion region to the number entering the region

V = applied reverse voltage

V_{BD}, = reverse breakdown voltage

n = empirical constant, which depends on the lattice material and the carrier type, for N-type silicon, n = 4 and for P-type, n as 2

- As V approaches the breakdown voltage V_{BD}, the value of M will become infinite and there is a rapid increase in carrier density and a corresponding increase in current. Because of the cumulative increase in carrier density after each collision, the process is known as **avalanche breakdown.**

- Even if the initially available carriers do not gain enough energy to disrupt bonds, it is possible to initiate breakdown through a direct rupture of the bonds because of the existence of strong electric field. Under these circumstances the breakdown is referred to as **Zener breakdown.**
- It is clear that the breakdown voltage for a particular diode can be controlled during manufacture by altering the doping levels in the junction. The breakdown voltage for silicon diodes can be made to occur at a voltage as low as 5 V with 1017 impurity atoms per cubic cm or as high as 1000 V when doped to a level of only 10^14 impurity atoms per cubic cm.

6. Derive the expression for drift current density and diffusion current density. (OR) Draw a diagram to illustrate drift current and diffusion current in a semiconductor material and explain. (A/M 2015) (N/D 2015)

- The flow of charge, i.e current, through a semiconductor material are of two types, namely drift and diffusion. The net current that flows through a PN junction diode also has two components, viz. (i) drift current and (ii) diffusion current.

DRIFT CURRENT:

- When an electric field is applied across the semiconductor material, the charge carriers attain a certain drift velocity v_d the holes move towards the negative terminal of the battery and electrons move towards the positive terminal.
- This combined effect of movement of the charge carriers constitutes a current known as the drift current.
- Thus the drift current is defined as the flow of electric current due to the motion of the charge carriers under the influence of an external electric field.
- The equation for drift current density due to electrons is $J_n = qn\mu E$ A/cm²
- The equation for drift current density due to holes is $J_p = qp\mu E$ A/cm²

Where n ⇨ No.of free electrons

p ⇨ No.of holes

μ ⇨ Mobility of electrons in cm²/V-s

μ ⇨ Mobility of holes in cm²/V-s

E ⇨ Applied electric field intensity in V/cm

q ⇨ Charge of an electron (1.6x10ˆ-19 coulomb)

DIFFUSION CURRENT:

- It is possible for an electric current to flow in a semiconductor even in the absence of applied voltage provided a concentration gradient exists in the material.
- In a semiconductor material, the charge carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers.
- Thus the movement of charge carriers takes place resulting in a current called diffusion current.
- The diffusion current depends on the material of the semiconductor, type of charge carriers and the concentration gradient.

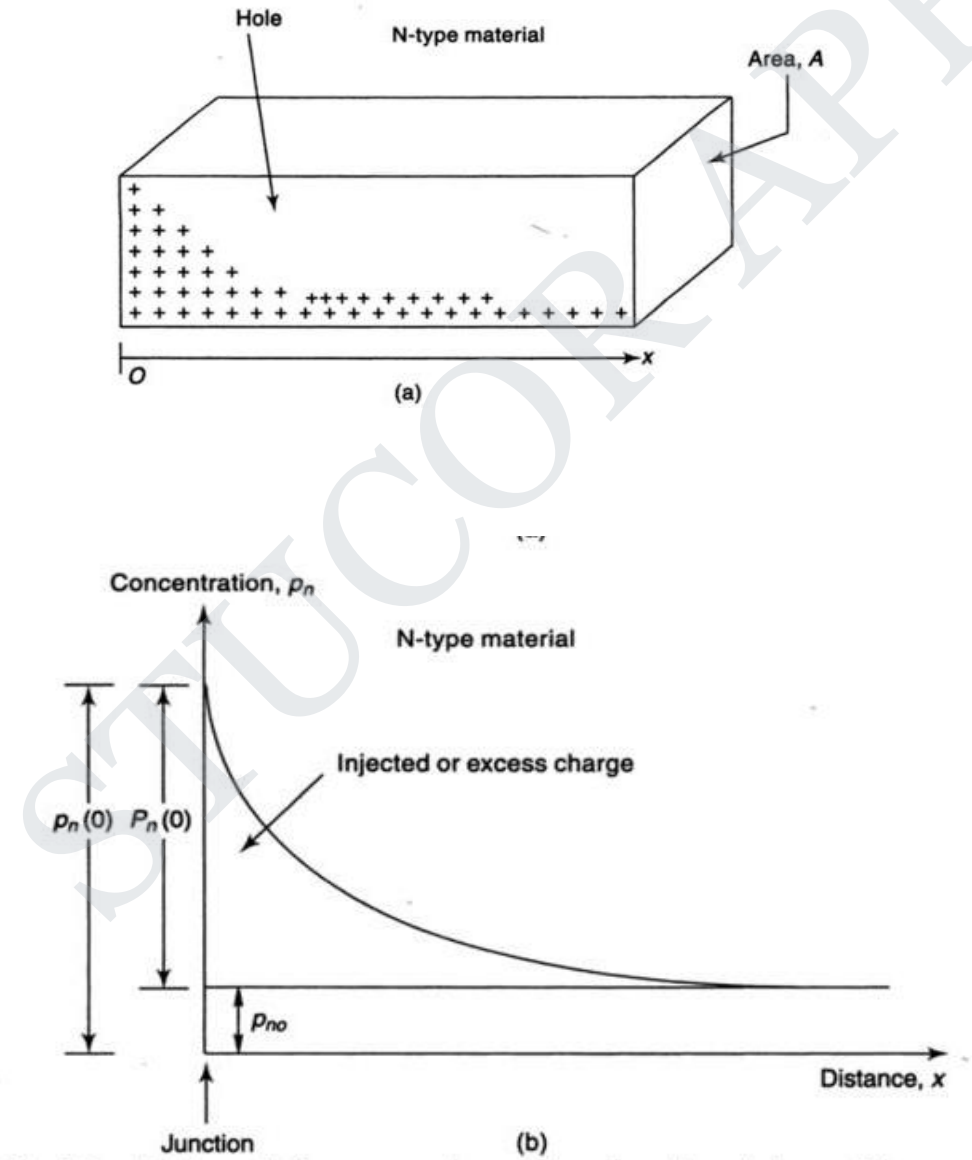


Fig. 4.6 (a) Excess hole concentration varying along the axis in an N-type semiconductor bar, and (b) The resulting diffusion current

As indicated in Fig., the hole concentration p(x) in a semiconductor bar varies from a high value to a low value along the x-axis and is constant in the y- and z-directions.

Diffusion current density due to holes is Jp= - q Dp dp/dx A/cm²

Diffusion current density due to electrons is Jn= q Dn dn/dx A/cm²

Dn & Dp ⇨ Diffusion coefficients

dn/dx & dp/dx ⇨ concentration gradients for electrons and holes

TOTAL CURRENT

- The total current in a semiconductor is the sum of drift current and diffusion current. Therefore, for a P-type semiconductor, the total current per unit area, i.e. the total current density is given by

$$J_p = qp\mu_p E - qD_p \frac{dp}{dx}$$

Similarly, the total current density for an N-type semiconductor is given by

$$J_n = qn\,\mu_n\,E + qD_n \frac{dn}{dx}$$

EINSTEIN RELATIONSHIP FOR SEMICONDUCTOR

There exists a definite relationship between the mobility and diffusion coefficient of a particular type of charge carrier in the same semiconductor.

The higher the value of mobility of a charge carrier, the greater will be its tendency to diffuse. The equation which relates the mobility μ and the diffusion coefficient D is known as the Einstein Relationship. The Einstein relationship is expressed as

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = \frac{kT}{q} = V_T \qquad (4.5)$$

The importance of Einstein relationship is that it can be used to determine D_p (or D_n), if the mobility of holes (or electrons) is measured experimentally. For an intrinsic silicon, $D_p = 13$ cm²/s and $D_n = 34$ cm²/s. For an intrinsic germanium, $D_p = 47$ cm²/s and $D_n = 99$ cm²/s

DIFFUSION LENGTH (L)

- As shown in Fig., the excess hole or electron densities fall off exponentially with distance as a result of the recombination of these excess minority carriers with the majority carriers of the semiconductor. Here, the excess charge carriers have a finite life time, ב, before they are totally destroyed by recombination.

- The average distance that on excess charge carrier can diffuse during its life time is called the diffusion length L, which is given by

$$L = \sqrt{D\tau}$$

where D is the diffusion coefficient that may be related to the drift mobility, μ, through the Einstein relation as

$$D = \mu \frac{kT}{q}$$

7. Briefly explain about depletion region and barrier voltage of a PN junction. (N/D 2015)

As holes enter the n-region, they find number of donor atoms. The holes recombine with the donor atoms. As donor atoms accept additional holes, they become **positively charged immobile ions**. This happens immediately when holes cross the junction hence number of positively charged immobile ions get formed near the junction **on n side.**

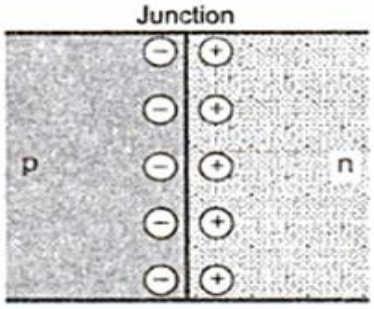


Fig. 1.5 Formation of immobile ions

Atoms on p side are acceptor atoms. The electrons diffusing from n side to p side recombine with the acceptor atoms on p side. As acceptor atoms accept additional electrons, they become **negatively charged immobile ions**. Such large number of negatively charged immobile ions get formed near the junction **on p side**. The formation of immobile ions near the junction is shown in the Fig. 1.5.

As more number of holes diffuse on n side, large positive charge gets accumulated on n side near the junction. Eventually the diffusing holes which are positively charged, get repelled due to accumulated positive charge on n side. And the diffusion of holes stops.

Similarly due to large negative charge accumulated on p side, the diffusing electrons get repelled and eventually the diffusion of electrons also stops.

Thus in thermal equilibrium, in the region near the junction, there exists a wall of negative immobile charges on p side and a wall of positive immobile charges on n side. In this region, there are no mobile charge carriers. Such a region is depleted of the free mobile charge carriers and hence called **depletion region** or **depletion layer**. The depletion region is also called **space-charge region**. **In equilibrium condition, the depletion region gets widened upto a point where no further electrons or holes can cross the junction.** Thus depletion region acts as the **barrier**.

The physical distance from one side to other side of the depletion region is called **width of the depletion region.**

Practically width of the **depletion region** is very small of the order of few microns where 1 micron = 1×10^{-6} m.

Calculation of Depletion Width:

The width of the depletion region in the junction is shown in Figure 1.8. The region contains space charge due to the fact that, donors on the N-side and acceptors on the P-side have lost their accompanying electrons and holes. Hence, an electric field is established which in turn, causes a difference in potential energy, qV_0. Thus, a potential is built up across the junction and Figure 1.8(e) represents the variation in potential. Here, P-side of the junction is at a lower potential than the N-side which means that the electrons on the P-side have a great potential energy.

Let us consider an Alloy junction in which there is an abrupt change from acceptor ions on P-side to donor ions on N-side. Assume that the concentration of electrons and holes in the depletion region is negligible and that all of the donors and acceptors are ionised. Hence, the regions of space charge may be described as:

$$\rho = -qN_A, \quad 0 > x > X_1$$

$$\rho = +qN_D, \quad X_2 > x > 0$$

$$\rho = 0, \quad \text{elsewhere}$$

where ρ is the space charge density, as indicated in Figure 1.8(c) (i) The axes have been chosen in Figure 1.8(e) in such a way that V_1 and X_1 have negative values. The potential variation in the space charge can be calculated by using Poison's equation, which is given by:

$$\nabla^2 V = -\frac{\rho(x, y, z)}{\varepsilon_o \varepsilon_r}$$

where ε_r is the relative permittivity. The equation for the required one-dimensional problem is:

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\varepsilon_o \varepsilon_r}$$

Applying the above equation to the P-side of the junction, we get

$$\frac{d^2V}{dx^2} = \frac{q N_A}{\varepsilon_o \varepsilon_r}$$

Integrating twice, we get

$$V = \frac{q N_A x^2}{2\varepsilon_o \varepsilon_r} + Cx + D$$

where C and D are the constants of integration.

From the Figure 1.8(e), we have $V = 0$ at $x = 0$ and hence $D = 0$. When $x < X_1$ on the p-side, the potential is constant, so that $\frac{dV}{dx}$ at $x = X_1$. Hence,

$$C = -\frac{q N_A}{2\varepsilon_o \varepsilon_r} \cdot X_1$$

Therefore,
$$V = \frac{q N_A x^2}{2\varepsilon_o \varepsilon_r} - \frac{q N_A}{\varepsilon_o \varepsilon_r} \cdot X_1 \cdot x$$

i.e., $$V = \frac{q N_A}{\varepsilon_o \varepsilon_r}\left(\frac{X^2}{2} - X_1 \cdot x\right).$$

As $V = V_1$ at $x = X_1$, we have

$$V_1 = \frac{q N_A}{2\varepsilon_o \varepsilon_r} \cdot X_1^2$$

If same procedure is applied to the N-side, we get

$$V_2 = \frac{q N_D}{2\varepsilon_o \varepsilon_r}\left(N_A X_1^2 + N_D X_2^2\right)$$

Therefore, the total built-in-potential or the contact potential is V_0, where

$$V_0 = V_2 - V_1 = \frac{q}{2\varepsilon_o \varepsilon_r}\left(N_A X_1^2 + N_D X_2^2\right)$$

The positive charge on the N-side must be equal in magnitude to the negative charge on the P-side. Hence

$$N_A X_1 = - N_D X_2$$

and substituting this relationship in the above equation and using the fact that X_1 is a negative quantity, we get

$$X_1 = - \sqrt{\frac{2\varepsilon_o \varepsilon_r V_0}{q N_A \left(1 + \frac{N_A}{N_D}\right)}}$$

Similarly,

$$X_2 = \sqrt{\frac{2\varepsilon_o \varepsilon_r V_0}{q N_D \left(1 + \frac{N_D}{N_A}\right)}}$$

The total depletion width, $W = X_2 - X_1$ and hence,

$$W^2 = X_1^2 + X_2^2 - 2X_1X_2$$

and then substituting for X_1 and X_2 from the above equations, we get

$$\boxed{W = \sqrt{\frac{2\varepsilon_o \varepsilon_r V_0}{q} \left(\frac{N_A + N_D}{N_A N_D}\right)}}$$

BARRIER POTENTIAL

Due to immobile positive charges on n side and negative charges on p side, there exists an electric field across the junction. This creates potential difference across the junction which is called barrier potential, junction potential, built-in potential or cut-in voltage of p-n junction.

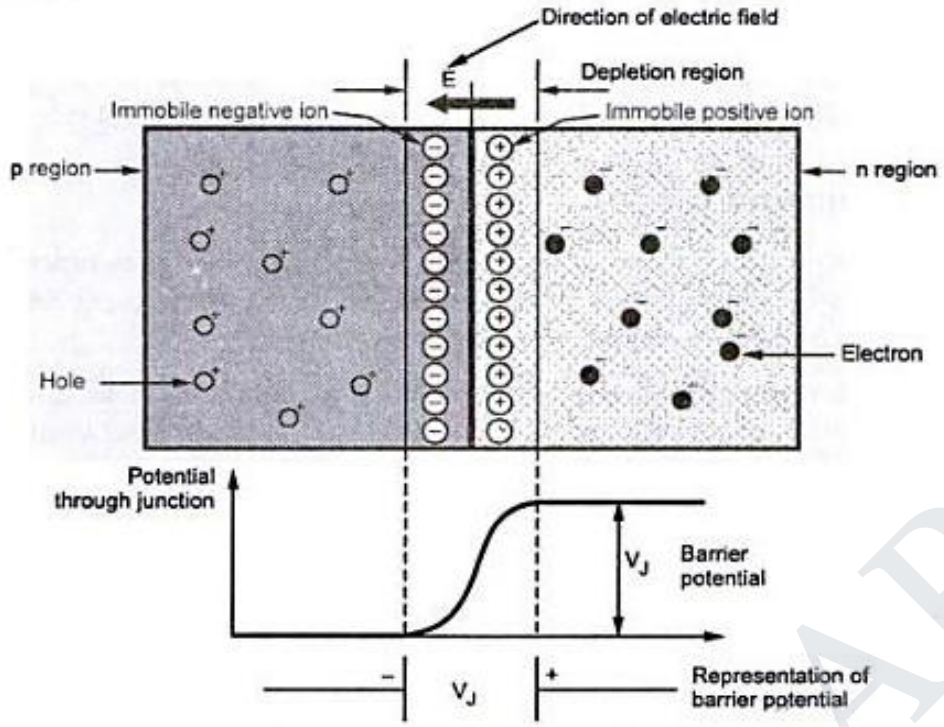


Fig. 1.6 Open circuited p-n junction

The barrier potential depends on,

1. Type of semiconductor
2. The donor impurity added
3. The acceptor impurity added
4. The temperature
5. Intrinsic concentration

Semiconductor material	Symbol	Barrier potential
Silicon	Si	0.6 V
Germanium	Ge	0.2 V

The barrier potential is called height of the depletion region and expressed in volts. Symbolically it is denoted as V_J, V_o or V_γ.

CALCUATION OF BARRIER POTENTIAL

Barrier Potential (V_o or V_{bi})

A contact difference of potential or barrier potential exists across an open circuited PN junction. From Figure 1.13, we have:

$$E_F - E_{vp} = \frac{1}{2} E_G - E_1 \quad \ldots (1)$$

$$E_{cn} - E_F = \frac{1}{2} E_G - E_2 \quad \ldots (2)$$

Combining Equations (1) and (2), we get:

$$E_0 = E_1 + E_2 = E_G - (E_{cn} - E_F) - (E_F - E_{vp}) \quad \ldots (3)$$

We know that,

$$np = N_c N_V e^{-E_G / kT}$$

and $$np = n_i^2 \quad \text{(Mass-action law).}$$

From the above equations, we get

$$E_G = KT \ln \frac{N_c N_V}{n_i^2} \quad \ldots (4)$$

We know that for N-type material

$$E_F = E_C - KT \ln \frac{N_C}{N_D}$$

Therefore, from this equation, we get

$$E_{cn} - E_F = KT\ ln\ \frac{N_c}{n_n} = KT\ ln\ \frac{N_C}{N_D} \qquad \ldots (5)$$

Similary for P-type material

$$E_F = E_V + KT\ ln\ \frac{N_V}{N_A}$$

Therefore, from this equation, we get

$$E_F - E_{vp} = KT\ ln\ \frac{N_V}{P_p} = KT\ ln\ \frac{N_V}{N_A} \qquad \ldots (6)$$

Substituting Equations (4), (5) and (6) into Equation (3), we get

$$E_0 = \left[ln\ \frac{N_C N_V}{n_i^2} - ln\ \frac{N_C}{N_D} - ln\ \frac{N_V}{N_A} \right]$$

$$= KT\ ln \left[\frac{N_C N_V}{n_i^2} \times \frac{N_D}{N_C} \times \frac{N_A}{N_V} \right]$$

Therefore, $$E_0 = KT\ ln\ \frac{N_D N_A}{n_i^2} \qquad \ldots (7)$$

As $E_0 = q\ V_0$, then the contact difference of potential or barrier voltage is given by:

$$\boxed{V_0 = \frac{KT}{q}\ ln\ \frac{N_D N_A}{n_i^2}} \qquad \ldots (8)$$

or $$\boxed{V_0 = V_T\ ln\ \frac{N_D N_A}{n_i^2}}$$

where $V_T = \dfrac{KT}{q}$

k – Boltzman constant = 1.38×10^{-23} J/°k

q – Electronic charge = 1.6×10^{-19}C.

8. Calculate the built in potential barrier in a PN junction. Consider a Si PN junction at T=300K with doping concentration of $N_a=10^{18}$ cm^{-3} and $N_D=10^{15}$ cm^{-3}. Assume that $n_i=1.5x10^{10}$ cm^{-3}. (N/D 2014)(N/D 2017)

So. : $T = 300\ °K,\ N_A = 1\times10^{18}/cm^3 = 1\times10^{24}/m^3,$

$N_D = 1\times10^{15}/cm^3 = 1\times10^{21}/m^3, n_i = 1\times10^{15}/cm^3$

$= 1\times10^{21}/m^3$

$$\therefore \quad V_T = 0.0259\ V \text{ at } T = 300\ °K$$

$$\therefore \quad V_J = V_T\ ln\left[\frac{N_A N_D}{n_i^2}\right] = \mathbf{0.178\ V}$$

9. Determine the ideal saturation current density in a Si PN junction at T=300K. Consider the following parameters in the Si PN junction: $N_D = N_a=10^{16}$ cm^{-3} , $n_i=1.5x10^{10}$ cm^{-3}, $D_n=25$ cm^2/s, $D_p=10$ cm^2/s, $\tau_{p0} = \tau_{n0} = 5x10^{-7}$ s and $\epsilon_r = 11.7$. Comment on the result. (A/M-2015)

Sol. : The reverse current density is given by,

$$J_0 = \frac{I_0}{A} = \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{p0}}{L_n} \quad \ldots (1)$$

The diffusion length for the holes and electrons is given by,

$$L_p = \sqrt{D_p \tau_{p0}},\ L_n = \sqrt{D_n \tau_{n0}}$$

$$n_{p0} = \frac{n_i^2}{N_A}$$

and $$p_{n0} = \frac{n_i^2}{N_D} \quad \ldots \text{by law of mass action}$$

$$\therefore \quad L_p = \sqrt{10\times10^{-4}\times5\times10^{-7}} = 2.236\times10^{-5},$$

$$L_n = \sqrt{25\times10^{-4}\times5\times10^{-7}} = 3.535\times10^{-5}$$

$$n_{p0} = \frac{(1.5\times10^{16})^2}{10^{22}} = 2.25\times10^{10},$$

$$p_{n0} = \frac{(1.5\times10^{16})^2}{10^{22}} = 2.25\times10^{10}$$

$q = 16\times10^{-19}$ C and using in (1),

$$J_0 = 1.6\times10^{-19}\left[\frac{10\times10^{-4}\times2.25\times10^{10}}{2.236\times10^{-5}}+\frac{25\times10^{-4}\times2.25\times10^{10}}{3.535\times10^{-5}}\right]$$

$$= 4.15\times10^{-7}\ A/m^2 \text{ i.e.} 4.15\times10^{-11}\ A/cm^2$$

Comment : Ideally reverse saturation current density is very small. If the area of cross-section A is given as 2×10^{-8} m^2 then I_0 becomes $J_0\times A$ i.e. $4.15\times10^{-7}\times2\times10^{-8} = 8.3119\times10^{-15}$ A. Thus ideally reverse saturation current is also very small.

10. The diode current is 0.6mA when the applied voltage is 400mV, and 20mA when the applied voltage is 500mV. Determine η. Assume kT/q = 25mV (A/M 2016)

Solution:

The diode current, $I = I_o\left(e^{\frac{qV}{\eta kT}}-1\right)$

Therefore, $0.6\times10^{-3} = I_o\left(e^{\frac{qV}{\eta kT}}-1\right) = I_o\, e^{\frac{qV}{\eta kT}}$

$$= I_o\cdot e^{\frac{400}{25\eta}} = I_o\cdot e^{\frac{16}{\eta}} \quad (1)$$

Also, $20\times10^{-3} = I_o\cdot e^{\frac{500}{25\eta}} = I_o\cdot e^{\frac{20}{\eta}}$ (2)

Dividing Eq. (2) by (1), we get

$$\frac{20\times10^{-3}}{0.6\times10^{-3}} = \frac{I_o\cdot e^{\frac{20}{\eta}}}{I_o\cdot e^{\frac{16}{\eta}}}$$

Therefore, $\frac{100}{3} = e^{\frac{4}{\eta}}$

Taking natural logarithms on both sides, we get

$$\log_e\frac{100}{3} = \frac{4}{\eta}$$

$$3.507 = \frac{4}{\eta}$$

Therefore, $\eta = \frac{4}{3.507} = 1.14$

11.The reverse saturation current of a siicon PN junction diode is 10μA. Calculate the diode current for the forward bias voltage of 0.6V at 25° C. (A/M 2016)

$I_o = 10\ \mu A = 1 \times 10^{-5}$ A and $\eta = 2$ for silicon.

The volt-equivalent of the temperature (T) is

$$V_T = \frac{T}{11,600} = \frac{298}{11,600} = 25.7 \times 10^{-3}\ \text{V}$$

Therefore, the diode current, $I = I_o \left(e^{\frac{V_F}{\eta V_T}} - 1 \right)$

$$I = 10^{-5} \left(e^{\frac{0.6}{2 \times 25.7 \times 10^{-3}}} - 1 \right)$$

$$= 1.174\ \text{A}$$

12. Calculate the speed of electron when it falls by a potential of 300 K Volts. (Nov 12)

Given:

Potential = 300 K Volts.

To find:

Speed of electron

Solution:

Speed of electron is given by,

$$V = \sqrt{\frac{2qv}{m}}\ \text{m/s}$$

q = 1.6×10^{-19} C

m = 9.107×10^{-31}

v = 300×10^3 V

$$= \sqrt{\frac{2 \times 1.6 \times 10^{-19} \times 300 \times 10^3}{9.107 \times 10^{-31}}}$$

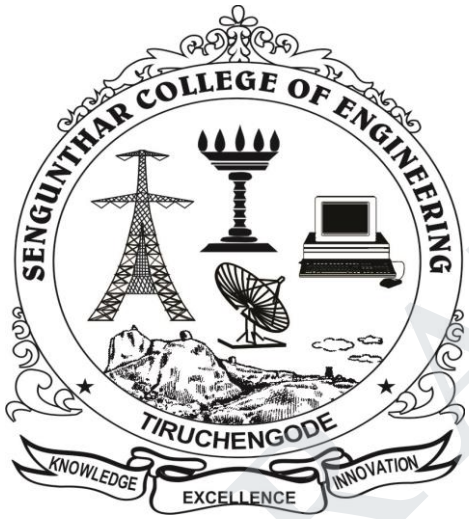
= 324.8 × 10^6 m/s.

EC8252- ELECTRONIC DEVICES

I YEAR / II SEMESTER B.E. (ME)

UNIT – II

BIPOLAR JUNCTION TRANSISTORS



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DEPARTMENT OF MEDICAL ELECTRONICS

SENGUNTHAR COLLEGE OF ENGINEERING – TIRUCHENGODE

UNIT – II

BIPOLAR JUNCTION TRANSISTORS

- NPN -PNP – Operations
- Early effect-Current equations
- **Input and Output characteristics of CE, CB, CC**
- **Hybrid -π model**
- **h-parameter model**
- **Ebers Moll Model**
- **Gummel Poon-model**
- **Multi Emitter Transistor**

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LIST OF IMPORTANT QUESTIONS

UNIT II – BIPOLAR JUNCTION TRANSISTORS

PART – A

1. **For a transistor, if β=200, find the value of α. (N/D-19)**
2. **Define bipolar junction transistor (BJT)/ Why BJT is called as current controlled device (A/M18) (N/D-19)**
3. **Define Early Effect in BJT? (OR) What is mean by base width modulation?(N/D-15, 17) (M/J-2017) (M/J-2016)(A/M-2018) (A/M-2019)**
4. **State the 'h' parameter equation for a NPN transistor under CE configuration (A/M-19)**
5. **State the reason behind the popularity of Common Emitter configuration of BJT. (N/D-17)**
6. **Compare BJT & FET / State the difference between BJT and FET(N/D-2017) (A/M-17)**
7. **If a transistor has a α = 0.97, find the value of β. (M/J-2017)**
8. **Draw the common base configuration. (N/D-16)**
9. **A transistor has β = 150, find the collector and base current, if I_E = 10mA (M/J-2016)**
10. **What are multiple emitter transistors? Draw the symbol of that. (N/D-15)**

PART – B

1. Explain the characteristics of BJT in CC, CB, and CE configuration and Compare the performance of a transistor in three configurations. (OR) Discuss the Input and Output characteristics of CE configuration. (OR) Draw the circuit diagram of an NPN junction transistor CB configuration and describe the static input and output characteristics. Also define the active, saturation and cut off regions. (OR) Draw the CE configuration of NPN transistor and explain its input and output characteristics with diagram. (OR) Explain the Input and Output characteristics of CB configuration. (OR) Discuss the three different configurations of BJT along with its characteristics and also highlight the impact of Base Width modulation.(OR) How do you modify the structure of a simple BJT to operate it fir 250V and 7A? Discuss the characteristics of such a device and identify its limitations. (M/J-14) (A/M-15) (N/D-15) (A/M-16) (N/D-16) (N/D-17)(A/M-2018) (A/M-19) (N/D-19)

2. Define the hybrid parameters for a basic transistor circuits in CE configuration and give its hybrid model. (OR) With relevant expression and sketch describe h parameter model. (OR) Draw the h parameter equivalent circuit for NPN transistor CE circuit. Define and derive for all components. (OR) Derive the hybrid parameters for the CE. (N/D-14)(A/M-15) (N/D-15) (N/D-16) (N/D-19)

3. Write short notes on :

(i)Early Effect (OR) With relevant expressions and figure, describe Early Effect. (N/D-14) (A/M-15)

(ii) Ebers Moll Model for BJT (OR) Draw the Eber's Moll Model for a PNP transistor and explain its significance. / Design and analyze a NPN bipolar junction transistor using Eber moll transistor model (N/D-14) (A/M-17) (N/D-17) (A/M-19) (A/M2018).

4. Derive the expression of Gummel Poon model with a neat circuit diagram. (OR) Analyze the two different functionality of BJT with appropriate equivalent circuit models. (N/D-16) (N/D-17)

5. What is known as current amplification factor? Derive the relationship between the amplification factor of CE, CB and CC configuration. (A/M-17)

PART – A

1. For a transistor, if β=200, find the value of α . (N/D-19)

2. Define bipolar junction transistor (BJT)/ Why BJT is called as current controlled device (A/M18) (N/D-19)

- In bipolar junction transistor, the current conduction depends on both majority and minority charge carriers. It is also called as Current controlled device.
- The bipolar junction transistor consists of two back-to-back *P-N* junctions manufactured in a single piece of a semiconductor crystal. These two junctions give rise to three terminals called emitter, base and collector.

3. Define Early Effect in BJT? (OR) What is mean by base width modulation?(N/D-15, 17) (M/J-2017) (M/J-2016)(A/M-2018) (A/M-2019)

- When the collector base voltage is increased, the depletion region across collector base tends to increases, with result that the effective width of base decreases.
- This variation of effective base width by collector base voltage is called base width modulation or early effect. This decrease in effective base-width has three consequences:
- There is less chance for recombination within the base region.
- The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.
- For extremely, large voltages, the effective base-width may be reduced to zero causing voltage breakdown in the transistor. This phenomenon is called the punch through.

4. State the 'h' parameter equation for a NPN transistor under CE configuration (A/M-19)

5. State the reason behind the popularity of Common Emitter configuration of BJT. (N/D-17)

The CE Configuration is most commonly used. The reasons are

- High voltage gain
- High Current gain
- High power gain
- Moderate input to output ratio.

6. Compare BJT & FET / State the difference between BJT and FET(N/D-2017) (A/M-17)

S.NO	BJT	FET
1	In BJT both holes and electrons conduction that is depends on both majority and minority carriers.	In FET only one charge carrier are responsible for conduction. It depends only on majority carriers.
2	It is current controlled device	It is voltage controlled device
3	It has thermal breakdown	No thermal breakdown
4	Configurations are CE,CB,CC	Configurations are CS,CG,CD
5	Higher sensitivity to changes in the applied signals	Less sensitivity to changes in the applied voltage.
6	Fabrication is difficult	Easy to fabricate and occupies less space
7	Due to junctions the speed is limited	It has higher switching speeds
8	Lower voltage gain	Higher voltage gain
9	Large gain band with product	Low gain band with product.

10	Thermal stability is less	Thermal stability is more

7. If a transistor has a α = 0.97, find the value of β. (M/J-2017)

Given :

$\alpha = 0.97$

To find

$\beta = ?$

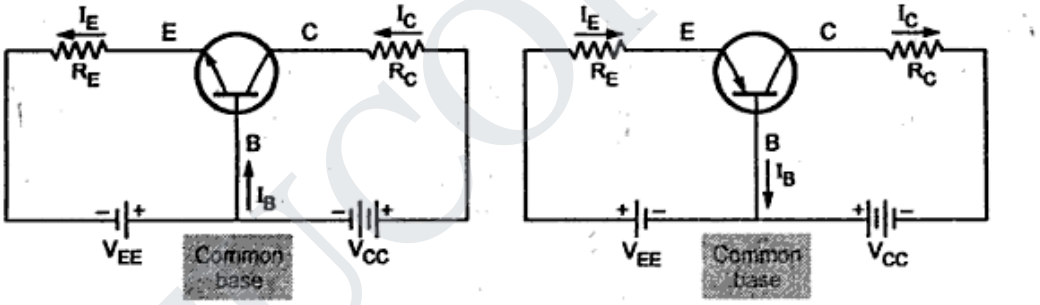
Solution :

$$\beta = \frac{\alpha}{1-\alpha}$$

$$= \frac{0.97}{1-0.97}$$

$$\boxed{\beta = 32.33}$$

8. Draw the common base configuration. (N/D-16)



9. A transistor has β = 150, find the collector and base current, if I_E = 10mA (M/J-2016)

10. What are multiple emitter transistors? Draw the symbol of that. (N/D-15)

A bipolar junction transistor, with 2 or more emitters is known as multi-emitter transistor. A multiple-emitter transistor in a specialized bipolar transistor mostly used at the inputs of TTL NAND logic gates. Input signals are applied to the emitter. Collector current stops flowing only if all emitters are driven by the logical high voltage, thus performing an AND logical operation using a single transistor.

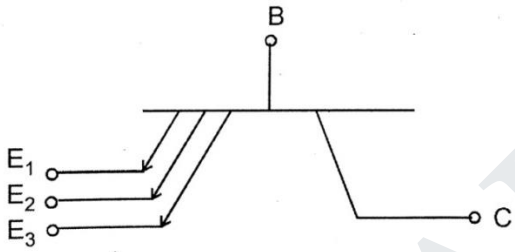


Fig. 2.31: Symbol of multi-emitter transistor

11. Sketch the Ebers Moll Model? (A/M-15)

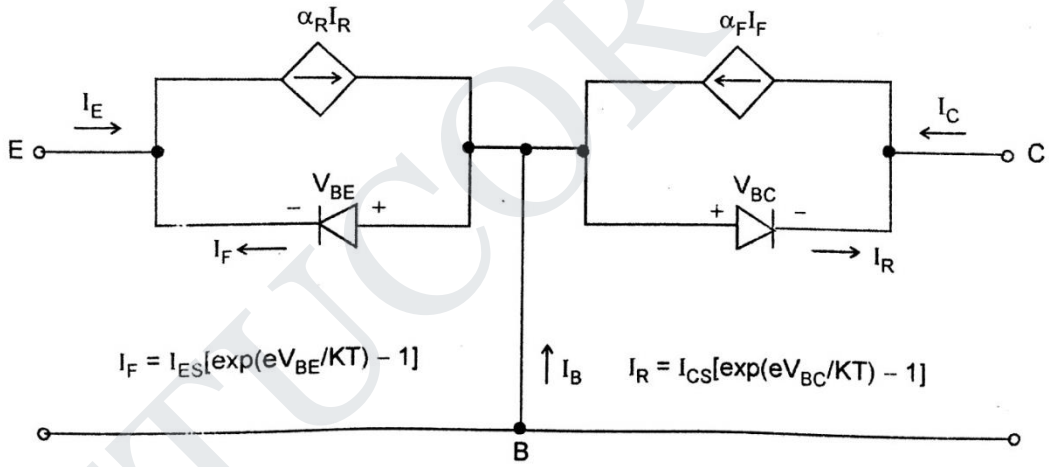


Fig. 2.28: Basic Ebers-Moll equivalent circuit

12. What is the major difference between a bipolar and unipolar device? (N/D-14)

Unipolar Device	**Bipolar Device**
The current conduction is only due to one type of carriers. i.e Majority carriers	The current conduction is due to both majority as well as minority carriers
Example : BJT	Example : FET

13. Calculate the collector and emitter current level for a BJT with α_{dc}=0.99 and I_B =20 μA (N/D-14)

Given :

α_{dc}=0.99 and I_B =20 μA

Solution:

We know that **$\alpha = I_C / I_E$**

$0.99 = I_C / I_E$

$0.99 \times I_E = I_C$

Emitter Current **$I_E = I_C + I_B$**

$= 0.99 \times I_E + 20\ \mu A$

$I_E - (0.99 \times I_E) = 20\ \mu A$

$= (1-0.99)\ I_E = 20\mu A$

$I_E = 20 \times 10^{-6} / 0.01 = 2.0 \times 10^{-3} = 2mA$

$I_C = 0.99 \times 2 = 1.98\ mA$

14. What is the need for biasing in the transistor? (M/J-2014)

- In order to operate transistor in the desired region we have to apply external dc voltages of correct polarity and magnitude to the two junctions of the transistor. This is nothing but the biasing of the transistor.
- Because dc voltages are used to bias the transistor biasing is known as dc biasing transistor

15. Draw the h – Parameters model for CE transistor? (M/J-2014)

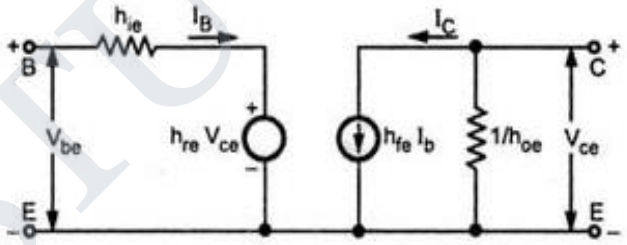


Fig. 2.12 h-parameter equivalent circuit for the common emitter configuration

16. Distinguish between h parameter and hybrid π model. (A/M-16)

HYBRID MODEL:

- It is very easy to calculate parameters like reverse voltage gain, forward current gain, input resistance/ admittance, output resistance/admittance
- We consider here resistances of BJT and capacitance also like junction capacitance, junction resistance, we here calculate gain easily by knowing load resistance and input resistance and the results are accurate.

HYBRID PI MODEL:

- We use hybrid model of BJT to simplify the analysis and for accurate gain values.
- In pi model we use millers theorem, for knowing input side capacitance (diffusion,drift) and input side resistance equivalent effect with formulae and analysis is made using it.

17. Write the Advantages of FET over BJT?

- Higher Voltage gain
- No thermal break down
- It has higher switching speeds
- It offers high input impedance
- It depends only on majority carriers

18. State the relation between α & β of a transistor (or) Define α & β of a transistor.

Relation between α & β:

$$\alpha = \frac{\beta}{\beta + 1}$$

α_{dc} : It Is defined as the ratio of the collector current resulting from carrier injection to the total emitter current.

$$\alpha_{dc} = \alpha = \frac{I_C}{I_E}$$

Since Ic< Ig the value of α_{dc} is always less than unity. It ranges from 0.95 to 0.995. It represents the current gain in the CB configuration.

β_{dc}: It is defined as the ratio of the collector current to the base current.

$$\beta_{dc} = \beta = \frac{I_C}{I_B}$$

19. What are the methods for biasing?

The transistor needs two bias voltages V_{BB} and V_{CC}. The V_{BB} supply is used for biasing of the emitter junction and V_{CC} supply for biasing the collector base junction. Also it is possible to bias both the junctions using a single supply.

Common Methods:

1. Fixed Bias or Base Bias.
2. Emitter feedback bias.
3. Collector feedback bias
4. Voltage divider bias and
5. Emitter bias.

20. Compare the three transistor configuration with regard to input & output resistance, current & voltage gain.

Characteristics	CB	CE	CC
Input Impedance	Low (about 100Ω)	Low (about 750kΩ)	High (about 750kΩ)
Output Impedance	Very High (about 1MΩ)	High (about 45kΩ)	Low (about 50Ω)
Voltage Gain	About 150 (Medium)	About 500 (Medium)	Less than 1
Current Gain	Less than unity	High	High
Application	For high frequency application	For audio frequency application	For impedance matching

21. What are the three transistor configurations?

- Common base configuration
- common emitter configuration
- common collector configuration

22. Define Transistor. What are the two types of transistors?

- Transistor is a semiconductor device. It is used to amplify the electronic signals such as radio and television signals.
- Transistor consists of two junctions formed by sand witching either P-type or N-type semiconductor between a pair of opposite types. There are two basic types of transistors:
  - The bipolar junction transistor (BJT)
  - The Unipolar Junction transistor (UJT)

23. What are the conditions for biasing?

The values to be maintained for perfect operation are:

- Proper dc value of the collector current.
- Proper value of V_{BE} (0.7V for Si and 0.3V for Ge)
- Proper value of V_{CE} (1V for Si and 0.5V for Ge) at any instant.

24. What are hybrid parameters (NOV/DEC -10)

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0}$$ = input resistance with output short-circuited, in ohms.

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_o=0}$$ = fraction of output voltage at input with open circuited.

This parameter is ratio of similar quantities, hence unitless.

$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0}$ = Forward current transfer ratio or current gain with output short

Circuited. This parameter is ratio of similar quantities, hence unitless.

$h_{22} = \left.\frac{I_o}{I_i}\right|_{I_i=0}$ =Output admittance with input open circuited, in mhos.

From the above discussion we can say that these parameters are not same. They have different units. In other words, they are mixture of different units and hence referred to as hybrid parameters. These are commonly known as h-parameters.

25. Define delay time & rise time in the switching characteristics of transistor.

The time between the application of the input pulse and the commencement of collector current flow is termed as delay time t_d. and the time required for collector current to reach 90% of its maximum level from 10% level is called rise time t_r.

Thus the turn-on time t_{ON} is the addition of t_r and t_d ($t_{ON} = t_r + t_d$)

26. Define h_{ie} & h_{fe} for a common emitter transistor configuration.

h_{ie} is the input resistance of a common emitter configuration.

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\text{ constant}} = \frac{V_{BE2} - V_{BE1}}{I_{B2} - I_{B1}}$$

The parameter h_{ie} can be obtained as the change in the base voltage V_{BE2}-V_{BE1} divided by the change in the base current I_{B2}-I_{B1} for a constant collector voltage at the quiescent point Q.

h_{fe} is the forward transfer current gain of a common emitter configuration.

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\text{ constant}} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}$$

It is the ratio of change in collector current Ic taken around the quiescent point Q to the corresponding change in the base current I_B for constant value of output voltage V_{CE} at the Q-point.

27. What are the different regions of transistor characteristics?

- Active Region
- Cutoff Region
- Saturation Region

Active region: It is the region in which transistor collector junction is reverse biased & Emitter junction is forward biased.

Cut-off Region: The region in which both the collector & emitter junctions are reverse biased. Acts as an open or OFF switch.

Saturation Region: The region in which both the collector & emitter junctions are forward biased. Acts as a closed or ON switch.

28. What are the difference between UJT and BJT?

S.NO	UJT	BJT
1	It has only one PN junction	It has only two PN junction
2	Three terminals are Emitter,Base1& Base2	Three terminals are Emitter, Base& Collector
3	It has no ability to amplify signals	It has amplify signals

29. A transistor has a typical β of 100. If the collector current is 40mA, what is the value of emitter current?

Given :

Collector current = 40 mA , β = 100

Solution:

We know that **$\beta = I_C / I_B$**

$I_B = I_C / \beta$ = (40x10^-3)/100

= 4×10^{-4} A = 0.4 mA (or) 0.4×10^{-3}

Emitter Current **$I_E = I_C + I_B$**

= (40x10^-3) + (0.4×10^{-3})

= 40.4 mA

30. Determine the base current for the CE transistor circuit if Ic = 80 mA and β = 170.

Given :

Collector current = 80 mA , β = 170

Solution:

We know that **$\beta = I_C / I_B$**

$I_B = I_C / \beta$

= 80 / 170

= 0.47 mA

31. Calculate I_c and I_E for a transistor that has α_{dc} = 0.99 and I_B = 150 μA. Determine the value of β_{dc} for the transistor. (NOV15)

Given:

α_{dc} = 0.99, I_B = 150 μA .

Solution:

β_{dc} **=** α_{dc} **/ (1-** α_{dc} **)**

= 0.99 / (1-0.99) = 99

β_{dc} **=** I_C **/** I_B

$I_C = \beta\ I_B$

= (150 x 99 x 10^ -6)

I_C = 14.85 mA

α_{dc} **=** I_C **/** I_E

$I_E = \alpha_{dc} . I_C$

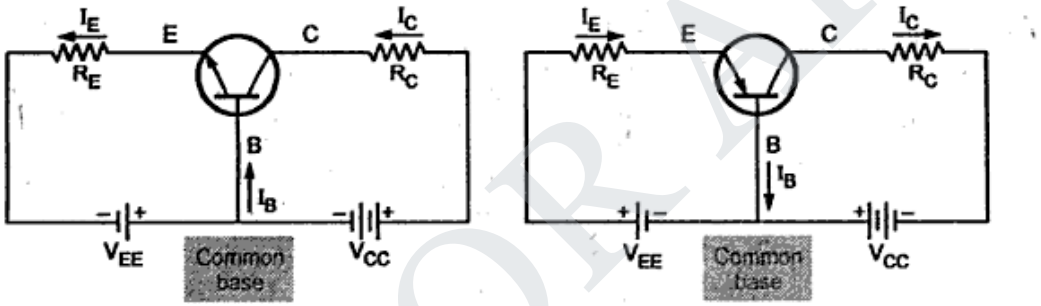
= 14.701 Ma

PART – B

1. Explain the characteristics of BJT in CC, CB, and CE configuration and Compare the performance of a transistor in three configurations. (OR) Discuss the Input and Output characteristics of CE configuration. (OR) Draw the circuit diagram of an NPN junction transistor CB configuration and describe the static input and output characteristics. Also define the active, saturation and cut off regions. (OR) Draw the CE configuration of NPN transistor and explain its input and output characteristics with diagram. (OR) Explain the Input and Output characteristics of CB configuration. (OR) Discuss the three different configurations of BJT along with its characteristics and also highlight the impact of Base Width modulation. (M/J-14) (A/M-15) (N/D-15) (A/M-16) (N/D-16) (N/D-17)(A/M-18) (A/M-19)(N/D-19)

COMMON BASE CONFIGURATION:

- Here the base is common to both the input (Emitter) and output (collector) and hence the name common base connection. This is shown in the fig. The input is applied to the emitter and base and output is taken from the collector and base.



CURRENT APPLICATION FACTOR (α)

- It is the ratio of output current to input current. In a common base connection, the input current is the emitter Current I_E and output current is the collector current I_c.

$$\alpha = I_C / I_E \qquad \text{at constant } V_{CB}$$

- The current amplification factor is less than unity. This value can be increased (but not more than unity) by decreasing the base current. This is achieved by making the base this and doping it lightly. Practical values of a range from 0.9 to 0.99.

EXPRESSION FOR COLLECTOR CURRENT:

- The whole of emitter current does not reach the collector. It is because a small percentage of it, as a result of electron-hole combinations occurring in base area, gives rise to base current flows due to minority carriers.
- The total collector current consists of (i) That part of emitter current which reaches the collector terminal (ii) The leakage current $I_{leakage}$ is due to the movement of minority carriers across base-collector junction on account of it being reverse biased. This is much smaller than $\underline{\alpha}\ I_E$

$$I_C = \underline{\alpha}\ I_E + I_{leakage}$$

- If I_E=0 (i.e. emitter circuit is open), a small leakage current still flows in the collector circuit. This leakage is abbreviated as I_{CBO}, meaning collector-base current with emitter open.

Now,

$$I_E = I_C + I_B$$

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

or

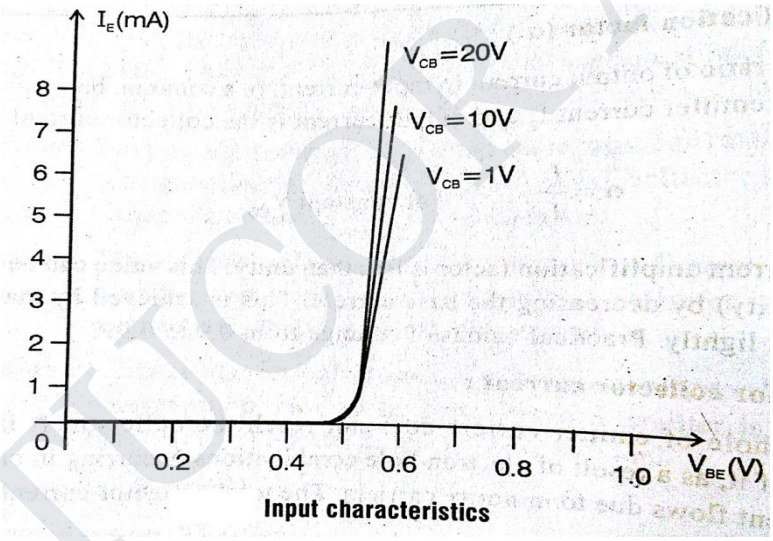
$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

COMMON BASE CHARACTERISTICS:

INPUT CHARACTERISTICS:

The input characteristic for the common base configuration is shown below. It relates an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage. (V_{CB}). The following points are observed from the input characteristics.



Input characteristics

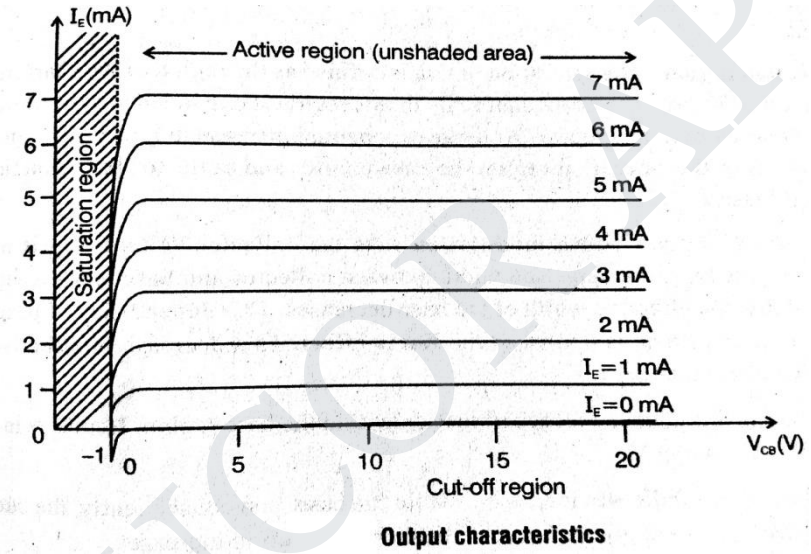
- The emitter current (I_E) increases rapidly after the cut-in voltage with small increase in emitter-base voltage (V_{EB}). It indicates that input resistance is very small. The input resistance is a ratio of change in emitter-base voltage (ΔV_{BE}) to the corresponding change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}) This input resistance is also known as dynamic input resistance in CB configuration.

  Dynamic input resistance = $\Delta V_{BE} / \Delta I_E$

- There is a slight increase in emitter current (I_E) with increase in V_{CB}. The reason behind this is due to the change in the width of the depletion region in the base region under the reverse biased condition.

OUTPUT CHARACTERISTICS:

- It relates an output current (I_C) to an output voltage (V_{CB}) for various levels of input current. (I_E). The output has three basic regions of interest as indicated in Figure. Active region, cut-off region and saturation region. The following points are observed from the output characteristics.
- **Active region** : In the active region, the collector current increases to a magnitude equal to that of the emitter current. The collector current (Ic) is independent on V_{CB}. The relationship between I_E and Ic in the active region is given by
- In the active region the base-emitter junction is forward biased, whereas the collector-base junction is reverse-biased.
- **Cut-off region :** If the emitter current (I_E) is zero, the collector current (I_C) is only due to reverse saturation current .



Output characteristics

Saturation region : The saturation region is defined as the region of the characteristics to the left of V_{CB} =0. The horizontal scale in this region is expanded to show the change in characteristics in this region.

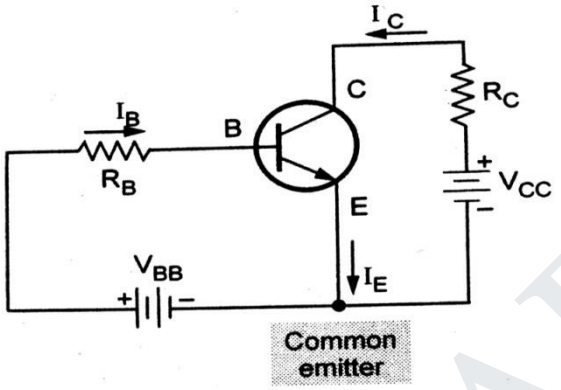
EARLY EFFECT OR BASE-WIDTH MODULATION :

- As the collector voltage Vcc is made to increase the reverse bias, the depletion width between collector and base tends to increase, with the result that the effective width of the base decreases.
- This dependency of base-width on collector-to-base voltage is known as the Early effect. This decrease in effective base-width has three consequences:
- There is less chance for recombination within the base region.
- The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.
- For extremely, large voltages, the effective base-width may be reduced to zero causing voltage breakdown in the transistor. This phenomenon is called the punch through.

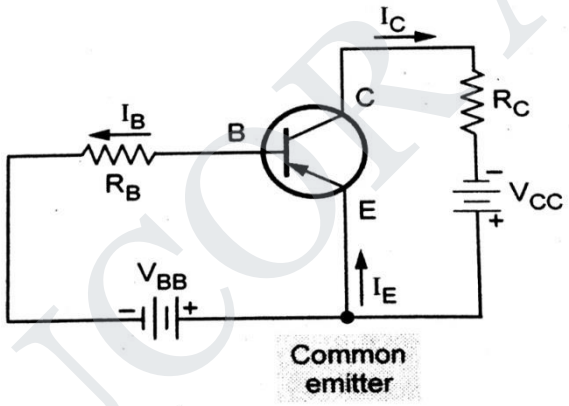
- For higher values of V_{CB} due to early effect, the value of α increases. For example, α changes, say from 0.98 to 0.985. Hence, there is a very small positive slope in the CB Output characteristics and hence the output resistance is not zero.

COMMON EMITTER CONFIGURATION:

- Here the emitter is common to both the input (base) and output (collector) and hence the name common emitter connection.. This is shown in the fig. The input is applied to the base and output is taken from the collector.



(a) npn transistor



(b) pnp transistor

Fig. 2.4.7 Common emitter configurations

Base current amplification factor (β)

It is defined as the ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B) is known as base current amplification factor i.e.

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Relationship between α and β

Using $\beta = \frac{I_C}{I_B}$ then $I_B = \frac{I_C}{\beta}$

$$I_B = \frac{I_C}{\beta} \qquad \text{then } I_E = \frac{I_C}{\alpha}$$

Substituting I_B and I_E into $I_E = I_B + I_C$ we get

$$\frac{I_C}{\alpha} = \frac{I_C}{\beta} + I_C$$

Dividing on both sides by I_C we get

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

$$\therefore \alpha = \frac{\beta}{\beta + 1}$$

and $\beta = \frac{\alpha}{1 - \alpha}$ $\qquad [\because \beta - \alpha\beta = \alpha]$

It is clear that as α approaches unity, β approaches infinity. In other words, the current gain in common emitter connection is very high. It is due to this reason that this circuit arrangement is used in about 90 to 95 percent of all transistor applications.

Expression for collector current :

We know that, $I_E = I_B + I_C$ .....(i)

and $I_C = \alpha I_E + I_{CBO}$ .....(ii)

From exp (ii), we get $I_C = \alpha I_E + I_{CBO} = \alpha(I_B + I_C) + I_{CBO}$

or $I_C(1-\alpha) = \alpha I_B + I_{CBO}$

or $$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$ .....(iii)

From exp (iii) if I_B=0 (i.e. base circuit is open), the collector current will be the current to the emitter. This is abbreviated as I_{CEO} meaning collector-emitter current with base open.

$$I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$$ ..... (iv)

Substituting exp (iv) in exp (iii), we get

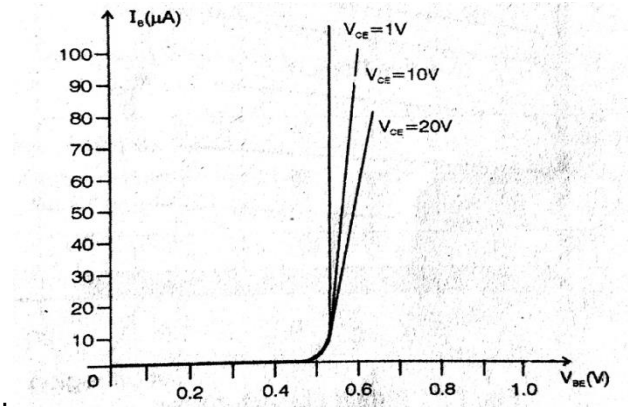
$$I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO}$$

$$I_C = \beta I_B + I_{CEO}$$

COMMON EMITTER CHARACTERISTICS:

INPUT CHARACTERISTICS:

The input characteristic for the common emitter configuration is shown below. It relates an input current (I_B) to an input voltage (V_{BE}) for various levels of output voltage. (V_{CE}). The following points are observed from the input characteristics



The following points are observed from the input characteristics.

(i) The base current (I_B) increases rapidly after the cut-in voltage with small increase in base-emitter voltage (V_{BE}). It indicates that input resistance is very small. The input resistance is a ratio of change in base-emitter voltage (ΔV_{BE}) to the corresponding change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE})

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\ \text{constant}}$$

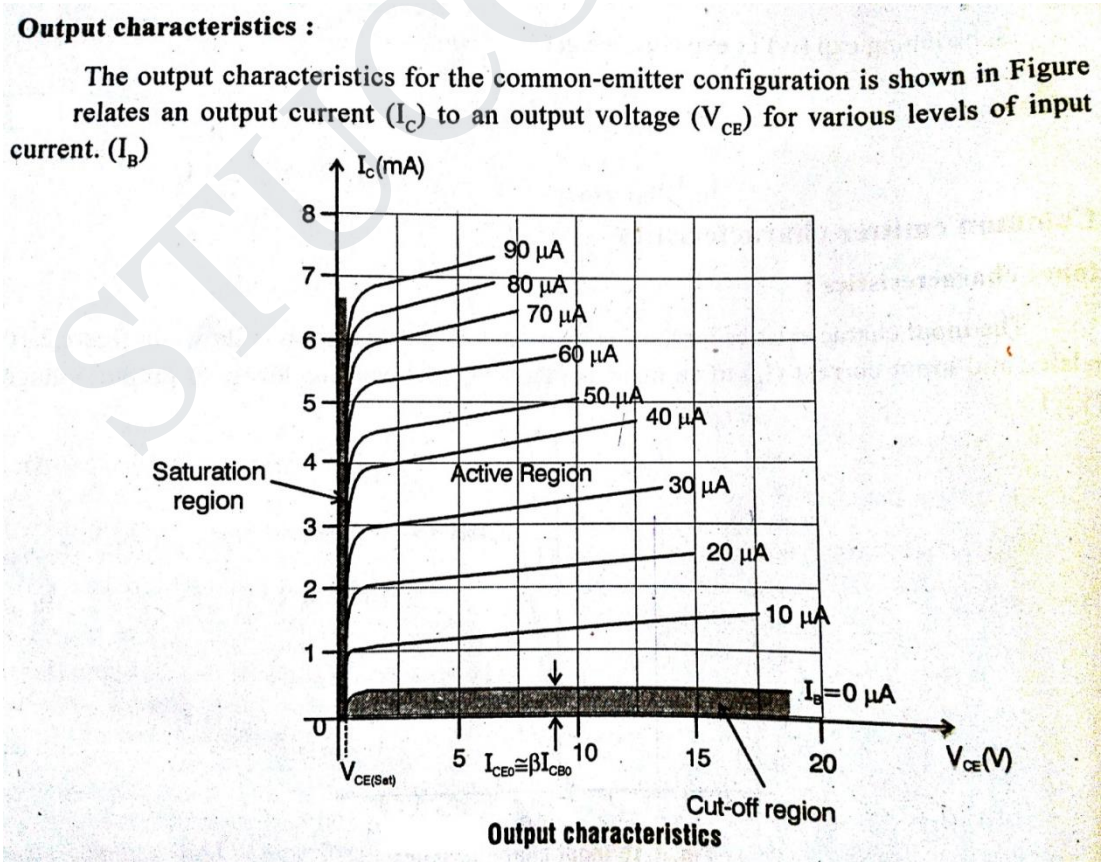
(ii) As V_{CE} is increased for a fixed value of V_{BE}, the base current (I_B) decreases. The reason behind this is, a large value of V_{CE} results in a large reverse bias at collector junction (J_C) i.e. collector-base junction. This increases depletion range and reduces the width of the base. As a result, there are fewer recombinations in the base region, reducing the base current (I_B) as shown in Figure 1

The curves of I_B are not as horizontal as those obtained in for I_E in the CB configuration, indicating that the V_{CE} will influence the magnitude of I_C.

OUTPUT CHARACTERISTICS:

Output characteristics :

The output characteristics for the common-emitter configuration is shown in Figure relates an output current (I_C) to an output voltage (V_{CE}) for various levels of input current. (I_B)



Output characteristics

The output has three basic regions of interest as indicated in Figure 2.11 the active region, cut-off region and saturation region. The following points are observed from the output characteristics.

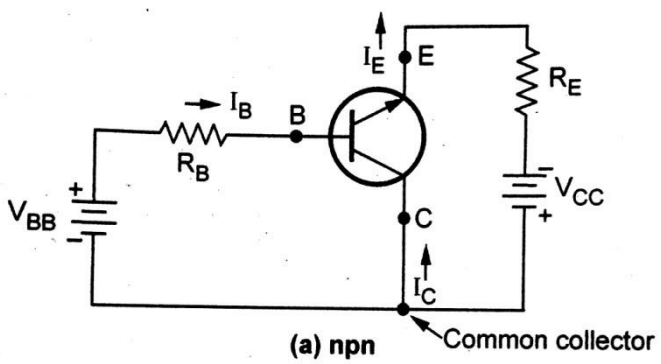
(i) **Active region :** In the active region, the base-emitter junction is forward-biased, whereas the collector-base junction is reverse-biased. As V_{CE} is increased, reverse bias increases. Due to early effect, a very small change is reflected in a very large change in β (when reverse bias is increased, the depletion region spreads more in base than in collector, reducing recombination in the base). When $\alpha = 0.98$, $\beta=49$ $\left[\therefore \beta = \frac{\alpha}{1-\alpha}\right]$. If α increases to 0.985 then β = 66. Here, a slight increase in α by about 0.5% results in an increase in β by about 34% Hence, the output characteristics of C_E configuration show a larger slope when compared with C_B configuration.

(ii) **Cut-off region :** In the cut-off region the base-emitter and collector-base junctions of a transistor are both reverse biased. If the input base current (I_B) is zero, the collector current is only due to reverse leakage current (I_{CEO}), as shown in figure

(iii) **Saturation region :** In the saturation region, the base-emitter and collector-base junction of a transistor are both forward biased. The region to the left of $V_{CE(sat)}$ is called the saturation region. If V_{CE} is reduced to a small value such as 0.2v, then collector-base junction becomes forward biased. The base-emitter junction is always forward biased to operate the transistor in active region. Hence, the transistor operates in the saturation region. The typical value of $V_{CE(sat)}$ ranges between 0.1 and 0.3V.

COMMON COLLECTOR CHARACTERISTICS:

- In this circuit arrangement, input is applied between base and collector while output is taken between the emitter and the collector. Here, collector of the transistor is common to both input and output circuits and hence the name common collector connection.



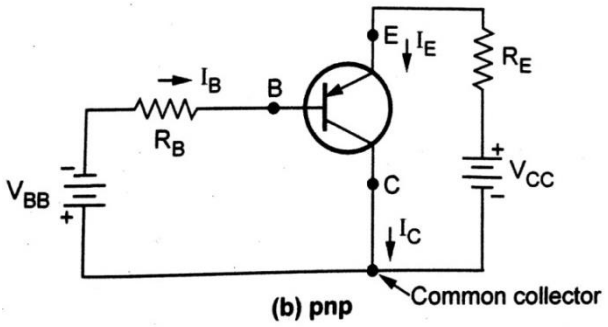


Fig. 2.4.11 Common collector configurations

The common collector configuration is used for impedance matching purpose since it has a high input impedance and low output impedance.

Current amplification factor (γ)

It is defined as the ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B) is known as current amplification factor in common collector (CC) arrangement. i.e.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Relation among α, β and γ

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \qquad \text{.....(i)}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \qquad \text{.....(ii)}$$

Now, $I_E = I_B + I_C$

or $\Delta I_E = \Delta I_B + \Delta I_C$

or $\Delta I_B = \Delta I_E - \Delta I_C$

Substituting the value of ΔI_B in exp (i), we get,

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_c}$$

Dividing the numerator and denominator on R.H.S by ΔI_E we get,

$$\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha}$$

$$\therefore \gamma = \frac{1}{1-\alpha} = (\beta + 1)$$

Expression for the output current

We know $I_C = \alpha I_E + I_{CBO}$

Also $I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO})$

$I_E(1-\alpha) = I_B + I_{CBO}$

or $I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$

or $I_E = (\beta+1)I_B + (\beta+1)I_{CBO}$

or $\boxed{I_E = \gamma I_B + \gamma I_{CBO}}$

INPUT CHARACTERISTICS:

- The input characteristics for the common-collector configuration are shown in Fig. relates an input current (I_B) to an input voltage (V_{BC}) for various levels of output voltage (V_{EC})
- The common-collector input characteristics are different from either common-base common-emitter input characteristics.

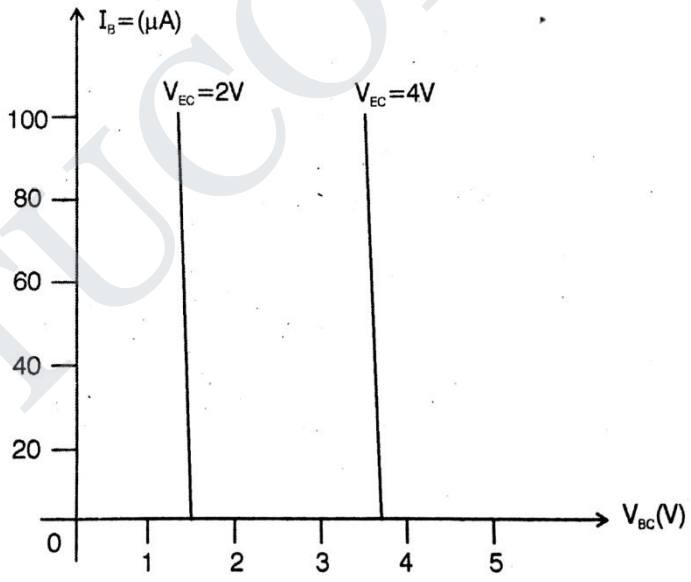


Fig. 2.14 Input characteristics

The difference due to the fact that the input voltage (V_{BC}) is largely determined by th output voltage (V_{CE}). Referring to Fig. 2.13

$$V_{EC} = V_{EB} + V_{BC}$$

or $$V_{EB} = V_{EC} - V_{BC}$$

Increasing the level of V_{BC} with V_{EC} held constant reduces the base-emitter voltag (V_{EB}) and thus reduces I_B. This explains the slope of the CC input characteristics.

A common-collector circuit configuration in Fig. 2.15 with the load resistor connecte from emitter to ground.

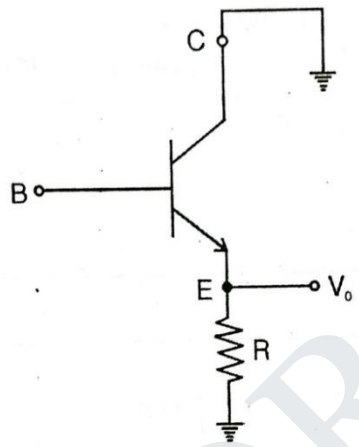


Fig. 2.15 CC configuration used for impedance-matching

The collector is tied to ground even though the transistor is connected similar to the common-emitter configuration for the common-collector configuration output is taken from the emitter terminal.

OUTPUT CHARACTERISTICS:

The output characteristics relates an output current (I_E) to an output voltage (V_{CE}) fo various levels of input current (I_B) as shown in Figure 2.16

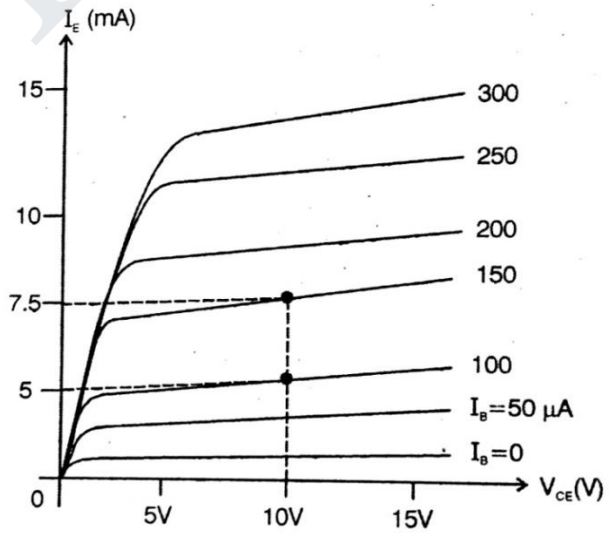


Fig. 2.16 Output characteristics

- For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration.
- For the common-collector configuration the output characteristics is I_E Vs V_{CE} for a range of values of I_B. The input current (I_B) is, same for both CE and CC characteristics.
- The horizontal voltage axis for the common collector configuration is obtained by changing the sign of the collector-to-emitter voltage of the CE characteristics.

2. Define the hybrid parameters for a basic transistor circuits in CE configuration and give its hybrid model. (OR) With relevant expression and sketch describe h parameter model. (OR) Draw the h parameter equivalent circuit for NPN transistor CE circuit. Define and derive for all components. (OR) Derive the hybrid parameters for the CE. (N/D-14)(A/M-15) (N/D-15) (N/D-16)(N/D-19)

Midband Analysis of BJT Single Stage Amplifiers

The Fig. shows basic amplifier circuit. From the Fig. we can notice that to form a transistor amplifier only it is necessary to connect an external load and signal source, along with proper biasing. Fig. represents a transistor in any one of the three possible configurations.

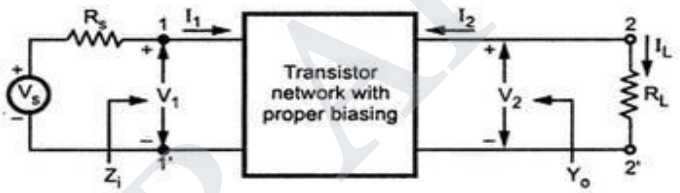


Fig. Basic transistor amplifier

We can replace transistor circuit shown in Fig. with its small signal hybrid model as shown in Fig.

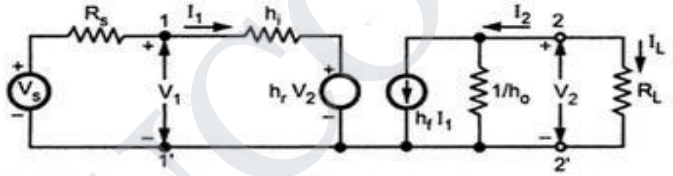


Fig. Transistor amplifier in its h-parameter model

h-parameter equivalent circuit for CE configuration

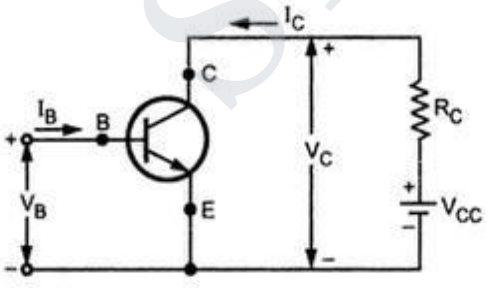


Fig. 2.11 Simple common emitter configuration

To see how we can derive a hybrid model for a transistor, let us consider the common emitter configuration shown in Fig. 2.11. The variables I_b, I_c, V_b and V_c represent total instantaneous currents and voltages.

I_b = Input current.

I_c = Output current.

V_{be} = Input voltage.

V_{ce} = Output voltage.

Fig. 2.12 shows the h-parameter equivalent circuit for the common emitter configuration.

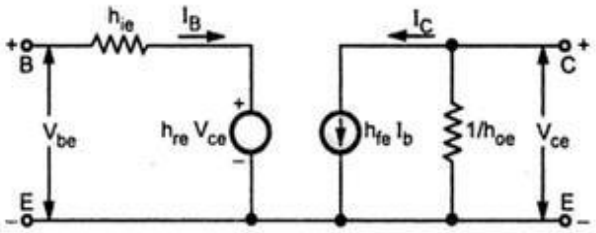


Fig. 2.12 h-parameter equivalent circuit for the common emitter configuration

Current Gain (A_i) :

For transistor amplifier A_i is defined as the ratio of output to input currents. It is given by,

$$A_i = \frac{I_L}{I_1} = -\frac{I_2}{I_1} \quad \ldots (1)$$

Here I_L and I_2 are equal in magnitude but opposite in sign, i.e. $I_L = -I_2$

From the circuit of Fig. 2.19 we have,

$$I_2 = h_f I_1 + h_o V_2 \quad \ldots (2)$$

Substituting $V_2 = -I_2 R_L$ in the equation we obtain

$$I_2 = h_f I_1 + h_o (-I_2 R_L)$$

$$\therefore \quad I_2 + h_o I_2 R_L = h_f I_1$$

$$\therefore \quad (1 + h_o R_L) I_2 = h_f I_1$$

$$\therefore \quad \frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L}$$

$$\therefore \quad A_i = -\frac{I_2}{I_1} = \frac{-h_f}{1 + h_o R_L} \quad \ldots (3)$$

Current Gain (A_{Is}) :

It is the current gain taking into account the source resistance, R_s if the model is driven by the current source instead of voltage source. It is given by

$$A_{is} = -\frac{I_2}{I_s} = -\frac{I_2}{I_1} \cdot \frac{I_1}{I_s} \quad \ldots (4)$$

$$= A_i \cdot \frac{I_1}{I_s}$$

(a) Input section of hybrid model

(b) Input section of hybrid model with current source instead of voltage source

Fig. 2.18

Looking at Fig. 2.18 (b) and using current divider equation we get

$$I_1 = \frac{I_s R_s}{Z_i + R_s}$$

$$\therefore \quad \frac{I_1}{I_s} = \frac{R_s}{Z_i + R_s}$$

and hence $$A_{is} = \frac{A_i R_s}{Z_i + R_s} \quad \ldots (5)$$

Input Impedance (Z_i)

As shown in the Fig. 2.16, R_i is the input resistance looking into the amplifier input terminals (1, 1′). It is given by,

$$R_i = \frac{V_1}{I_1} \quad \ldots (6)$$

From the input circuit of Fig. 2.19, we have

$$V_1 = h_i I_1 + h_r V_2 \quad \ldots (7)$$

Hence $$Z_i = \frac{V_1}{I_1} = \frac{h_i I_1 + h_r V_2}{I_1}$$

$$\therefore \quad Z_i = h_i + h_r \frac{V_2}{I_1} \quad \ldots (8)$$

Substituting $$V_2 = -I_2 R_L = A_i I_1 R_L \quad \ldots (9)$$

In the above equation we get,

$$Z_i = h_i + \frac{h_r A_i I_1 R_L}{I_1} = h_i + h_r A_i R_L \quad \ldots (10)$$

Substituting $$A_i = -\frac{h_f}{1 + h_o R_L}$$

we get, $$Z_i = h_i - \frac{h_r h_f R_L}{1 + h_o R_L} \quad \ldots (11)$$

Dividing numerator and denominator by R_L we get,

$$Z_i = h_i - \frac{h_r h_f}{1/R_L + h_o}$$

$$\therefore \quad Z_i = h_i - \frac{h_r h_f}{Y_L + h_o} \quad \text{where } Y_L = \frac{1}{R_L} \quad \ldots (12)$$

From this equation we can note that input impedance is a function of the load impedance.

Voltage Gain (A_v) :

It is the ratio of output voltage V_2 to the input voltage V_1 . It is given by

$$A_v = \frac{V_2}{V_1} \quad \ldots (13)$$

From equation (9) we have,

$$A_v = \frac{A_i I_1 R_L}{V_1} = \frac{A_i R_L}{Z_i} \quad \ldots (14)$$

Since, $\frac{I_1}{V_1} = \frac{1}{Z_i}$

Voltage Gain (A_{vs}) : It is voltage gain including the source. It is given by,

$$A_{vs} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \times \frac{V_1}{V_S} \quad \ldots (15)$$

$$\therefore \quad A_{vs} = A_v \times \frac{V_1}{V_S} \quad \ldots (16)$$

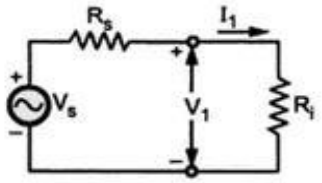


Fig. 2.19

Looking at Fig. 2.19 and applying potential divider theorem we can write,

$$V_1 = \frac{Z_i}{R_s + Z_i} V_S$$

$$\therefore \quad \frac{V_1}{V_S} = \frac{Z_i}{R_s + Z_i}$$

Substituting value of $\frac{V_1}{V_S}$ in equation 16 we get,

$$A_{vs} = A_v \cdot \frac{Z_i}{R_s + Z_i} \quad \ldots (17)$$

$$= \frac{A_i R_L}{R_s + R_i} \quad \because A_v = \frac{A_i R_L}{Z_i} \quad \ldots (18)$$

Output Admittance Y_o :

It is the ratio of output current I_2 to the output voltage V_2. It is given by,

$$Y_o = \frac{I_2}{V_2} \text{ with } V_s = 0 \quad \ldots (19)$$

From equation 2, we have, $I_2 = h_f I_1 + h_o V_2$

Dividing above equation by V_2 we get,

$$\frac{I_2}{V_2} = \frac{h_f I_1}{V_2} + h_o$$

$$\therefore \quad Y_o = h_f \frac{I_1}{V_2} + h_o \quad \ldots (20)$$

From Fig. 2.17, with $V_s = 0$ we can write,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0 \quad \ldots (21)$$

$$\therefore \quad (R_s + h_i) I_1 = -h_r V_2$$

$$\therefore \quad \frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i} \qquad \ldots (22)$$

Substituting value of $\frac{I_1}{V_2}$ from equation 22 in equation 20, we obtain,

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} \qquad \ldots (23)$$

From this equation we can note that output admittance is a function of the source resistance.

3. Write short notes on:

(i)Early Effect (OR) With relevant expressions and figure, describe Early Effect. (N/D-14) (A/M-15)

BASE WIDTH MODULATION OR EARLY EFFECT

- We know that the emitter-base diode characteristic shifts upwards by increasing the value of collector-to-base voltage (V_{CB}). This occurs due to the phenomenon called base width modulation or early effect, which may be explained as follows:
- We know that in a PN junction, the width of a depletion region increases as the reverse-bias voltage increase. In a transistor, since the emitter-base junction is forward-biased, therefore this has no effect on the width of depletion region.
- However, the collector-base junction is reverse biased. Therefore as the reverse-bias voltage across the collector-base junction increases the width of depletion region also increases.

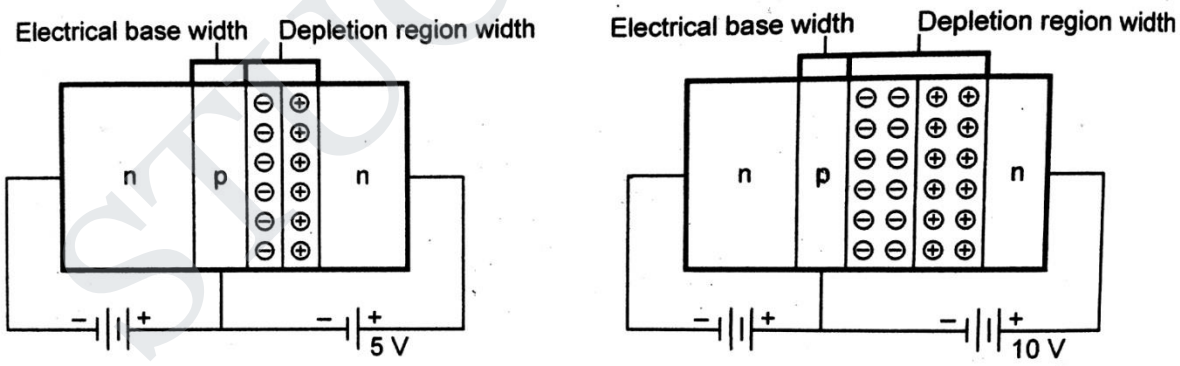


Fig. 2.4.6 Change in base and depletion region width with change in reverse biased voltage

- Since the base is lightly doped, as compared to the collector, therefore depletion region penetrates deeper into the base region. This reduces the effective width of the base region.

- This variation or modulation of the effective base width, by the collector voltage, is known as base width modulation or early effect. The decrease in base width by the collector voltage, has the following three effects:
  - It reduces the chances of recombination of electrons with the holes in the base region. Hence the common base current gain (a) increases with the increase of collector-to-base voltage (V_{CB})
  - The concentration gradient of minority carriers within the base increases. This, in turn, increases the emitter current.
  - For extremely large collector voltage, the effective base width may be reduced to zero, causing voltage breakdown of a transistor. This phenomenon is known as punch through.

be explained with the help of equation

$$V = \frac{e \cdot N_A \cdot W^2}{2\varepsilon}$$

where V = Reverse bias voltage.

and W = Width of the space-charge region/depletion region.

(ii) Ebers Moll Model for BJT (OR) Draw the Eber's Moll Model for a PNP transistor and explain its significance. (N/D-14) (A/M-17) (A/M -18) (N/D-17) (A/M-19)

Ebers-Moll Model is a bipolar transistor model is used in switching applications. This model is based on the interacting diode junctions and is applicable in any of the transistor operating modes. Figure 2.27 shows the current directions and voltage polarities used in the Ebers-Moll model. The currents are defined as all entering the terminals so that:

$$I_E + I_B + I_C = 0 \quad \ldots (1)$$

The direction of the emitter current is opposite, but as long as the analysis are consistent, the defined direction does not matter.

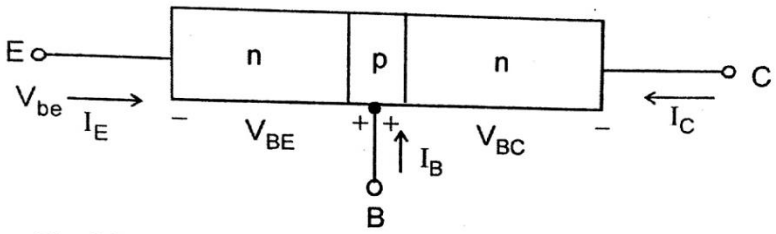


Fig. 2.27: Current direction and voltage polarity for Ebers-Moll model

Figure 2.28 shows the Ebers-Moll equivalent circuit.

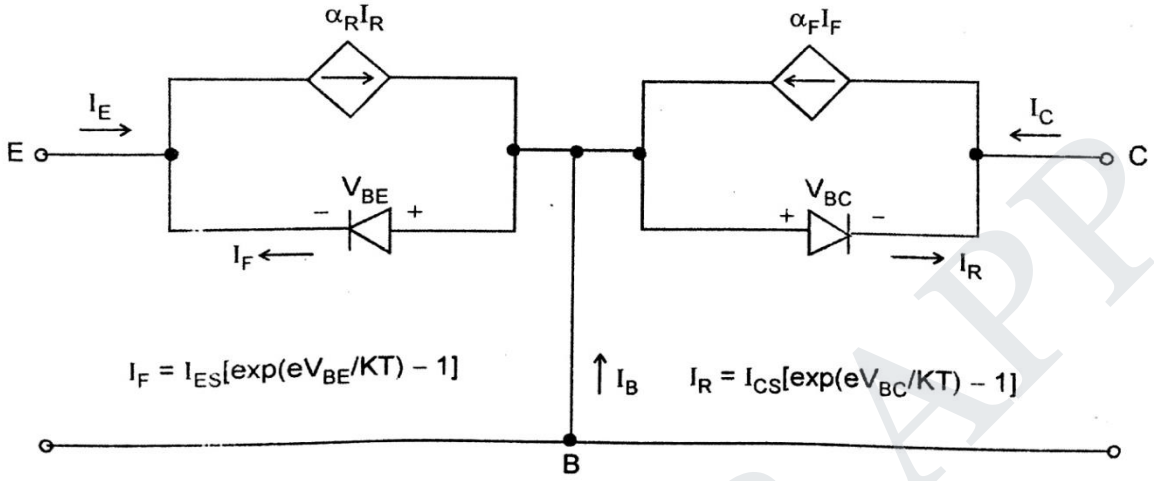


Fig. 2.28: Basic Ebers-Moll equivalent circuit

Two diodes are placed back to back with reverse saturation current I_{ES} (Emitter Base Junction) and I_{CS} (Collector Base Junction) and two dependent current-controlled current sources, represented by $\alpha_R I_R$ and $\alpha_F I_F$. α_F is the forward transmission from emitter to collector, known as common base current gain of transistor. α_R is the reverse transmission from collector to emitter, known as inverse mode of a transistor.

The collector current can be written as:

$$I_C = \alpha_F I_F - I_R \quad \ldots (2)$$

where α_F is the common base current gain in the forward-active mode. In this mode. Equation (2) becomes:

$$I_C = \alpha_F I_F + I_{CS} \quad \ldots (3)$$

where the current I_{CS} is the reverse-bias B – C junction current.

The current I_F is given by:

$$I_F = I_{ES}\left[\exp\left(\frac{eV_{BE}}{KT}\right) - 1\right] \quad \ldots (4)$$

If the B – C junction becomes forward biased, such as in saturation, then the current I_R can be written as:

$$I_R = I_{CS}\left[\exp\left(\frac{eV_{BC}}{KT}\right)-1\right] \quad \ldots (5)$$

Substituting Equation (4) and Equation (5) in Equation (2), the collector current can be written as

$$I_C = \alpha_F I_{ES}\left[\exp\left(\frac{eV_{BE}}{KT}\right)-1\right]-I_{CS}\left[\exp\left(\frac{eV_{BC}}{KT}\right)-1\right] \quad \ldots (6)$$

From Figure 2.28, the emitter current can be written as:

$$I_E = \alpha_R I_R - I_F \quad \ldots (7)$$

Substituting values of I_F and I_R from Equation (4) and Equation (5) in Equation (7), the emitter current can be written as:

$$I_E = \alpha_R I_{CS}\left[\exp\left(\frac{eV_{BC}}{KT}\right)-1\right]-I_{ES}\left[\exp\left(\frac{eV_{BE}}{KT}\right)-1\right] \quad \ldots (8)$$

The current I_{ES} is the reverse bias B – E junction current and α_R is the common base current gain for the inverse-active mode. Equation (6) and Equation (8) are the Ebers-Moll equations.

Figure 2.28 shows the equivalent circuit corresponding to Equations (6) and (8). The current sources in the equivalent circuit represent current components that depend on voltages across other junctions. Ebers-Moll model has four parameters: α_F, α_R, I_{ES} and I_{CS}. The reciprocity relationship states the:

$$\alpha_F I_{ES} = \alpha_R I_{CS} \qquad \ldots (9)$$

Ebers-Moll model can be used for the transistor in saturation. In the saturation mode, both B – E and B – C junctions are forward biased, so that $V_{BE} > 0$ and $V_{BC} > 0$. The B – E voltage is a known parameter since a voltage is applied across this junction. The forward biased B – C voltage is a result of driving the transistor into saturation and is the unknown to be determined from the Ebers-Moll equations. In electronic circuit applications, the collector-emitter voltage at saturation is of interest. Hence, the C – E saturation voltage can be defined as:

$$V_{CE\,(sat)} = V_{BE} - V_{BC} \qquad \ldots (10)$$

An expression for $V_{CE\,(sat)}$ can be found by combining the Ebers-Moll equations.

From Equation (1), the emitter current can be written as:

$$I_E = -(I_C + I_B) \qquad \ldots (11)$$

Combining Equations (11) and (8), we have:

$$-(I_C + I_B) = \alpha_R I_{CS}\left[\exp\left(\frac{eV_{BC}}{KT}\right) - 1\right] - I_{ES}\left[\exp\left(\frac{eV_{BE}}{KT}\right) - 1\right] \qquad \ldots (12)$$

Solving for $\left[\exp\left(\frac{eV_{BC}}{KT}\right) - 1\right]$ from equation (12), and subsitute the resulting expression into equation (6), we can then find V_{BE},

$$V_{BE} = V_T \ln\left[\frac{I_C(1-\alpha_R) + I_B + I_{ES}(1-\alpha_F\alpha_R)}{I_{ES}(1-\alpha_F\alpha_R)}\right] \qquad \ldots (12)$$

where V_T is the thermal voltage $\left[V_T = \frac{KT}{e}\right]$. $\qquad \ldots (13)$

Neglecting I_{ES} in the numerator of Equation (13), we get

$$V_{BE} = V_T \ln\left[\frac{I_C(1-\alpha_R)+I_B}{I_{ES}(1-\alpha_F\alpha_R)}\right] \quad \ldots(14)$$

Similarly, solving for $\left[\exp\left(\frac{eV_{BE}}{KT}\right)-1\right]$ from Equation (6) and substitute this expression into Equation (12), we can find V_{BC} as:

$$V_{BC} = V_T \ln\left[\frac{\alpha_F I_B-(1-\alpha_F)I_C+I_{CS}(1-\alpha_F\alpha_R)}{I_{CS}(1-\alpha_F\alpha_R)}\right] \quad \ldots(15)$$

Neglecting I_{CS} in the numerator of Equation (15), we get

$$V_{BC} = V_T \ln\left[\frac{\alpha_F I_B-(1-\alpha_F)I_C}{I_{CS}(1-\alpha_F\alpha_R)}\right] \quad \ldots(16)$$

The collector to emitter voltage at saturation $[V_{CE\,(sat)}]$ can be found from Equation (10). Substituting Equations (14) and (16), we get,

$$V_{CE\,(sat)} = V_T \ln\left[\left(\frac{I_C-(1-\alpha_R)+I_B}{I_{ES}(1-\alpha_F\alpha_R)}\right)-\left(\frac{\alpha_F I_B-(1-\alpha_F)I_C}{I_{CS}(1-\alpha_F\alpha_R)}\right)\right]$$

$$= V_T \ln\left[\frac{I_C(1-\alpha_R)+I_B}{\alpha_F I_B-(1-\alpha_F)I_C}\cdot\frac{I_{CS}}{I_{ES}}\right] \quad \ldots(17)$$

The ratio of I_{CS} to I_{ES} can be written in terms of α_F and α_R from Equation (9). Hence,

$$V_{CE\,(sat)} = V_T \ln\left[\frac{I_C(1-\alpha_R)+I_B}{\alpha_F I_B-(1-\alpha_F)I_C}\cdot\frac{\alpha_F}{\alpha_R}\right] \quad \ldots(18)$$

4. Derive the expression of Gummel Poon model with a neat circuit diagram. (OR) Analyze the two different functionality of BJT with appropriate equivalent circuit models. (N/D-16) (N/D-17)

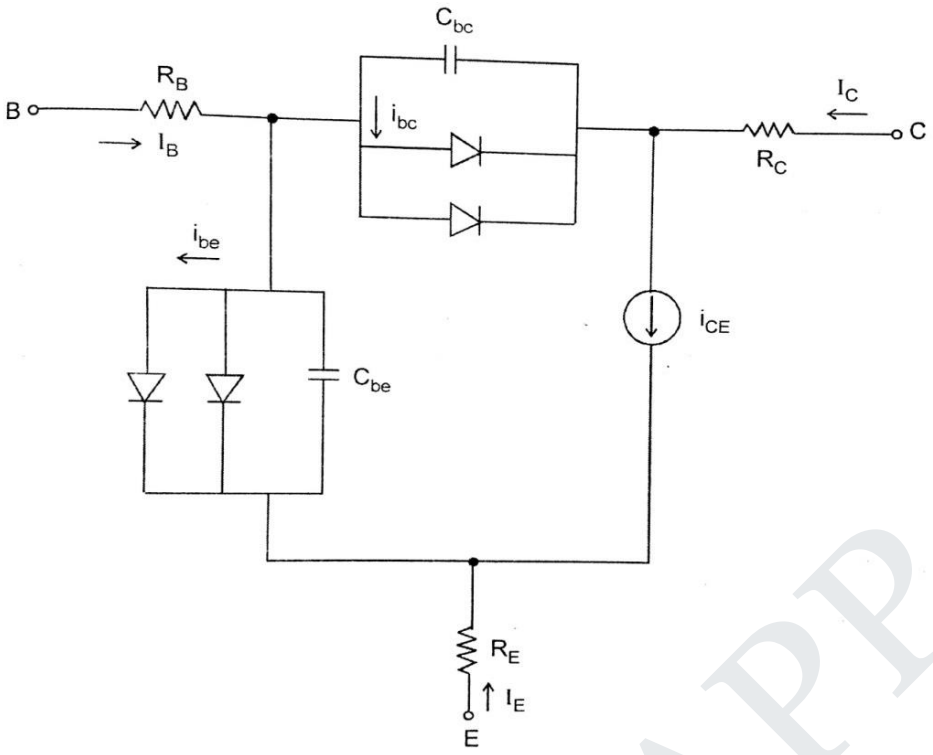


Fig. 2.29 : Gummel-Poon model of bipolar transistor

Gummel-Poon model is a model of the bipolar junction transistor. This model can be used if there is a non-uniform doping concentration in the base. It is used to describe the basis operation of the transistor as well as to describe non-ideal effects such as early effect and high level injection effects. Figure 2.29 shows Gummen-Poon Model of bioplar transmiter.

The two diodes carrying currents i_{bc} and i_{be} represent the base current due to recombination in the depletion the base current due to recombination in the depletion regions. c_{bc} and c_{be} capacitances represent the diffusion and transiton capacitance respectively.

The electron current density in the base of a *npn* transistor can be written as:

$$J_n = e\mu_n n(x)E + eD_n \frac{dn(x)}{dx} \qquad \ldots (1)$$

An electric field will occur in the base if non-uniform doping exists in the base. This is given by:

$$E = \frac{KT}{e} \cdot \frac{1}{p(x)} \cdot \frac{dp(x)}{dx} \qquad \ldots (2)$$

where $p(x)$ is the majority carrier hole concentration in the base.

where $p(x)$ is the majority carrier hole concentration in the base.

The presence of this electric field aids the flow of electron across the base. Substituting Equation (2) into Equation (1), we get

$$J_n = e\mu_n n(x)\cdot\frac{KT}{e}\cdot\frac{1}{p(x)}\frac{dp(x)}{dx} + eD_n\frac{dn(x)}{dx} \qquad \ldots (3)$$

We know that the Einstein reltion is given by:

$$\frac{D_n}{\mu_n} = \frac{KT}{e}$$

Hence Equation (3) can be written as:

$$J_n = e\, n(x)\cdot D_n \cdot \frac{1}{p(x)} \cdot \frac{dp(x)}{dx} + eD_n\frac{dn(x)}{dx}$$

$$= \frac{eD_n}{p(x)}\left[n(x)\cdot\frac{dp(x)}{dx} + p(x)\cdot\frac{dn(x)}{dx}\right]$$

$$= \frac{eD_n}{p(x)}\cdot\frac{d(pn)}{dx} \qquad \ldots (4)$$

Equation (4) can be written in the form

$$\frac{J_n\, p(x)}{e\, D_n} = \frac{d(pn)}{dx} \qquad \ldots (5)$$

Integrating Equation (5) through the base region while assuming that the electron current density is a constant and the diffusion coefficient is a constant, we

$$\frac{J_n}{e\, D_n} \int_0^{x_B} p(x)\, dx = \int_0^{x_B} \frac{dp(x)}{dx}\, dx = p(x_B)n(x_B) - p(0)n(0) \qquad \ldots (6)$$

Assuming the B – E junction is forward biased and the B – C junction is reverse biased, we have $n(0) = n_{BO} \exp(V_{BE}/V_t)$ and $n(x_B) = 0$. But $n_{BO}\, P = n_i^2$, so that Equation (6) can be written as

$$J_n = \frac{-e\, D_p\, n_i^2 \exp(V_{BE}/V_t)}{\int_0^{x_B} p(x)\, dx} \qquad \ldots (7)$$

The integral in the denominator is the total majority carrier charge in the base and is known as the base Gummel number, defined as Q_B.

Similarly, if same analysis is performed in the emitter, then the hole current density in the emitter of an *npn* transistor can be expressed as:

$$J_p = \frac{-e\, D_p\, n_i^2 \exp(V_{BE}/V_t)}{\int_0^{x_E} n(x')\, dx'} \qquad \ldots (8)$$

The integral in the denominator is the total majority carrier change in the emitter and is known as the **emitter Gummel number**, defined as Q_E.

Since the currents in the Gummel-Poon model are function of the total integrated charges in the base and emitter, these currents can be determined for non-uniformly doped transistors.

The Gummel-Poon model can also take into account non-ideal effects, such as the Early effect and high-level injection.

As the B – C voltage changes, the neutral base width changes so that the base Gummel number Q_B changes. The change in Q_B with B – C voltage then makes the electron current density given by Equation (7) a function of the B – C voltage. This is known as **base width modulation** effect or **Early effect**.

If the B – E voltage becomes too large, low injection is no longer possible, which leads to high-level injection. In this case, the total hole concentration in the base increases because of the increased excess hole concentration. This means that the base Gummel number will increase. The change in base Gummel indicates from Equation (7), that the electron current density will also change.

Hence, Gummel-Poon model can be used to describe the basic operation of the transistor as well as to describe non-ideal effects.

5. What is known as current amplification factor? Derive the relationship between the amplification factor of CE, CB and CC configuration. (A/M-17)

CURRENT APPLICATION FACTOR (α)

- It is the ratio of output current to input current. In a common base connection, the input current is the emitter Current I_E and output current is the collector current I_c.

  $\alpha = I_C / I_E$ at constant V_{CB}

- The current amplification factor is less than unity. This value can be increased (but not more than unity) by decreasing the base current. This is achieved by making the base this and doping it lightly. Practical values of a range from 0.9 to 0.99.

Base current amplification factor (β)

It is defined as the ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B) is known as base current amplification factor i.e.

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Relationship between α and β

Using $\beta = \frac{I_C}{I_B}$ then $I_B = \frac{I_C}{\beta}$

$$I_B = \frac{I_C}{\beta} \qquad \text{then } I_E = \frac{I_C}{\alpha}$$

Substituting I_B and I_E into $I_E = I_B + I_C$ we get

$$\frac{I_C}{\alpha} = \frac{I_C}{\beta} + I_C$$

Dividing on both sides by I_C we get

$$\frac{1}{\alpha}=\frac{1}{\beta}+1$$

$$\beta=\alpha\beta+\alpha=(\beta+1)\alpha$$

$$\therefore\alpha=\frac{\beta}{\beta+1}$$

and $\beta=\frac{\alpha}{1-\alpha}$ $\quad[\because \beta-\alpha\beta=\alpha]$

Current amplification factor (γ)

It is defined as the ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B) is known as current amplification factor in common collector (CC) arrangement. i.e.

$$\gamma=\frac{\Delta I_E}{\Delta I_B}$$

Relation among α, β and γ

$$\gamma=\frac{\Delta I_E}{\Delta I_B} \qquad \text{.....(i)}$$

$$\alpha=\frac{\Delta I_C}{\Delta I_E} \qquad \text{.....(ii)}$$

Now, $I_E=I_B+I_C$

or $\Delta I_E=\Delta I_B+\Delta I_C$

or $\Delta I_B=\Delta I_E-\Delta I_C$

Substituting the value of ΔI_B in exp (i), we get,

$$\gamma=\frac{\Delta I_E}{\Delta I_E-\Delta I_c}$$

Dividing the numerator and denominator on R.H.S by ΔI_E we get,

$$\gamma=\frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E}-\frac{\Delta I_C}{\Delta I_E}}=\frac{1}{1-\alpha}$$

$$\therefore\gamma=\frac{1}{1-\alpha}=(\beta+1)$$

6. The reverse leakage current of the transistor when connected in CB configuration is 0.2mA and it is 18μA when same transistor is connected in CE configuration. Calculate α_{dc} & β_{dc} of the transistor. (Assume I_B = 30mA) (A/M-16)

Solution :

The leakage current, $I_{CBO} = 0.2\mu A$

$I_{CEO} = 18\mu A$

We know that, $I_{CEO} = \frac{I_{CBO}}{1-\alpha} = (1+\beta) I_{CBO}$

$$\beta = \frac{I_{CEO}}{I_{CBO}} - 1 = \frac{18}{0.2} - 1$$

$$\therefore \boxed{\beta = 89}$$

We know that, $I_{CEO} = \frac{I_{CBO}}{1-\alpha}$

$$\alpha = 1 - \frac{I_{CBO}}{I_{CEO}} = 1 - \frac{0.2\times10^{-6}}{18\times10^{-6}}$$

$$\therefore \boxed{\alpha = 0.988}$$

7. A transistor with I_B = 100μA and I_C = 2mA find (i)β of the transistor (ii)α of the transistor (iii)Emitter current (I_E) (iv)If I_B changes by 25μA and I_C changes by 0.6mA Find the new value of β (A/M-17)

Given :

$I_B = 100\mu A$

$I_C = 2mA$

Solution :

(i) $\beta = \frac{I_C}{I_B}$

$= \frac{2\times10^{-3}}{100\times10^{-6}}$

$\beta = 20$

(ii) $\alpha = \frac{I_C}{I_E}$

$I_E = I_B + I_C$

$= (100 \times 10^{-6}) + (2 \times 10^{-3})$

$= 2.1 \times 10^{-3} = 2.1 mA$

$\alpha = \frac{2 \times 10^{-3}}{2.1 \times 10^{-3}}$

$\alpha = 0.952$

(iv) If $I_B = 25 \mu A$

$I_C = 0.6 mA$

$\beta = \frac{I_C}{I_B}$

$= \frac{0.6 \times 10^{-3}}{25 \times 10^{-6}}$

$\beta = 24$

8. Describe the working of PNP junctions. (A/M-15)

BIPOLAR JUNCTION TRANSISTOR (BJT)

- A Bipolar Junction Transistor (BJT) is a three terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and hence the name Bipolar.
- The BJT is analogous to a vacuum triode and is comparatively smaller in size. It is used in amplifier and oscillator circuits, and as a switch in digital circuits.
- It has wide applications in computers, satellites and other modern communication systems.

TRANSISTOR CONSTRUCTION

- The BJT consists of a silicon (or germanium) crystal in which a thin layer of N-type Silicon is sandwiched between two layers of P-type silicon. This transistor is referred to as PNP. Alternatively, in a NPN transistor, a layer of P-type material is sandwiched between two layers of N-type material. The two types of the BJT are represented in Fig.
- There are two types of transistors:

- NPN transistor
- PNP transistor

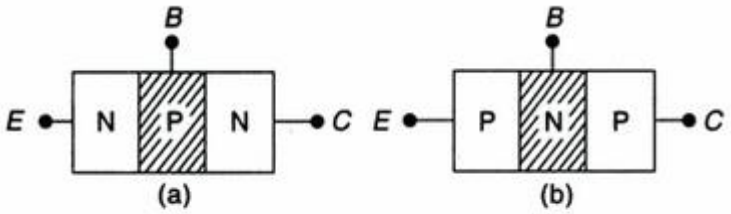


Fig. 6.1 Transistor (a) NPN and (b) PNP

- The symbolic representation of the two types of the BJT is shown in Fig. The arrow on the emitter specifies the direction of current flow when the EB junction is forward biased.

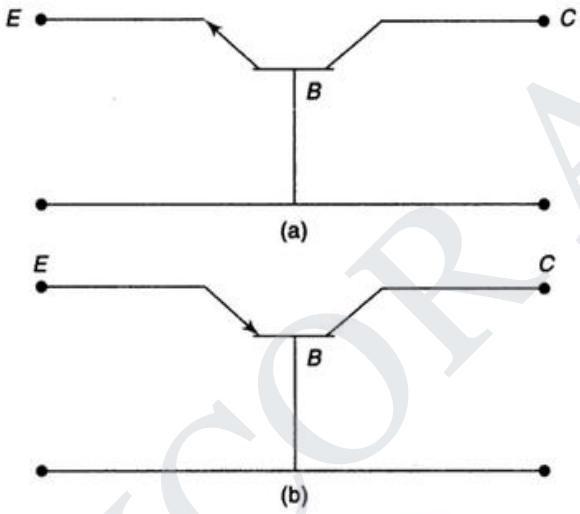


Fig. 6.2 Circuit symbol. (a) NPN transistor and (b) PNP transistor

- A bipolar transistor has three regions known as emitter, base and collector. They are labeled as E, B and C respectively.
- **Emitter:** The main function of the emitter is to supply charge carriers. It is always forward biased with respect to the base. The emitter is heavily doped region.
- **Base:** It is the middle region that forms two PN junctions in the transistor. The base of the transistor is very lightly doped and it may pass most of the injected charge carriers to the collector.
- **Collector:** The main function of the collector is to collect the charge carriers. It is always reverse biased. The doping level is intermediate between heavy doping and light doping.

TRANSISTOR BIASING

As shown in Fig. usually the emitter-base junction is forward biased and collector-base junction is reverse biased. Due to the forward bias on the emitter-base

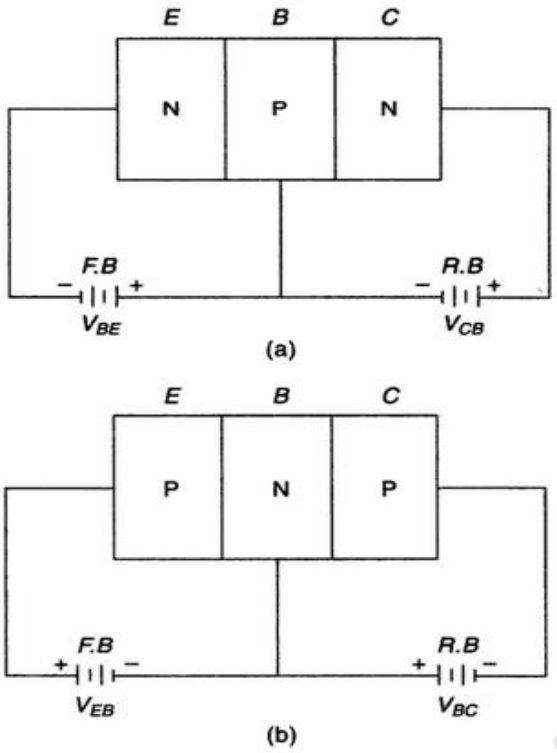


Fig. 6.3 Transistor biasing (a) NPN transistor and (b) PNP transistor

TRANSISTOR OPERATION

- The emitter base junction of a transistor is forward biased where as collector base junction is reverse biased. The emitter current almost entirely flows in the collector circuit. So the collector current depends upon the emitter current.

WORKING OF NPN TRANSISTOR:

- In this, emitter-base junction is forward biased and collector-base junction is reverse biased. The forward bias causes the electrons in the N-type emitter flow through the P-type base, they tend to combine with holes.

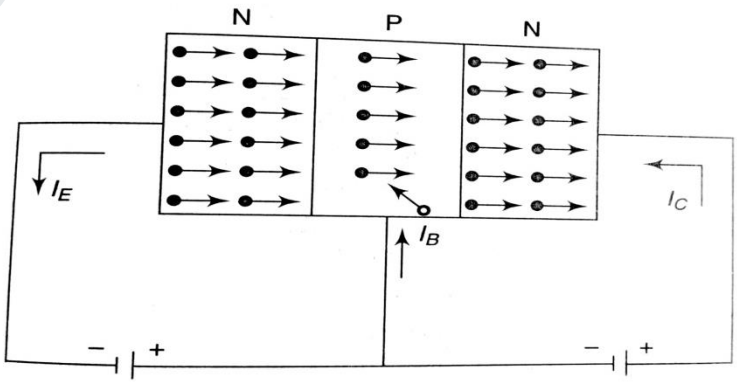


Fig. 6.4 Current in NPN transistor

- As the base is lightly doped, only a few electrons combine with holes to constitute base current I_B.
- The remaining electrons cross over into the collector region to constitute collector current I_C. In this way, almost the entire current flows in the collector circuit. So emitter current is sum of collector current and base current.
- $\mathbf{I_E = I_B + I_C}$

WORKING OF PNP TRANSISTOR:

- The operation of PNP transistor is similar to that of NPN transistor. The current within a PNP transistor is due to the movement of holes.
- In this, emitter-base junction is forward biased and collector-base junction is reverse biased. The forward bias causes the holes in the P-type emitter to flow towards the base. This constitutes the emitter current I_E.

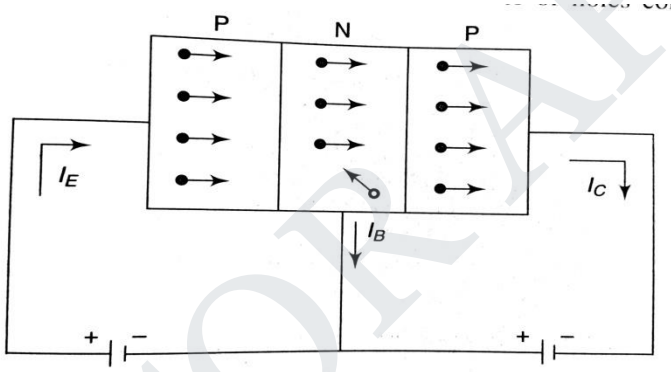


Fig. 6.5 Current in PNP transistor

- As these holes flow through the N-type base, they tend to combine with electrons. As the base is lightly doped, only a few holes combine with electrons to constitute base current I_B.
- Most of the holes do not combine with the electrons in the base region. It is due to the fact that base width is made extremely small and holes do not get sufficient electrons for recombination. Thus most of the holes diffuse to the collector region.
- The remaining holes cross over into the collector region to constitute collector current I_C. In this way, almost the entire current flows in the collector circuit.
- The collector current is called injected current because this current is produced due to the holes injected from the emitter region.
- There is another small component of collector current due to thermally generated carriers. This current component is called reverse saturation current and is quite small.

9. Justify transistor as an amplifier. (A/M-17)

6.7 TRANSISTOR AS AN AMPLIFIER

A load resistor R_L is connected in series with the collector supply voltage V_{CC} of CB transistor configuration as shown in Fig. 6.16

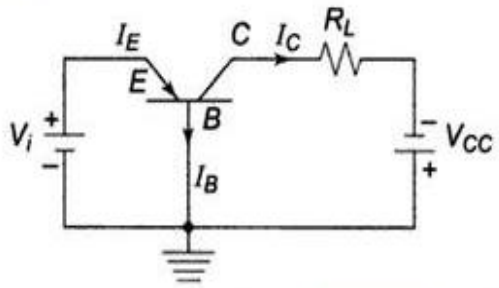


Fig. 6.16 Common base transistor configuration

A small change in the input voltage between emitter and base, say ΔV_i, causes a relatively larger change in emitter current, say ΔI_E. A fraction of this change in current is collected and passed through R_L and is denoted by symbol α'. Therefore the corresponding change in voltage across the load resistor R_L due to this current is $\Delta V_0 = \alpha' R_L \Delta I_E$.

Here, the voltage amplification $A_v = \dfrac{\Delta V_0}{\Delta V_i}$ is greater than unity and thus the transistor acts as an amplifier.

EC8252- ELECTRONIC DEVICES

I YEAR / II SEMESTER B.E. (ME)

UNIT – III

FIELD EFFECT TRANSISTORS

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UNIT – III

FIELD EFFECT TRANSISTORS

- **JFETs – Drain and Transfer characteristics**
- Current equations-Pinch off voltage and its significance
- **MOSFET- Characteristics**
- **Threshold voltage -Channel length modulation**
- **D-MOSFET, E-MOSFET- Characteristics**
- Comparison of MOSFET with JFET.

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LIST OF IMPORTANT QUESTIONS

UNIT III – FIELD EFFECT TRANSISTORS

PART – A

1. What is channel length modulation? (A/M-15) (N/D-19)
2. Compare MOSFET and JFET/ Differentiate MOSFET and JFET. (M/J-16) (N/D-19)
3. Calculate the internal pinch off voltage of JFET with a= 0.75μm, $N_d = 10^6/cm^3$ $€_r$=11.6 and $€_0 = 8.854 \times 10^{-12}$ F/m
4. Evaluate the body effect coefficient (y) in a MOSFET with Na= 3×10^{16} $/cm^3$, $€_r$=11.6 and $€_0 = 8.854 \times 10^{-12}$ F/m and $C_{ox} = 1.726 \times 10^{-7}$ F / cm^2 (A/M-2019)
5. Define pinch off voltage (N/D-14) (A/M-2018)
6. . Differentiate between JFET and BJT/Compare FET and BJT. (M/J-14)(N/D-17)(M/J-17) (A/M-18)
7. Assume that the PN junction of a uniformly doped silicon n channel JFET at T=300K has doping concentration of $N_a=10^{18}cm^{-3}$ and $N_d=10^{16}$ cm^{-3}. Assume that the channel thickness a is 0.7μm. Calculate the pinch off voltage. (A/M-15) (N/D-15) (N/D-17)
8. Give the current voltage relationship of the D-MOSFET and E-MOSFET(M/J-17)
9. What is JFET? And give its different modes of operation. (N/D-16)
10. Give some applications of JFET. (M/J-16)

PART – B

1. The reverse gate voltage of JFET, when changes from 4.4V to 4.2V, the drain current changes from 2.2 mA to 2.6 mA. The device parameters of JFET are Maximum current I_{DSS} = 10 mA, Pinch off voltage, Vp = -47V. Find out the value of transconductance of the transistor and drain current for VGS = -4V. (N/D-19)

2. Explain the four distinct regions of the output characteristics of the JFET? Also Briefly describe some application of JFET. (OR) Draw a circuit diagram for obtaining the drain and transfer characteristics for an N channel JFET. (OR) Discuss the drain and transfer characteristics of JFET. (OR) With neat diagram explain the construction working principle and V-I characteristics of P channel JFET. (OR) Explain the construction and operations of N channel JFET with neat diagram. (OR) Field effect transistor is a Voltage controlled device justify the statement and mention various parameters such as pinch off voltage, source drain voltage and gate source voltage. (M/J-14) (N/D-14) (A/M-15) (N/D-15) (N/D-16) (A/M-17) (N/D-17) (A/M-2018) (A/M-2019) (N/D-19)

3. With the help of suitable diagrams explain the working of different types of MOSFET? (OR) Draw a circuit diagram of the cross section of a Enhancement MOSFET. Also discuss the drain and transfer characteristics for EMOSFET. (OR) Discuss the characteristics of MOFET. (OR) With neat diagram explain the operation of Depletion mode MOSFET and sketch the characteristics. (OR) Explain the construction and principle of operation of Depletion mode MOSFET. (OR) With relevant sketches explain the working mechanisms of Enhancement and Depletion mode MOSFET. (M/J-14) (N/D-14) (A/M-15) (N/D-15) (A/M-16) (N/D-16) (A/M-17) (N/D-17) (A/M-2018) (A/M-2019) (N/D-19)

4. Discuss the effect of channel length modulation. (A/M-17)

5. Derive an expression for drain current of FET in Pinch off region with necessary diagram. (A/M-16)

PART – A

1. What is channel length modulation? (A/M-15) (N/D-19)

- When the MOSFET is biased in the saturation region, the depletion region at the drain terminal extends laterally into the channel, reducing the effect of channel length. i.e for saturation region (V_{DS} V_{DS}(sat)). This phenomenon is called channel length modulation.
- Since the depletion region width is bias dependent, the effective channel length is also bias dependent and is modulated by the drain to source voltage.

2. Compare MOSFET and JFET/ Differentiate MOSFET and JFET. (M/J-16) (N/D-19)

JFET	MOSFET
JFET's can only be operated in depletion mode.	MOSFET's can be operated in depletion mode or in enhancement mode.
Input resistance is high (> 10 MΩ).	Input resistance is very high (> 10^{15} Ω).
Gate is not insulated from channel.	Gate is insulated from channel by a larger of SiO_2.
Channel exists permanently.	Channel exists permanently in depletion type MOSFET but not in enhancement type MOSFET.
It is not easy to fabricate.	It is easy to fabricate.
Due to manufacture problems they are less widely used in IC's.	They are most widely used in IC's.

3. Calculate the internal pinch off voltage of JFET with a= 0.75μm, $N_d = 10^6/cm^3$ $€_r$=11.6 and $€_0 = 8.854 \times 10^{-12}$ F/m

Given:

a= 0.75μm

$N_d = 10^6/cm^3$

$€_r$=11.6

$€_0 = 8.854 \times 10^{-12}$ F/m

Solution:

$$V_P = \frac{qN_d a^2}{2\varepsilon}$$

The internal pinch off voltage

4. Evaluate the body effect coefficient (y) in a MOSFET with Na= 3 x 10^{16} /cm^3, €$_r$=11.6 and €$_0$ = 8.854 x 10^{-12} F/m and C_{ox} = 1.726 x 10^{-7} F / cm^2 (A/M-2019)

Given:

Na= 3 x 10^{16} /cm^3

N_d = 10^6/cm^3

€$_r$=11.6

€$_0$ = 8.854 x 10^{-12} F/m

C_{ox} = 1.726 x 10^{-7} F / cm^2

Solution

5. Define pinch off voltage (N/D-14) (A/M-2018)

- At some value of drain to source voltage V_{DS} , drain current I_D can be increased further, due to reduction in channel width. Any further increase in V_{DS} does not increase the drain current I_D.
- Drain current I_D approaches the constant saturation value. The voltage V_{DS} at which the current I_D reaches to its constant saturation level is called pinch off voltage (V_P)

$$V_P = \frac{qN_d a^2}{2\varepsilon}$$

q = charge in coulombs
N_d = electron concentration in electrons per cubic meter
ϵ_s = permittivity of the material in farads per meter
$\epsilon_s = \epsilon_r \epsilon_o$, ϵ_r is the relative dielectric constant
$\epsilon_o = 8.854 \times 10^{-12}$ F/m is the permittivity of free space

6. Differentiate between JFET and BJT/Compare FET and BJT. (M/J-14)(N/D-17)(M/J-17) (A/M-18)

S.NO	BJT	FET
1	In BJT both holes and electrons conduction that is depends on both majority and minority carriers.	In FET only one charge carrier are responsible for conduction. It depends only on majority carriers.
2	It is current controlled device	It is voltage controlled device
3	It has thermal breakdown	No thermal breakdown
4	Configurations are CE,CB,CC	Configurations are CS,CG,CD
5	Higher sensitivity to changes in the applied signals	Less sensitivity to changes in the applied voltage.
6	Fabrication is difficult	Easy to fabricate and occupies less space
7	Due to junctions the speed is limited	It has higher switching speeds
8	Lower voltage gain	Higher voltage gain
9	Large gain band with product	Low gain band with product.
10	Thermal stability is less	Thermal stability is more

7. Assume that the PN junction of a uniformly doped silicon n channel JFET at T=300K has doping concentration of $N_a=10^{18}cm^{-3}$ and $N_d=10^{16}\ cm^{-3}$. Assume that the channel thickness a is 0.7μm. Calculate the pinch off voltage. (A/M-15) (N/D-15) (N/D-17)

The internal pinchoff voltage is given by:

$$V_{PO} = \frac{e a^2 N_d}{2\varepsilon_s}$$

$$= \frac{(1.6 \times 10^{-19})\,(0.75 \times 10^{-4})^2\,(10^{16})}{2(11.7)\,(8.85 \times 10^{-14})}$$

Therefore, $\boxed{V_{PO} = 4.35\ V.}$

The built-in potential barrier is given by:

$$V_{bi} = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right)$$

where $V_T = \frac{KT}{q\ (\text{or})\ e} = \frac{(1.38 \times 10^{-23})\,(300)}{1.6 \times 10^{-19}} = 0.0259\ V$.

Hence, $V_{bi} = (0.0259) \ln\left[\frac{(10)^{18}(10)^{16}}{(1.5 \times 10^{10})^2}\right] = 9.814\ V$.

The pinchofff voltage, V_p is given by:

$$V_p = V_{bi} - V_{PO}$$

$$= 0.814 - 4.35$$

Therefore, $V_p = -3.54\ V.$

8. Give the current voltage relationship of the D-MOSFET and E-MOSFET(M/J-17)

The relationship between drain current and V_{GS} is given by,

$$I_D = K\,(V_{GS} - V_T)^2$$

I_D = drain current

V_{GS} = Gate source voltage

V_T = Threshold voltage, K = Conduction parameter

9. What is JFET? And give its different modes of operation. (N/D-16)

- The field effect transistor is a three terminal device used for a variety of applications that match, to a large extent, those of the, BJT transistor.
- The FET is a unipolar device depending on either electron (n channel) or hole (p-channel) conduction. The important characteristic of the FET is its high input impedance. There are 4 modes of operation.
    - Cut-off region
    - Saturation region
    - Ohmic region
    - Breakdown region

10. Give some applications of JFET. (M/J-16)

- FET is used as buffer in measuring instruments, receivers since it has high input impedance and low output impedance.
- FETs are used in RF amplifiers in FM tuners and communication equipment for low noise level.
- The device is voltage controlled it is used as a voltage variable resistor in operational amplifiers and tone controls
- It is used in digital circuits in computers and memory circuits because of its small size.
- FETs are used in mixer circuits in FM and TV receivers and communication equipment because distortion is low.

11. What are the features of FET?

- It is a unipolar device because current is carried by only one type of charge particles, either electrons or holes.
- It is less noisy than a bipolar transistor.
- It does not have thermal runaway.
- It is relatively immune to radiation.
- It has high input impedance.
- It has thermal stability.

12. Give the drain current equation of JFET.

$$I_D = I_{Dss}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

where I_{Dss} = Drain current when gate is shorted to source

V_{GS} = Gate the source voltage

V_p = Pinch off voltage

13. List the JFET parameters.

- DC drain resistance (R_{DS})
- AC drain resistance (r_d)
- Amplification factor (μ)
- Input resistance (R_i)
- Transconductance (g_m)

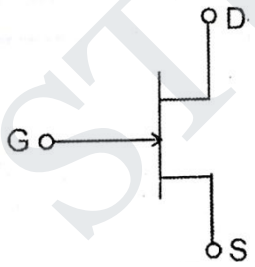
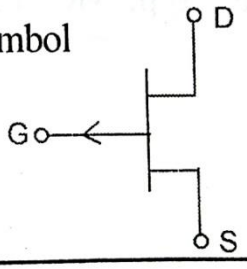
14. Define Amplification Factor In JFET

- The amplification factor is ratio of a small change in the drain voltage to the corresponding small change in the gate voltage, at a constant drain current.
- It is denoted by μ and it is given by,

$$\text{Amplification factor, } \mu = -(\Delta V_{DS}/\Delta V_{GS}) \text{ at } I_D \text{ constant}$$

- Here the negative sign shows that when V_{GS} is increased, V_{DS} must be decreased for I_D to remain constant

15. Compare N-FET and P-FET

n-Channel JFET	*p*-Channel JFET
Current carriers are electrons.	Current carriers are holes.
Less input noise.	More input noise.
Mobility of electrons is large.	Mobility of holes is poor.
Large transconductance.	Less transconductance.
Symbol 	Symbol 

16. Depletion MOSFET is commonly known as "Normally - ON - MOSFET". Why?

The depletion MOSFET can conduct even if the gate to source voltage (V) is Zero, because of this reason depletion MOSFET is commonly known as "Normally - ON - MOSFET.

17. Why the input impedance of FET is more than that of a BJT?

The input impedance of FET is more than that of a BJT because the input junction of FET is reverse biased whereas the input junction of BJT is forward biased.

18. Give an important reason for which N-channel FET's are preferred over P-channel FET's.

- In N-channel FET's the charge carriers are the electrons which have a mobility of about 1300 cm^2/ vs whereas in P-channel FET's the charge carrires are the holes which have a mobility of about 500cm^2/vs.
- The current in a semiconductor is directly proportional to mobility, therfore the current in N.-channel FET is more than that of P-channel FET.

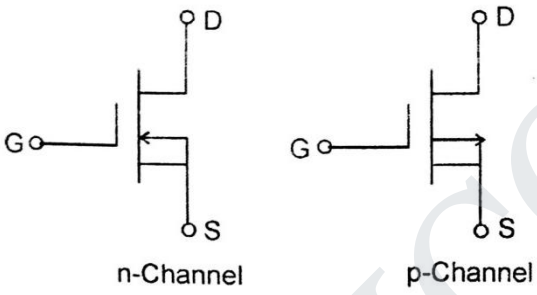
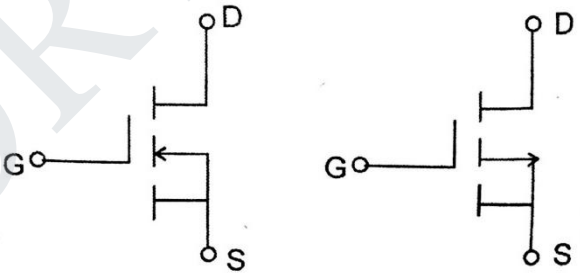
19. What are the applications of MOSFET?

- It can be used as input amplifiers in oscilloscope, electronic voltmeters.
- It is used in computer memories.
- It is used in logic circuits.
- It is used in phase shift oscillators
- It is used in FM and TV receivers (for mixer operation).

20. Why E-MOSFET is normally, called as OFF - MOSFET?

- When V_{GS} = 0, the biasing supply V_{DD} this to force the free electron to move from source to drain. But the 'P' substitute has only few generated conduction band electrons.
- Aside from these minority carriers and some surface leakage, the current between source and drain is zero hence E-MOSFET is called as OFF MOSFET.

21. Compare D-MOSFET and E-MOSFET

D-MOSFET	E-MOSFET
Channel is present permanently.	Channel is absent initially. It is induced after application of positive gate voltage above the threshold value for *n*-channel enhancement type MOSFET and negative gate voltage above threshold value for *p*-channel enhancement type MOSFET.
Drain current flows on application of drain to source voltage at $V_{GS} = 0$ V.	No current flows on application of drain-to-source at $V_{GS} = 0$ V. Current flows only when V_{GS} is above threshold level.
Can be operated in depletion mode as well as enhancement mode.	Can be operated only in enhancement mode.
Symbols  n-Channel p-Channel	Symbols 

PART – B

1. The reverse gate voltage of JFET, when changes from 4.4V to 4.2V, the drain current changes from 2.2 mA to 2.6 mA. The device parameters of JFET are Maximum current I_{DSS} = 10 mA, Pinch off voltage, Vp = -47V. Find out the value of transconductance of the transistor and drain current for VGS = -4V. (N/D-19)

2. Explain the four distinct regions of the output characteristics of the JFET? Also Briefly describe some application of JFET. (OR) Draw a circuit diagram for obtaining the drain and transfer characteristics for an N channel JFET. (OR) Discuss the drain and transfer characteristics of JFET. (OR) With neat diagram explain the construction working principle and V-I characteristics of P channel JFET. (OR) Explain the construction and operation of N channels JFET with neat diagram. (OR) Field effect transistor is a Voltage controlled device justify the statement and mention various parameters such as pinch off voltage, source drain voltage and gate source voltage. (M/J-14) (N/D-14) (A/M-15) (N/D-15) (N/D-16) (A/M-17) (N/D-17) (A/M-2018) (A/M-2019) (N/D-19)

FIELD EFFECT TRANSISTOR (FET):

- The field effect transistor is a three terminal device used for a variety of applications that match, to a large extent, those of the, BJT transistor.
- The primary difference between the two types of transistor is the fact that the BJT is a current-controlled device, while the JFET transistor is a voltage-controlled device. i e the output current is controlled by the electric field created by the applied potential to the control terminal. Hence the name "Field Effect Transistor."
- The FET is a unipolar device depending on either electron (n channel) or hole (p-channel) conduction. The important characteristic of the FET is its high input impedance.

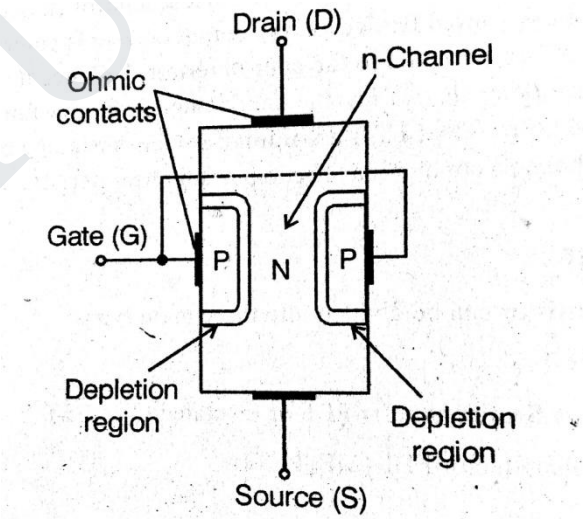
TYPES OF FET

Field effect transistor can be divided into three main types.

- Junction FET (JFET)
  - N – Channel JFET
  - P - Channel JFET
- Metal – oxide semiconductor FET (MOSFET)
- Metal – semiconductor FET (MESFET)

N – CHANNEL FET

- A FET consists of a P-type or N-type semiconductor bar with two PN junctions at the opposite sides of its middle part. The space between the junction is called a channel. If the bar is of N-type, it is called N-Channel FET and if the bar is of P-type, it is called P-channel FET.

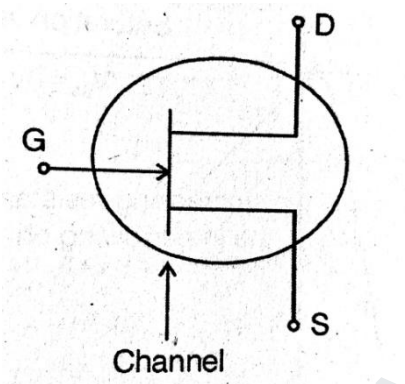


Structure of n-channel & p-channel JFET

- The regions forming diodes are connected internally and a single wire is taken out in the form of a terminal called the gate (G). The electrical connections are made to both ends of

the semiconductor bar and are taken out in the form of two terminals called drain(D) and Source(S).

- **Source:** The source S is the terminal through which the majority carriers enter the bar. Conventional current entering the bar at S is designated by I_S.
- **Drain:** The drain D is the terminal through which the majority carriers enter the bar. Conventional current entering the bar at D is designated by $I_{D,}$



Symbol for n-channel JFET.

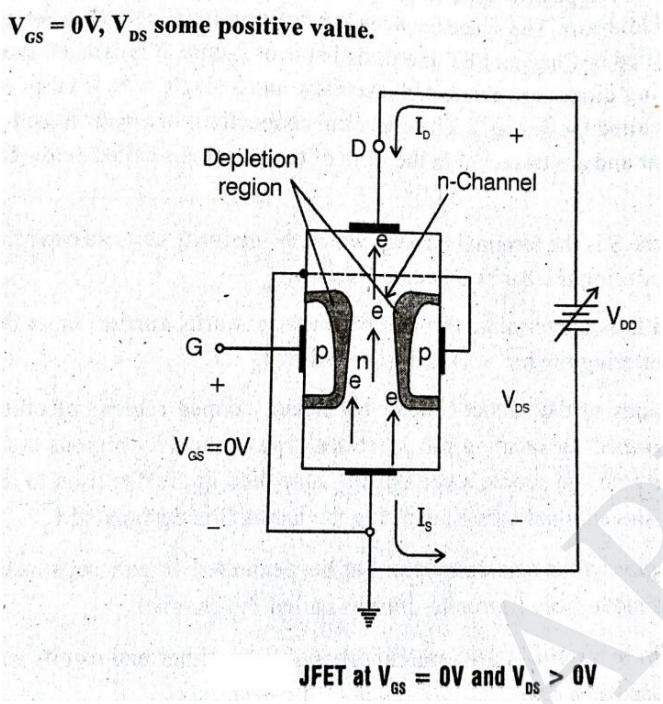
- **Gate:** On both sides of the semiconductor bar heavily doped regions of other type impurities have been formed for creating P-N junctions. These impurity regions are called the gate G. Between the gate and source a voltage V_{GS} is applied in the direction to reverse-bias the p-n junction. Conventional current entering the bar at G is designated I_G
- **Channel:** The region in the semiconductor bar between the two gate regions through which majority carriers move from source to drain is called the channel.
- The source and drain terminals are interchangeable (i.e.) either end can be used as a source with other end used as a drain. In an N- channel JFET, the arrow points towards the vertical line. The vertical line represents the N channel.

OPERATION OF JFET

(i) V_{GS} = 0V, V_{DS} some positive value

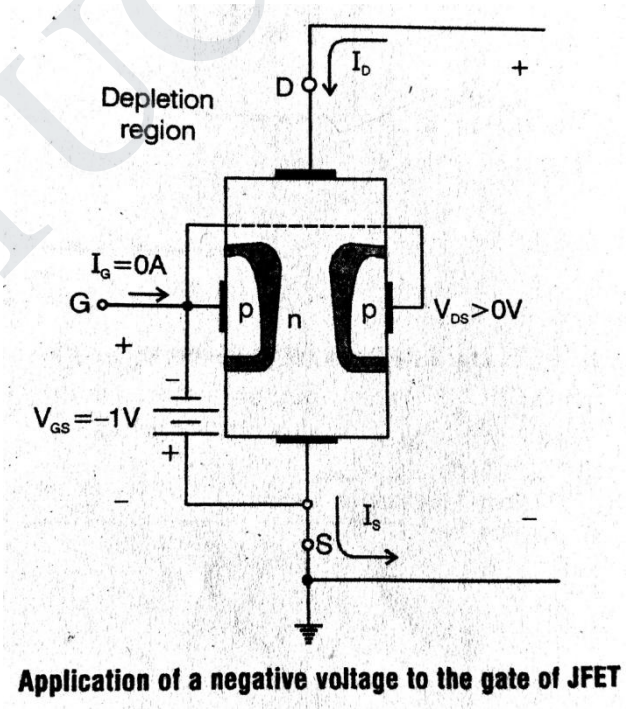
- If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" (the depletion regions cannot actually meet), a condition referred to as pinch-off will result. The level of V_{DS} that establishes this condition is referred to as **pinch-off voltage** and is denoted by V_P.
- Hence, the current saturates i.e. for further increase in drain-to-source voltage, the drain current remains constant. This region is called "**pinch-off region**". As V_{DS} is increased

beyond V_P, the region between the two depletion regions will increase in length along the channel, but the level of I_D remains the same.



(ii)) V_{GS} < 0V

- The voltage from gate to source, denoted by V_{GS} is the controlling voltage of the JFET. For the n-channel device the controlling voltage V_{GS} is made more and more negative from its V_{GS}=0V level.



- In the figure, A positive voltage V_{DS} has been applied across the channel and the gate has been connected directly to the source to establish the condition V_{GS}=0V. The instant the voltage V_{DD} (=V_{DS}) is applied, the electrons will be drawn to the drain terminal. The path of charge flow reveals that the drain and source currents are equivalent ($I_D = I_S$).
- As the voltage V_{DS} is increased from 0 to a few volts, the current will increase. As V_{DS} increases and approaches a level referred to as V_P, the depletion regions will widen, causing reduction in the channel width.
- As V_{GS} increases ($V_{GS} < 0$) by increasing reverse bias voltage, the depletion region widens than for V_{GS}=0V and pinch-off occurs at a lower value of V_{DS}. When $V_{GS} = -V_P$ will be sufficiently negative to establish a saturation level that is 0mA, and the device will be "turned off."
- If V_{DS} is increased sufficiently large value, avalanche breakdown occurs in the pinch-off region and drain current increases rapidly.
- The region to the left of the pinch-off occurs is referred to as the ohmic or voltage-controlled resistance region. In this region the JFET acts as a variable resistor whose resistance is controlled by the applied gate-to-source voltage.
- As V_{GS} becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding with an increasing resistance level.

JFET CHARACTERISTICS:

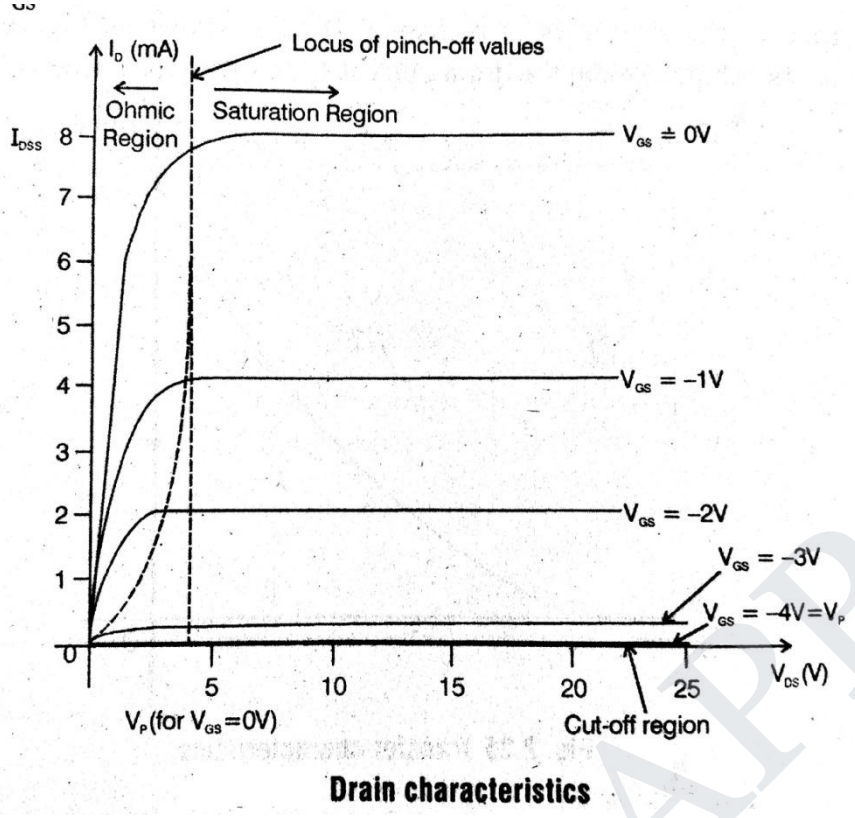
- The V - I characteristics of a JFET is useful to understand the behavior of the device. These characteristics are plotted graphically with voltage on one axis and current on the other axis. The two important characteristics of a JFET are

  1. Drain characteristics

  2. Transfer characteristics

1. DRAIN CHARACTERISTICS:

- Drain characteristics of a n-channel JFET is shown in Figure. Drain characteristic is a plot of drain current I_D versus drain to source voltage V_{DS} at different values of gate to source voltage V_{GS}.



Drain characteristics

The drain characteristic has various regions as shown. The following points are observed from the output characteristics.

(i) **Cut-off region:** With increase in the negative V_{GS} voltage, the channel width available for conduction decreases. At a certain voltage, the depletion region touch each other to close the channel completely. The cut-off region corresponds to I_D= 0

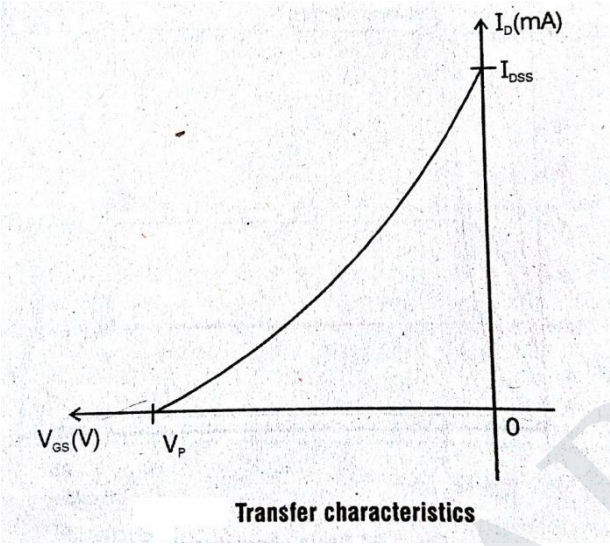
(ii) **Saturation region:** Saturation region is that portion of the characteristics where I_D remains constant and does not change with changes in V_{DS}. To use FET as an amplifier, it is operated in this saturation region.

(iii) **Ohmic region:** In the ohmic region, the drain current I_D varies with variation in the drain to source voltage V_{DS}. The JFET operates as a voltage variable resistance in the ohmic region. The resistance offered by the JFET decreases with decrease in the value of negative gate to source bias voltage

(iv) **Breakdown region:** If the value of V_{DS} increased beyond pinch-off voltage V_P, the drain current I_D remains constant, up to certain value of V_{DS}. If V_{DS} is further increased, the voltage will be reached at which the gate-channel junction breaks down, due to avalanche effect. At this point, the drain current (I_D) increases very rapidly, and the device may be destroyed.

2. TRANSFER CHARACTERISTICS:

The Transfer characteristics of N – channel JFET is shown below. The curve represents relationship between the drain current I_D and gate to source voltage V_{GS}.



Transfer characteristics

The transfer curve is obtained using Shockley's equation :

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The squared term of the equation results in a non-linear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}.

The transfer curve shows the operating limits of a JFET.

When $V_{GS} = 0V$, $I_D = I_{DSS}$

When $V_{GS} - V_P$[i.e. $V_{GS}(off)$, I_D =0mA

APPLICATIONS:

- FET is used as buffer in measuring instruments, receivers since it has high input impedance and low output impedance.
- FETs are used in RF amplifiers in FM tuners and communication equipment for low noise level.
- The device is voltage controlled it is used as a voltage variable resistor in operational amplifiers and tone controls
- It is used in digital circuits in computers and memory circuits because of its small size.
- FETs are used in mixer circuits in FM and TV receivers and communication equipment because distortion is low.

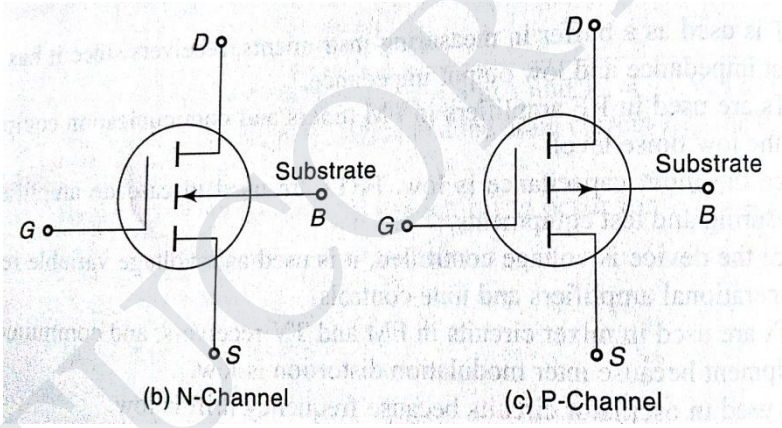
3. With the help of suitable diagrams explain the working of different types of MOSFET? (OR) Draw a circuit diagram of the cross section of a Enhancement MOSFET. Also discuss the drain and transfer characteristics for EMOSFET. (OR) Discuss the characteristics of MOFET. (OR) With neat diagram explain the operation of Depletion mode MOSFET and sketch the characteristics. (OR) Explain the construction and principle of operation of Depletion mode MOSFET. (OR) With relevant sketches explain the working mechanisms of Enhancement and Depletion mode MOSFET. (M/J-14) (N/D-14) (A/M-15) (N/D-15) (A/M-16) (N/D-16) (A/M-17) (N/D-17) (A/M-2018) (A/M-2019) (N/D-19)

METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET):

- MOSFET is the common term for the Insulated Gate Field Effect Transistor (IGFET). There are two basic forms of MOSFET

(i) Enhancement MOSFET

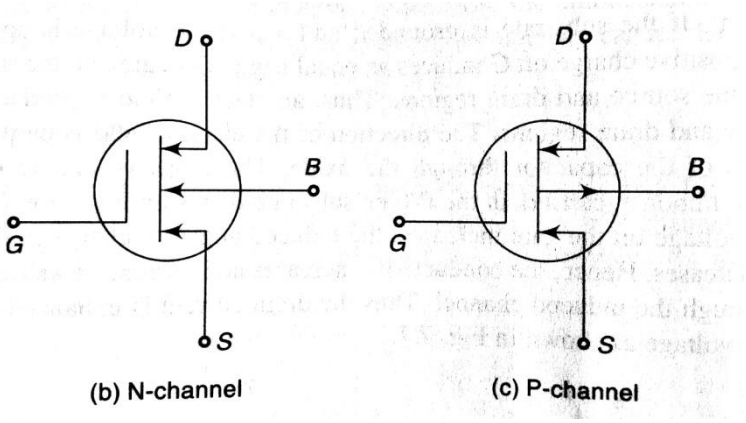
- N – Channel MOSFET (E – MOSFET)
- P - Channel MOSFET (E – MOSFET)



Symbols for Enhancement MOSFET

(ii) Depletion MOSFET.

- N – Channel MOSFET (D – MOSFET)
- P - Channel MOSFET (D – MOSFET)



Symbols for Depletion MOSFET

- The terms depletion and enhancement define their basic mode of operation.

PRINCIPLE:

- By applying a transverse electric field across an insulator, deposited on the semiconductor material, the thickness and hence the resistance of a conducting channel of a semi conducting material can be controlled.
- In depletion MOSFET, the controlling electric field reduces the number of minority carriers available for conduction, where as in the enhancement MOSFET, application electric field causes an increase in the majority carrier density in the conducting regions of the transistor.

N – CHANNEL DEPLETION MOSFET (D – MOSFET)

Depletion type MOSFET operates both in the enhancement and depletion mode. D – MOSFET has physical channel.

CONSTRUCTION:

- A slab of p-type material is formed from a silicon base and is referred to as the **substrate**. The substrate is internally connected to the source terminal. Two highly doped n+ regions are diffused in a lightly doped substrate of p-type silicon substrate. One n+ region is called the **source** S and the other one is called the **drain** D.
- A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into the oxide layer, allowing contact with the source and drain. Then a thin layer of metal aluminium is formed over the layer of SiO_2, This metal layer covers the entire channel region and it forms the **gate** G.
- SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing electric fields within the dielectric when exposed to an externally applied field. In this construction an n-channel is diffused between the source and drain to the basic structure of MOSFET.

- The primary difference between the construction of depletion-type and enhancement-type MOSFET is that there is absence of channel in the enhancement type whereas there is a diffused channel in the depletion type.

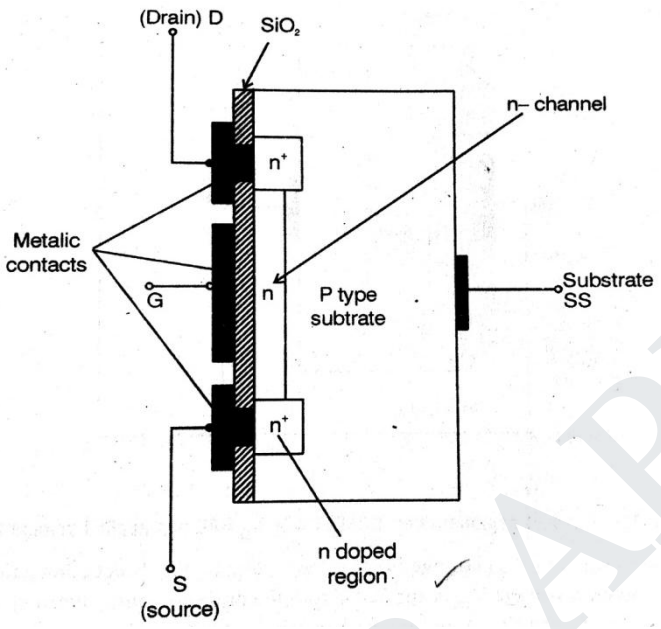


Fig N – channel depletion MOSFET

OPERATION:

- The gate-to-source (V_{GS} = 0) voltage is set to zero volts by the direct connection from one terminal to the other, a voltage V_{DS} is applied across the drain-to-source terminals.
- The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current is established through the channel. The resulting current with V_{GS} = 0V labeled as I_{DSS}.

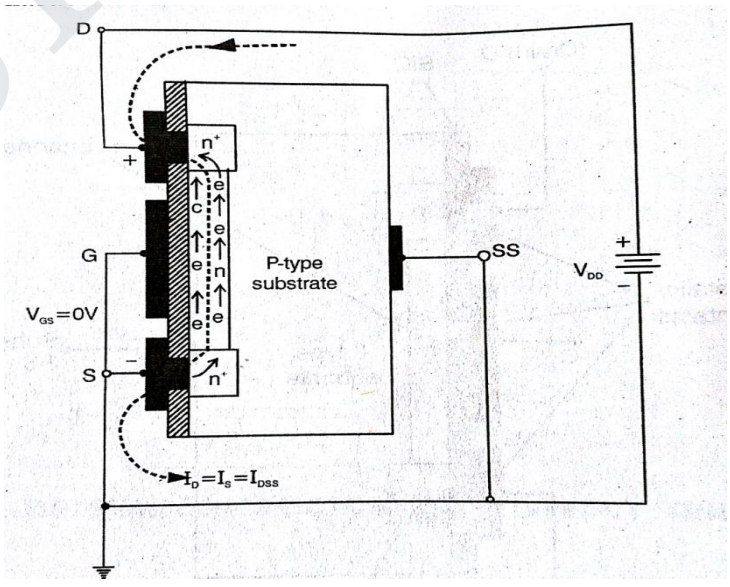


Fig N – channel depletion MOSFET with V_{GS} = 0V

- Now set the V_{GS} at a **negative voltage**. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract).
- Depending on the magnitude of the negative bias established by V_{GS} a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction.
- The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}.
- For **positive values** of V_{GS} the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current. As the V_{GS} continues to increase in the positive direction, the drain current will increase at a rapid rate.
- The application of positive V_{GS} has "enhanced" the level of free carriers in the channel compared to that encountered with. V_{GS} = 0V. For this reason, the region of positive gate voltages on the drain or transfer characteristics is referred to as the enhancement region, with the region between cut-off and the saturation level of I_{DSS} to as depletion region.

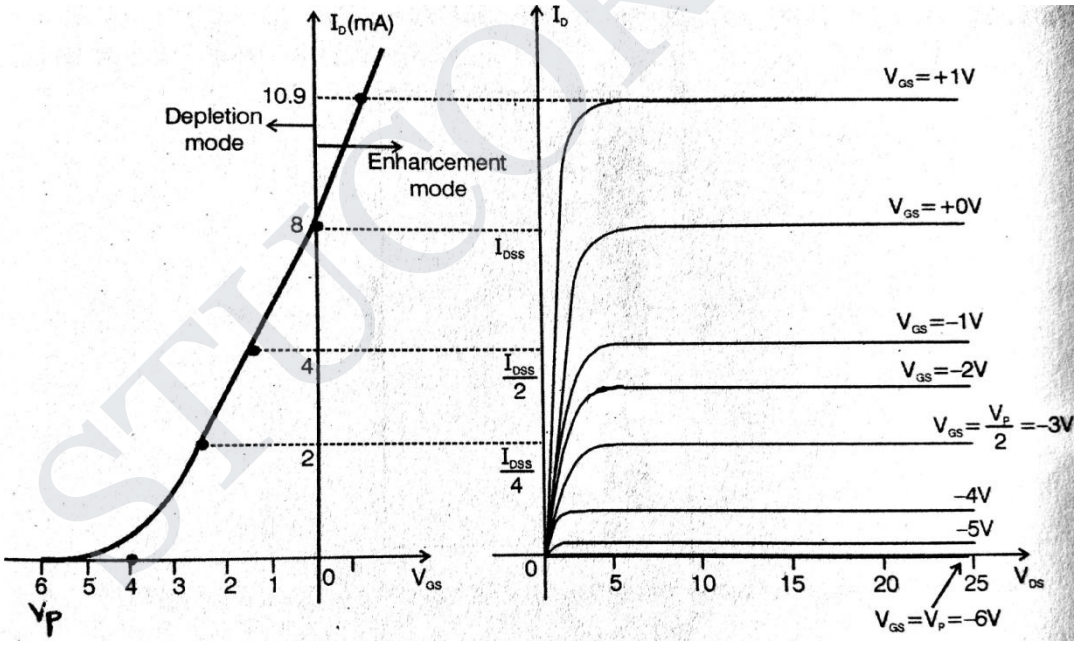


Fig Drain and Transfer characteristics of N – channel depletion MOSFET

P – CHANNEL DEPLETION MOSFET (D – MOSFET)

- The construction of a P – channel depletion type MOSFET is exactly the reverse of N – channel depletion MOSFET. Now there is an N – type substrate and P – type channel as shown.

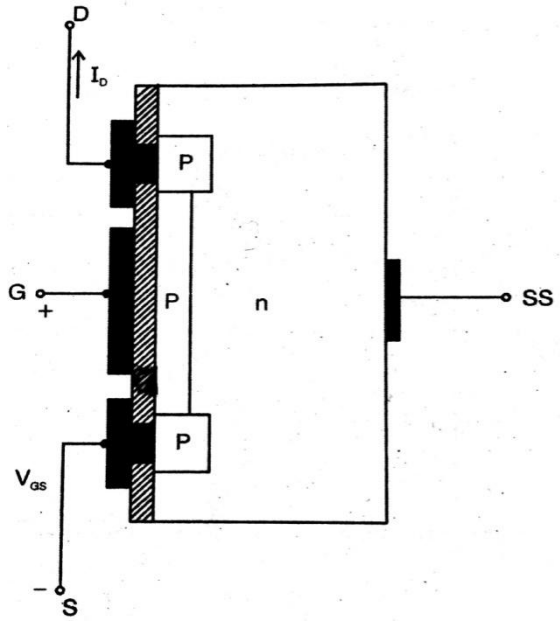


Fig P – channel depletion MOSFET

- In this diagram voltage polarities and current directions are reversed. The drain characteristics would appear exactly as in N – channel depletion MOSFET but with V_{DS} having negative values, I_D having positive values and V_{DS} having opposite polarities.

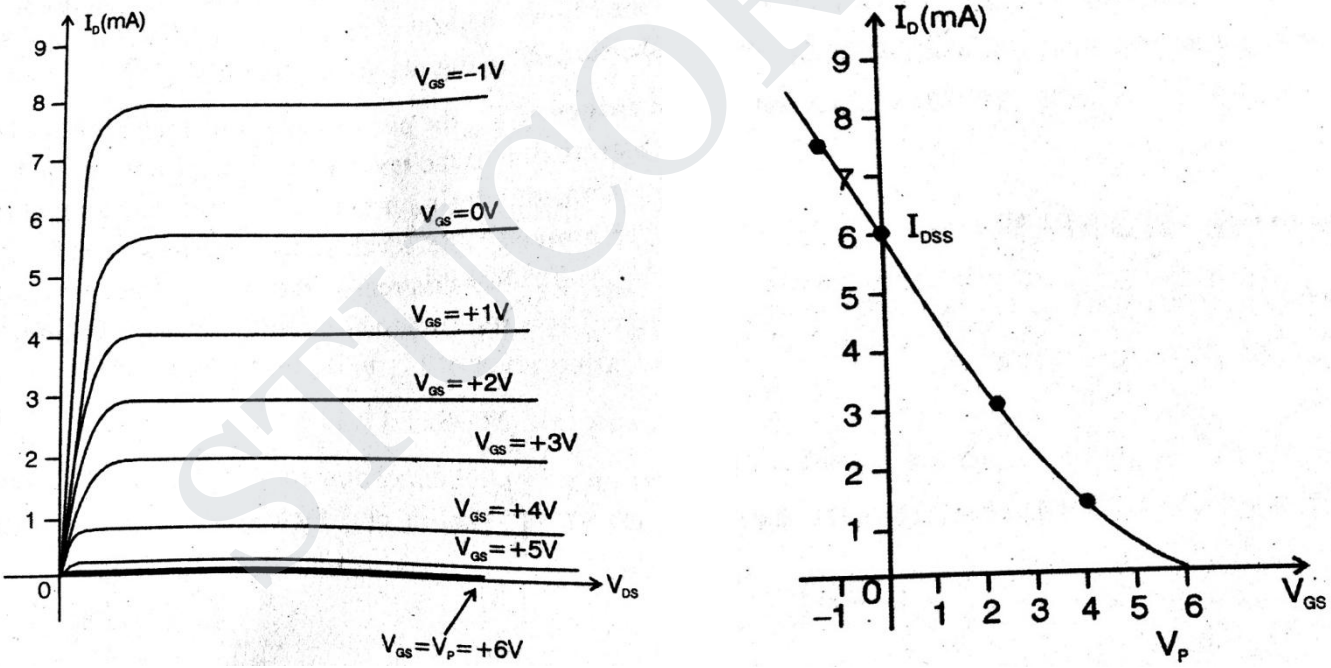


Fig Drain and Transfer characteristics of P – channel depletion MOSFET

- The drain current will increase from cut off at $V_{GS} = V_P$ in the positive V_{GS} region to I_{DSS} and then continue to increase foe negative values of V_{GS}.

N – CHANNEL ENHANCEMENT MOSFET (E – MOSFET)

Enhancement type MOSFET operates only in the enhancement mode and has no depletion mode. E-MOSFET has no physical channel.

CONSTRUCTION

- A slab of p-type material is formed from a silicon base and is referred to as the **substrate**. The substrate is internally connected to the source terminal. Two highly doped n+ regions are diffused in a lightly doped substrate of p-type silicon substrate. One n+ region is called the **source** S and the other one is called the **drain** D.

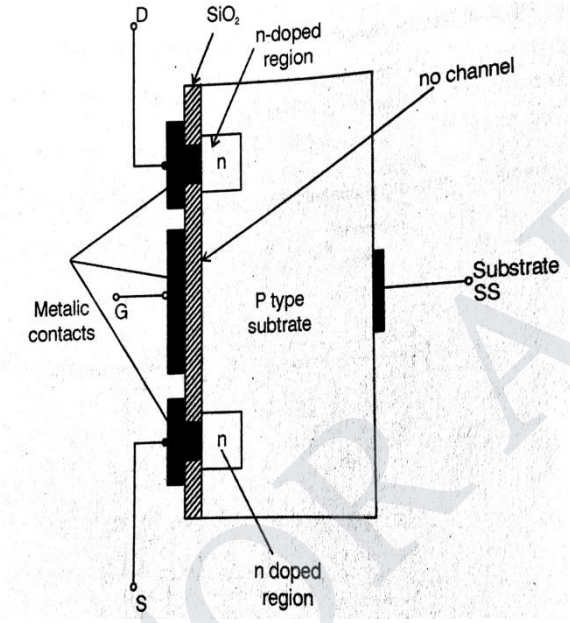


Fig N – channel enhancement MOSFET

- A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into the oxide layer allowing contact with the source and drain. Then a thin layer of metal aluminium is formed over the layer of SiO_2. This metal layer covers the entire channel region and it forms the **gate** G.
- SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing electric fields within the dielectric when exposed to an externally applied field. There is no channel present between the two n-doped regions.
- The metal area of the gate, in conjunction with the insulating oxide layer of SiO_2 and the semiconductor channel forms a parallel plate capacitor. This device is called the insulated gate FET because of the insulating layer of SiO_2. This layer gives extremely high input impedance for the MOSFET.
- As there is no continuous channel in an enhancement MOSFET, this condition is represented by broken line in the symbols.

OPERATION

- If V_{GS} is set at 0V and a voltage applied between the drain and source, the absence of an n-channel will result in a current of effectively zero amperes.
- If both V_{DS} and V_{GS} have been set at some positive voltage greater than 0V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the p - substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p-substrate.

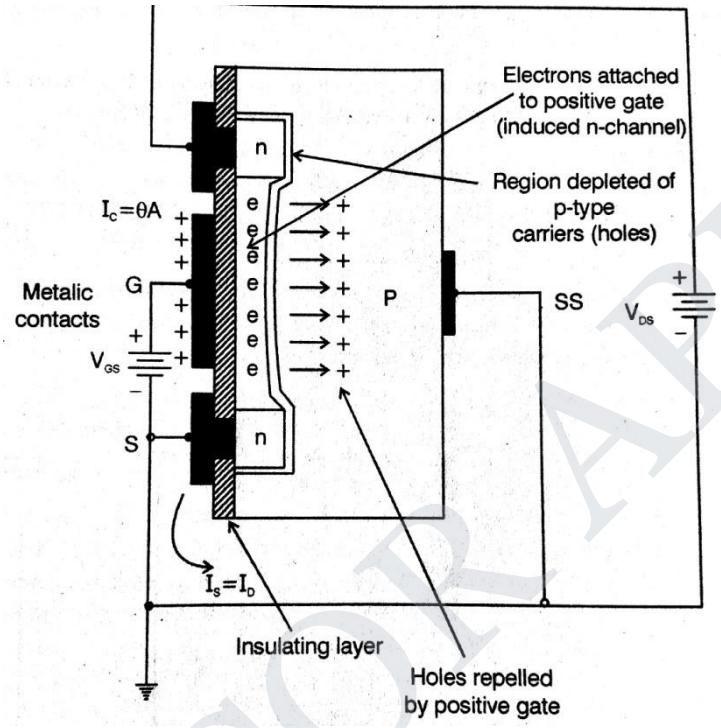
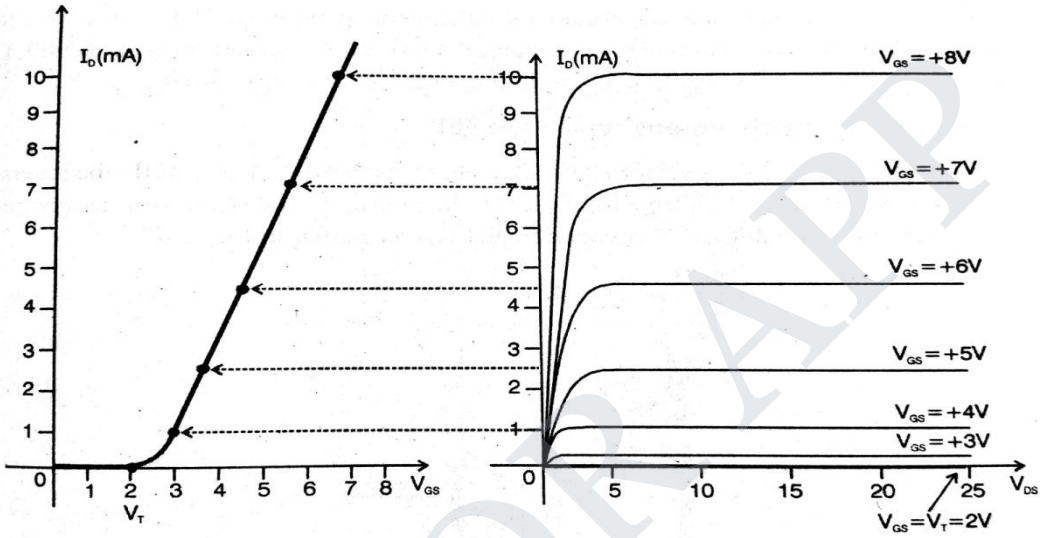


Fig Channel formation in the N – channel enhancement type.

- The result is depletion region near the SiO_2 insulating layer void of holes. However, the electrons to the(p-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer.
- The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until the induced n - type region can support a measurable flow between drain and source.
- The level of V_{GS} that results in the significant in the drain current is called the threshold voltage (V_T). Since the channel is nonexistent with V_{GS}= 0V and "enhanced" by the application of positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET.
- As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current.

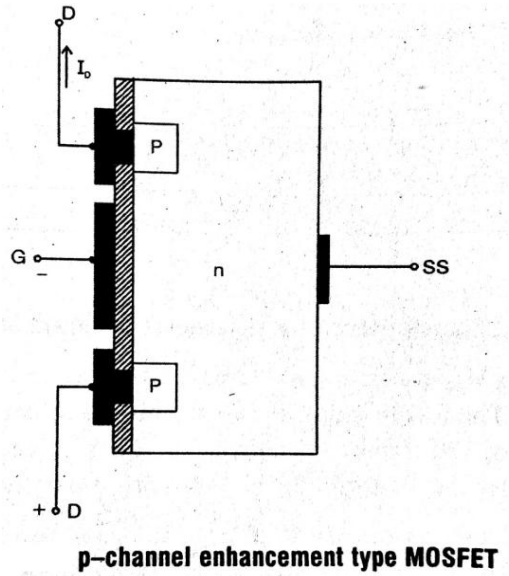
- If we keep V_{GS} constant and increase the level of V_{DS}, the drain current will reach the saturation level. Any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown condition occurs.
- The drain characteristics shows that as the level of V_{GS} increases from 0V to 8V the resulting saturation level for I_D also increases, from a level of 0mA to 10mA.
- The transfer characteristics shows that it is totally in the positive V_{GS} region and I_D does not flow until $V_{GS} = V_T$



Characteristics of n–channel enhancement MOSFET.

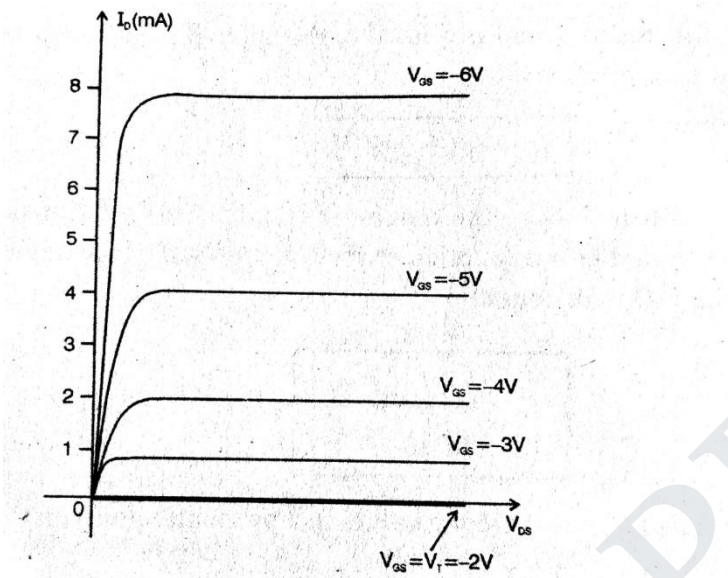
P – CHANNEL ENHANCEMENT MOSFET (E – MOSFET)

- The construction of a P – channel enhancement type MOSFET is exactly the reverse of that N – channel enhancement MOSFET. Now there is an N – type substrate and P – type region under the drain and source connections as shown.



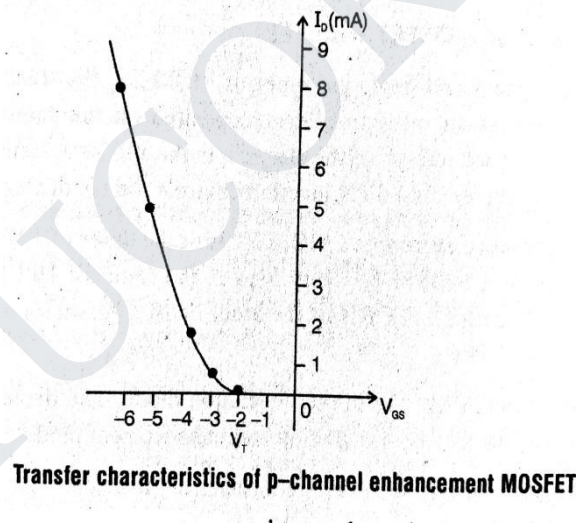
p–channel enhancement type MOSFET

The drain characteristics appears with increasing levels of current for increasing negative values of V_{GS}



Drain characteristics of p–channel enhancement MOSFET.

The drain characteristic appears with increasing the drain current for increasing negative values of V_{GS} beyond V_T.



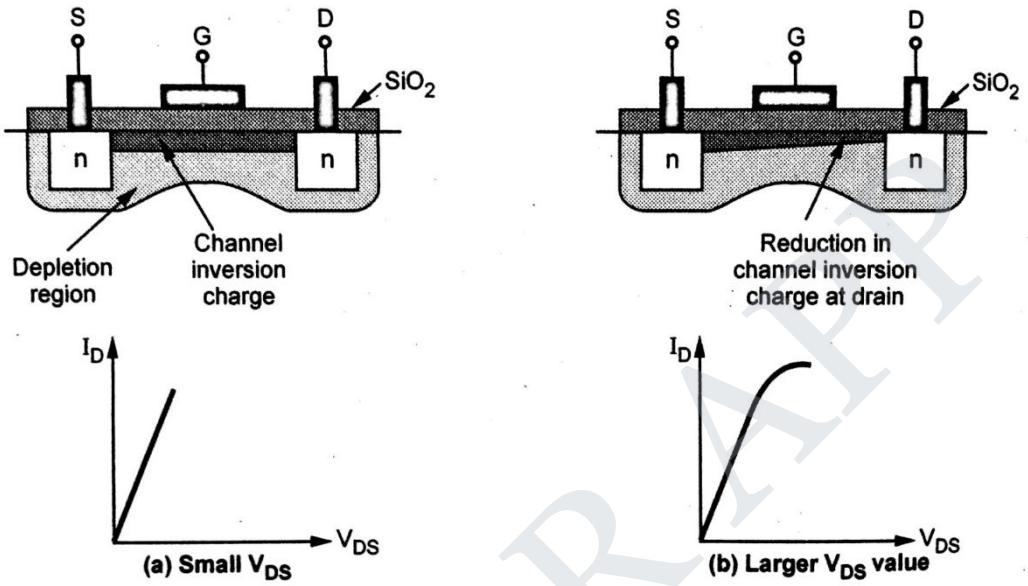
Transfer characteristics of p–channel enhancement MOSFET

4. Discuss the effect of channel length modulation. (A/M-17)

CHANNEL LENGTH MODULATION

- The Fig. shows induced channel at different levels of V_{DS}. In the figure, the thickness of the induced channel layer qualitatively indicates the relative charge density.
- In Fig. (a), applied V_{DS} is small and for this case the relative charge density is constant along the entire channel length.

- The Fig.(b) shows the situation when V_{DS} increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases.
- The incremental conductance of the channel at the drain then decreases, which causes the slope of the I_D versus V_{DS} curve to decrease. This effect is shown in the I_D versus curve in the figure.



- As V_{DS} increases to the point where the potential difference across the oxide at the drain terminal is equal to V_T, the induced inversion charge density at the drain terminal is zero. This is illustrated in Fig. (c).
  - When V_{DS} becomes larger than $V_{DS\,(sat)}$ the point in the channel at which the inversion charge is just zero moves towards the source terminal.

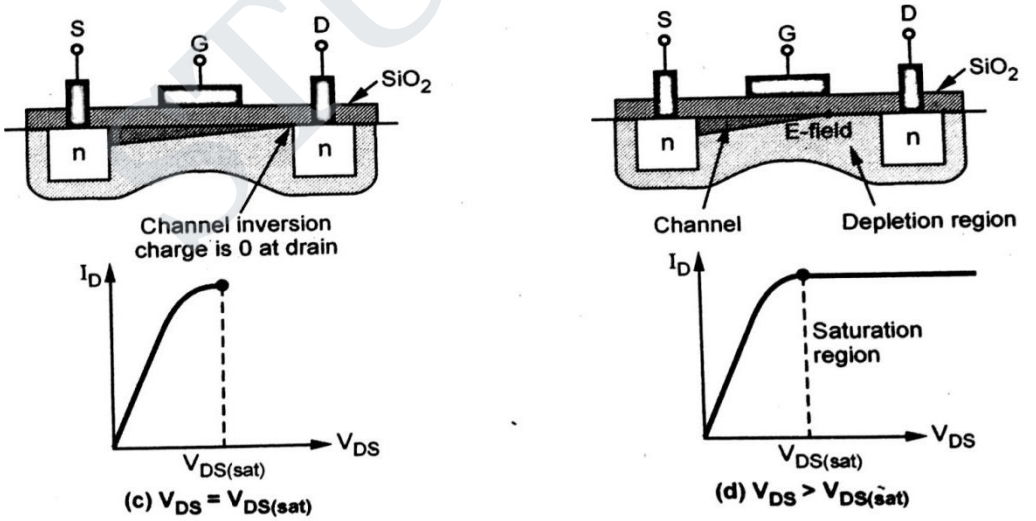


Fig. 3.14.1 Channel length modulation

- In this case, electrons enter the channel at the source, travel through the channel towards the drain, and then at the point where the charge goes to zero, are injected into the depletion region, where they are swept by the E-field to the drain contact.
- It is observed that as V_{DS} increases beyond $V_{DS\ (sat)}$ effective channel length decreases, producing the phenomenon called channel length modulation.

5. Derive an expression for drain current of FET in Pinch off region with necessary diagram. (A/M-16)

- In a transfer characteristics we have seen that the relationship between the drain current I_D and gate to source voltage V_{GS} is non-linear. This relationship is defined by **Shockley's** equation

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \quad \ldots (3.8.1)$$

- The squared term of the equation will result in a non-linear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}.

- In equation (3.8.1) I_D represents saturation drain current. I_{DSS} is the value of I_D when $V_{GS} = 0$, and V_P is the pinch-off voltage. Differentiating this expression we get,

$$\frac{\partial I_D}{\partial V_{GS}} = I_{DSS} \times 2\left(1-\frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right)$$

$$\therefore \quad g_m = \frac{-2\,I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$$

since $$\left.\frac{\partial I_D}{\partial V_{GS}}\right|_{\substack{V_{DS}\\ \text{constant}}} = g_m \quad \ldots (3.8.2)$$

- From expression (3.8.1) we also have,

$$\left(1-\frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_D}{I_{DSS}}} \quad \ldots (3.8.3)$$

- Substituting this value in equation (3.8.2) we have,

$$g_m = \frac{-2\,I_{DSS}}{V_P}\sqrt{\frac{I_D}{I_{DSS}}} = \frac{-2\sqrt{I_D I_{DSS}}}{V_P} \quad \ldots (3.8.4)$$

- When $V_{GS} = 0$, $g_m = g_{mo}$ then from equation (3.8.2).

$$g_{mo} = \frac{-2\,I_{DSS}}{V_P} \quad \ldots (3.8.5)$$

- Therefore, from equations (3.8.2) and (3.8.5)

$$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_P}\right) \quad \ldots (3.8.6)$$

- The equation (3.8.4) shows that g_m varies as the square root of the saturation current I_D and equation (3.8.4) shows that g_m decreases linearly with increase of V_{GS}.

6. For an n-channel silicon FET with a = 3×10^{-4} cm and Nd = 10^{15} electrons/cm^{-3}. Find (a) the pinch off voltage and (b) the channel half width for $V_{GS}=0.5V_P$.

Given: a = 3×10^{-4} cm = 3×10^{-6} m

Nd = 10^{15} electrons/cm^{-3} = 10^{21} electrons/m^{-3}

$V_{GS}=0.5V_P$

To Find:

(i). pinch off voltage

(ii). Channel half width

Solution: Since the relative dielectric constant of silicon is 12. We have $\varepsilon=12\varepsilon_0$, using values of q and ε_0 we have,

(i). pinch off voltage:

$$V_P=\frac{qN_da^2}{2\varepsilon}$$

$$V_P=\frac{1.6\times10^{-19}\times10^{21}\times(3\times10^{-6})^2}{2\times12\times(36\pi\times10^9)^{-1}}$$

Pinch off voltage, $V_P=6.8$ V

(ii). Channel half width:

$$V_{GS}=(1-\frac{b}{a})^2V_P$$

$$(1-\frac{b}{a})^2=\frac{V_{GS}}{V_P} \qquad [V_{GS}=0.5V_P]$$

$$(1-\frac{b}{a}) = \frac{1}{\sqrt{2}}$$

$$\frac{b}{a}=1-0.707$$

b = 0.293×a = $0.293\times(3\times10^{-6})$

b = 0.879 m

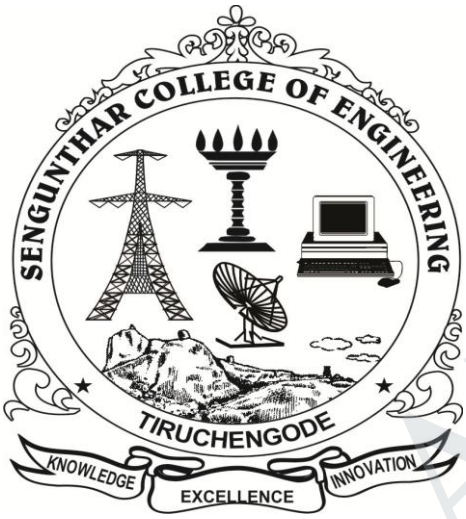
This result shows that the channel width is reduced to about one-third its value for $V_{GS}=0.5V_P$.

EC8252- ELECTRONIC DEVICES

I YEAR / II SEMESTER B.E. (ME)

UNIT – IV

SPECIAL SEMICONDUCTOR DEVICES



COMPILED BY

V.KAVITHA M.E., (AP/ME)

VERIFIED BY

HOD **PRINCIPAL** **CORRESPONDENT**

DEPARTMENT OF MEDICAL ELECTRONICS

SENGUNTHAR COLLEGE OF ENGINEERING – TIRUCHENGODE

UNIT – IV

SPECIAL SEMICONDUCTOR DEVICES

- Metal-Semiconductor Junction
- MESFET , FINFET, PINFET, CNTFET
- **DUAL GATE MOSFET**
- **Schottky barrier diode**
- **Zener diode**
- **Varactor diode**
- **Tunnel diode**
- **Gallium Arsenide device**
- **LASER diode**
- **LDR.**

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LIST OF IMPORTANT QUESTIONS

UNIT IV – SPECIAL SEMICONDUCTOR DEVICES

PART – A

1. What is the basic principle behind the LDR? / Outline the working principle of Light Dependent Resistor. (N/D-2015) (N/D-19)
2. Differentiate CNTFET structure and traditional MOSFET structure. (N/D-19)
3. Give the difference between JFET and MESFET. (A/M-2019)
4. What is tunneling phenomenon? / What is meant by tunneling? (A/M-2019) (N/D-2016)
5. Draw the symbol of FINFET/ What is FINFET. (N/D-15) (A/M-18)
6. What is referred as CNTFET? (A/M-18)
7. Define Snell's law. (N/D-2017)
8. State the significance of MOSFET devices. (N/D-2017)
9. Mention the applications of Varacter Diode. (N/D-2015) (A/M-2017)
10. . Define Gunn Effect. (A/M-2017)
11. What is metal semiconductor contact? (N/D-16)
12. What is recovery time? Give its types. (N/D-16)

PART – B

1. Write short notes on schottky diode. (OR) Sketch the basic construction and characteristics for a schottky diode and explain the operation. (OR) Draw the VI characteristics of schottky diode and explain its operation. (M/J-2014) (N/D-2015) (M/J-2017) (A/M-2019) (N/D-2017)

2. Explain the principle behind the varactor diode and list out its application. (OR) Explain the principle and operation of varactor diode (M/J-2014) (N/D-2014) (M/J-2015) (M/J-2016) (N/D-2017)

3. Describe the working of metal semiconductor junction/ illustrate the operation of a MESFET with energy band diagram and space charge regions. (A/M-2015) (A/M-2019) (N/D-2019)

4. Give the details about the laser diode. (OR) Briefly describe about the operation of Laser diode. (OR) Explain the working and characteristics of laser diode (M/J-14)(M/J-16)(N/D-16) (A/M-18) (N/D-19)

5. Write short notes on: Tunnel diode (OR) Explain the operation of Tunnel diode and its characteristics with diagram. (OR) What is mean by tunneling? Explain the VI characteristics of Tunnel diode using energy band diagram. (OR) Explain the construction and volt ampere characteristics of Tunnel diode (M/J-2015) (N/D-2015) (M/J-2016) (N/D-2016) (N/D-2017) (A/M-2018) (A/M-2019)

6. Draw the VI characteristics of zener diode and explain its operation. (OR) Explain the VI characteristics of zener diode and distinguish between Avalanche and Zener Breakdown. (OR) With neat diagram explain the operation of zener diode and its characteristics and also brief how it can be used as a regulator. (M/J-2014) (N/D-2014) (N/D-2015) (N/D-2016) (M/J-2017) (N/D-2017) (A/M-2018)

PART – A

1. What is the basic principle behind the LDR? / Outline the working principle of Light Dependent Resistor. (N/D-2015) (N/D-19)

A light dependent resistor works on the principle of **photo conductivity**. Photo conductivity is an optical phenomenon in which the materials conductivity is increased when light is absorbed by the material.

- When light falls i.e. when the photons fall on the device, the electrons in the valence band of the semiconductor material are excited to the conduction band.
- When light having enough energy strikes on the device, more and more electrons are excited to the conduction band which results in large number of charge carriers. The result of this process is more and more current starts flowing through the device

2. Differentiate CNTFET structure and traditional MOSFET structure. (N/D-19)

A **carbon nanotube field-effect transistor (CNTFET)** refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure.

MOSFET structure

It is a four-terminal device with source(S), gate (G), drain (D) and body (B) terminals. The body is frequently connected to the source terminal, reducing the terminals to three. It works by varying the width of a channel along which charge carriers flow (electrons or holes).

3. Give the difference between JFET and MESFET. (A/M-2019)

MOSFET is the acronym for "metal-oxide–semiconductor field-effect transistor" and MESFET is the acronym for "metal–semiconductor field-effect transistor".

The main difference between them is in the gate (G) terminal fabrication.

In the MOSFET, between the G and the channel (whose ends are the drain (D) and the source (S)) it is a thin **layer of dielectric material**, SiO2 (silicon dioxide, but often just called **"oxide"**) and the gate input behaves somewhat as a capacitor.

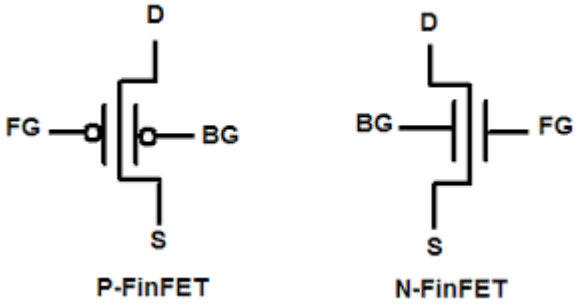
4. What is tunneling phenomenon? / What is meant by tunneling? (A/M-2019) (N/D-2016)

- According to the classical laws of physics a charged particle sin order to cross an energy barrier should possess energy at least equal to the energy barrier.
- Hence the particle will cross the energy barrier if its energy is greater than the barrier and cannot cross the barrier if its energy is less than the energy barrier.

- But quantum mechanically there exists non zero probability that the particle with energy less than the energy barrier will cross the barrier as if it tunnels across the barrier. This is called as Tunneling effect.

5. Draw the symbol of FINFET/ What is FINFET. (N/D-15) (A/M-18)

- FINFET technology takes its name from the fact that the FET structure used looks like a set of fins when viewed.
- The FINFET conducting channel is covered by a thin silicon fin, which forms the body of the device. The thickness of the fin determines the effective channel length of the device.



6. What is referred as CNTFET? (A/M-18)

- A **carbon nanotube field-effect transistor (CNTFET)** refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure.

7. Define Snell's law. (N/D-2017)

Snell's law (also known as **Snell-Descartes law** and the **law of refraction**) is a formula used to describe the relationship between the angles of incidence and refraction, when referring to light or other waves passing through a boundary between two different isotropic media, such as water, glass, or air.

8. State the significance of MOSFET devices. (N/D-2017)

- A power MOSFET is a specific type of metal oxide semiconductor field-effect transistor (MOSFET) designed to handle significant (high) power levels.
- These exhibit high switching speed and can work much better in comparison with other normal MOSFETs in the case of low voltage levels.

- However its operating principle is similar to that of any other general MOSFET. Power MOSFETs which are most widely used are n-channel or p-channel Enhancement-mode or n-channel Depletion-mode in nature.
- The power MOSFET is the most widely used low-voltage (that is, less than 200 V) switch. It can be found in most power supplies, DC to DC converters, and low voltage motor controllers.

9. Mention the applications of Varacter Diode. (N/D-2015) (A/M-2017)

The varactor diodes are used in

- FM radio and TV receivers,
- AFC circuits,
- self adjusting bridge circuits and adjustable bandpass filters.
- LC resonant circuit in microwave frequency multipliers and
- in very low noise microwave parametric amplifiers.

10. Define Gunn Effect. (A/M-2017)

- The Gunn Effect can be defined as generation of microwave power (power with microwave frequencies of around a few GHz) whenever the voltage applied to a semiconductor device exceeds the critical voltage value or threshold voltage value.
- Gunn effect is exhibited by semiconductor materials like gallium arsenide, indium phosphide, cadmium telluride and indium arsenide.

11. What is metal semiconductor contact? (N/D-16)

- A metal semiconductor junction is a type of junction in which a metal comes in close contact with a semiconductor material. A metal semiconductor junction can either be rectifying or non rectifying.
- The rectifying metal semiconductor junction forms a schottky barrier and non rectifying semiconductor junction is called an ohmic contact.

12. What is recovery time? Give its types. (N/D-16)

❖ **Forward recovery time**

Forward **recovery** is **the time** that it takes for **the diode** to come out of **the** forward conduction mode and change to **the** not conducting condition.

❖ **Reverse recovery time**

Reverse **recovery** is **the time** that it takes for **the diode** to come out of **the** reverse conduction condition mode and begin to change to **the** conduction condition.

13. Mention some advantages and disadvantages of Tunnel Diode. (A/M-2016)

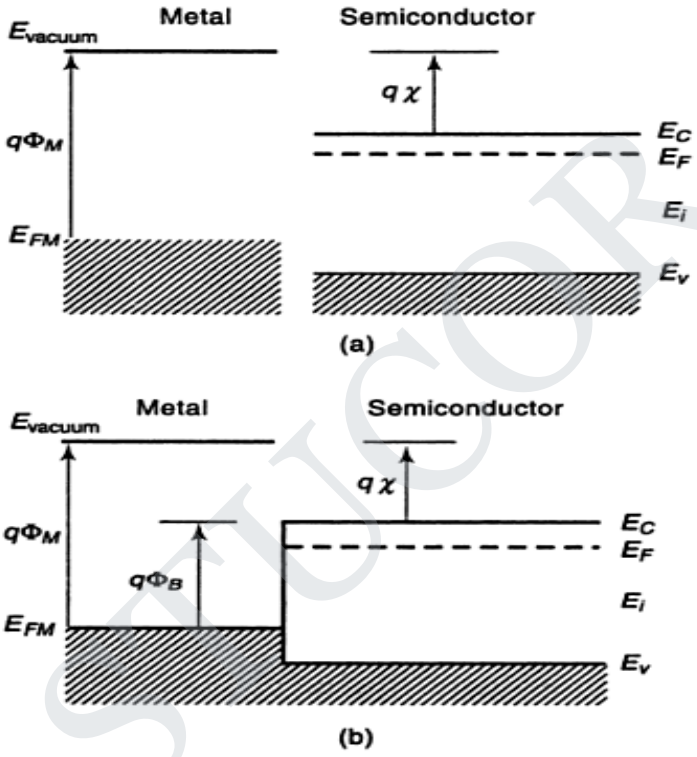
ADVANTAGES

- Low noise
- Ease of operation due to fact that tunnelling
- High speed
- Environmental immunity
- Low power dissipation

DISADVANTAGES

- Voltage range over which it can be operated is 1 V less
- Being a two terminal device, there is no isolation between the input and output circuit.

14. Draw the energy band diagram of metal and semiconductor before and after conduction is made (M/J-2014) (A/M-2016)



- **a)before b)after**

15. Expand LASER, LDR (A/M-2015)

Light Amplification by Stimulated Emission of Radiation

1. Light-dependent resistor - A Light Dependent Resistor (LDR) or a photo resistor is a device whose resistivity is a function of the incident electromagnetic radiation. Hence, they are light sensitive devices. They are also called as photo conductors, photo conductive cells or simply photocells.

16. What is MESFET? (A/M-2015)

- MESFET stands for metal–semiconductor field-effect transistor. It is quite similar to a JFET in construction and terminology. The difference is that instead of using a p-n junction for a gate, a Schottky (metal-semiconductor) junction is used.
- The MESFET is a high performance form of field effect transistor that is used mainly for high performance microwave applications and in semiconductor RF amplifiers.

17. Compare between schottky diode and conventional diode. (N/D-2016)

Parameter	p-n junction diode	Schottky diode
Junction	Semiconductor to semiconductor	Semiconductor to metal
Carriers	Minority and majority	Only majority
Reverse recovery time	More	Less
Barrier potential	More about 0.7 V	Less about 0.25 V
Breakdown voltage	More	Less
Switching speed	Less	High
PIV rating	More	Less
Frequency range	Upto 10 MHz	Very high more than 300 MHz
Applications	Mainly rectifiers and low frequency devices	High frequency devices digital computers, radar systems, Schottky TTL logics, mixers etc.

18. List out the application of tunnel diode. (M/J-2014)

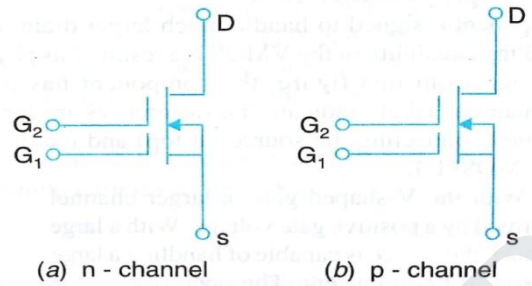
- Tunnel diode is used as an ultra-high speed switch with switching speed of the order of ns or ps.
- As logic memory storage device
- As microwave oscillator
- In relaxation oscillator circuit
- As an amplifier.

19. Mention the applications of LDR. (N/D-2014)

- The detector is used either as an ON/OFF device to detect the presence or absence of a light source which is used for automatic street lighting
- it is used to measure a fixed amount of illumination and to record a modulating light intensity.

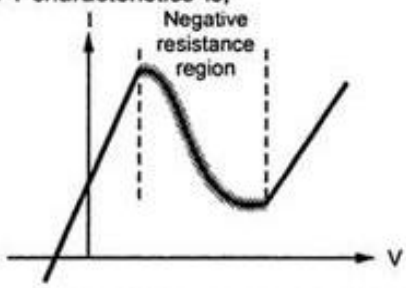
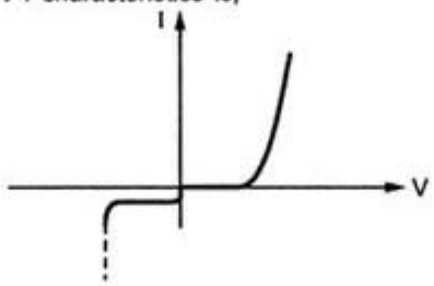
- It is used in counting systems where the objects on a conveyor belt interrupt a fight beam to produce a series of pulses which operates a counter.
- When the day light has faded to a given level, the corresponding resistance of the detector causes another circuit to switch ON the required lights.
- It is widely used in cameras to control shutter opening during the flash.

20. Draw the symbol for Dual Gate MOSFET. (N/D-2014) (N/D-15)

- 

21. What are the difference between a tunnel diode and an ordinary PN junction diode? (N/D-2014)

	Tunnel diode	Conventional p-n junction diode
1.	Impurity concentration is high about 1 part in 10^3 atoms.	Impurity concentration is low about 1 part in 10^8 atoms.
2.	Depletion region width is about 5 microns, which is 1/ 100th the width of typical p-n junction diode.	The width of depletion region is high compared to the tunnel diode.
3.	The carrier velocities are very high at low forward bias, hence can punch through the depletion region.	The carrier velocities are low at low forward bias, hence can not penetrate the depletion region.

4.	The V-I characteristics shows the negative resistance region.	The V-I characteristics does not show the negative resistance region.
5.	The V-I characteristics is, 	The V-I characteristics is, 
6.	The materials used for construction are germanium or gallium arsenide.	The silicon is most popularly used.
7.	The symbol is, 	The symbol is, 
8.	The switching time is very low of the order of nano to picoseconds.	The switching time is high.
9.	Used for high frequency oscillators, high speed applications such as computers, pulse and digital circuits and switching networks.	Used in rectifiers and other general purpose applications.

22. State the applications of Metal – Semiconductor junction.

- Used as microwave diodes.
- Used as ohmic contacts in many electronic devices.
- Used as shunt diodes to reduce switching transients
- Used in Ultraviolet detectors.

23. What are the features of MESFET?

- Mobility of electron is very high.
- Since the transit time is small, response is very fast.
- Can be operated at very high frequencies because of short channel length
- The fabrication process is simple.
- Parastic capacitance is small.

24. What are the advantages of Dual Gate MOSFET?

- Reduction of leakage current.
- Better control of short channel effects.
- Higher current drive capability because of double gate.
- Low noise.

- High-gain and high frequency amplifiers because of their low feedback capacitance and high transconductance.

25. What are the applications of Dual Gate MOSFET?

- Used as mixer in RF circuits.
- Used as a RF amplifier.
- Used in Automatic Gain Control (AGC).

26. What are the advantages of FINFET?

- Reduces short channel effects.
- Lower leakage current.
- Provides better electrostatic control over the channel.

2. What are the applications of FINFET?

- Because of its low leakage current, it used in low power design in digital circuit such as RAM.
- Power amplifier or other application in analog area which requires good linearity.

PART – B

1. Write short notes on schottky diode. (OR) Sketch the basic construction and characteristics for a schottky diode and explain the operation. (OR) Draw the VI characteristics of schottky diode and explain its operation. (M/J-2014) (N/D-2015) (M/J-2017) (A/M-2019) (N/D-2017)

SCHOTTKY BARRIER DIODE:

- A Schottky barrier diode is a metal semiconductor junction formed by bringing metal in contact with a moderately doped n type semiconductor material.
- A Schottky barrier diode is also called as known as Schottky or hot carrier diode. It is named after its inventor Walter H. Schottky, barrier stands for the potential energy barrier for electrons at the junction.
- It is a unilateral device conducting currents in one direction (Conventional current flow from metal to semiconductor) and restricting in the other.
- This device can simply rectify frequencies greater than 300 MHz. Its forward voltage drop is also very low (0.15 to 0.45 V). This results in higher switching speed and improved system efficiency.

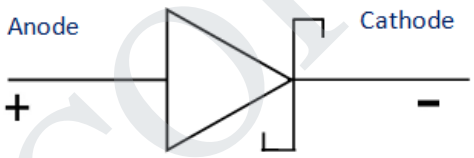


Figure 1

- Schottky diode symbol is shown in the figure. A Schottky barrier diode is a two terminal device with metal terminal acting as anode and semiconductor terminal acting as anode.

CONSTRUCTION:

- A metal semiconductor junction is formed at one end, it is a unilateral junction. Another metal semiconductor contact is formed at the other end. It is an ideal Ohmic bilateral contact with no potential existing between metal and semiconductor and is non rectifying.
- The typical metals used in the manufacture of Schottky barrier diode are molybdenum, platinum, chromium, tungsten Aluminium, gold etc and the semiconductor used is N type silicon is used.

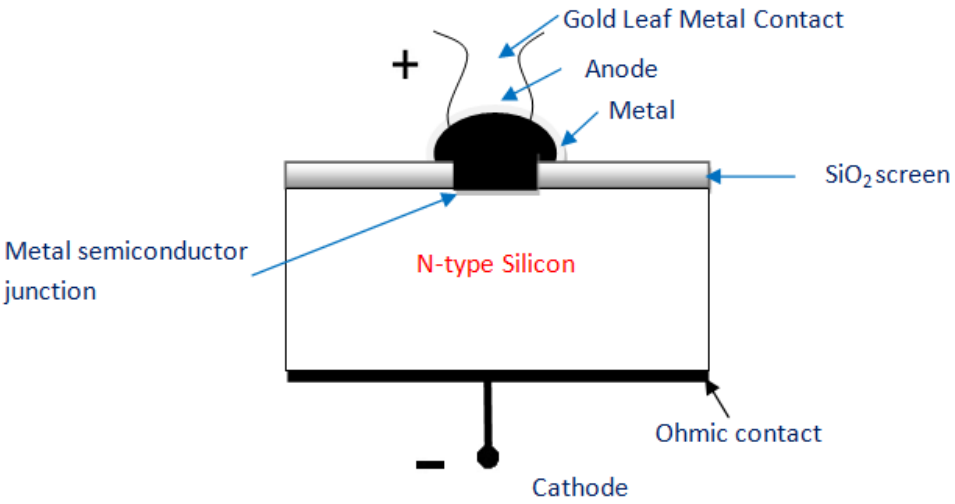


Figure 2: Passivated Schottky Diode

OPERATION:

- When a Schottky diode is in unbiased condition, the electrons lying on the semiconductor side have very low energy level when compared to the electrons present in metal. Thus, the electrons cannot flow through the junction barrier which is called **Schottky barrier**.

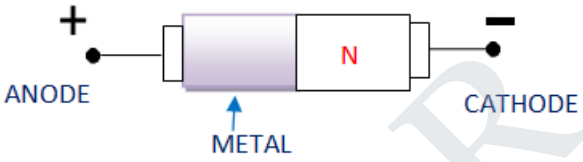


Figure 3

- If the diode is forward biased, electrons present in the N-side gets sufficient energy to cross the junction barrier and enters into the metal. These electrons enter into the metal with tremendous energy. Consequently these electrons are known as hot carrier. Thus the diode is so called as **hot-carrier diode**.
- The heavy flow of electrons into the metal creates a region near the junction which is similar to the depletion region in the PN junction diode.
- The additional carriers in the metal establish a negative wall in the metal at the boundary between the two materials. As a result, a **surface barrier** is formed between the two materials preventing any further flow of current.
- As there is very little minority carrier injection from semiconductor into metal, Schottky diodes are also said to be **majority carrier devices.**

CURRENT COMPONENTS IN SCHOTTKY DOIDE:

The current condition in this diode is through electrons (majority carriers) in N-type semiconductor.

$$I_T = I_{Diffusion} + I_{Tunneling} + I_{Thermonic\ emission}$$

$I_{Diffusion}$ → Diffusion current

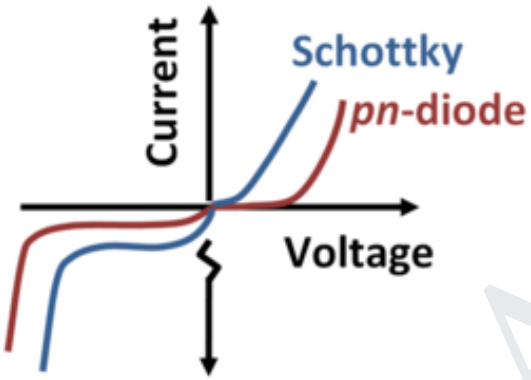
D_n → Diffusion constant of electrons.

q → Electronic charge =1.6 ×10^{19} C.

$I_{Tunneling}$ → Tunneling current

$I_{Thermonic\ emission}$ → As a result of electron ejection due to thermal energy (thermionic emission), this current will be produced across the electrodes.

V - I CHARACTERISTICS:



- From the VI characteristics it is obvious that the VI characteristics of Schottky barrier diode is similar to normal PN junction diode with the following exceptions
- The forward voltage drop of Schottky barrier diode is low compared to normal PN junction diode. The forward voltage drop of Schottky barrier diode made of silicon exhibits a forward voltage drop of 0.3 volts to o.5 volts.
- The forward voltage drop increases with the increasing doping concentration of n type semiconductor.
- The VI characteristics of Schottky barrier diode is Steeper compared to VI characteristics of normal PN junction diode due to high concentration of current carriers.

ADVANTAGES

- It has fast recovery time due to very low quantity of stored charge. So this diode is used for high speed switching application.
- It has low turn on voltage.
- It has low junction capacitance.
- Voltage drop is low.

DISADVANTAGES

- Reverse leakage current.
- Low reverse voltage rating

APPLICATIONS

- Used in Switched-mode power supplies.

- Used in reverse current protection.
- Used in discharge protection.
- Used in voltage clamping application.
- Used in RF mixer and Detector diode.
- Used in solar cell application.

2. Explain the principle behind the varactor diode and list out its application. (OR) Explain the principle and operation of varactor diode (M/J-2014) (N/D-2014) (M/J-2015) (M/J-2016) (N/D-2017)

VARACTER DIODE

- **Varactor Diode** is a reverse biased p-n junction diode, whose capacitance can be varied electrically. As a result these diodes are also referred to as varicaps, tuning diodes, voltage variable capacitor diodes, parametric diodes and variable capacitor diodes.
- It is well known that the operation of the p-n junction depends on the bias applied which can be either forward or reverse in characteristic.
- It is also observed that the span of the depletion region in the p-n junction decreases as the voltage increases in case of forward bias.
- On the other hand, the width of the depletion region is seen to increase with an increase in the applied voltage for the reverse bias scenario.
- Under such condition, the p-n junction can be considered to be analogous to a capacitor (Figure 1) where the p and n layers represent the two plates of the capacitor while the depletion region acts as a dielectric separating them.

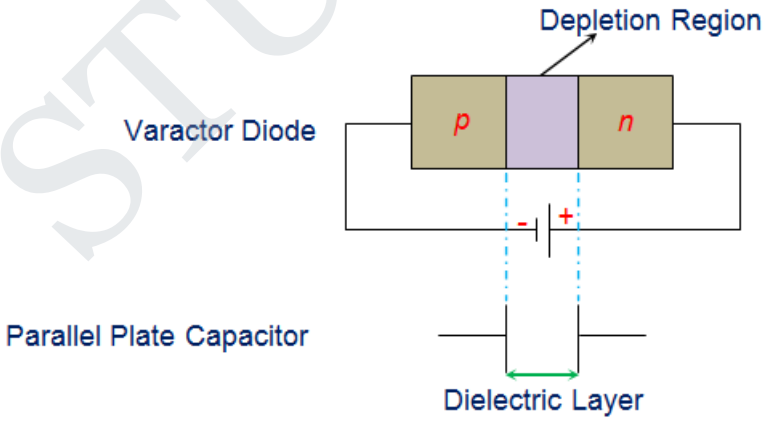


Figure 1 Varactor Diode Analogous to a Parallel Plate Capacitor

- The varacter diode with its symbol is shown in figure.

(a) (b)

Figure 2 (a) Electrical Equivalent Circuit of Varactor Diode (b) Symbol of Varactor Diode

- Hence, mathematical expression for the capacitance of varactor diode is given by

$$C_j = \frac{\varepsilon A}{d}$$

Where,

C_j is the total capacitance of the junction.

ε is the permittivity of the semiconductor material.

A is the cross-sectional area of the junction.

d is the width of the depletion region.

- The relationship between the capacitance and the reverse bias voltage is given as

$$C_j = \frac{CK}{(V_b - V_R)^m}$$

Where,

C_j is the capacitance of the varactor diode.

C is the capacitance of the varactor diode when unbiased.

K is the constant, often considered to be 1.

V_b is the barrier potential.

V_R is the applied reverse voltage.

m is the material dependent constant.

OPERATION & V-I CHARACTERISTICS:

- Varacters are operated in a reverse biased state. No current flows, but since the thickness of the depletion region varies with the applied bias voltage.
- As a result, one can conclude that the capacitance of the varactor diode can be varied by varying the magnitude of the reverse bias voltage as it varies the width of the depletion region, d.

- From the capacitance equation that d is inversely proportional to C. This means that the junction capacitance of the **varactor diode** decreases with an increase in the depletion region width caused to due to an increase in the reverse bias voltage (V_R), as shown by the graph in Figure 3.
- varactor diodes are manufactured with an intention to obtain a definite C-V curve which can be accomplished by controlling the level of doping during the process of manufacture.
- At zero volt, the varactor depletion region W is small and the capacitance is large at approximately 600 pF. When the reverse bias voltage across the varactor is 15 V, the capacitance is 30 pF.

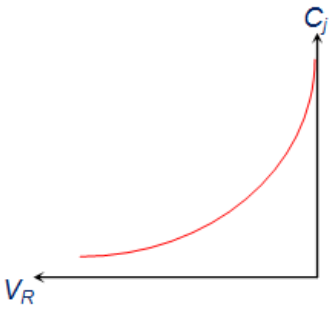


Figure 3 Characteristic Curve of a Varactor Diode

ADVANTAGES

These varactor diodes are advantageous as they are compact in size, economical, reliable and less prone to noise when compared to other diodes.

APPLICATIONS

The varactor diodes are used in

- FM radio and TV receivers,
- Automatic Frequency Control circuits,
- self adjusting bridge circuits and adjustable bandpass filters.
- LC resonant circuit in microwave frequency multipliers and
- In very low noise microwave parametric amplifiers.

3. Describe the working of metal semiconductor junction/ illustrate the operation of a MESFET with energy band diagram and space charge regions. (A/M-2015) (A/M-2019) (N/D-2019)

METAL-SEMICONDUCTOR JUNCTIONS

- Metal—semiconductor junctions are very common in all semiconductor devices and have very high importance.

- Depending upon the doping concentration, materials, and the characteristics of the interface, the metal—semiconductor junctions can act as either an ohmic contact or as a Schottky barrier.

STRUCTURE AND CONSTRUCTION

- A metal—semiconductor junction, as the name indicates, consists of a metal in contact with a piece of semiconductor. The structure of a typical metal—semiconductor junction is shown in Fig.
- The active junction is the interface between the metal, which acts as an anode, and the semiconductor.
- The other interface between the semiconductor and the metal, which acts as a cathode, is an Ohmic contact and there is no potential drop at this junction.

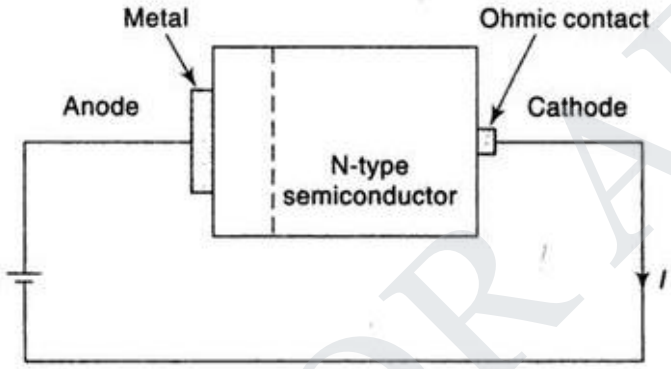


Fig. 5.11 Structure of a metal–semiconductor junction

ENERGY BAND DIAGRAM

- The energy band diagram helps in identifying the barrier between the metal and the semiconductor. In order to understand the energy band structure at a metal—semiconductor junction, first let us consider the energy bands in metal and semiconductors separately, as shown in Fig.(a).
- The energy bands are aligned at the same vacuum level. When the metal and semiconductor are brought together, the Fermi levels do align themselves at thermal equilibrium. The condition that exists just before the thermal equilibrium is reached is depicted in Fig.(b).

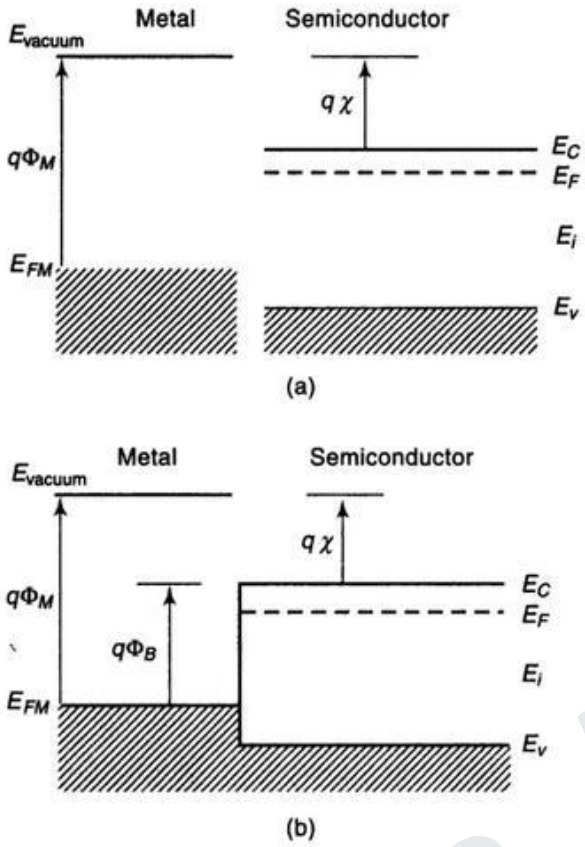


Fig. 5.12 Energy band diagram of metal and semiconductor (a) before and (b) after contact is made

Let us define, Φ_B, the barrier height as the potential difference between the Fermi level of the metal and the band edge where the majority carriers exist. For an N-type semiconductor, the barrier height is given by the difference between the metal work function (Φ_M) and the electron affinity (χ).

$$\Phi_{BN} = \Phi_M - \chi \tag{5.1}$$

The work function, Φ_M varies depending upon surface preparation. For P-type semiconductor, the barrier height is given by the difference between the valence band level and the Fermi level in the metal,

$$\Phi_{BP} = \chi + \frac{E_g}{q} - \Phi_M \tag{5.2}$$

- where E_g is the energy gap between the conduction and valence bands. The sum of the barrier heights on N-type and P-type substrate is expected to be equal to the energy gap. E_g.
- In a metal-semiconductor junction, a barrier is formed if the Fermi level of the metal is somewhere between the valence and conduction band edges of the semi-conductor, as shown in Fig.(b).
- Let us also define a built-in potential (Φ) as the difference between the Fermi level of the metal and the Fermi level of the semiconductor.

For an N-type semiconductor, the barrier height is given by

$$\Phi_{BN} = \Phi_M - \chi$$

$$\Phi_{IN} = \Phi_{BN} - \frac{E_C - E_F}{q} = \Phi_M - \chi - \frac{E_C - E_F}{q} \quad (5.3)$$

For a P-type semiconductor, the Fermi level is closer to the valence band and the built-in potential is given by

$$\Phi_{IP} = \chi + \frac{E_F - E_V}{q} - \Phi_M \quad (5.4)$$

The Fermi level in an N-type semiconductor is given by

$$E_F = E_C - kT \ln \frac{N_C}{N_D} \quad (5.5)$$

and the Fermi level in a P-type semiconductor is given by

$$E_F = E_V + kT \ln \frac{N_V}{N_A} \quad (5.6)$$

Substitution Eq. (5.5) and Eq. (5.6) in Eq. (5.3) and Eq. (5.4), respectively, would give expressions for built in potentials in terms of the barrier height and doping concentration, as follows.

$$\Phi_{IN} = \Phi_{BN} - \frac{E_C - E_F}{q} = \Phi_{BN} - \frac{kT}{q} \ln \frac{N_C}{N_D} \quad \text{for N-type semiconductor} \quad (5.7)$$

and

$$\Phi_{IP} = \Phi_{BP} - \frac{E_F - E_V}{q} = \Phi_{BP} - \frac{kT}{q} \ln \frac{N_V}{N_A} \quad \text{for P-type semiconductor} \quad (5.8)$$

THERMAL EQUILIBRIUM

- After the metal and semiconductor have been brought into contact, electrons start to flow from the semiconductor into the metal, and as a result, a depletion region of width x_d, with uncompensated donors (positive charge) is formed.
- Electrons continue to flow into the metal until the Fermi energy levels of metal and semiconductor align with each other.
- In metal, the electron current forms a negative surface charge layer. This results in an electric field and the band edges are lowered in the semiconductor (Fig)

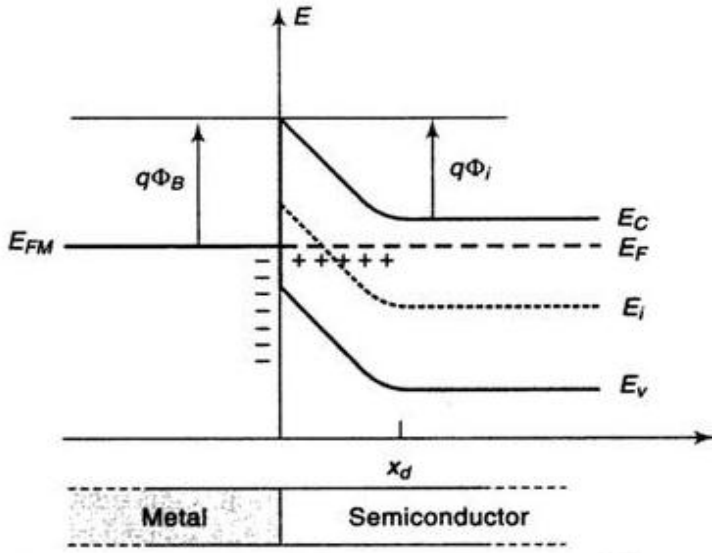


Fig. 5.13 Energy band diagram in thermal equilibrium

FORWARD BIAS:

- When an external bias is applied, the metal-to-semiconductor barrier remains unchanged, whereas, the semiconductor-to-metal barrier is either decreased (forward bias) or increased (reverse bias).
- When the metal is connected to a positive bias with respect to the semiconductor. The Fermi energy level of the metal is lowered from its equilibrium level. The depletion region is narrowed, and the potential barrier in the semiconductor is reduced.
- The number of electrons that diffuse from semiconductor to metal is now more than the number of electrons that drift from metal into the semiconductor. Thus, there will be a positive current through the device. Figure illustrates a metal—semiconductor junction under forward-bias condition.

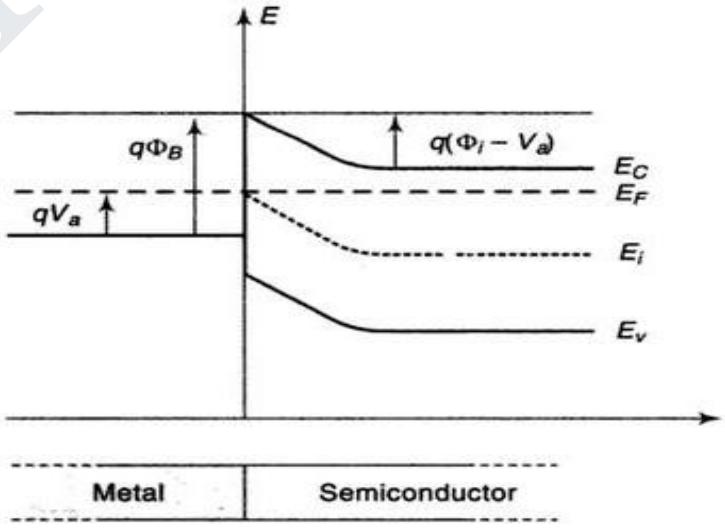


Fig. 5.14 Energy band diagram under forward bias

REVERSE BIAS

- If the metal is connected to a negative bias with respect to the semiconductor, the metal is charged even more negatively than without any bias.
- The Fermi energy level of the metal is raised. The electrons in the semiconductor are repelled even more. The depletion region becomes wider and the potential barrier on semiconductor side is further increased, as shown in Fig.
- The barrier on the metal side remains unchanged and limits the flow of electrons. A small current flows as a result of a few electrons in the metal acquiring enough thermal energy to overcome barrier.

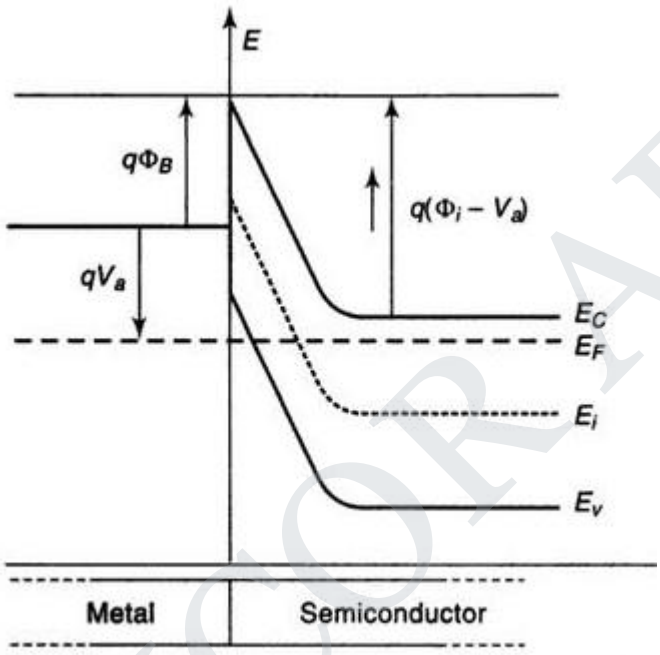


Fig. 5.15 Energy band diagram under reverse bias

Consider an n-channel GaAs MESFET at T = 300 K with a gold Schottky barrier contact. Assume the barrier height is $\Phi_{Bn} = 0.89$ *V. The n-channel doping is* $N_d = 2 \times 10^{15}$ cm^{-3}. *Determine the channel thickness such that* $V_T = +0.25$ *V. Also* $N_C = 4.7 \times 10^{17}$ cm^{-3} *and* ε_r *of GaAs = 13.1.*

Sol. :

$$V_n = \frac{KT}{q} \ln\left(\frac{N_C}{N_D}\right)$$

$$= 0.026 \ln\left(\frac{4.7\times10^{17}}{2\times10^{15}}\right) 0.14 \text{ V}$$

∴ **Built in potential is**

$$V_{bi} = \phi_{Bn} - V_n = 0.89 - 0.14 = \mathbf{0.75\ V}$$

$$V_T = V_{bi} - V_p$$

$$\therefore \quad V_p = V_{bi} - V_T = 0.75 - 0.25 = 0.5 \text{ V}$$

$$V_p = \frac{q N_D}{2\varepsilon} a^2$$

$$0.5 = \frac{(1.6\times10^{-19})(2\times10^{15})\, a^2}{2\times13.1\times(8.85\times10^{-14})}$$

$$\ldots \varepsilon_r = 13.1\varepsilon_0$$

$$a = 60\ \mu\text{cm} = 0.6\ \mu\text{m}$$

The channel thickness is 0.6 μm

4. Give the details about the laser diode. (OR) Briefly describe about the operation of Laser diode. (OR) Explain the working and characteristics of laser diode (M/J-14)(M/J-16)(N/D-16) (A/M-18) (N/D-19)

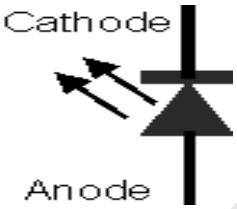
LASER DIODE:

- **Laser diodes** are the semiconductor lasers which generate highly intense coherent beam of light. and are also referred to as injection lasers.
- Similar to LED, Lasers are used to convert the electrical signal to light signal.
- It is well known that an incident photon can interact with the atom to release a photon which will be identical to the impinging photon in all respects viz., phase, frequency, polarization and direction of travel.
- This phenomenon is referred to as stimulated emission and forms the basis of working for Lasers (Light Amplification by Stimulated Emission of Radiations).

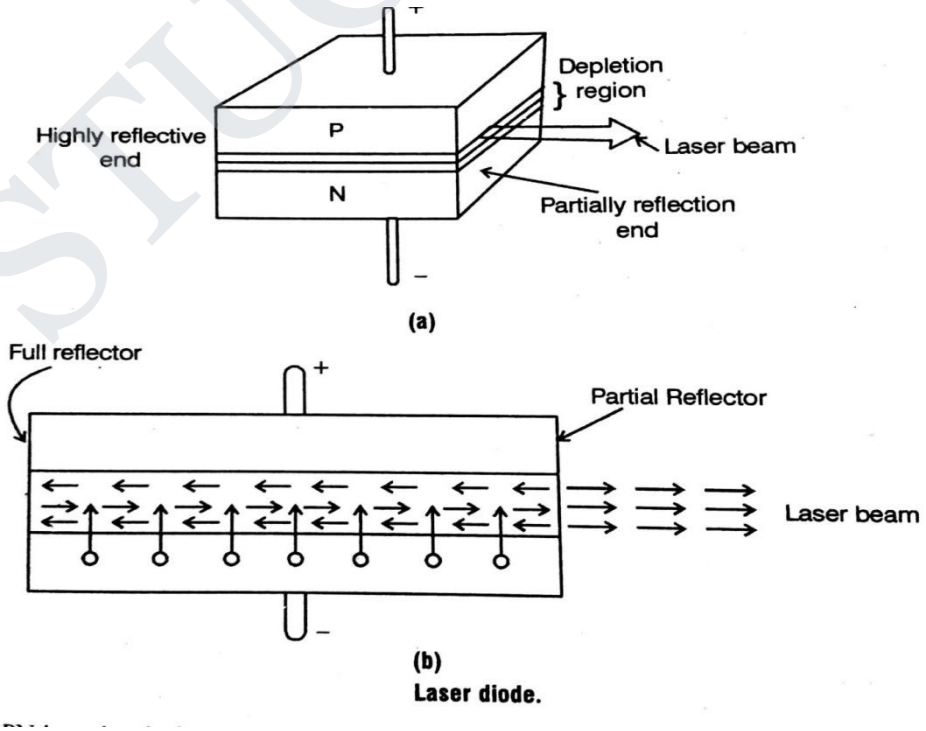
- Further, if this event occurs in case of a p-n junction, then the diode is referred to as **Laser diode**.
- Laser Diodes are usually made of three layers (sometimes even two) where Gallium Arsenide (GaAs) like materials are doped with aluminium or silicon or selenium to produce p and n layers while the central, undoped, active layer is intrinsic in nature.
- Laser diodes are constructed of Ga AlAs (Gallium Aluminium Arsenide) for short wavelength and InGaAsP(Indium Gallium Arsenide phosphide) for long wavelength devices.

CONSTRUCTION AND SYMBOL

- It consists of PN junction formed by two doped gallium arsenide layers. The two ends of the structure are flat and parallel with one end mirrored and one partially reflective. The laser diode structure can be divided into two categories

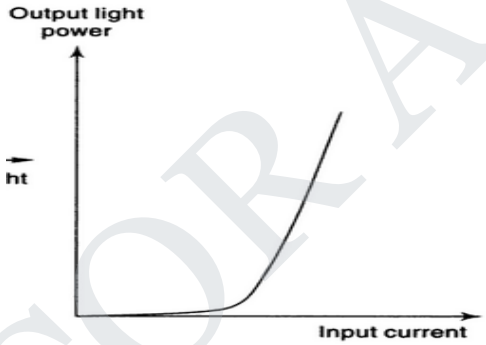


- Surface emitting laser diode : These laser diode emits light in a direction perpendicular to the PN junction plane.
- Edge emitting laser diode: These laser diode emits light in a direction parallel to the PN junction plane.



OPERATION :

- When the PN junction is forward biased by an external voltage source the electrons move through the junction and recombines as in an ordinary diode. When electrons recombine with holes photons are released. These photons strike atoms causing more photons to be released.
- As the forward bias current is increased more electrons enter the depletion region and cause more photons to be emitted. Some of the photons are randomly drifting within the depletion region strike the reflected surfaces perpendicularly so that they are reflected back along their original path. These reflected photons are then reflected back again from the other end of the junction.
- This movement of photons from one end to another end continues for thousands of times. During this movement photons strike more atoms and release additional photons due to the avalanche effect.



- As temperature increases, the threshold current also increases.

FEATURES:

- **Coherent:** There is no path difference between the waves comprising the beam
- **Monochromatic:** It consists of one wavelength and hence one color only.
- **Collimated:** Emitted light waves travel parallel to each other.

ADVANTAGES:

- Laser diodes are very compact.
- Relatively efficient when compared to gas lasers.
- Rugged and long life.

DISADVANTAGES:

- Optical performance is usually not equal to that of other laser types.
- Most laser diodes would not be suitable light sources for holography.
- The coherence length and monochromicity are likely to be inferior

APPLICATIONS:

- Medical equipment used in surgery

- Consumer products like optical disk equipment, laser printers, compact disc, players
- Laser diodes emitting visible light are used as pointers
- Laser diodes emitting visible and infrared light are used to measure range.

5. Write short notes on: Tunnel diode (OR) Explain the operation of Tunnel diode and its characteristics with diagram. (OR) What is mean by tunneling? Explain the VI characteristics of Tunnel diode using energy band diagram. (OR) Explain the construction and volt ampere characteristics of Tunnel diode (M/J-2015) (N/D-2015) (M/J-2016) (N/D-2016) (N/D-2017) (A/M-2018) (A/M-2019)

TUNNEL DIODE:

- Tunnel diode is a highly doped semiconductor device and is used mainly for low voltage high frequency switching applications.
- It works on the principle of Tunneling effect. It is also called as Esaki diode named after Leo Esaki, who in 1973 received the Nobel Prize in Physics for discovering the electron tunneling effect used in these diodes.
- Tunnel diode is the p-n junction device that exhibits negative resistance under low forward bias conditions. That means when the voltage is increased the current through it decreases.
- The tunnel diode is a two terminal device with p type semiconductor acting as anode and n type semiconductor as cathode. The circuit symbol of tunnel diode is shown.

- According to the classical laws of physics a charged particle sin order to cross an energy barrier should possess energy at least equal to the energy barrier. Hence the particle will cross the energy barrier if its energy is greater than the barrier and cannot cross the barrier if its energy is less than the energy barrier. But quantum mechanically there exists non zero probability that the particle with energy less than the energy barrier will cross the barrier as if it tunnels across the barrier. This is called as **Tunneling effect**.

V - I CHARACTERISTICS

- It is seen that at first forward current rises sharply as applied voltage is increased, where it would have risen slowly for an ordinary PN junction diode (which is shown as dashed line for comparison).

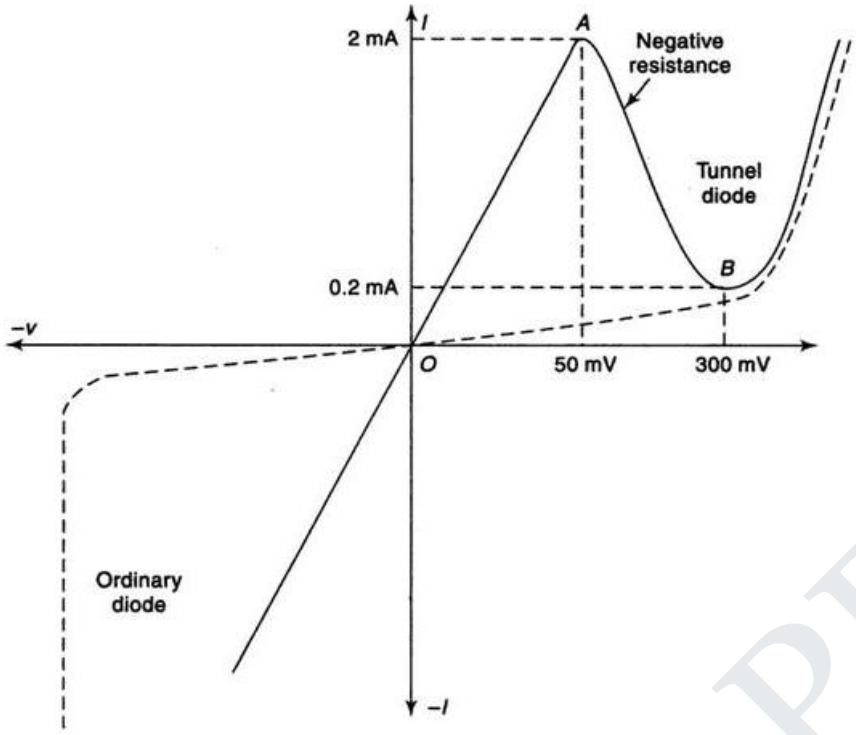
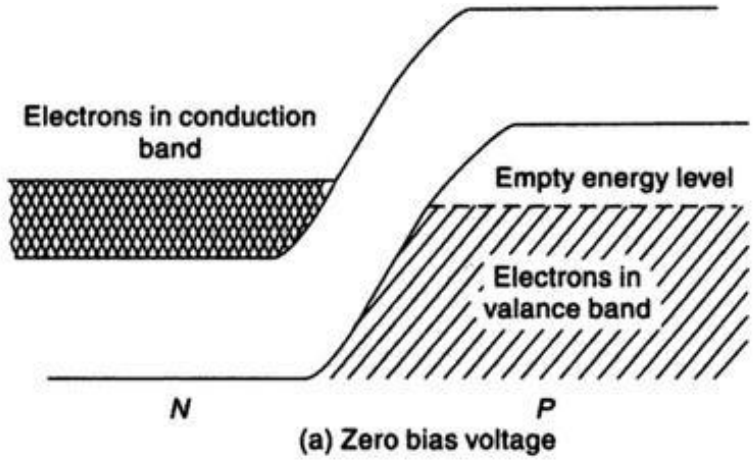


Fig. 5.21 *V–I characteristic of tunnel diode*

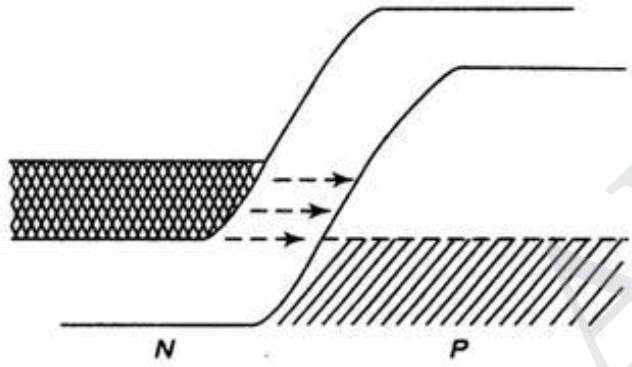
- The interesting portion of the characteristic starts at the point A on the curve, i.e. **the peak voltage**. As the forward bias is increased beyond this point, the forward current drops and continues to drop until point B is reached. This is the **valley voltage**. At B, the current starts to increase once again and does so very rapidly as bias is increased further.
- Beyond this point, characteristic resembles that of an ordinary diode. Apart from the peak voltage and valley voltage, the other two parameters normally used to specify the diode behaviour are the **peak current** and the **peak-to-valley current ratio**, which are 2 mA and 10 respectively, as shown. The V-I characteristic of the tunnel diode illustrates that it exhibits dynamic resistance between A and B.

ENERGYLEVEL:

- Figure shows energy level diagrams of the tunnel diode for three interesting bias levels. The shaded areas show the energy states occupied by electrons in the valence band, whereas the cross hatched regions represent energy states in the conduction band occupied by the electrons.
- When the bias is zero, these lines are at the same height. Unless energy is imparted to the electrons from some external source, the energy possessed by the electrons on the N—side of the junction is insufficient to permit them to climb over the junction barrier to reach the P-side.
- When a small forward bias is applied to the junction, the energy level of the P-side is lower as compared with the N-side. As shown in Fig.(b), electrons in the conduction band of the N-side see empty energy level on the P-side.

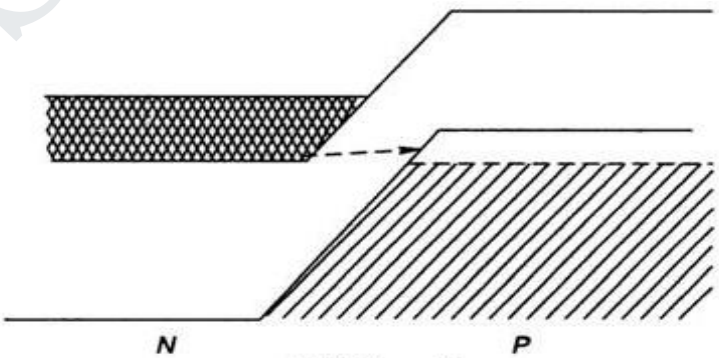


(a) Zero bias voltage



(b) Peak voltage

- Hence, tunneling from N-side to P-side takes place. Tunneling in other directions is not possible The energy band diagram shown in Fig.(b), is for the peak of the diode characteristic.
- When the forward bias is raised beyond this point, tunneling will decrease as shown in Fig.(c). The energy of the P-side is now depressed further, with the result that fewer conduction band electrons on the N-side are opposite to the unoccupied P-side energy levels.
- As the bias is raised, forward current drops. This corresponds to the negative resistance region of the diode characteristic. As forward bias is raised further it behaves as a normal PN junction diode.



(c) Valley voltage

Fig. 5.22 Energy level diagrams of tunnel diode

ADVANTAGES

- Low noise
- Ease of operation due to fact that tunnelling
- High speed
- Environmental immunity
- Low power dissipation

DISADVANTAGES

- Voltage range over which it can be operated is 1 V less
- Being a two terminal device, there is no isolation between the input and output circuit.

APPLICATIONS

- Tunnel diode is used as an ultra-high speed switch with switching speed of the order of ns or ps.
- As logic memory storage device
- As microwave oscillator
- In relaxation oscillator circuit
- As an amplifier.

6. Draw the VI characteristics of zener diode and explain its operation. (OR) Explain the VI characteristics of zener diode and distinguish between Avalanche and Zener Breakdown. (OR) With neat diagram explain the operation of zener diode and its characteristics and also brief how it can be used as a regulator. (M/J-2014) (N/D-2014) (N/D-2015) (N/D-2016) (M/J-2017) (N/D-2017) (A/M-2018)

ZENER DIODE:

- A zener diode is a special purpose diode that is operated in reverse biased condition. Its operation depends on the zener breakdown phenomenon.
- When a zener diode is operated in the breakdown region, it maintains a constant voltage across it. This property of a zener diode is utilized in regulators.
- A zener diode is also called a voltage reference, voltage regulator or break down diode. it is important in many power application .

Symbol

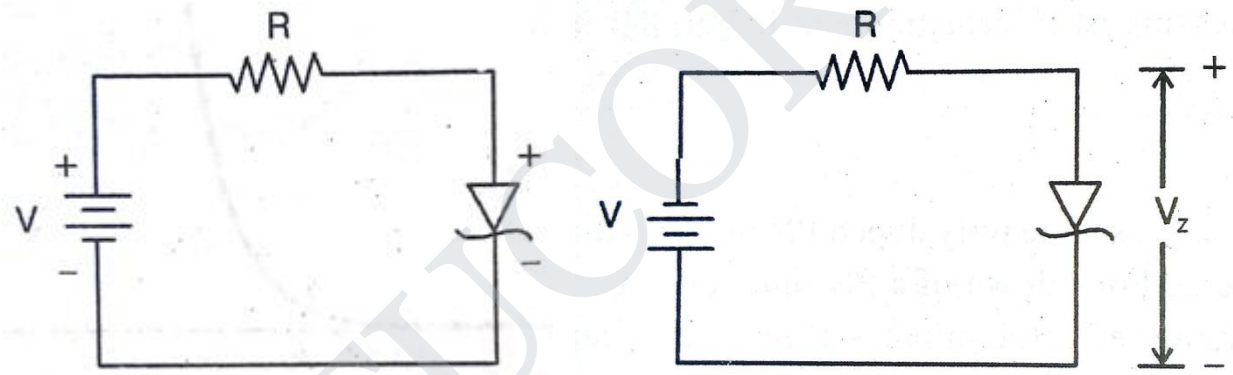
- The arrow head is the symbol points towards the conventional direction of current through the zener diode, when it is forward biased.
- In a reverse biased, heavily doped silicon or germanium PN junction diode that is operated in the break down region where current is limited by both external resistance and power dissipation of the diode. Silicon is preferred over germanium because of its higher temperature and current carrying capabilities .

WORKING OF ZENER DIODE:

- The conduction of any diodes depends on their biasing. There are two types of biasing:
  (i)Forward biasing (ii) Reverse biasing

(i)FORWARD BIASING:

- When the anode of the zener diode is connected to the positive terminal of the dc source and the cathode is connected to the negative terminal the zener diode is said to be forward biased.
- The forward biased zener diode behaves identical to a forward biased diode. The zener diode is generally not used in the forward biased condition.



(ii)REVERSE BIASING:

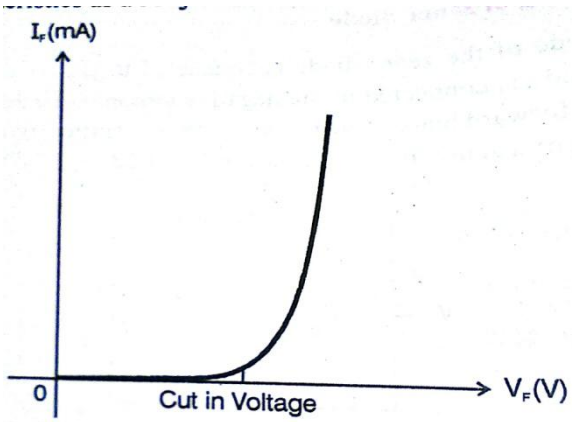
- When the anode of the zener diode is connected to the negative terminal of the dc source and the cathode is connected to the positive terminal, the zener diode is said to be reverse biased.
- The operation of zener diode in the reverse biased condition is different from that of a diode. Zener diode in the reverse biased condition is used as a voltage regulator.

VI CHARACTERISTICS:

- The V-I characteristics of a zener diode can be divide into two parts:
  - Forward characteristics

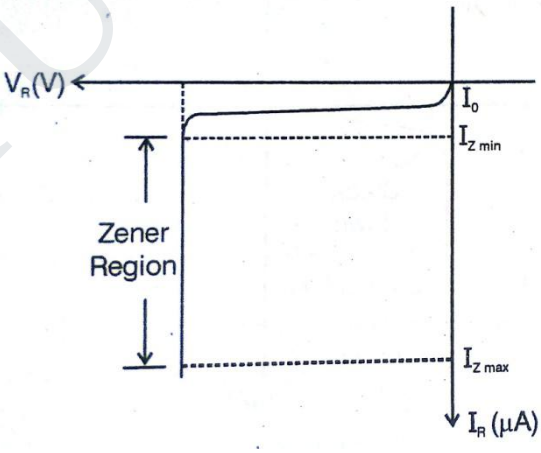
- Reverse characteristics

1.Forward characteristics: It is almost identical to the forward characteristics as a PN junction diode.



2. Reverse characteristics: As the reverse voltage is increased initially a small reverse saturation current I_o which is in micro amps will flow. This current flows due to the thermally generated minority carriers.

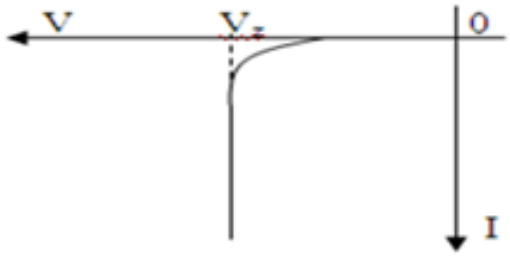
- At a certain value of reverse voltage, the reverse current will increase suddenly and sharply. This is the identification that the breakdown has occurred. This breakdown voltage is called as zener breakdown voltage or zener voltage and it is denoted by V_Z.
- After breakdown occurred, the voltage across zener diode remains constant equal to V_Z. Any increase in the source voltage will result in the increase in reverse zener current.



BREAKDOWN MECHANISM

- If the reverse bias voltage applied to a PN junction is increased, a point will reach when the junction breaksdown and reverses current rises sharply to a value limited only by external resistance connected in series with the junction.

- This specific value of the reverse bias voltage is known as **break down voltage**. The break down voltage depends upon the width of the depletion layer. The width of the depletion layer depends upon the doping level.



- Once break down has occurred, very little further increase in voltage is required to increase the current to relatively high values. The junction offers almost zero resistance at this point.
- There are two mechanisms are responsible for break down under increasing reverse voltage
    - Zener break down
    - Avalanche break down

ZENER BREAK DOWN:

- When the P and N regions are heavily doped, direct rupture of covalent bonds takes place because of strong electric field at the junction of PN diode.
- The new electron-hole pairs so created increase the reverse current in a reverse biased PN diode. The increase in current takes place at a constant value of reverse bias typically below 6V for heavy doped diodes.
- As a result of heavy doping of P and N regions, the depletion region width becomes very small and for an applied voltage of 6V or less, the field across the depletion region becomes very high of the order of 10^7 V/m making conditions suitable for Zener breakdown.

AVALANCHE BREAK DOWN:

- As the reverse bias increases, the field across the junction increases correspondingly. Thermally generated carriers while traversing the junction acquire a large amount of kinetic energy from this field.
- As a result the velocity of these carriers increases. These electrons disrupt covalent bond by colliding with immobile ions and create new electron-hole pair.
- This process is cumulative in nature and results in generation of avalanche of charge carriers within a short time.

- This mechanism of carrier generation is known as Avalanche multiplication. This process results in flow of large amount of current at the same value of reverse bias.

DISTINGUISH BETWEEN AVALANCHE AND ZENER BREAKDOWN:

ZENER BREAKDOWN	AVALANCHE BREAKDOWN
Breakdown occurs due to heavily doped junction and applied strong electric field	Breakdown occurs due to avalanche multiplication between thermally generated ions.
Doping level is high	Doping level is low
Breakdown occurs at lower voltage	Breakdown occurs at higher voltage
The breakdown voltage decreases with increase in the junction temperature.	The breakdown voltage increases with increase in the junction temperature.

NEED OF VOLTAGE REGULATORS:

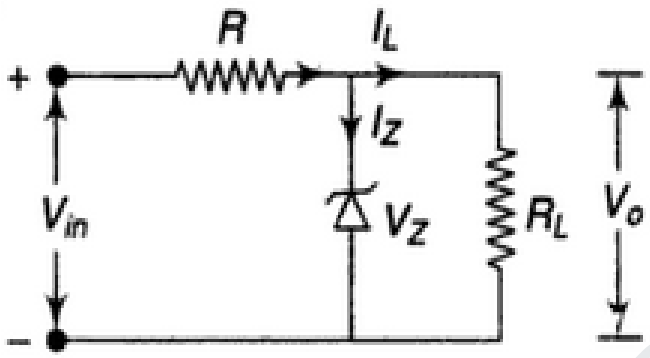
- All the electronic devices and circuits {i.e.. diodes, transistors, integrated circuits, etc.,) require a constant d.c voltage for their operation. The d..c voltage can be supplied using batteries or dry cells.
- But these are so expensive when compared with the conventional or traditional d.c power supplies. But, an ordinary (unregulated) power supply has the following, drawbacks:
  - Poor regulation.
  - The DC output voltage varies with the AC supply voltage which fluctuates at different times of the day and is different at different locations.
  - The DC output voltage varies with temperature semiconductors are used.
  - For certain applications the output of the filter even with small amount of ripple is not acceptable.

In order to overcome the above drawbacks, a ‘voltage regulator’ is to be used after the filter circuits.

- A voltage regulator is a circuit which makes the rectifier-filter output voltage constant regardless of the variations in the input voltage or load.
- A regulator is normally connected between an ‘filter’ and the ‘load’. The aim of the regulator circuit is to maintain a constant output.

ZENER REGULATOR:

- In the breakdown or zener region the voltage of a zener diode is substantially constant for large change of current through it. This characteristics of zener diode allows us to use it as a voltage regulator.



- Assume current I_L is to be supplied to the load R_L at constant voltage V_Z. In order to meet this requirements, connect a zener diode with zener voltage V_Z in shunt or parallel to the load resistor. Assume normal conditions current of I_Z flows through the zener diode.
- Therefore total current $I=I_L+I_Z$ flows through the current limiting resistors R_S.
  The input voltage $V_i=V_Z+IR_S$

$$V_i=V_Z+(I_L+I_Z)R_S$$

- Load current I_L increases the zener current I_Z decreases so that the total current I remains constant.

  The output voltage is $V_{out}=V_Z=Vi-IR_s$

- The output voltage remains unchanged.

OPTIMUM VALUE OF CURRENT LIMITING RESISTOR:

- The optimum value of the current limiting resistor can be determined by using the below equations,

$$I_{z\,(max)}=\frac{V_{i(max)-V_z}}{R_s}-I_{L(min)} \quad \text{.....(1)}$$

$$I_{z\,(min)}=\frac{V_{i(min)-V_z}}{R_s}-I_{L(max)} \quad \text{.....(2)}$$

From equation (1)

$$I_{z\,(max)}+I_{L(min)}=\frac{V_{i(max)-V_z}}{R_s}$$

$$R_{s(min)}=\frac{V_{i(max)-V_z}}{Iz\ (max)+ I_{L(min)}}$$

From equation (2)

$$I_{z\ (min)}+ I_{L(max)}=\frac{V_{i(min)-V_z}}{R_s}$$

$$R_{s(max)}=\frac{V_{i(min)-V_z}}{Iz\ (min)+ I_{L(max)}}$$

- The value of current limiting resistor R_S should be chosen in such a way that its value lies between $R_{s(max)}$ and $R_{s(min)}$

APPLICATIONS OF ZENER DIODE:

- It is used as a Voltage regulator.
- It is used as a Fixed reference voltage in transistor biasing circuits.
- It is used as a Peak clipper in wave shaping circuits.

7. Explain the VI characteristics of LDR (N/D-2016) (N/D-2017)

LDR:

- A *Light Dependent Resistor* (LDR) or a photo resistor is a device whose resistivity is a function of the incident electromagnetic radiation. Hence, they are light sensitive devices. They are also called as photo conductors, photo conductive cells or simply photocells.
- They are made up of semiconductor materials having high resistance. There are many different symbols used to indicate a **LDR**, one of the most commonly used symbol is shown in the figure below. The arrow indicates light falling on it.

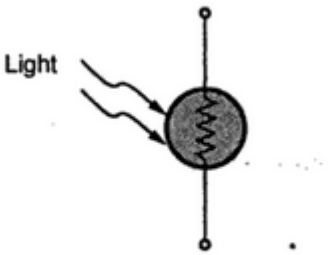
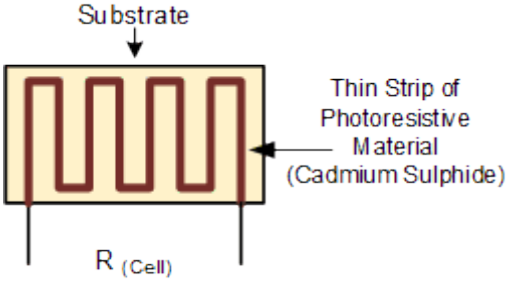


Fig. 5.95 Symbol



- As its name implies, the **Light Dependent Resistor** (LDR) is made from a piece of exposed semiconductor material such as cadmium sulphide that changes its electrical resistance from several thousand Ohms in the dark to only a few hundred Ohms when light falls upon it by creating hole-electron pairs in the material.

WORKING PRINCIPLE OF LDR:

- A light dependent resistor works on the principle of **photo conductivity**. Photo conductivity is an optical phenomenon in which the materials conductivity is increased when light is absorbed by the material.
- When light falls i.e. when the photons fall on the device, the electrons in the valence band of the semiconductor material are excited to the conduction band. These photons in the incident light should have energy greater than the band gap of the semiconductor material to make the electrons jump from the valence band to the conduction band.

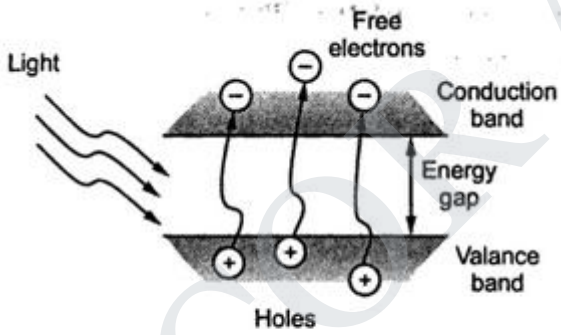


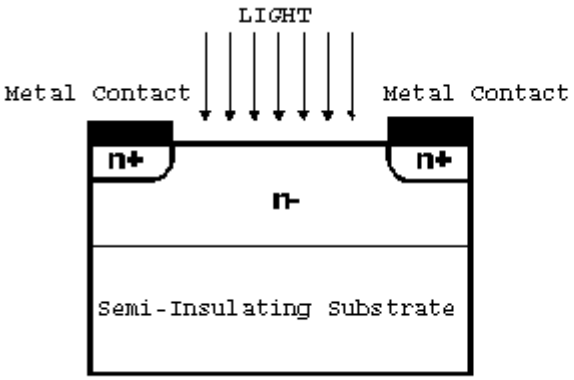
Fig. 5.94 Generation of charge carries due to light

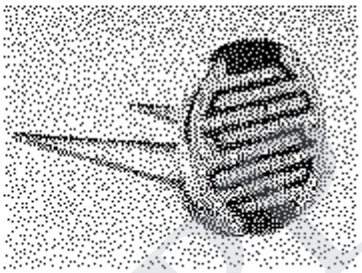
- Hence when light having enough energy strikes on the device, more and more electrons are excited to the conduction band which results in large number of charge carriers. The result of this process is more and more current starts flowing through the device when the circuit is closed and hence it is said that the resistance of the device has been decreased.

CONSTRUCTION:

- The structure of a light dependent resistor consists of a light sensitive material which is deposited on an insulating substrate such as ceramic. The material is deposited in zigzag pattern in order to obtain the desired resistance and power rating.
- This zigzag area separates the metal deposited areas into two regions. Then the ohmic contacts are made on the either sides of the area.

- The resistances of these contacts should be as less as possible to make sure that the resistance mainly changes due to the effect of light only.
- Materials normally used are cadmium sulphide, cadmium selenide, indium antimonide and cadmium sulphonide. The use of lead and cadmium is avoided as they are harmful to the environment.



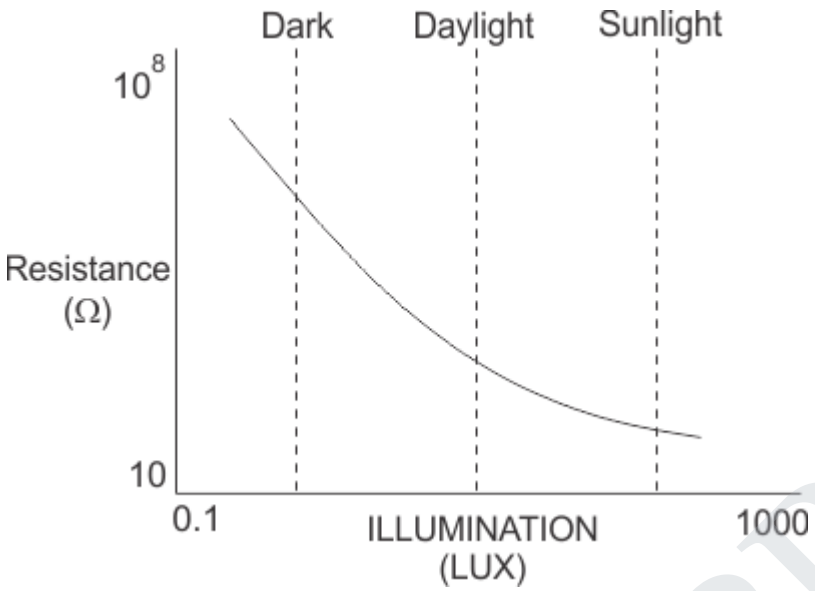


OPERATION

- A simple circuit for a photoconductive detector is shown in Fig. The semiconductor layer is enclosed in a sealed housing. A glass window in the housing permits light to fall on the active material of the cell.
- Here, the resistance of the photoconductive detector, in series with R, limits the amount of current I in the circuit. The ammeter A is used to measure the current I.
- When no light falls on the cell, its resistance is very high and the current I is low. Hence the voltage drop 1/0 across R is relatively low.
- When the cell is illuminated, its resistance becomes very low. Hence, current I increases and voltage V, increases. Thus, this simple circuit arrangement with slight modification can be used in control circuits to control the current.

CHARACTERISTICS OF LDR

- LDR's are light dependent devices whose resistance is decreased when light falls on them and that is increased in the dark. When a light dependent resistor is kept in dark, its resistance is very high. This resistance is called as dark resistance. It can be as high as 10^{12} Ω and
- if the device is allowed to absorb light its resistance will be decreased drastically. If a constant voltage is applied to it and intensity of light is increased the current starts increasing. Figure below shows resistance vs. illumination curve for a particular **LDR**.



ADVANTAGES

- LDR's are cheap
- Readily available in many sizes and shapes.
- They need very small power and voltage for its operation

APPLICATIONS OF LDR

- The detector is used either as an ON/OFF device to detect the presence or absence of a light source which is used for automatic street lighting
- it is used to measure a fixed amount of illumination and to record a modulating light intensity.
- It is used in counting systems where the objects on a conveyor belt interrupt a fight beam to produce a series of pulses which operates a counter.
- When the day light has faded to a given level, the corresponding resistance of the detector causes another circuit to switch ON the required lights.
- It is widely used in cameras to control shutter opening during the flash.

8. With relevant sketches explain the working mechanisms of Gallium Arsenic Devices. (N/D-2017)

GALLIUM ARSENIDE DEVICES

- Gallium arsenide is a compound semiconductor made of a compound of two elements. Gallium having three valence electrons can be combined with arsenic, which has five valence electrons to form the compound GaAs. Figure shows the arrangement of atoms in a gallium arsenide substrate.

Fig. 19.36 Arrangement of atoms in GaAs

- The gallium and arsenic atoms are alternatively positioned in exact crystallographic locations. Being a binary semiconductor, GaAs requires special care to avoid high temperatures during processing to prevent dissociation of the surface. This is one of the basic difficulties in the growth of bulk GaAs material.

ENERGY BAND STRUCTURE

- Gallium arsenide is a direct gap semiconductor, with its valence band maximum and conduction band minimum occuring at the same wave vectors.
- This means little momentum change is necessary for transition of an electron from the conduction band to the valence band. This property makes the GaAs an excellent light-emitting diode.
- For the GaAs effective mass of the electrons traveling through the crystal is 0.067 times the mass of a free electron. This means electrons travel faster in gallium arsenide than in silicon.
- Gallium arsenide has a superior electron mobility characteristic because of the shapes of their conduction bands as shown in Fig.

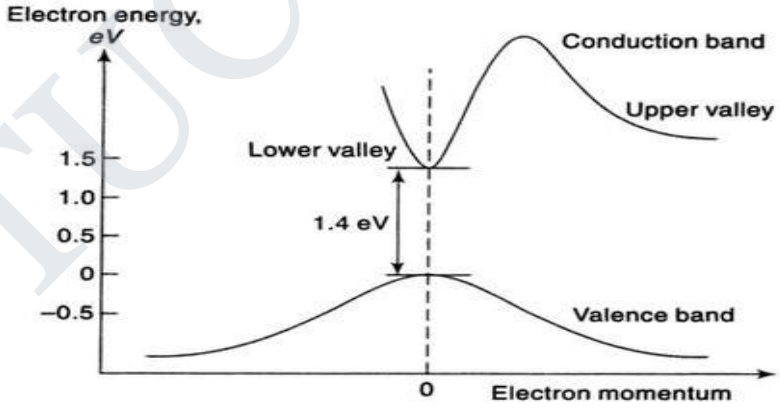


Fig. 19.38 Energy band structure of GaAs

GaAS TECHNOLOGY

As a result of considerable development in GaAs integrated circuitry and the technology, GaAs devices are widely gaining popularity. The GaAs devices provide the following typical characteristics:

- less than one-micron gate geometry

- less than two-micron metal pitch
- up to four-layer metal
- ON and OFF devices
- Four-inch diameter wafers
- Suitability for clock rates in the range of 1-2 GHz.

The salient features of this technology include:

- Improved electron mobility over the silicon technology, resulting in very fast electron transit times.
- The saturation velocity for GaAs occurs at a lower threshold filled than for silicon.
- Large energy band gap offers bulk semi-insulating substrate with resistivity in the order of hundreds to thousands of megaohms-cm.
- GaAs devices operate over a wider temperature range (-200 to +200°C)
- Direct bandgap allows GaAs to be used as light emitters.
- Less power dissipation compared to silicon technology.

GALLIUM ARSENIDE DEVICES

A number of devices have been developed in the last few years using GaAs technology, which includes:

- Depletion-mode metal semiconductor field-effect transistor, D-MESFET
- Enhancement-mode metal semiconductor field-effect transistor, E-MESFET
- Enhancement-mode junction field-effect transistor, E-JFET and
- Complementary enhancement-mode junction field-effect transistor, CE-JFET.

The first generation devices developed using GaAs technology exhibits switching delays as low as 70 p sec to 80 p sec while dissipating power of the order of 1.5 mW to 150 microwatts.

9. Discuss about FINFET and Dual Gate MOSFET. (OR) Describe the concept of Dual Gate MOSFET (A/M-2014) (A/M-2015) (A/M-16) (N/D-16)

DUAL GATE MOSFET

- The dual gate MOSFET is an n channel enhancement type, dual insulated gate, field effect transistor that utilizes MOS construction.
- Dual gate MOSFET comprises of a conducting channel, surrounded by gate electrodes on either side. It has second separate insulated gate. This ensures that no part of the channel is far away from a gate electrode.

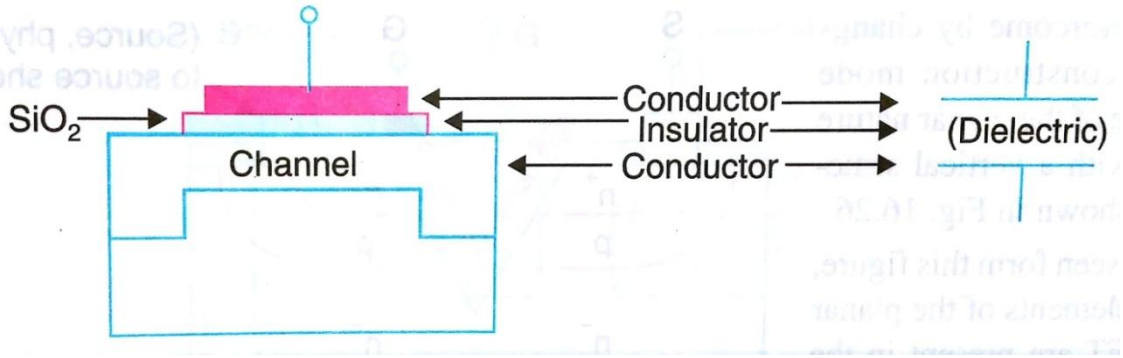
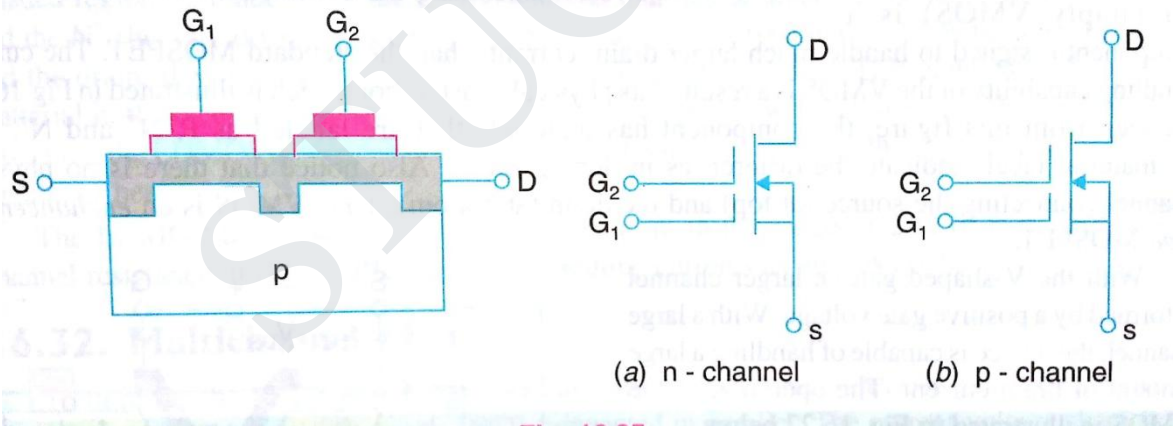


plate that is used for the gate is a conductor.

- The silicon dioxide between the gate and the channel in an insulator. The channel itself can be viewed as being a conductor to the silicon dioxide layer.
- Thus the combination of the three forms a parallel-plate capacitor. The capacitance offered by this parallel plate capacitor can be reduced by employing a dual gate MOSFET structure. The physical construction and schematic symbols for the dual-gate MOSFET are shown in Fig.
- The reduced capacitance of the dual-gate MOSFET is the result of the way in which the component is used. Normally the component is used in such a way as to act as two series-connected MOSFETs.
- When the dual gate MOSFET is used as series MOSFETs, the effect is similar to connecting two capacitors in series.



- Recall that the total capacitance in a series connection is lower than either individual component value. Thus by connecting the two gates in a series configuration, the overall capacitance is reduced.
- This allows the dual-gate MOSFET to have a better high-frequency response as compared to a normal MOSFET.

ADVANTAGES

- Reduction of leakage current.
- Better control of short channel effects.
- Higher current drive capability because of double gate.
- Low noise.
- High-gain and high frequency amplifiers because of their low feedback capacitance and high transconductance.

APPLICATIONS

- Used as mixer in RF circuits.
- Used as a RF amplifier.
- Used in Automatic Gain Control (AGC).

FINFET

- The basic electrical layout and the mode of operation of a FINFET does not differ from a traditional field effect transistor. There is one source and one drain contact a swell as a gate to control the current flow.
- In contrast to planar MOSFETs the channel between source and drain is build as a three dimensional bar on top of the silicon substrate, called fin.
- The gate electrode is then wrapped around the channel, so that there can be formed several gate electrodes on each side which leads to reduced leakage effects and an enhanced drive current.
- FINFET technology takes its name from the fact that the FET structure used looks like a set of fins when viewed.
- The FINFET transistors employ a single gate stacked on top of two vertical gates allowing for essentially three times the surface area for electrons to travel. Figure shows the cross-section of FINFET.

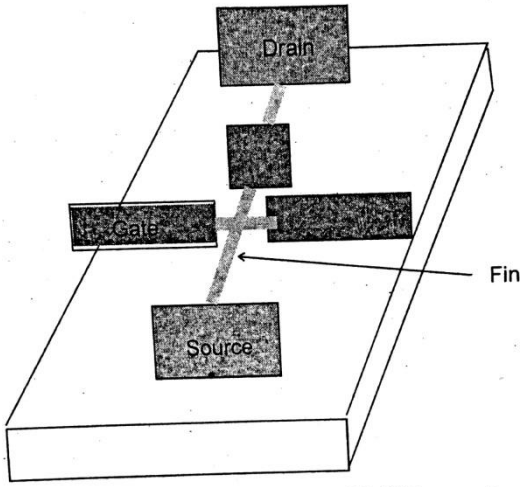


Fig. 4.9 : Cross section of FinFET

- The FINFFT is designed to address shortcomings due to short channel effects by wrapping the gate around the conducting channel instead of having it laid on the top of transistor.
- The characteristic of the FINFET is that the conducting channel is covered by a thin silicon fin, which forms the body of the device. The thickness of the fin determines the effective channel length of the device.
- The FINFET cross-section indicates that the gate is on both sides and the top of the fin. This means that it wraps the conducting channel on both sides and at the top. The gate controls this thin body more than one side providing better control over the channel.
- Hence, only very little current is allowed to leak through the body. As a result, it results in higher switching speed and power.

ADVANTAGES OF FINFET

- Provides better electrostatic control over the channel.
- Reduces short channel effects.
- Excellent control of short channel effects makes transistors still scalable.
- Much lower leakage current (I_{off})
- Higher drain current.

APPLICATIONS

- Low power design in digital circuit, such as RAM, because of its low off-state (leakage) current.
- Power amplifier or other application in analog area which requires good linearity.

EC8252- ELECTRONIC DEVICES

I YEAR / II SEMESTER B.E. (ME)

UNIT – V

POWER DEVICES AND DISPLAY DEVICES

COMPILED BY

V. KAVITHA M.E., (AP/ME)

VERIFIED BY

HOD **PRINCIPAL** **CORRESPONDENT**

DEPARTMENT OF MEDICAL ELECTRONICS

SENGUNTHAR COLLEGE OF ENGINEERING – TIRUCHENGODE

UNIT – V

POWER DEVICES AND DISPLAY DEVICES

- **UJT**
- **SCR**
- Diac,Triac
- Power BJT
- Power MOSFET - DMOS,VMOS
- **LED, LCD**
- **Photo transistor**
- **Opto Coupler**
- **Solar cell**
- **CCD .**

LIST OF IMPORTANT QUESTIONS

UNIT V – POWER DEVICES AND DISPLAY DEVICES

PART – A

1. **Mention the types of LCD's. (N/D-2019)**
2. **What is an optocoupler and where it is used. (N/D-2019)**
3. **Define an intrinsic standoff ratio of UJT and draw its equivalent circuit. (A/M-19)**
4. **Define Quantum efficiency in an LED (A/M-19)**
5. **What is the effect of temperature in Solar cell? (A/M 2018)**
6. **Draw the basic structure of TRIAC and its symbol. (M/J 2014) (A/M 2018)**
7. **State the differences between DIAC and TRIAC (N/D 2017)**
8. **Define conversion efficiency of solar cell. (N/D 2017)**
9. **Give the Symbol, structure and equivalent circuit of DIAC. (N/D 2016) (M/J 2017)**
10. **Define Holding current (M/J 2017)**
11. **Compare SCR and TRIAC (N/D 2016)**
12. **What is mean by regenerative action of SCR (M/J 2016)**

PART – B

1. Explain the operation, characteristics and applications of SCR. (OR) Explain the operation of SCR with structural diagram and draw the characteristics for a SCR. (OR) Explain the operation and of V-I characteristics of SCR. (OR) Draw the transistor model of an SCR and Describe the operation of SCR with V-I characteristics for a SCR. (OR) Discuss the V-I characteristics of SCR also explain with neat circuit how it can used as Battery charging regulator and temperature controller. (M/J 2014) (N/D 2015) (N/D 2016) (M/J 2017) (M/J 2018) (N/D 2017) (N/D 2019)

2. Give the construction details of UJT & explain its operation with the help of equivalent circuits. (OR) Explain how UJT function as Relaxation Oscillator. (OR) Draw the basic structure of UJT & explain V-I characteristics of UJT with equivalent circuits. (N/D 2014) (N/D 2015) (M/J 2016) (N/D 2019)

3. Explain the Construction and operation of LED/ Outline the theory of light generation in light emitting diode, with necessary expressions for internal and external quantum efficiencies / An indicator requires Voltage to be displayed in seven segment format. However, the power requirement for the display should be very low. Choose a proper display device and justify your choice. Also indicate the characteristics and operating principle of such a display device (A/M-2019) (A/M-2018)

4. Write Shot notes on: (i)Solar cell (M/J 2014) (N/D 2017)
(ii)CCD(M/J 2014) (M/J 2015) (N/D 14,2015) (N/D 2017)
(iii)LCD (OR) Explain the Construction and operation of LCD (N/D 2016) (M/J 2015)(N/D 2015) (M/J 2017)

5. Write Shot notes on: (i)Optocoupers (N/D 2014) (M/J 2017) (N/D 2017)
(ii)Photo transistor (OR) Describe the working of Photo transistor (N/D 2014,16,17)

6. Write Shot notes on: (i)Power BJT (M/J 2015)
(ii)Power MOSFET (OR) Explain the working and characteristics of DMOS (M/J 2015) (N/D 2016)

PART – A

1. Mention the types of LCD's. (N/D-2019)

- Dynamic scattering Displays.
- Twisted nematic display (or) Field effect display

2. What is an optocoupler and where it is used. (N/D-2019)

Optocopuler is an electronic component, that transfer electrical signals between two isolated circuits by using light

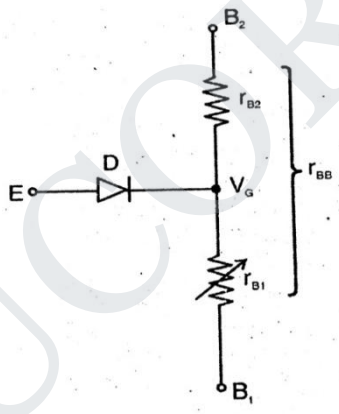
- ❖ Mainly used to isolate two circuits
- ❖ AC detection
- ❖ DC control returned operations

3. Define an intrinsic standoff ratio of UJT and draw its equivalent circuit. (A/M-19)

The resistance ratio r_{B1} / r_{BB} is known as intrinsic standoff ratio and is designated by,

$$\eta = r_{B1} / r_{BB} = r_{B1} / (r_{B1} + r_{B2})$$

The value of η is between 0.5 and 0.8



Equivalent circuit.

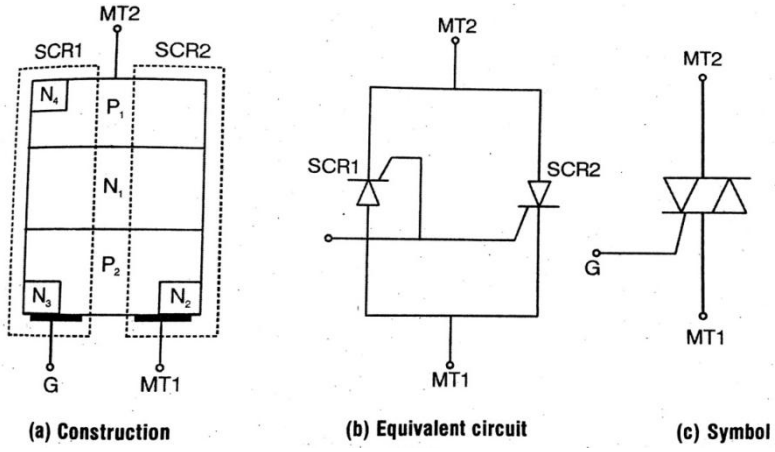
4. Define Quantum efficiency in an LED (A/M-19)

The fraction of the electrons that are injected into the depletion layer which results in photons getting produced is known as internal Quantum efficiency of the LED

5. What is the effect of temperature in Solar cell? (A/M 2018)

As the **temperatures** of the **solar cells** rise above 25 degrees Celsius, the current rises very slightly, but the voltage decreases more rapidly. The net **effect** is a decrease in output power with increasing **temperature**. Typical silicon **solar panels** have a **temperature** coefficient of about -0.4 to -0.5 percent.

6. Draw the basic structure of TRIAC and its symbol. (M/J 2014) (A/M 2018)



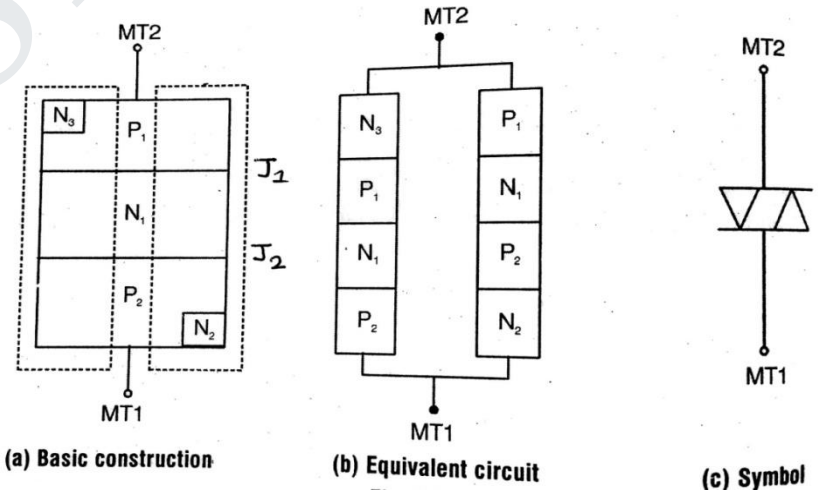
7. State the differences between DIAC and TRIAC (N/D 2017)

DIAC	TRIAC
DIAC is diode AC switch	TRIAC is triode AC switch
It has 2 terminals main terminal-1 and main terminal-2	It has 3 terminal main terminal-1, main terminal-2 and gate
The DIAC consists of two 4 layer diodes connected in parallel but in opposite directions.	The TRIAC behaves like two SCRs connected in parallel but in opposite directions.

8. Define conversion efficiency of solar cell. (N/D 2017)

- The efficiency of the solar cell is measured by the ratio of electric energy output to the light energy input expressed as a percentage. At present, efficiency in the range of 10 to 40% is obtained.
- Efficiency = electric energy output / light energy input

9. Give the Symbol, structure and equivalent circuit of DIAC. (N/D 2016) (M/J 2017)



10. Define Holding current (M/J 2017)

- It is the value of anode current below which the SCR switches from its ON position to OFF position under the given conditions.
- In other words holding current is the minimum value of current required to maintain conduction (to hold the device in ON state). It is denoted by I_H
- For turning the device OFF, the anode current should be lowered below I_H

11. Compare SCR and TRIAC (N/D 2016)

SCR	TRIAC
SCR is silicon controlled rectifier	TRIAC is triode AC switch
It has 3 terminal anode, cathode and gate	It has 3 terminal main terminal-1, main terminal-2 and gate
SCR is unidirectional control Device. It can conduct current in forward direction only	TRIAC is bidirectional control Device. It can conduct current in forward as well as reverse direction.
It can be triggered with positive Pulse applied at gate terminal.	It can be triggered by a pulse of either positive (or) negative polarity applied at gate terminal.
SCRs are available with a large current rating	TRIACs are available for lower current rating

12. What is mean by regenerative action of SCR (M/J 2016)

i.e. $$I_A = \left[\frac{\alpha_2 I_g}{1-(\alpha_1 + \alpha_2)}\right] \quad (8.6)$$

Equation (8.6) indicates that if $(\alpha_1 + \alpha_2) = 1$, then $I_A = \infty$, i.e. the anode current I_A suddenly reaches a very high value approaching infinity. Therefore, the device suddenly triggers into ON state from the original OFF state. This characteristic of the device is known as its *regenerative action.*

13. Mention some advantages and disadvantages of LCD (M/J 2016)

ADVANTAGES OF LCD

- Less power consumption
- Low cost
- Uniform brightness with good contrast
- Low operating voltage and current

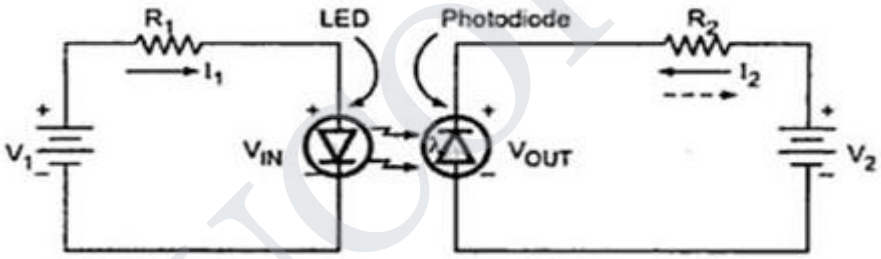
DISADVANTAGES OF LCD

- Poor reliability
- Limited temperature range
- Poor visibility in low ambient temperature
- Slow speed
- Requires an a.c. drive.

14. What is the name implies VMOS? (N/D 2015)

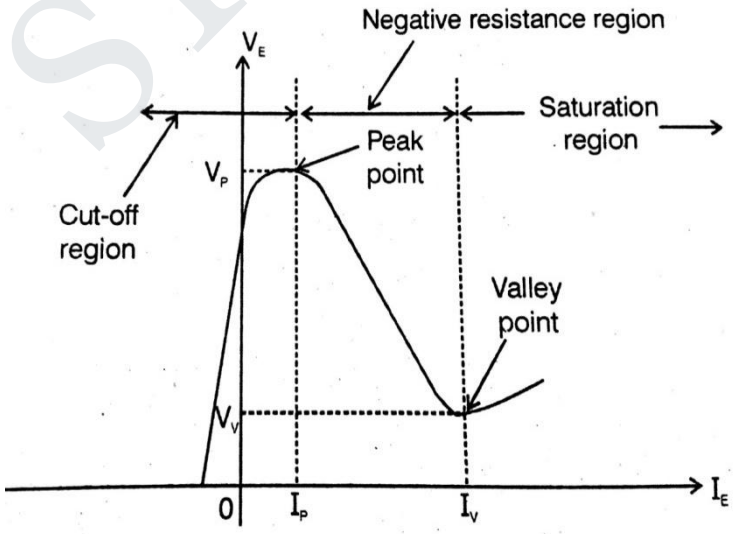
- A VMOS transistor is a type of metal oxide semiconductor transistor. VMOS is also used for describing the V-groove shape vertically cut into the substrate material.
- VMOS is an acronym for **"vertical metal oxide semiconductor", or "V-groove MOS**".
- The "V" shape of the MOSFET's gate allows the device to deliver a higher amount of current from the source to the drain of the device. The shape of the depletion region creates a wider channel, allowing more current to flow through it.

15. Draw the circuit diagram of Optocoupler (N/D 2015)



Optocoupler

16. Sketch the V- I characteristics of an UJT. (A/M-2015)



VI characteristics of UJT

- There are two important points on the characteristics curve namely peak point and the valley point. These points divide the curve into three important regions:
  (i)Cut-off region

  (ii)Negative resistance region

  (iii)Saturation region

17. A solar cell is a PN junction device with no voltage directly applied across the junction if it is so how does a solar cell deliver power to a load? (A/M-2015)

- A solar cell (also called a photovoltaic cell) is an electrical device that converts the energy of light directly into electricity by the photovoltaic effect. It Works as follows:
- Photons in sunlight hit the solar panel and are absorbed by semiconducting materials, such as silicon.
- Electrons (negatively charged) are knocked loose from their atoms, causing an electric potential difference. Current starts flowing through the material to cancel the potential and this electricity is captured. Due to the special composition of solar cells, the electrons are only allowed to move in a single direction.
- An array of solar cells converts solar energy into a usable amount of direct current (DC) electricity.

18. Draw the two transistor equivalent circuit of an SCR (N/D-2014)

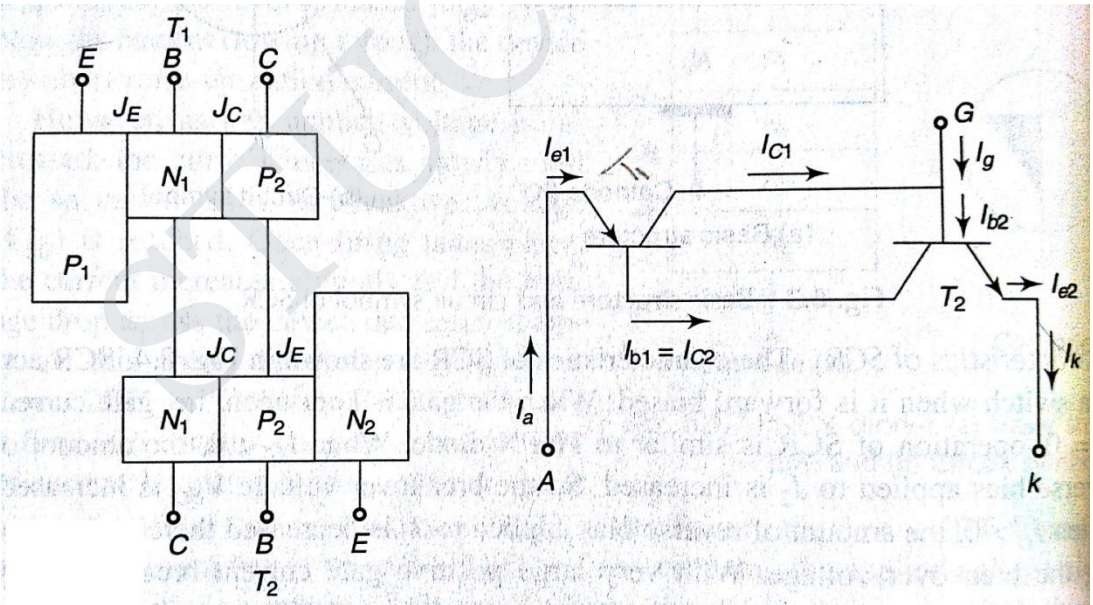
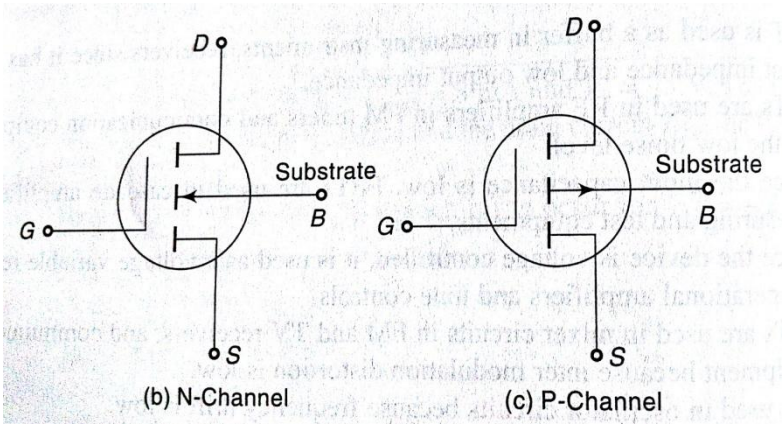
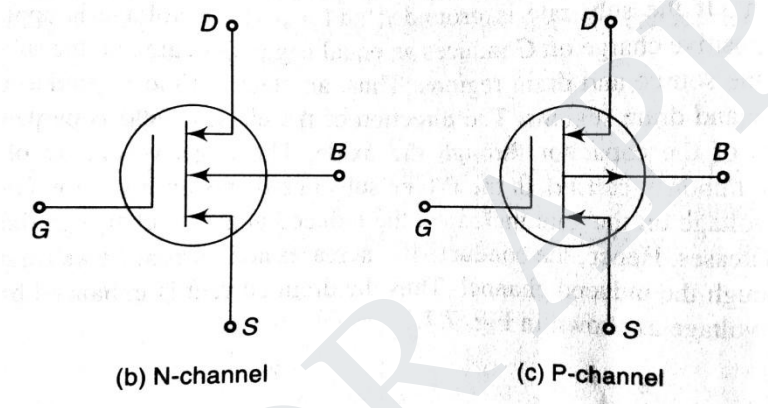


Fig. Two transistor version of SCR

19. Sketch the graph symbol for n channel and p channel MOSFET? (N/D-2014)



Symbols for Enhancement MOSFET



Symbols for Depletion MOSFET

20. Write down the significance of opto coupler (M/J-2014)

- In electronics, an opto-isolator, also called an optocoupler, photocoupler, or optical isolator, is a component that transfers electrical signals between two isolated circuits by using light.
- Opto-isolators prevent high voltages from affecting the system receiving the signal. Commercially available opto-isolators withstand input-to-output voltages up to 10 kV and voltage transients with speeds up to 10 kV/μs.
- The combined package of a LED and a photodiode is called an optocoupler

21. Distinguish between LED and LCD.

LED	LCD
It consumes more power(in mW).	It consumes less power. (in μW).
Life time is more.	Life time is less.
High cost.	Low cost.
Capable of generating its	Requires an external (or)

own light.	internal light source.
Emitting colour depends upon the materials used.	Monochrome in nature.
LED is an active display device.	LCD is an passive display device
Applications • 7 segment display • Indicator • Matrix displays	Applications • 7 segment display • Calculators, Pages and Wrist watch • Flat panel display • Alpha numeric display

22. What are the types of display devices?

(i)Active display devices – These are the display units which modulates emit the light radiation on their own.

Example : Light Emitting Diode (LED)

(ii)Passive display devices – These are the display units which modulate the incident radiation and then gives

the display information. Example : Liquid Crystal Display (LCD)

23. What is Latching current?

- The latching current is defined as the minimum value of anode current which it must attain during turn on process to maintain conduction when gate signal is removed.
- In other words latching current is the minimum current required to latch or trigger the device from its OFF state to its ON state.

24. What is forward breakover voltage?

- SCR is forward bias with a small voltage, it is in OFF and no current flows through the SCR.
- The applied forward voltage is increased, a certain critical voltage called forward breakover voltage.

25. Difference between Power Transistor (BJT) and Power MOSFET.

S.No	*Power Transistor*	*Power MOSFET*
1.	Switching speed is reletively less than power MOSFET.	Fast switching time.
2.	Two break down occurs.	No second breakdown.
3.	Should operate in safe operating region.	Stable gain. Should operate in safe operating region.
4.	Variation of g_m with temperature is reletively high.	Variation g_m with temperature is less.
5.	Thermal runaway problem will occur hence heaksink may be required.	No thermal runaway problem.
6.	Current gain is small.	Input impedance is extremely large.
7.	Larger junction capacitance and lower cut off frequency.	Large currents can be controlled by small gate current.
8.	Large driver circuit is required to operate power BJT.	Driver circuit is simples.

PART – B

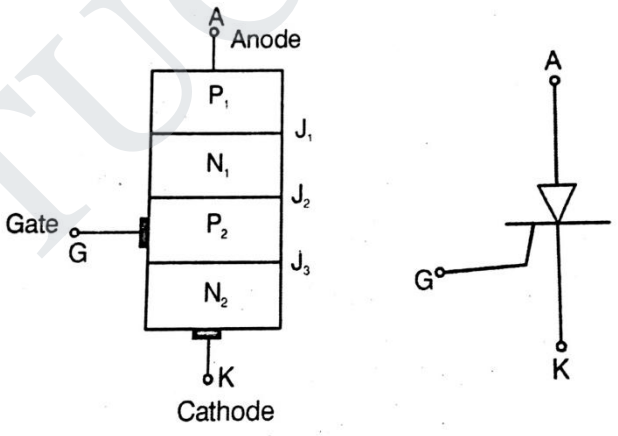
1. Explain the operation, characteristics and applications of SCR. (OR) Explain the operation of SCR with structural diagram and draw the characteristics for a SCR. (OR) Explain the operation and of V-I characteristics of SCR. (OR) Draw the transistor model of an SCR and Describe the operation of SCR with V-I characteristics for a SCR. (OR) Discuss the V-I characteristics of SCR also explain with neat circuit how it can used as Battery charging regulator and temperature controller. (M/J 2014) (N/D 2015) (N/D 2016) (M/J 2017) (M/J 2018) (N/D 2017) (N/D 2019)

SILICON CONTROLLED RECTIFIER (SCR):

- The SCR is an unidirectional device and like diode, it allows to flow current in only one direction. It is a family of four layer PNPN devices. SCR is also known as thyristors.
- SCR is a rectifier constructed of silicon material with a third terminal for control purposes. Silicon is chosen because of its high temperature and power capabilities.

CONSTRUCTION:

- SCR consists of four semiconductor layers forming a PNPN structure. It has three PN junctions namely J_1,J_2 and J_3.
- There are three terminals. The Anode terminal (A) is taken out from the P_1 layer. The Cathode (K) terminal is taken out from the N_2 layer and the Gate (G) terminal from the P_2 layer.



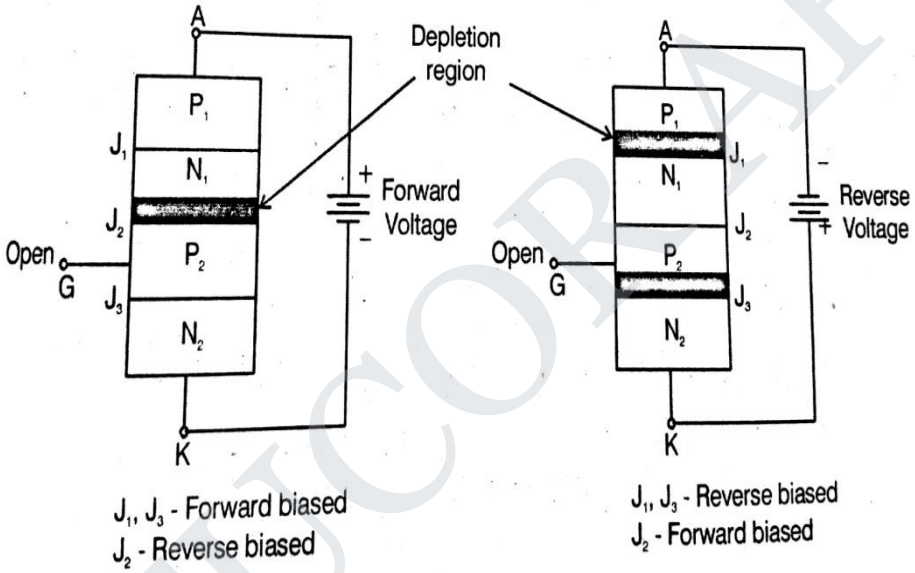
(a) Construction, (b) Symbol

- As leakage current in silicon is very small compared to Germanium, SCRs are made of Silicon and not Germanium.

OPERATION

(i)When gate is open:

- Consider that the anode is positive with respect to cathode and gate is open, the junctions J_1 and J_3 are forward biased and junction J_2 is reverse biased.
- There is depletion region around J_2 and only leakage current flows which is small. The SCR is said to be OFF. This is called **forward blocking state** of SCR and voltage applied to anode and cathode is called forward voltage.
- With gate is open, if cathode is made positive with respect to anode, the junctions J_1 and J3 are reverse biased and junction J_2 is forward biased. Still, the current flowing is leakage current which can be neglected as it is very small. The voltage applied to make cathode positive is called reverse voltage and SCR is said to be in **reverse blocking state**.

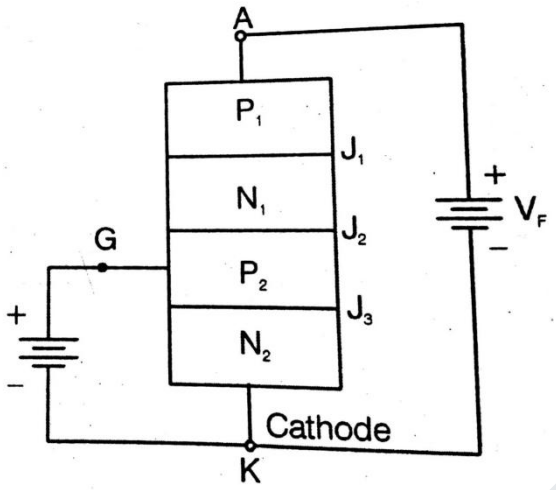


- In the forward blocking state, if the applied voltage is increased the current increases slowly until the break over voltage (V_{BO}) is reached. Once V_{BO} is reached, the current abruptly increases and the voltage drop across the device decreases sharply.
- At this point, the diode switches over from 'OFF' to 'ON' state. Once the device is fired into the conduction, a minimum amount of current known as **holding current** I_H is required to flow to keep the device in ON state.

(ii)When gate is closed:

- When the gate is made positive with respect to the cathode, the electrons from n-type cathode which are majority in number, cross the junction J_3 to reach to positive of battery,

- While the holes from P-type move towards the negative of battery. This constitutes the gate current. This current increases the anode current as some of the electrons cross junction J_2.



- As anode current increases, more electrons cross the Junction J_2 and the anode current further increases. Due to regenerative action within short time, the junction J_2 breaks an SCR conducts heavily.
- If the anode to cathode voltage is reversed, then the device enters into the reverse blocking region. The current is negligibly small.
- If the reverse voltage is increased, at a particular value avalanche breakdown occurs and a large current flows through the device. This is called **reverse breakdown** and the voltage at which this happens is called reverse breakdown voltage

EQUIVALENT CIRCUIT OF SCR USING TRANSISTOR:

- The operation of SCR can be explained in a very simple way by considering it in terms of two transistors called as the two transistor version of SCR.
- An SCR can be split into two parts and displaced mechanically from one another but connected electrically. Thus the device may be considered to be constituted by two transistors T_1 (PNP) and T_2 (NPN) connected back to back.

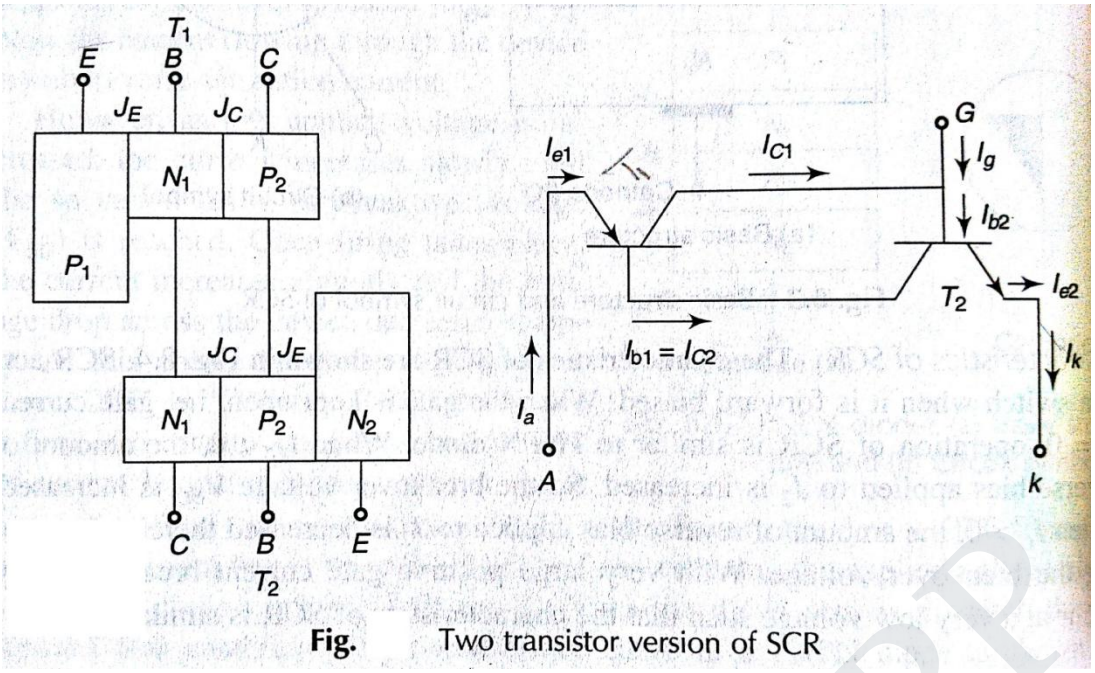


Fig. Two transistor version of SCR

Assuming the leakage current of T_1 to be negligibly small, we obtain

$$I_{b1} = I_A - I_{e1} = I_A - \alpha_1 I_A = (1 - \alpha_1)\, I_A \qquad 1$$

Also, from the Fig. it is clear that

$$I_{b1} = I_{C2} \qquad 2$$

and

$$I_{C2} = \alpha_2 I_K \qquad 3$$

Substituting the values given in Eqs 2 and 3 in Eq. 1 we get

$$(1 - \alpha_1)\, I_A = \alpha_2 I_K \qquad 4$$

We know that

$$I_K = I_A + I_g \qquad 5$$

Substituting Eq. 5 in Eq. 4 we obtain

$$(1 - \alpha_1)\, I_A = \alpha_2 (I_A + I_g)$$

i.e.

$$(1 - \alpha_1 - \alpha_2) I_A = \alpha_2 I_g$$

i.e.

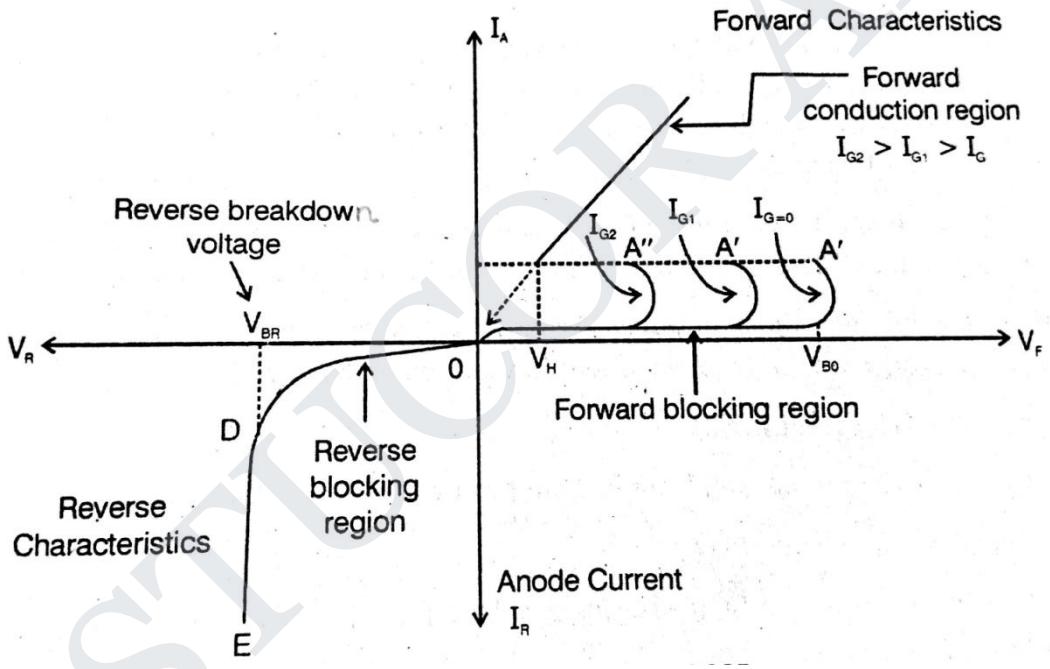
$$I_A = \left[\frac{\alpha_2 I_g}{1 - (\alpha_1 + \alpha_2)}\right] \qquad 6$$

Equation 6 indicates that if $(\alpha_1 + \alpha_2) = 1$, then $I_A = \infty$, i.e. the anode current I_A suddenly reaches a very high value approaching infinity. Therefore, the device suddenly triggers into ON state from the original OFF state. This characteristic of the device is known as its *regenerative action.*

V – I CHARACTERISTICS OF SCR:

FORWARD CHARACTERISTICS

- As the applied anode-to-cathode voltage (V_{AK}) increases above zero, a very little anode current flows through the device. Under this condition, the SCR is OFF. It continues till the voltage V_{AK} reaches the forward break over voltage marked by point A.
- As the V_{AK} exceeds the break over voltage the SCR turns ON and the anode-to-cathode voltage decreases quickly to a value marked by point B. At this stage, the current through the SCR increases rapidly to a large value.
- The current corresponding to the point B is called the holding current (I_D). It is the-minimum value of anode current to keep the SCR in ON state. If the anode current falls below the value of holding current, the SCR turns OFF.
- As the value of gate current (I_G) is increased above zero, the SCR turns ON at lower break over voltages as indicated by the points marked A' and A".



- The region lying between the points O and A is called **forward blocking region**. In this region, the SCR is OFF and blocks the forward anode-to-cathode voltage.
- The region lying between the points O and A is called **forward conduction region**. Il this region, the SCR is ON and conducts current.

REVERSE CHARACTERISTICS:

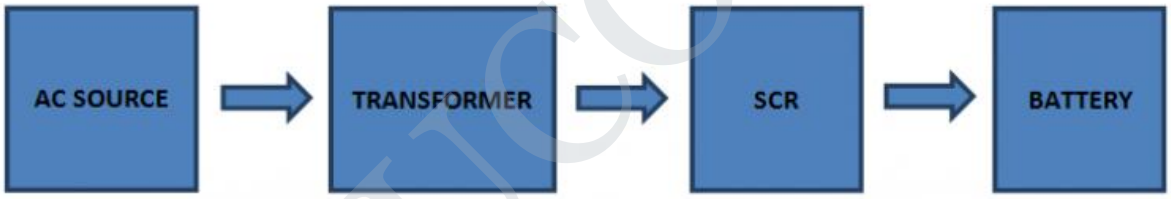
- As the applied reverse voltage (V_R) is increased above zero, a very little current (called leakage current) flows through the SCR. Under this condition, the SCR is OFF, It continues till the applied reverse voltage reaches breakdown voltage (V_{BR})

- As the applied reverse voltage is increased above the breakdown voltage, the reverse current increases more rapidly as shown by the curve DE. This rapid increase is because of the breakdown of SCR (due to avalanche effect) and may damage the device if the current exceeds the rated value.
- The region lying between the points O and D is called **reverse blocking region**. In this region, the SCR is OFF. Therefore it blocks the reverse anode-to-cathode voltage.
- The region lying between the points D and E is called reverse avalanche region. In this region, a large value of reverse current flows through the device.

BATTERY CHARGER CIRCUIT USING SCR

- The battery is charged with small amount of AC voltage or DC voltage. So if you want to charge your battery with AC source then should follow these steps, we need first limit the large AC voltage, need to filter the AC voltage to remove the noise, regulate and get the constant voltage and then give the resulting voltage to the battery for charging.
- Once charging is completed the circuit should automatically turned off.

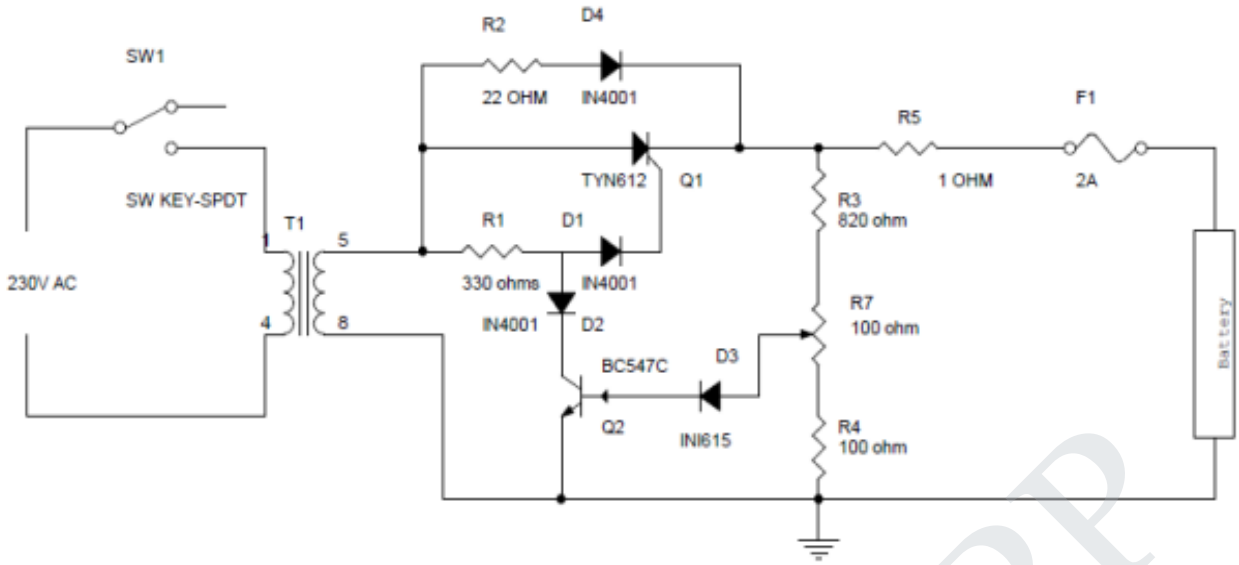
BLOCK DIAGRAM OF BATTERY CHARGER



Block Diagram of Battery Charger Using SCR

- The AC source is given to the step down transformer which converts the large AC source into limited AC source, filter the AC voltage and remove the noise and then give that voltage to the SCR where it will rectify the AC and give the resulting voltage to the battery for charging.

CIRCUIT DIAGRAM



- The AC main voltage is given to the step down transformer the voltage should be down to 20V approx. the step down voltage is given to the SCR for rectification and SCR rectifies AC main voltage. This rectified voltage is used to charge battery.
- When the battery connecter to the charging circuit, the battery will not be dead completely and it will get discharged this will give the forward bias voltage to the transistor through the diode D2 and resistor R7 which will get turned on. When the transistor is turned on the SCR will get off.
- When the battery voltage is dropped the forward bias will be decreased and transistor gets turned off. When the transistor is turned off automatically the diode D1 and resistor R3 will get the current to the gate of the SCR, this will triggers the SCR and gets conduct. SCR will rectifies the AC input voltage and give to the battery through Resistor R6.
- This will charge the battery when the voltage drop in the battery decreases the forward bias current also gets increased to the transistor when the battery is completely charged the Transistor Q1 will be again turned on and turned off the SCR.

TURNING ON (TRIGGERING) SCR:

- The SCR can be turned ON, from its OFF position, by several methods as discussed below;
  - ➢ Forward breakover voltage
  - ➢ Gate triggering
  - ➢ Rate-effect or dV/dt triggering
  - ➢ Light triggering

TURNING OFF SCR:

- Once the SCR turns ON (starts conducting), it continues to conduct even when the gate signal is removed. This ability of the SCR to remain conducting, even when the gate signal is removed, is known as **latching.**
- It means that SCR cannot be turned OFF simply by removing the gale signal, A number of methods are used for turning OFF the SCR as mentioned below:
  - Reversing polarity of anode-to-cathode voltage.
  - Interrupting anode current by means of momentarily series or parallel switching arrangement. This method is known as anode current interruption,
  - Reducing the current through SCR below the holding current. This method is known as forced commutation.

APPLICATIONS:

- Motor speed control
- Light – dimming control
- Heater control
- Battery charger
- Inverters
- Static switches

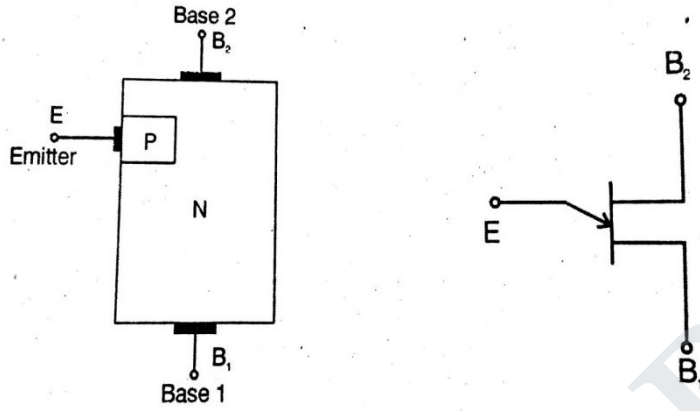
2. Give the construction details of UJT & explain its operation with the help of equivalent circuits. (OR) Explain how UJT function as Relaxation Oscillator. (OR) Draw the basic structure of UJT & explain V-I characteristics of UJT with equivalent circuits. (N/D 2014) (N/D 2015) (M/J 2016) (N/D 2019)

UNI JUNCTION TRANSISTOR (UJT)

- A uni junction transistor is a three terminal silicon semiconductor device. UJT has only one PN junction like an ordinary diode that acts exclusively as an electrically controlled switch.
- The UJT is not used as a linear amplifier. It is used in free-running oscillators, synchronized or triggered oscillators, and pulse generation circuits at low to moderate frequencies (hundreds of kilohertz). It is widely used in the triggering circuits for silicon controlled rectifiers.

CONSTRUCTION:

- It consists of an N-type silicon semiconductor bar and a P-type silicon region. The N-type bar is called a base and the P-type region as the emitter. Thus PN junction is formed between the emitter and base region.

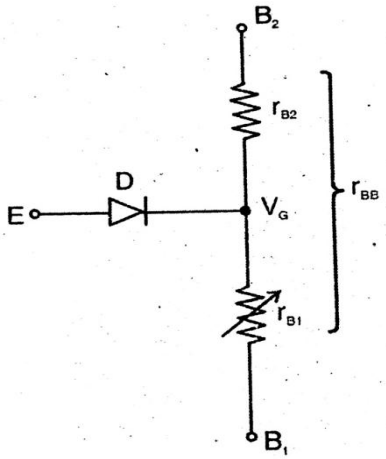


(a) Construction (b) Symbol

- The emitter region is heavily doped, while the base region is lightly doped. Due to this reason, the resistivity of the base material is very high.
- Three terminals are taken out of the whole structure one from the emitter region and the two from the ends of the base regions. These terminals are labeled as Emitter (E), Base1 (B_1) and Base2 (B_2).

EQUIVALENT CIRCUIT:

- It consists of a diode and a resistance. The diode (D) represents the PN junction, while the resistance (r_{B1} and r_{B2}) is the internal bulk resistance of the silicon bar from one end to the other.



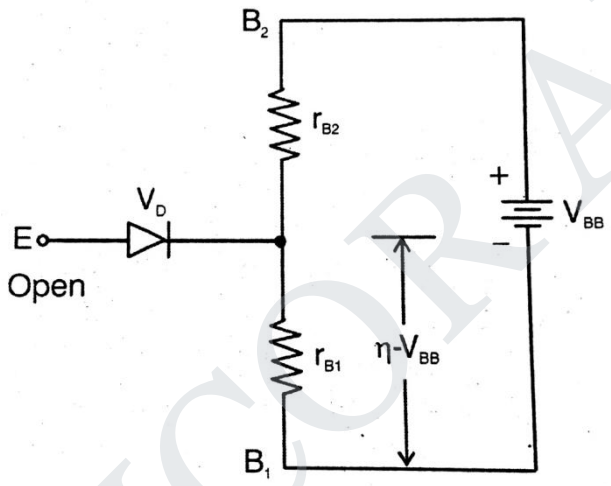
Equivalent circuit.

- The resistance r_{BB} represents the total resistance between the base terminals and is called the interbase resistance.
- The resistance r_{B1} represents the bulk resistance between the Emitter (E) and Base1 (B_1). The resistance r_{B2} represents the bulk resistance between the Emitter (E) and Base2 (B_2).

$$r_{BB} = r_{B1} + r_{B2}$$

- When there is no voltage applied to the UJT, the value of resistance r_{BB} is 5 to 10KΩ. The resistance r_{B1} is a variable resistance because the value of resistance r_{B1} varies inversely with emitter current (I_E).

INTRINSIC STAND-OFF RATIO (η):



As the emitter is open, the applied voltage V_{BB}, divides itself across resistance r_{B1} and r_{B2}.

The voltage across the resistance r_{B1} is

$$V_1 = \frac{r_{B1}}{r_{B1} + r_{B2}} \times V_{BB} = \frac{r_{B1}}{r_{BB}} \times V_{BB}$$

The resistance ratio $\frac{r_{B1}}{r_{BB}}$ is known as **intrinsic stand-off ratio** and is designated by η

$$\therefore \eta = \frac{r_{B1}}{r_{BB}} = \frac{r_{B1}}{r_{B1} + r_{B2}}$$

The value of η is between 0.5 and 0.8

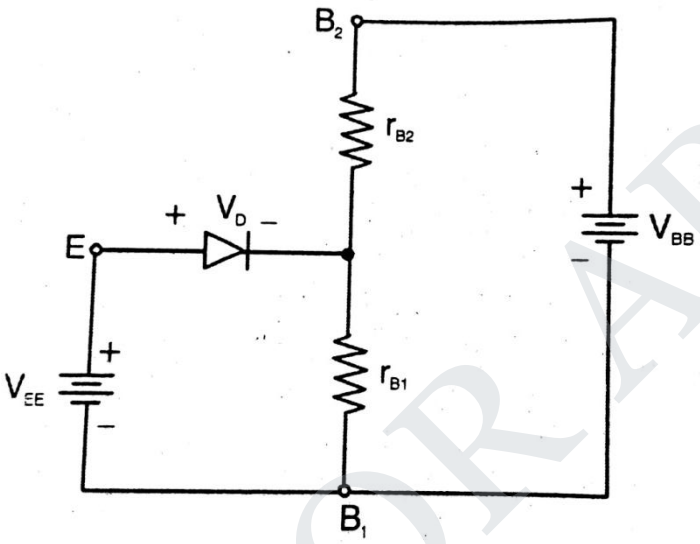
UJT OPERATION

- The emitter diode (D) is reverse biased by a voltage drop across the resistance r_{B1} (η. V_{BB}) and its own barrier potential (V_D). Thus the total reverse bias voltage across a

diode is equal to the sum of ŋ. V_{BB} and V_D . This voltage reverse biases the PN junction and emitter current is cut-off. But a small leakage current flows from B_2 to emitter due to minority carriers.

- As the applied emitter voltage reaches or exceeds the value equal to ŋ. V_{BB} + V_D the diode conducts and the emitter current flows . The value of emitter voltage which cause the diode to conduct, is called **peak point voltage (V_p).**

$$V_p = ŋ. V_{BB} + V_D$$



- As the emitter voltage reaches the peak point voltage, the diode conducts and the emitter current begins to flow. Under this condition the UJT is said to be fired, triggered or turned ON.
- Under this condition, holes are injected into N-type bar. These holes are repelled by the terminal B_2 and are attracted by the terminal B_1. The presence of excess holes, slightly reduces the resistance r_{B1} which in turn reduces the intrinsic stand-off voltage.
- It produces a negative region in the V-I characteristics of UJT and the UJT switches from its OFF position to ON position.
- If a negative voltage is applied to the emitter PN junction remains reverse biased and the emitter current is cut-off. The device is said to be OFF state.

V-I CHARACTERISTICS:

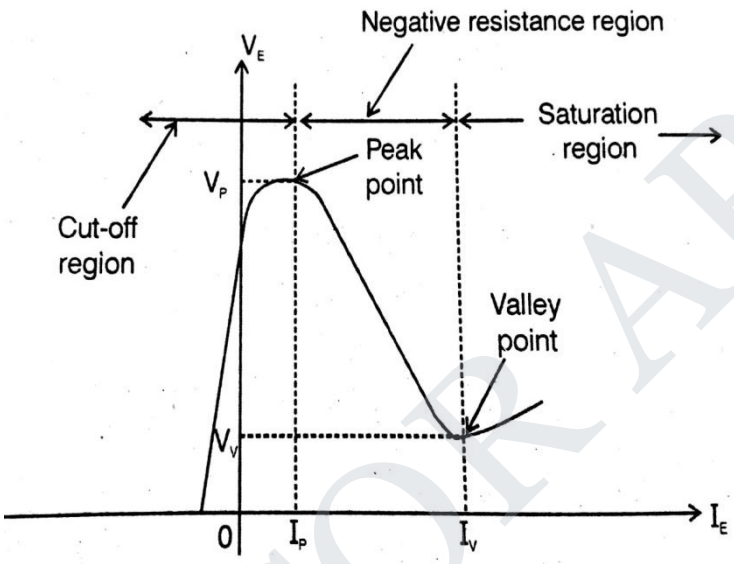
- There are two important points on the characteristics curve namely peak point and the valley point. These points divide the curve into three important regions. They are explained below:

(i)Cut-off region:

- The region to the left of the peak point is called cut-off region. In this region, the emitter voltage is below the peak point voltage and emitter current is approximately zero. The UJT is in its OFF position in this region.

(ii)Negative resistance region:

- The region between the peak point and the valley point is called Negative resistance region. In this region, the emitter voltage decreases from V_p to V_V and the emitter current increases from I_p to I_V.



VI characteristics of UJT

(iii)Saturation region:

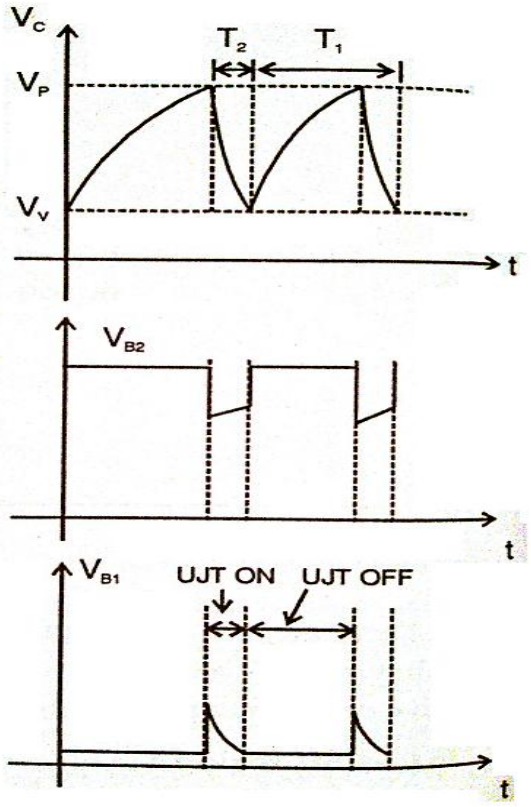
The region beyond the valley point is called saturation region. In this region the device is in its ON position. The emitter voltage remains almost constant with the increasing emitter current.

APPLICATIONS:

- Trigger device for SCRs and TRIACs
- Non sinusoidal oscillators
- Saw tooth generators
- Timing circuits.

UJT RELAXATION OSCILLATOR:

- The relaxation Oscillator using UJT is used to generate sawtooth waveform. It consists of a capacitor C which is charged through R as the supply voltage V_{BB} is switched ON.



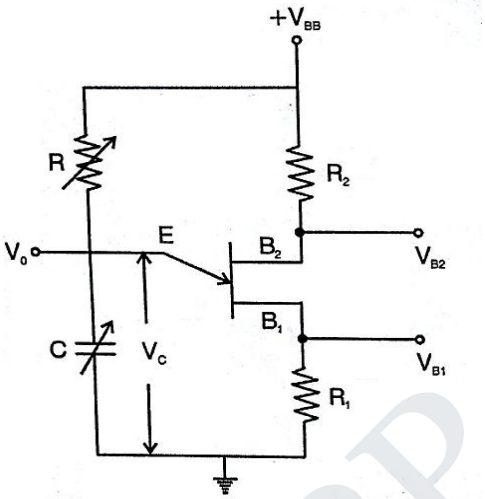


Fig UJT Relaxation oscillator

- The voltage across the capacitor increases exponentially and when the capacitor voltage reaches the peak point voltage V_P (= V_D+ ηV_{BB}), the UJT starts conducting and the capacitor voltage is discharged through E_{B1} and R_1.
- After the peak point voltage of UJT is reached, it provides negative resistance to the discharge path which is useful in the working of the relaxation oscillator.
- As the capacitor voltage reaches zero, the device then cuts off and capacitor C starts to charge again. This cycle is repeated continuously generating a sawtooth waveform across 'C'.
- The inclusion of external resistors R_2 and R_1 in series with B_2 and B_1 provides spike waveforms. When the UJT fires, the sudden surge of current through B_1 causes potential rise across R_1 which provides positive going spikes. Also, at the time of firing, negative going spikes are generated across R_2.
- By changing the values of capacitance C or resistance R, frequency of the output waveform can be changed as desired, since these values control the time constant RC of the capacitor charging circuit.

FREQUENCY OF OSCILLATION:

- The time period and hence the frequency of the sawtooth wave can be calculated as follows:

Assuming that the capccitor is initially uncharged, the voltage V_C across the capacitor prior to the breakdown is given by:

$$V_C = V_V + V_{BB}\,(1-e^{-1/RC})$$

The discharge of the capacitor occurs when V_C is equal to the peak-point voltage

$$V_P\ (= V_D + \eta V_{BB}) \qquad \text{(ie.) } V_P = V_C$$

Substituting (1) and (2) we got

$$V_D + \eta V_{BB} = V_V + V_{BB}\,(1-e^{-1/RC})$$

$$\text{(ie) } \eta V_{BB} = V_{BB}\,(1-e^{-1/RC}) \qquad \text{(neglecting } V_D, V_V)$$

$$e^{-1/RC} = 1-\eta$$

Taking logarithm on both sides we got,

$$\ln(e^{-1/RC}) = \ln(1-\eta)$$

$$-t / RC = \ln(1-\eta)$$

$$t = -RC \ln(1-\eta)$$

$$= RC \ln(1-\eta)^{-1}$$

$$t = RC \ln[1/(1-\eta)]$$

$$t = 2.303\ RC \log_{10}[1/(1-\eta)]$$

if the discharge time of the capacitor is neglected, then t=T, the period of the wave. Therefore, frequency of oscillation of sawtooth wave, $f = 1/T = 1/\ 2.303\ RC \log_{10}(1/1-\eta)$.

3. Explain the Construction and operation of LED/ Outline the theory of light generation in light emitting diode, with necessary expressions for internal and external quantum efficiencies / An indicator requires Voltage to be displayed in seven segment format. However, the power requirement for the display should be very low. Choose a proper display device and justify your choice. Also indicate the characteristics and operating principle of such a display device (A/M-2019) (A/M-2018)

LIGHT EMITTING DIODE (LED)

- Principle: It converts electrical energy into light output.
- A PN junction diode which emits light when forward biased is known as LED. The emitted light may be visible or invisible.

- The amount of light output is directly proportional to the forward current, thus higher the forward current, higher is the light output. There are two basic configuration

  i) Surface emitting LED ii) Edge emitting LED
- In surface emitting LED, the light is emitted perpendicular to the junction plane and in the edge emitting LED, emitted, light is parallel to the junction and emitted light is more directional in nature.
- The requirement of the material of which an LED is to be fabricated are as follows.
  - ➢ It must have an energy gap of appropriate width to emit radiation in a desired wavelength range.
  - ➢ Both 'p' and 'n' type forms of semiconductor material must be available.
  - ➢ Efficient radiative pathways must be present.
- Some of the commercial LED materials are
  - ➢ Gallium Arsenide (GaAs)
  - ➢ Gallium Phosphide (Gal')
  - ➢ Gallium Arsenide Phosphide (GaAsP)
  - ➢ Gallium Aluminium Arsenide (GaAIAs)
- Commercially LEDs are produced both as single element and as monolithic arrays.

CONTRUCTION :

- A cross-sectional view of a typical diffused LED is shown in figure. The semiconductor material used for fabricating LED's are gallium arsenide (Ga, As), gallium Arsenide phosphide (Ga AsP), or gallium phosphide (GaP)
- The arrow pointing away from the diode symbol represents the light, which being transmitted away from the junction.
- An N-type epitaxial layer is grown upon a substrate, and the P-region is created by diffusion of charge carrier recombinations occurs in the P-region, so this region must be kept uppermost.

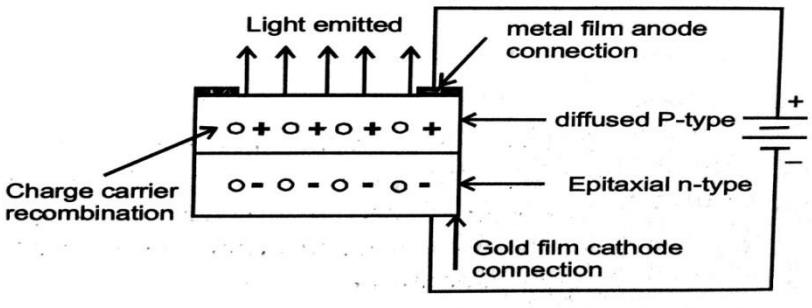


Figure 10 LED

- The P-region, therefore, becomes the surface of the device, and the metal film anode connection must be patterned to allow most of the light to be emitted.
- A gold film is applied to the bottom of the device and to provide a cathode connection LEDS made from GaAs, emits infrared (i.e. invisible) radiation.
- GaAsP(Gallium Arsendie phosphate) material provides either red light or yellow light, while red or green emission can be produced by using GaP(Gallium Phosphide).
- LED works by the process of the of spontaneous emission. It is a semiconductor junction diode which emits light when current is passed through it in the forward biased condition.
- One side of the diode is p-type semiconductor material containing a very large number of holes. The other side of the diode is n-type semiconductor containing a large number of free conduction electrons.

OPERATION:

- When enough forward bias voltage is applied to the junction to overcome the junction barrier potential, the depletion zone disappears, and holes are free to move into the p-region, where they are minority carriers. The minority carriers have only a very short life time before they meet up with carrier of opposite type and recombine.
- The amount or intensity of light emitted depends on the number of minority carriers available for recombination The frequency of the light emitted is determined by the energy band gap of the materials used to make the junction.

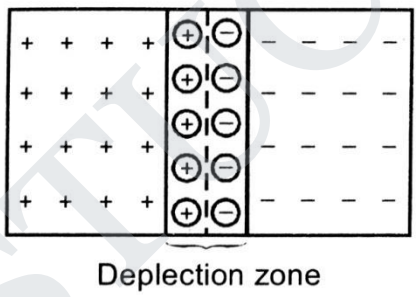


Figure 10(a) LED at zero bias

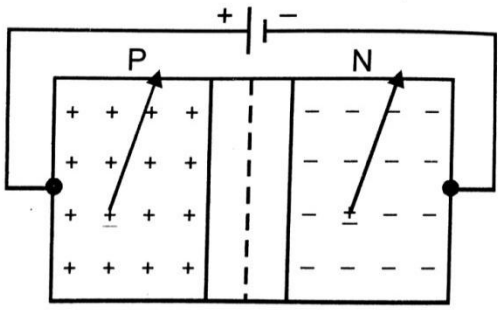


Figure 10(b) LED at forward bias

- After recombination, the electrons lying in the conduction bands of "N 'region fall into the holes lying in the valance band of a P region.
- The difference of energy between the conduction band and valence band is radiated in the form of light energy. In semiconductor diodes, this energy radiated in the form of heat.
- The LEDs have certain forward voltage drop when they are used in the circuit, it depends upon the LED current, (10 to 50mA).

- It is important to understand that LED's are not able to withstand reverse bias of even very small voltages. Due to this it is necessary to assure that reverse bias is never applied to an LED.

Quantum efficiency

Electronic Devices are semiconductor devices that emit light via the recombination of electrons and holes within the active region (a sequence of specially designed layers) of the device. Most of these recombination events are termed “radiative” because they result in the production of a photon of light.

The wavelength of the emitted light is determined by the bandgap of the active region - a wider bandgap results in higher energy emission, which equates to a shorter wavelength.In turn, the bandgap is determined by the chemical composition and sequence of the semiconductor layers within the active region.

External Quantum Efficiency (EQE)

The ratio of the number of photons emitted from the LED to the number of electrons passing through the device - in other words, how efficiently the device coverts electrons to photons and allows them to escape.

EQE = [Injection efficiency] x [Internal quantum efficiency] x [Extraction efficiency]

Injection Efficiency

In order that they can undergo electron-hole recombination to produce photons, the electrons passing through the device have to be injected into the active region. Injection efficiency is the proportion of electrons passing through the device that are injected into the active region

Internal Quantum Efficiency (IQE - also termed Radiative Efficiency)

Not all electron-hole recombinations are radiative. IQE is the proportion of all electron-hole recombinations in the active region that are radiative, producing photons.

The fraction of the electrons that are injected into the depletion layer which results in photons getting produced is known as internal **quantum efficiency** of the **LED**. It is denoted as η.

Extraction Efficiency (also termed Optical Efficiency)

Once the photons are produced within the semiconductor device, they have to escape from the crystal in order to produce a light-emitting effect. Extraction

efficiency is the proportion of photons generated in in the active region that escape from the device.

ADVANTAGES OF LEDS

Advantages of LED's over conventional incandescent and other lamps.

- Less power Consumption
- Very fast action (few nano second)
- Very small size and weight
- Extremely long life
- Operating voltage and current is less.
- Adaptability to coherent laser operation.
- Variety of spectral output colors.

DISADVANTAGES OF LEDS

- Very sensitive device, i.e., it damage by over voltage or over current
- Radiated output power is temperature dependent.
- Low efficiency.

APPLICATIONS:

Following are the important applications of the LED's

- In power level indicator to indicate power ON/OFF conditions
- In optical switching applications.
- In the field of optical communication, to transfer or couple energy from one circuit to another. It is also used to send light energy to fiber optic cable.
- In 7 segment, 16 segment and dot matrix displays
- In visual display units.

4. Write Shot notes on: (i)Solar cell (M/J 2014) (N/D 2017)
(ii)CCD(M/J 2014) (M/J 2015) (N/D 14,2015) (N/D 2017)
(iii)LCD (OR) Explain the Construction and operation of LCD (N/D 2016) (M/J 2015)(N/D 2015) (M/J 2017)

(i)SOLAR CELL:

- When sunlight is incident on a photovoltaic cell, it is converted into electric energy. Such an energy converter is called solar cell or solar battery and is used in satellites to provide the electrical power.
- A solar cell (also called a photovoltaic cell) is an electrical device that converts the energy of light directly into electricity by the photovoltaic effect.

- It is a form of photoelectric cell (in that its electrical characteristics—e.g. current, voltage, or resistance—vary when light is incident upon it) which, when exposed to light, can generate and support an electric current without being attached to any external voltage source, but do require an external load for power consumption.
- Cells can be described as photovoltaic even when the light source is not necessarily sunlight (lamplight, artificial light, etc.). In such cases the cell is sometimes used as a photo detector (for example infrared detectors), detecting light or other electromagnetic radiation near the visible range, or measuring light intensity.
- The operation of a photovoltaic (PV) cell requires 3 basic attributes:
  - The absorption of light, generating either electron-hole pairs or excitons.
  - The separation of charge carriers of opposite types.
  - The separate extraction of those carriers to an external circuit.
- The solar cell works in three steps:
  1. Photons in sunlight hit the solar panel and are absorbed by semiconducting materials, such as silicon.
  2. Electrons (negatively charged) are knocked loose from their atoms, causing an electric potential difference. Current starts flowing through the material to cancel the potential and this electricity is captured. Due to the special composition of solar cells, the electrons are only allowed to move in a single direction.
  3. An array of solar cells converts solar energy into a usable amount of direct current (DC) electricity.

OPERATION:

- This cell consists of a single semiconductor crystal which has been doped with both P and N type impurities thereby forming a PN junction. The basic construction of a PN junction solar cell is shown in Figure.
- Sunlight incident on the glass plate G passes through it and reaches the junction. An incident light photon at the junction may collide with a valence electron and impart sufficient energy to make a transition to the conduction band.
- As a result, an electron-hole pair is formed. The newly formed electrons are minority carriers in the P-region. They move freely across the junction.
- Similarly, holes formed in the N-region cross the junction in the opposite direction. The flow of these electrons and holes across the junction is in a direction opposite to the conventional forward current in a PN junction.

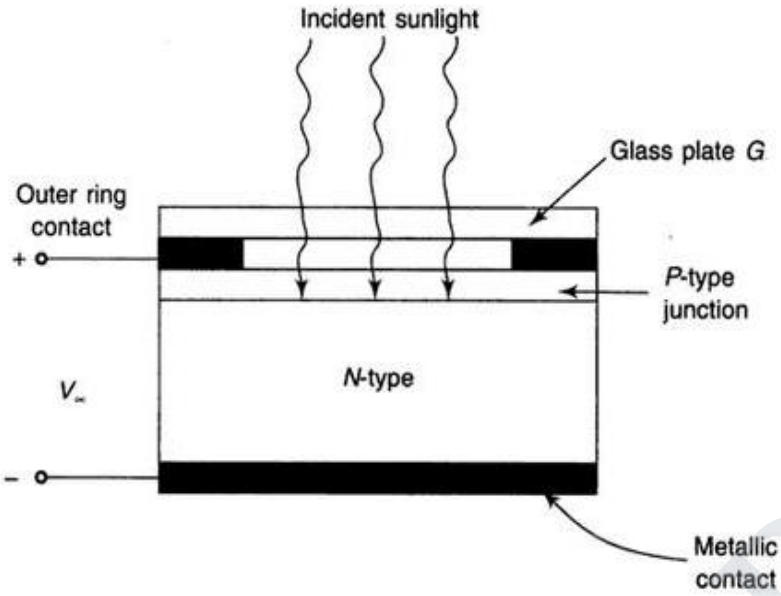


Fig. 22.14 Basic construction of a PN junction solar cell

- Further, it leads to the accumulation of a majority carriers on both sides of the junction. This gives rise to a photovoltaic voltage across the junction in the open circuit condition. This voltage is a logarithmic function of illumination.
- In bright sunlight, about 0.6 V is developed by a single solar cell. The amount of power the cell can deliver depends on the extent of its active surface.
- An average cell will produce about 30 mW per square inch of surface, operating in a load of 4Ω. To increase the power output, large banks of cells are used in series and parallel combinations.
- The efficiency of the solar cell is measured by the ratio of electric energy output to the light energy input expressed as a percentage. At present, an efficiency in the range of 10 to 40% is obtained.
- Silicon and selenium are the materials used widely in solar cells because of their excellent temperature characteristics.

ADVANTAGES

- Renewable energy - The energy can be used both to generate electricity and heat in the house.
- Environmentally friendly energy - With solar cells occurs almost no pollution.
- Long term energy - PV systems often have a long life and a good durability

DISADVANTAGES

- High investment - One-time cost of acquiring a photovoltaic system and have it installed are relatively high.

- Seasonal energy - Compared to other types of renewable energy, the solar power plant is highly seasonal,
- Interior needs - Not all households that can satisfy their requirements and get the optimum out of their solar cells yet. Solar cells are very sensitive in terms of their location.

APPLICATIONS:

- Power supply for satellites and space vehicles.
- Charging the batteries
- Automated street lights
- Solar panels for domestic purposes.

(ii) CHARGE COUPLED DEVICE (CCD):

- A Charge-Coupled Device (CCD) is a highly sensitive photon detector. CCDs are dynamic devices that move charge along a predetermined paths under control of clock pulses.
- A Charge-Coupled Device (CCD) is a shift register formed by a string of closely spaced MOS capacitors. A CCD can store and transfer analog signals, either electrons or holes, which may be introduced electrically or optically.
- A cross-sectional view of a three-phase charge-coupled device (CCD) is illustrated in Figure. The structure consists of a series of metal gate electrodes, separated from a P- (or an N-) type semiconducting silicon substrate (for an N-channel device) by a thin silicon dioxide layer.
- On top of the silicon dioxide is an array of metalized electrodes which are connected to signal voltages VI, V2 and V3.

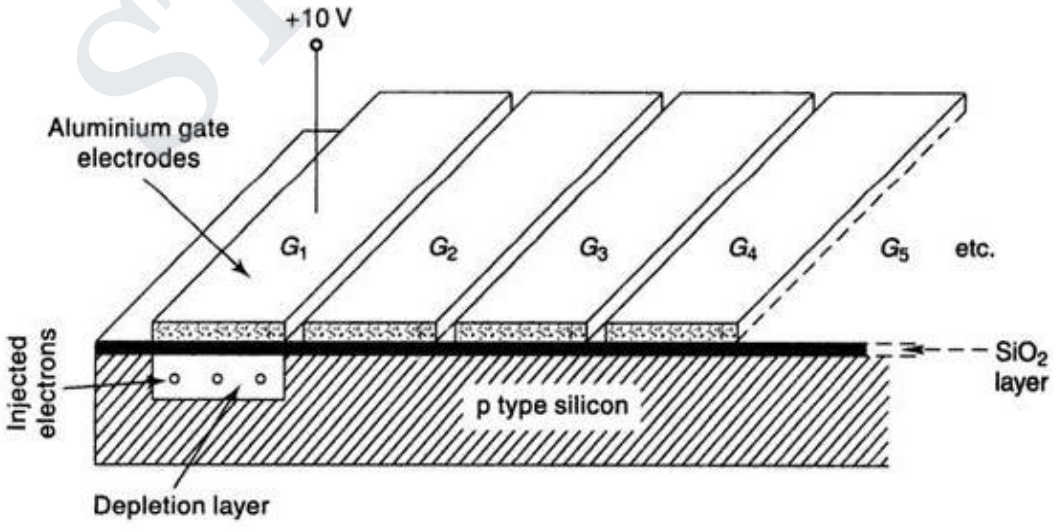


Fig. 7.19 Basic structure of CCD

- A three-phase clocked voltage pulse system supplied to the gates ensures that the charge is transferred serially between gates and its direction is controlled, as given below.
- The first phase connects a positive voltage V1, say +10 V, to G1, where V1 is greater than either V2 or V3, a depletion layer is formed, in typically less than I μs. This produces the potential well into which information, in the form of minority electrons, is stored.
- During the second phase, the adjacent gate G2 is biased to a greater positive voltage V2, say +15 V, to produce a deeper well under it as shown in Fig. (a).
- The stored charge then transfers into the deeper potential well by diffusion down the potential gradient, which incidentally can be a relatively slow process. In order to ensure the charge transfer, the potential wells must physically overlap.
- As depletion layers are typically only a few micrometers deep, the spacing between neighbouring gates must be as small as possible, to ensure sufficient over-lap. The charge is then completely stored in the well under G2 and hence, the voltage on G1 is reduced to a low value, say +5 V and that on G2 to a sustaining level of say +10 V as shown in Fig. (b).

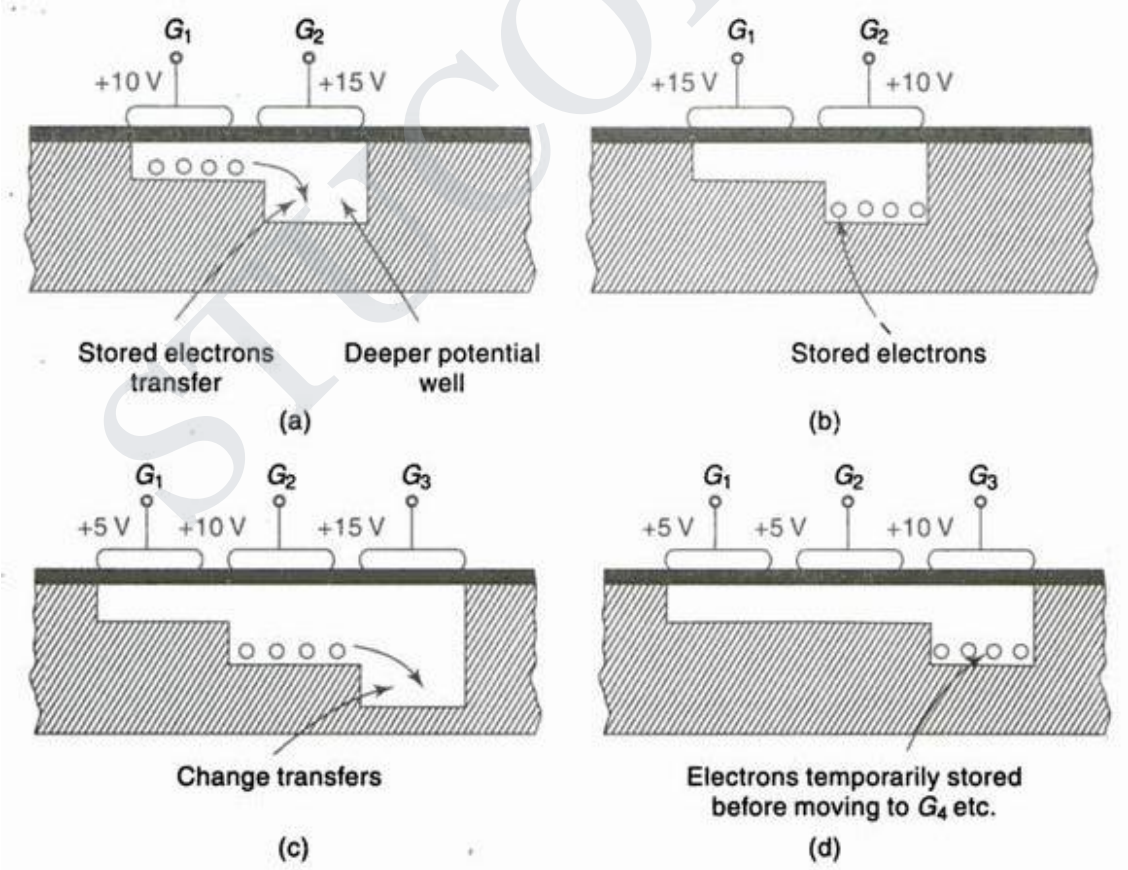


Fig. 7.20 The mechanism of charge transfer in a three phase CCD

- A third-phase transfers a +15 V voltage pulse to the next gate G3 and the charge is transferred from G2 to the well under it, as shown in Fig.(c). The voltages on G2 and G3 can be relaxed as before as shown in Fig. 7.20(d), to complete one cycle of the clock frequency.
- The charge has been transferred from under G1 to under G3 in one cycle of the clocked three-phase pulse which causes a series of voltages in the sequence of +15, +10, +5, +15, etc., to be applied to each gate electrode.
- In this manner, the charge in the substrate is transferred under one electrode to the next, and so on. Here each storage cell of three adjacent of three electrodes accommodates the bit of information.
- As soon as charge is moved out of one set of three electrodes, say from G3 to G4, then the input gate is again put in a state to receive a further bit of information.
- The CCD structure thus behaves as a dynamic shift register, and charge has to be transferred to less than 1 ms.
- This process is only possible provided the charge is not stored in any well for long time for an inversion layer to form, in which case the charge would disappear and the corresponding information will be lost.

ADVANTAGES

- Relative simple
- Cheaper to replace if failure.
- No chemical processing is needed.
- More sensitive than photographic film.

APPLICATIONS

- The CCD can be used as memories by storing charge corresponding to full and empty wells (1 and 0). However, as the charge storage is limited to the storage time of the associated capacitor, the charge has to be periodically refreshed. The commercial CCDs can transfer up to 20 MHz.
- The CCD finds application as a dynamic shift register in computers and in solid-state imaging. such as video cameras.
- CCD is used in photosensor arrays and such signal processing components as variable delay lines and signal correlators.
- Digital Photography.
- Medical Fluoroscopy.

(iii) LIQUID CRYSTAL DISPLAYS (LCDS)

- A liquid crystal display is a special thin flat panel that can let light go through it, or can block the light. (Unlike an LED it does not produce its own light).
- The panel is made up of several blocks, and each block can be in any shape. Each block is filled with liquid crystals that can be made clear or solid, by changing the electric current to that block. Liquid crystal displays are often abbreviated LCDs.
- The liquid crystals are one of the most fascinating material systems in nature, having properties of liquids as well as of a solid crystal. The terms liquid crystal refers to the fact that these compounds have a crystalline arrangement of molecules, yet they flow like a liquid.
- Liquid crystal displays do not emit or generate light, but rather alter externally generated illumination. Their ability to modulate light when electrical signal is applied has made them very useful in flat panel display technology.
- The crystal is made up of organic molecules which are rod-like in shape with a length of ~20A° - 100A°. The orientation of the rod like molecule defines the "director" of the liquid crystal. The different arrangements of these rod-like molecules lead to three main categories of liquid crystals.
    - Smectic
    - Nematic
    - Cholesteric

1. Smectic

- Fig. (a) shows smectic structure of liquid crystals. In this structure the rod like molecules are arranged in layers, and within each layer there is orientational order over a long range.
- Thus in a given layer, the rods are all oriented in the same direction Also, in the smectic liquid crystals the molecules of different layers are ordered as shown in Fig. (a).
- Thus both orientation order and positional order is present in the smectic crystals.

2. Nematic

- Fig (b) shows nematic structure of liquid crystals. In the nematie structure the positional order between layer of molecules is lost, but the orientation order is maintained.

3. Cholesteric

- Fig (c) shows cholesteric structure of liquid crystals. In these crystals the rod-like molecules in each layer are oriented a different angle within each layer.

- Orientation order is maintained in each layer. The cholesteric liquid crystal is related to the nematic crystal, with the difference being the twist of the molecules as one goes from one layer to another.
- The optical activity of the crystal depends upon the orientation and the twist of the molecules as one goes from one layer to another

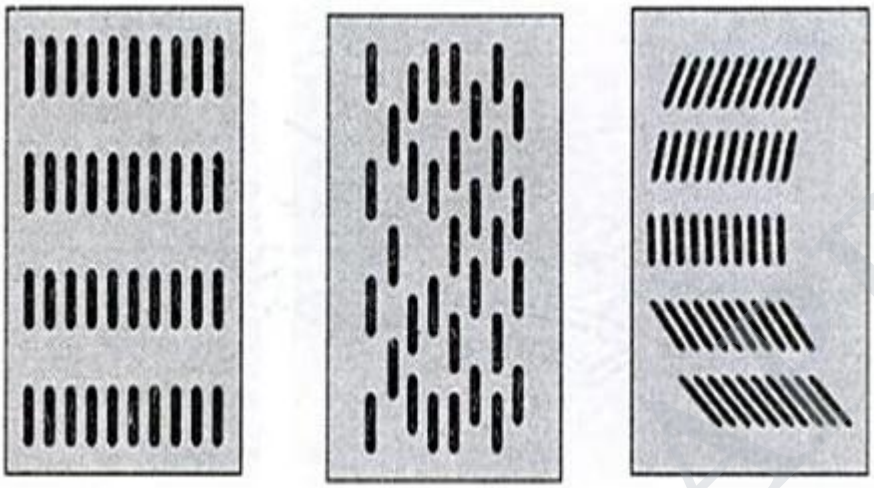


Fig. (a) Smectic Fig. (b) Nematic Fig. (c) Cholesteric

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TYPES OF LCD

There are two types of liquid crystal displays (LCDs) according to the theory of operation:

1. Dynamic scattering
2. Field effect.

1. Dynamic Scattering Type LCDs

- Fig. shows the construction of *a* typical liquid crystal display. It consists of two glass plates with a liquid crystal fluid in between.
- The back plate is coated with thin transparent layer of conductive material, whereas front plate has a photoetched conductive coating with seven segment pattern as shown in Fig.
- Figure shows the operation of liquid crystal display. In the absence of the electrical signal, orientation order is maintained in the crystal allowing light to transmit. This makes LCD display clear.
- The current through the liquid crystal causes orientation order to collapse. The random orientation results scattering of light which lights display segment on a dark background as shown in Figure.

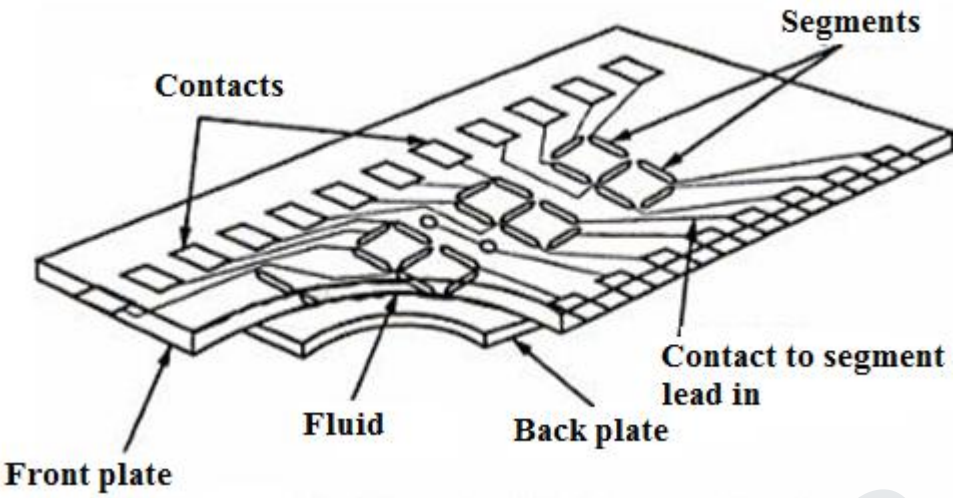


Fig. Liquid Crystal Display Construction

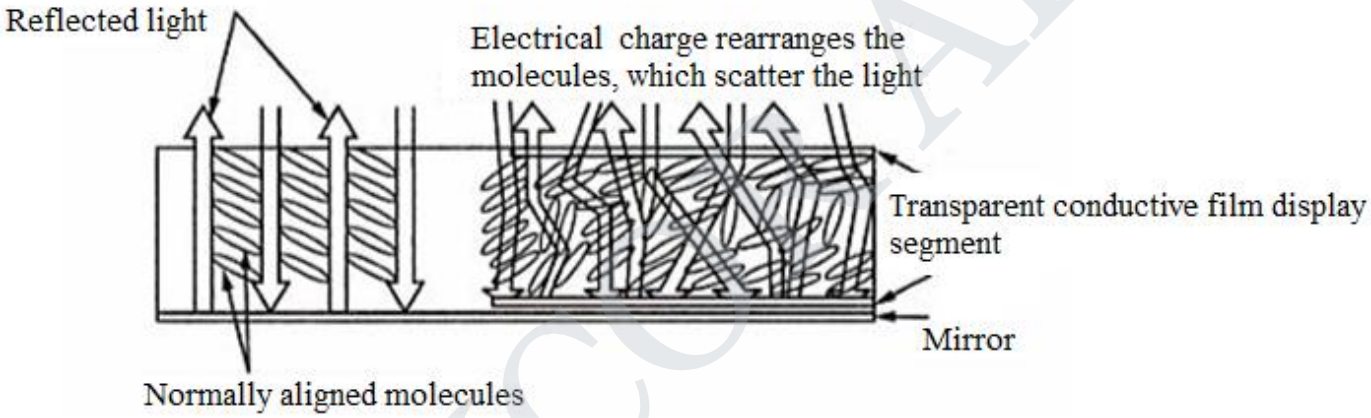


Fig. Dynamic Scattering

Fig. Typical liquid crystal

2.Field Effect Display

- In these displays nematic liquid crystals are used. Figure shows operation of field effect liquid crystal display with nematic crystals. It consists of two glass plates, a liquid crystal fluid, polarizers and transparent conductors.
- The liquid crystal fluid is sandwiched between two glass plates. Each glass plate is associated with light polarizer. The light polarizers are placed at right angle to each other.

- In the absence of electrical excitation, the light coming through the front polarizer is rotated through 90° in the fluid and passed through the rear polarizer. It is then reflected to the viewer by the back mirror as shown in Fig (a).

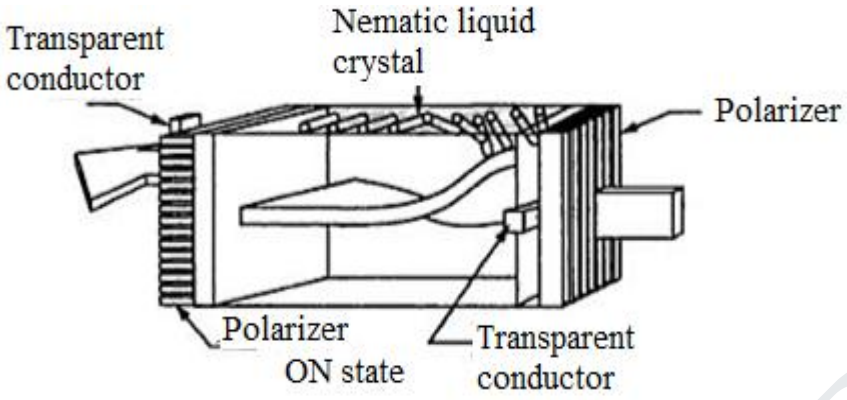


Fig. (a) Field effect display "ON state"

- On the application of electrostatic field, the liquid crystal fluid molecules get aligned and therefore light through the molecules is not rotated by 90° and it is absorbed by the rear polarizer as shown in Fig (b).
- This causes the appearance of dark digit on a light background as shown in Fig (c).

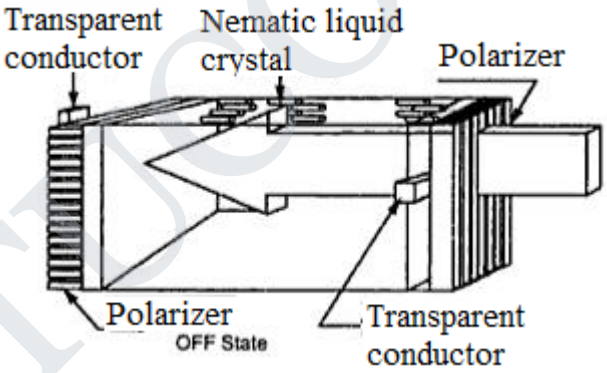


Fig.(b)

Fig. (c)

ADVANTAGES OF LCDS

- Less power consumption
- Low cost

- Uniform brightness with good contrast
- Low operating voltage and current

DISADVANTAGES OF LCD

- Poor reliability
- Limited temperature range
- Poor visibility in low ambient temperature
- Slow speed
- Requires an a.c. drive.

APPLICATIONS

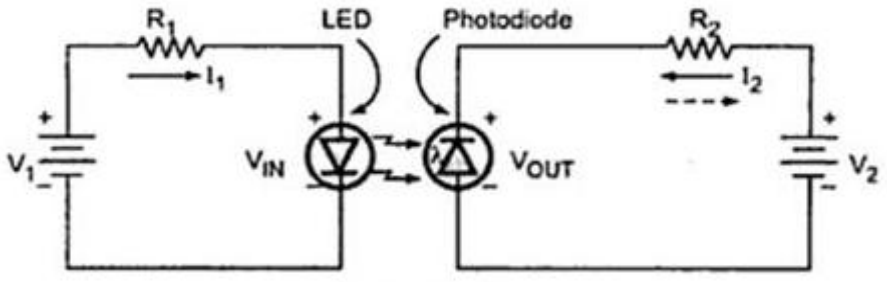
- Digital watches to indicate time, day and date etc.
- Electronic toys and calculators.
- Instrument display.
- They are also used for flat screen TV's.

5. Write Shot notes on: (i)Optocoupers (N/D 2014) (M/J 2017) (N/D 2017)

(ii)Photo transistor (OR) Describe the working of Photo transistor (N/D 2014,16,17)

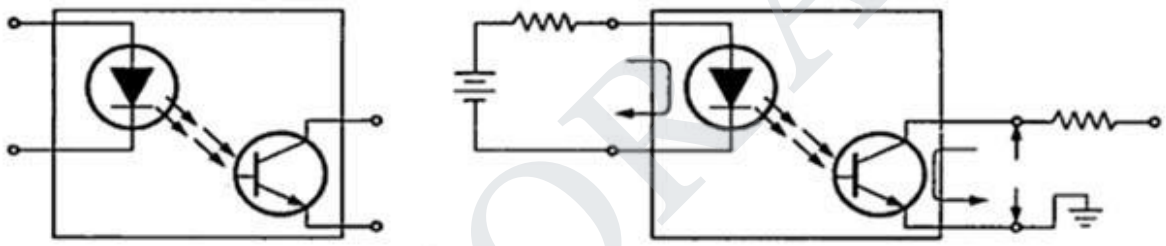
(i)OPTOCOUPLER

- In electronics, an opto-isolator, also called an optocoupler, photocoupler, or optical isolator, is a component that transfers electrical signals between two isolated circuits by using light.
- Opto-isolators prevent high voltages from affecting the system receiving the signal. Commercially available opto-isolators withstand input-to-output voltages up to 10 kV and voltage transients with speeds up to 10 kV/μs.
- The combined package of a LED and a photodiode is called an optocoupler. It is also called an optoisolator or an optically coupled isolator. The basic circuit of an optocoupler. It has LED on the input side and a photodiode on the output side.



Optocoupler

- The source V_1 and series resistance R_1 decide the forward current I through the LED. Thus LED emits the light.
- This light is incident on a photodiode. Due to this, a reverse current is set up in the output circuit. This current produces a drop across the output resistance R_2. The output voltage is the difference between the supply voltage V_2 and the drop across the resistor R_2.
- $V_{Out} = V_2 - I_2 R_2$
- Now if input voltage is changed, the amount of light emitted by LED changes. This varies the reverse current in the output circuit and hence the output voltage.
- The output voltage is thus varying in step with the input voltage. This coupling between LED and photodiode is hence called optocoupler. As the name suggests this device can couple an input signal to the output circuit.
- Figure (a) shows the typical optoisolator. It consist of LED and Phototransistor.



(a) Optoisolator (b) Optoisolator circuit

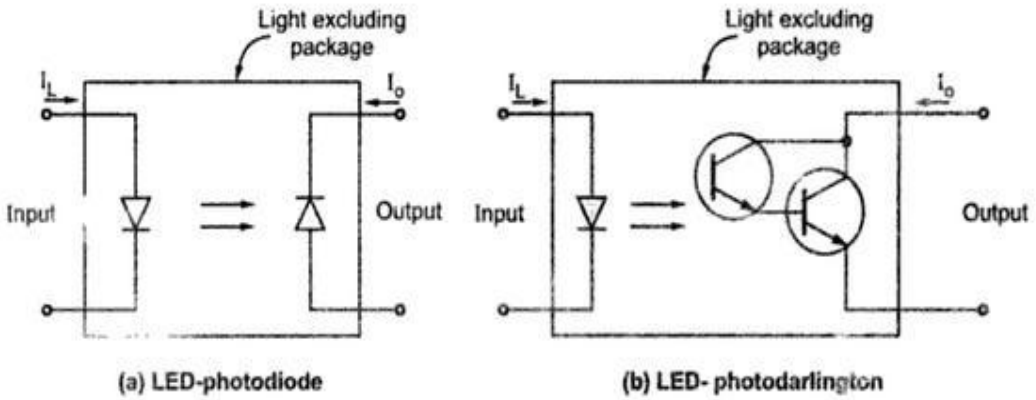
When the input voltage forward biases the LED, light transmitted to the phototransistor turns it on, resulting current through the external load, as shown in

TYPES OF OPTOCOUPLERS :

- Other than the combination of LED and phototransistor, two more types of optocouplers are available which are,

1. LED-Photodiode
2. LED-Photo darlington

- In both the circuits, the input current which is the forward current of LED, results in the emission of light by LED. This light is detected by photodiode and photo darlington to produce the output current. These two optocouplers are shown in the Fig. (a) and (b).



(a) LED-photodiode (b) LED- photodarlington

CHARACTERISTICS OPTOCOUPLERS

Following are the important characteristics of an optocoupler :

i) Current transfer ratio
ii) Isolation voltage
iii) Response time
iv) Common mode rejection.

(i)Current transfer ratio (CTR) : The current transfer ratio refers to the ratio of the output collector current (I_C) to the input forward current (I_F).

$$\text{Current transfer ratio} = \frac{I_C}{I_F} \times 100\ \%$$

The CTR greatly differs depending on the type of the phototransistor used in photocoupler.

(ii)Isolation voltage between input and output (Vim,) : Isolation voltage (V_{iso}) between input and output is another important factor in choosing a photocoupler. This is because photocouplers are often used for signal transmission between circuits that have different potentials or as interfaces with actuator circuits which tend to generate impulsive voltage, such as motor controllers or solenoid driver circuits. Isolation voltage is specified in $KV_{rms}$with a relative humidity of 90 to 60%

(iii) Response time : The response time of a optocoupler depends mainly on the output phototransistor. The response time also depends on the input forward current and load resistance.

Since load resistance has a greater influence on the response time, careful setting is required while defining the circuit constant.

(iv) Common mode rejection : While the photocouplers output is electrically isolated from its input for relatively low frequency signal, an impulsive input voltage may cause a displacement current to flow due to the floating capacitance (C_F) between the input and output of the optocoupler, causing noise voltage to appear at the output.

ADVANTAGES:

- The electrical isolation between input and output circuit. The coupling between input and output is through the beam of light. There is a transparent insulating cap between the two elements embedded in the design to permit the passage of light. So there exists an insulation resistance of several megaohrns between input and output circuit. This type of isolation is useful in high voltage applications where the voltages of the input and output circuits differ by several thousand volts.
- The response times of optocouplers is so small that they can be used to transmit data in the megahertz range.
- Capable of wideband signal transmission.
- Unidirectional signal transfer means that output does not loop back to the input circuit.
- Easy interfacing with logic devices.
- Compact and light weight.
- Much faster than the isolation transformers and relays.
- As signal transfer is unilateral, changing load do not affect input.
- The problems such as noise, transients, contact bounce etc. are completely eliminated.

APPLICATIONS:

- Due to electrical isolation, used for high voltage applications.
- In driving the motors, relays, alarms, etc.
- In high power choppers and inverters.
- In a.c to d.c converters used for d.c motor speed control.

(ii)PHOTOTRANSISTOR

- **Phototransistors** are either tri-terminal (emitter, base and collector) or bi-terminal (emitter and collector) semiconductor devices which have a light-sensitive base region. Although all transistors exhibit light-sensitive nature, these are specially designed and optimized for photo applications.
- These are made of diffusion or ion-implantation and have much larger collector and base regions in comparison with the ordinary transistors.
- These devices can be either homojunction structured or heterojunction structured, as shown by Figure 1a and 1b, respectively.

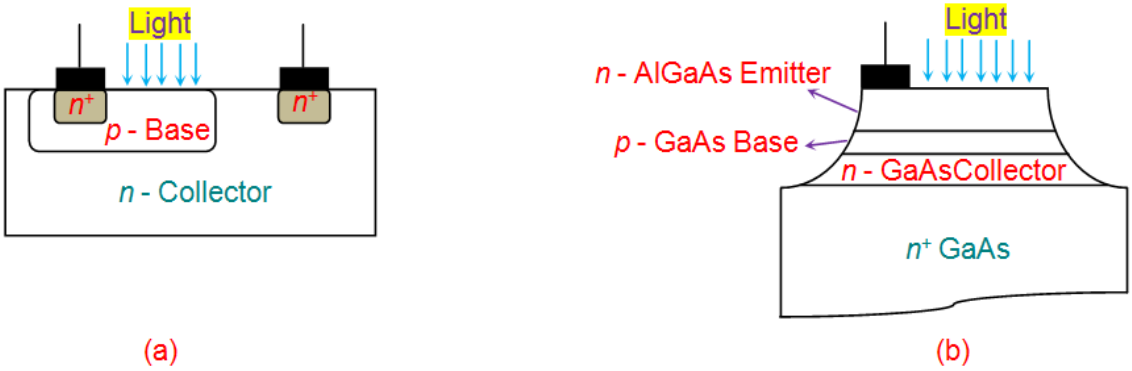


Figure 1 Phototransistor (a) Homojunction Structure (b) Heterojunction Structure

- In the case of homojunction phototransistors, the entire device will be made of a single material-type; either silicon or germanium.
- However to increase their efficiency, the phototransistors can be made of non-identical materials (Group III-V materials like GaAs) on either side of the pn junction leading to heterojunction devices. Nevertheless, homojunction devices are more often used in comparison with the hetero junction devices as they are economical.
- The circuit symbol for npn phototransistors is shown by Figure which is nothing but a transistor (with or without base lead) with two arrows pointing towards the base indicating its sensitivity to light. Similar symbolic representation holds well even in the case of pnp phototransistors with the only change being the arrow at emitter pointing in, instead of out.

Figure 1 *npn* Phototransistor Symbol with (a) Three Leads (b) Two Leads

- The output of the phototransistor depends on varies factors like

➢ Wavelength of the incident light
➢ Area of the light-exposed collector-base junction
➢ DC current gain of the transistor.

- Figure shows the circuit of an NPN phototransistor. It is usually connected in a CE configuration with the base open. A lens focuses the light on the base-collector junction. Although the phototransistor has three sections, only two leads, the emitter and collector leads, are generally used.

- In this device, base current is supplied by the current created by the light falling on the base-collector photodiode junction.
- When there is no radiant excitation, the minority carriers are generated thermally, and the electrons crossing from the base to the collector and the holes crossing from the collector to the base constitute the reverse saturation collector current I_{CO} With $I_B = 0$, the collector current is given by $I_C=(\beta+1)\ I_{CO}$
- When the light is turned ON, additional minority carriers are photogenerated and the total collector current is $I_C=(\beta+1)(I_{CO}+I_L)$. where I_L is the reverse saturation current due to the light.
- Current in a phototransistor is dependent mainly on the intensity of light entering the lens and is less affected by the voltage applied to the external circuit.

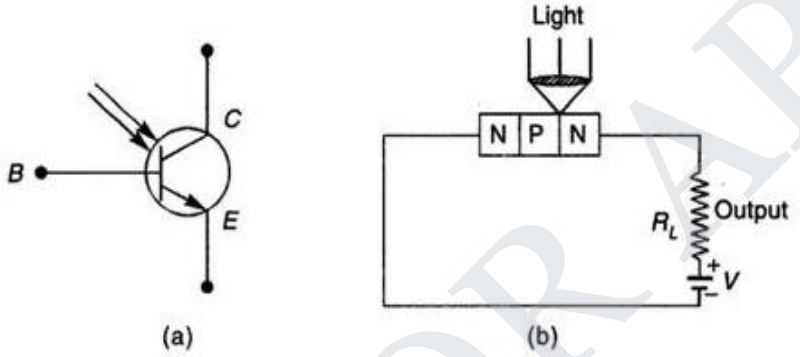


Fig. 22.9 NPN phototransistor (a) Symbol, and (b) Biasing arrangement

- Figure shows a graph of collector current Ic as a function of collector-emitter voltage VG: and as a function of illumination H.

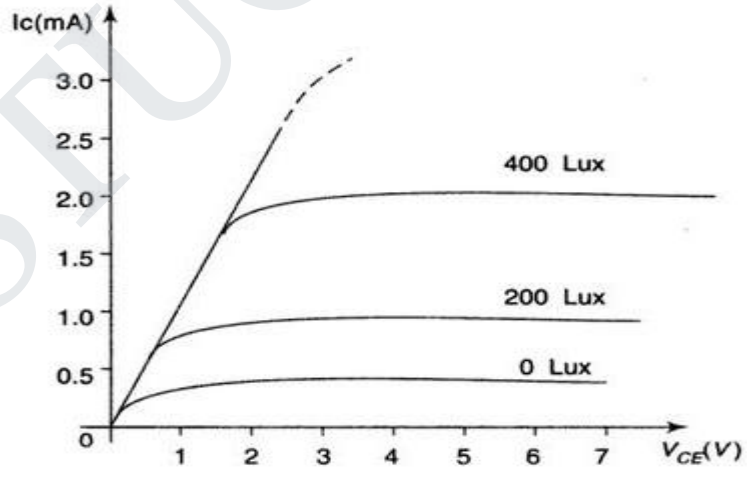


Fig. 22.10 Characteristics of phototransistor

- The phototransistors find extensive applications in high-speed reading of computer punched cards and tapes, light detection systems, light operated switches, reading of film sound track, production line counting of objects which interrupt a light beam, etc.

ADVANTAGES

- Simple, compact and less expensive.
- Higher current, higher gain and faster response times in comparison with photodiodes.
- Sensitive to a wide range of wavelengths ranging from ultraviolet (UV) to infrared (IR) through visible radiation.
- Sensitive to large number of sources including incandescent bulbs, fluorescent bulbs, neon bulbs, lasers, flames and sunlight.
- Highly reliable
- Less noisy when compared to avalanche photodiodes.

DISADVANTAGES

- Cannot handle high voltages if made of silicon.
- Prone to electric spikes and surges.
- Affected by electromagnetic energy.
- Do not permit the easy flow of electrons unlike electron tubes.

APPLICATIONS

- Object detection
- Encoder sensing
- Automatic electric control systems such as in light detectors
- Punch-card readers
- Computer logic circuitry

6. Write Shot notes on: (i)Power BJT (M/J 2015)

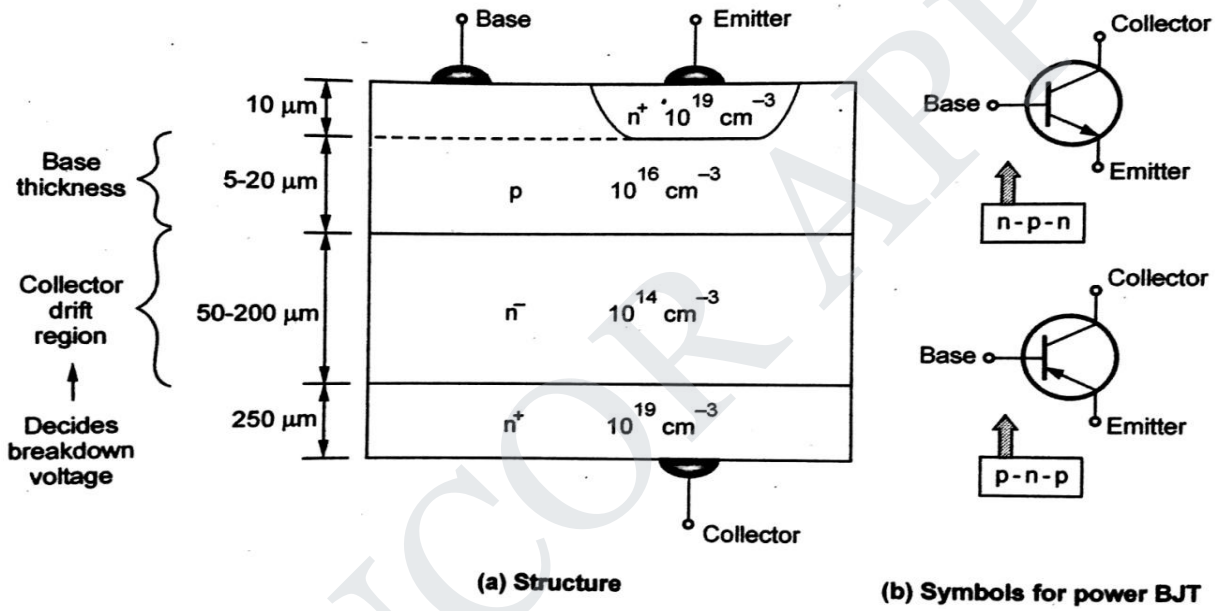
(ii)Power MOSFET (OR) Explain the working and characteristics of DMOS (M/J 2015) (N/D 2016)

(i)POWER TRANSISTORS

- Power transistors are devices that have controlled turn-on and turn-off characteristics. These devices are used as a switching devices and are operated in the saturation region resulting in low on-state voltage drop.
- They are turned on when a current signal is given to base or control terminal. The transistor remains on so long as the control signal is present.
- The switching speed of power transistor is much higher than that of thyristors and are used extensively in dc - dc and dc - ac converters. However their voltage and current ratings are lower than those of thyristors and are therefore used in low to medium power applications.

POWER BJT STRUCTURE

- A Power transistor is a vertically oriented four layer structure of alternating p-type and n-type as shown in Figure. The vertical structure is preferred because it maximizes the cross sectional area and through which the current in the device is flowing.
- This also minimizes on-state resistance and thus power dissipation in the transistor.
- The doping of emitter layer and collector layer is quite large typically 10^{19} cm^{-3}. A special layer called the collector drift region (n-) has a light doping level of 10^{14} cm^{-3}.
- The thickness of the drift region determines the breakdown voltage of the transistor. The base thickness is made as small possible in order to have good amplification capabilities.



(a) Structure (b) Symbols for power BJT

POWER TRANSISTOR I-V CHARACTERISTICS

- The power transistor has characteristics almost similar to the standard transistor except that the V-I characteristics has a region of quasi saturation as shown in Figure.
- There are four regions namely cut-off region, active region, quasi saturation and hard saturation.

CUT-OFF REGION:

- In the cut-off region (I_B < 0) the collector current is almost zero. Hence the transistor is 'OFF'. In cut-off region, it acts as an open switch.
- The maximum voltage between collector and emitter under this condition is termed **Maximum forward blocking voltage** with base terminal open (I_B = 0) and is denoted by V_{CEO}. This is the maximum voltage that can be applied in the forward direction (C positive with respect to E) across a power transistor.

ACTIVE REGION:

- In the active region the ratio of collector current to base current [DC current gain β] remains fairly constant up to certain value of the collector current after which it falls off rapidly.
- The maximum collector-emitter, voltage that a power transistor can withstand in active region is determined by the **Base collector avalanche breakdown voltage** denoted by V_{sus}
- At still higher levels of collector currents the allowable active region is further restricted by a potential failure mode called "**Second Breakdown**". It appears on the output characteristics of the BJT as a drop in the collector-emitter voltage at large collector currents.
- In this region, the junction temperature increases beyond the safe limit and power BJT gets damaged.

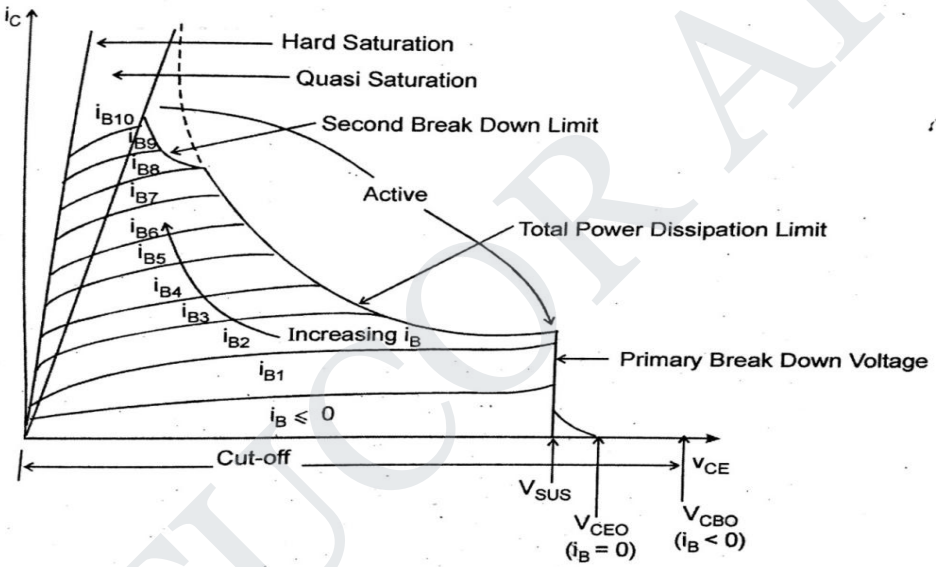


Fig. 5.22: Output ($i_c - v_{CE}$) characteristics of an $n-p-n$ type Power Transistor

SATURATION REGION

- It is in the saturation region that the output characteristics of a power transistor differs from the small signal BJT.
- The saturation region of a power transistor is subdivided into quasi saturation region and hard saturation region.

QUASI-SATURATION REGION

- Quasi-saturation region in the output characteristics of a power transistor is due to the introduction of the drift region into the structure of a power transistor.
- In the quasi-saturation region the base-collector junction is forward biased but the lightly doped drift region is not completely shorted out by excess minority carrier injection from the base.

- Therefore, in the quasi saturation region, the base current still retains some control over the collector current although the value of β decreases significantly.

HARD SATURATION

- In the hard saturation region base current looses control over the collector current which is determined entirely by the collector load and the biasing voltage V_{CC} Therefore, for large collector currents the collector-emitter voltage drop is almost proportional to the collector current.

Advantages of Power BJT

1. Power BJTs have small turn-on losses.
2. Power BJTs have small turn-on and turn-off times, hence their switching frequencies are higher.
3. Power BJTs cost are less.
4. Base drive has full control over the operation.

DISADVANTAGES OF POWER BJT

1. Storage charge in base reduces switching frequencies.
2. Drive circuit of power BJT is complex.
3. Negative temperature co-efficient causes problems in paralleling of BJTs.

Applications of Power BJT

1. DC-to-DC converter.
2. DC-to-AC converter.
3. Switched Mode Power Suppliers.
4. Bridge Inverters.

(ii)Power MOSFET

- The operation of power MOSFET is same as that of conventional MOSFET but the power handling capacity of conventional MOSFET is less than 1W.
- New design and recent techniques developed to produce three dimensional gate structure which is used in power MOSFET.

The features of power MOSFETs are:

- The power-handling level is more than 10 W.
- The current handling level is in the ampere range.
- Power MOSFET has large forward transconductance.
- The drain to source blocking voltage may be more than 100 V.
- Power MOSFETs have faster switching times.

Two types of structures are used in power MOSFET. They are:

(i) DMOS - Double-diffused vertical MOS transistor.

(ii) VMOS - Vertical metal-oxide-silicon FET.

DMOS - Double-diffused vertical MOS transistor:

The most popular structure for power MOSFET is the double-diffused MOS transistor as shown in fig.

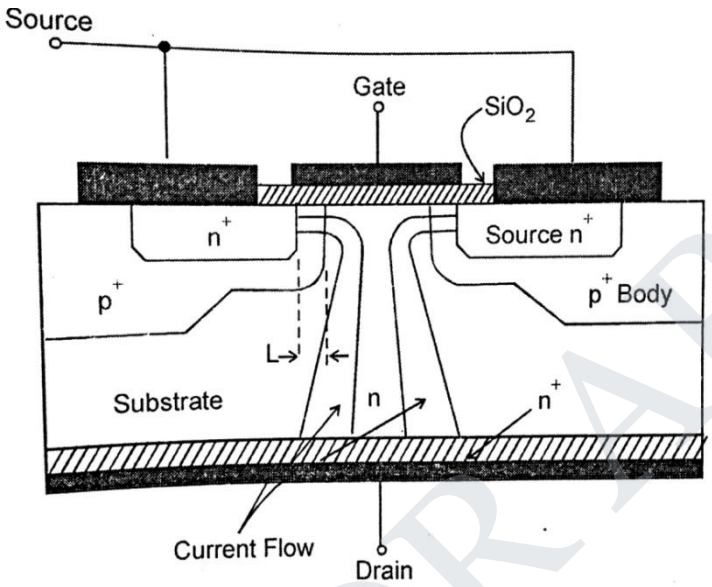


Fig. 5.24 : Double-Diffused Vertical MOS Transistor (DMOS)

STRUCTURE OF DMOS

- The device is fabricated on a lightly doped n-type substrate with a heavily doped region at the bottom for the drain contact.
- Two diffusions are employed, one to form the p-type body region and another to form the n+-type source region.
- The p-type body region is diffused deeper than n+ source. The channel length is the difference between diffusion distance of p-type body region and the n+-source, which is very short.

OPERATION OF DMOS

- Application of a positive gate voltage, V_{GS}, greater than the threshold voltage V_t induces a n-channel in the p-type body region below the gate oxide. The resulting channel is short; its length is denoted L as shown in Figure
- Current is then conducted by electrons from the source moving through the resulting short channel to the substrate and then vertically down the substrate to the drain.
- Even though the DMOS transistor has a short channel, its breakdown voltage can be very high (as high as 600 V). This is because the depletion region between the

substrate and the body extends mostly in the lightly doped substrate and does not spread into the channel.

- As a result, DMOS transistor simultaneously on handles high current capability (in the range of Amperes) as well as the high breakdown voltage.

VMOS (or V – Groove MOSFET)

- One of the major disadvantage of a typical MOSFET is reduced power handling level as compared to BJT transistors. The power handling level of a typical MOSFET is less than 1W.
- This drawback of the MOSFET can be overcome by changing the construction mode from one of the planar nature to one with a vertical structure as shown in Figure.
- As seen from this figure, all the elements of the planar MOSFET are present in the vertical metal-oxide silicon FET (or simply VMOS) the metallic surface connection to the terninalnsis a component designed to handle much larger.

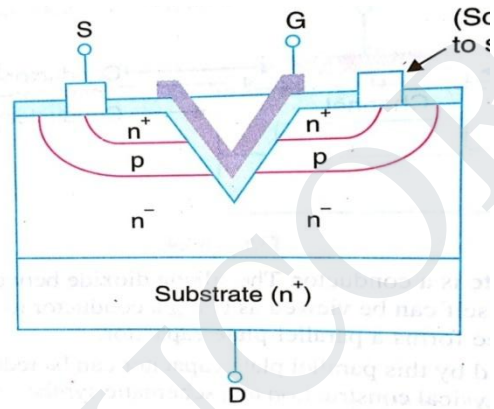


Figure : Illustrating the construction of VMOS

- The vertival MOSFET (or simply VMOS) is a component designed to handle much larger drain currents than the standard MOSFET.
- The current handling capability of the VMOS is a result of its physical construction which is illustrated in Fig. As seen from this figure, the component has materials that are labeled as P, N+ and N-.
- The N- material labels indicate the differences in doping levels. Also notice that there is no physical channel connecting the source (at top) and the drain (at bottom). Thus VMOS is an enchancement type MOSFET.
- With the V-shaped gate, a larger channel is formed by a positive gate voltage. With a large channel, the device is capable of handling a large amount of drain current.

OPERATION:

- The operation of the VMOS is illustrated in Fig. When a positive gate voltage is applied to the device, an N- type channel forms in the P-type region.
- This effective channel connects the source to the drain. As seen from Fig. the shape of the gate causes a wider channel to form than is created in the standard MOSFET.
- Because of this, the amount of drain current is much higher for this component. Moreover, the VMOS can exhibit a higher transconductance and a lower turn-on resistance than the conventional planer MOSFET.

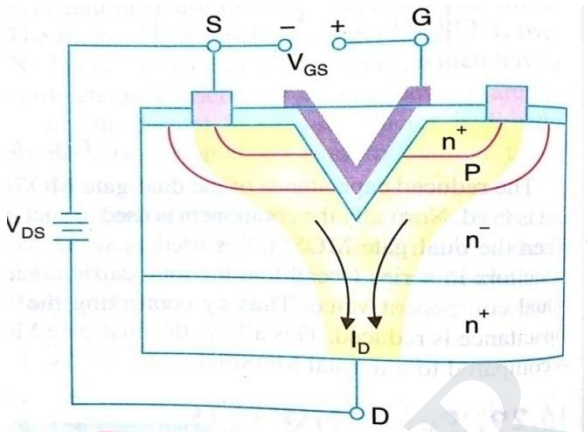


Fig. 16.27. Illustrating VMOS Opertor.

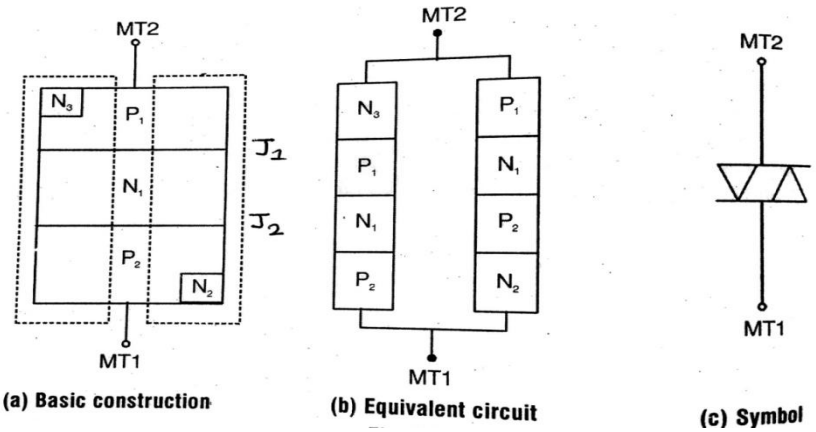
ADVANTAGES:

- It is not susceptible to thermal runway,
- The VMOS has a positive temperature coefficient. This means that the resistance of the component increases when temperature increases. Thus increases in temperature will cause a decrease in drain current.
- The VMOS device can be fabricated with more than one V- move to increase amount of drain current and some other performance characteristics.

7. Draw the V-I characteristics of TRIAC and DIAC & explain its operation. (M/J 2016)

DIAC (DIODE AC SWITCH):

- The DIAC is a two terminal device, which can pass current in either direction when the breakover voltage is reached in either polarity across the two terminals.
- The DIAC is a full-wave or bi-directional semiconductor switch that can be turned on in both forward and reverse polarities. The DIAC gains its name from the contraction of the words DIode Alternating Current.

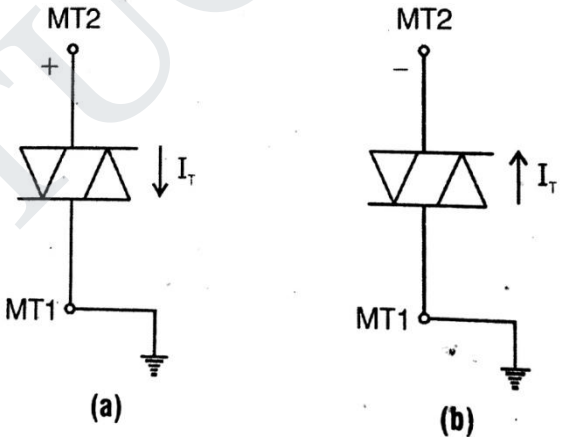


CONSTRUCTION:

- A diac consists of two 4-layer diodes connected in parallel but in opposite directions, The four layer diodes are P_1 N_1 P_2, N_2, and P_2 N_1 P_1 N_3.
- The diac has two main terminals namely MT1 and MT2.
- The diac can pass current in either direction depending upon the polarity of voltage across its main terminals. It can be turned ON only when the applied voltage across its main terminals reaches the breakover voltage.

OPERATION:

- When the applied voltage makes the MT2 positive with respect to MT1, the diac passes current through the diode P_1 N_1 P_2, N_2 from MT2 to MT1. [fig. (a)]
- If the applied voltage makes MT2 negative with respect to the MT1, the diac passes current through the diode P_2 N_1 P_1 N3 from MT1 to MT2. [fig. (b)]



- Diac acts as a switch in both directions. As the doping level at the two ends of the device is the same, the diac has identical characteristics for both positive and negative half of an ac cycle.
- The diac turns OFF when the current drops below the holding value.

V-I CHARACTERISTICS

- A diac can conduct in either direction, depending upon the polarity of the applied voltage across its main terminals.
- When a diac is operated with MT2 positive with respect to MT1. the V—I characteristic is obtained by the curve OAB.

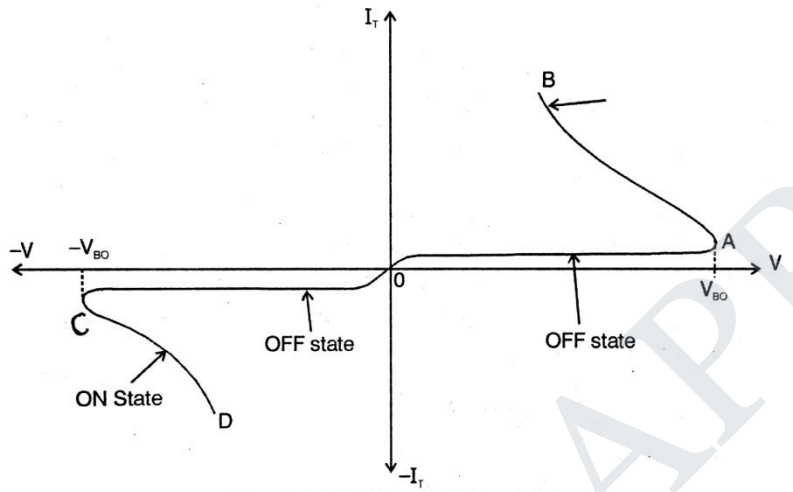


Fig. 2.161 VI Characteristics of DIAC

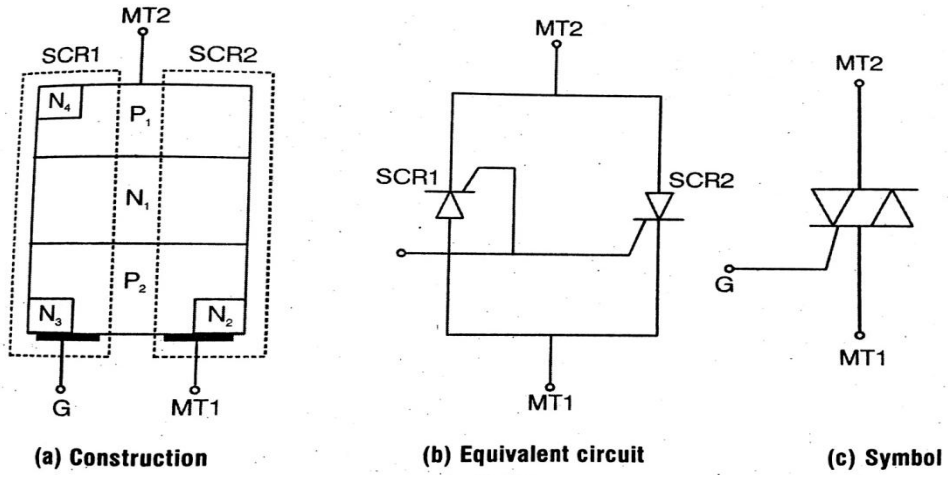
- Similarly, when the diac is operated with its MT2 negative with respect to MT1, the V—I characteristic is obtained by the curve OCD. The curves OAB and OCD are symmetrical and identical.
- The diode does not pass any current, until the applied voltage of either polarity reaches the breakover voltage. At the breakover voltage, the diac turns ON and the current through the diac increases rapidly. The operating voltage and currents are the same in either direction.

APPLICATIONS:

- It is used as a triggering device for TRIAC in phase control circuits such as light dimming , heat control and motor speed control etc.

TRIAC (TRIODE AC SWITCH):

- A triac is a three terminal device, which can conduct in either direction, when triggered either by a positive or a negative pulse irrespect of the polarity of the voltage across its main terminals.
- The triac behaves like two SCR's connected in parallel but in opposite directions with a common gate terminal.



- The anode and gate voltage applied in either direction will trigger the triac. It is due to the fact that the applied voltage will trigger atleast one of the SCR's connected in opposite direction.
- The triac consists of two four layer switches in parallel. These switches are P_1 N_1 P_2, N_2 and P_2 N_1 P_1 N_4.
- The triac has two main terminals, namely, main terminal 1[MT1] and main terminal 2 [MT2] and one gate terminal G
- The equivalent circuit of a triac consists of two SCR's connected in parallel but in opposite directions with a common gate terminal.

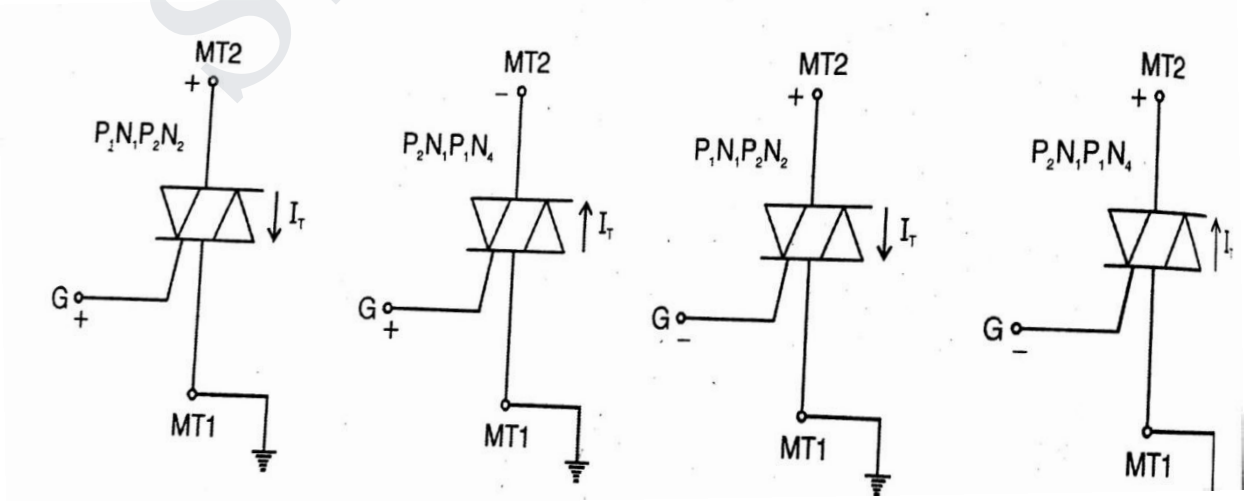
OPERATION:

(i)MT2 is positive and G is positive :

- In this mode, the operation of the triac is identical to SCR. The current flows through the switch P_1 N_1 P_2, N_2 from MT2 to MT1.

(ii)MT2 is negative and G is positive

- In this mode, the current flows through the switch P_2 N_1 P_1 N_4. from MT1 to MT2. This is an inefficient mode and must be avoided.



(iii) MT2 is positive and G is negative

- In this mode, the current flows through the switch P_1 N_1 P_2, N_2 from MT2 to MT1. This mode is less efficient than mode I but not as poor as mode 2.

(iv) MT2 is negative and G is negative

- In this mode, the current flows through the switch P_2 N_1 P_1 N_4 from MT1 to MT2. This mode is slightly less efficient than mode 1. The mode 1 and mode 4 are efficient modes in triac operation.
- Therefore these two modes are called normal modes of triac operation. The triac can be turned OFF only by reducing the device current below the holding value of the current.

V-I CHARACTERISTICS

- When the triac is operated with its main terminal: and gate both positive with respect to main terminal 1, the V---1 Characteristic is obtained by the curve OABC.
- Similarly, when the Triac is operated with its main terminal 2 and gate both negative with respect to main terminal 1, the V-1 characteristic is obtained by the curve marked ODEF.
- The curves OABC and ODEF are symmetrical and identical. The Triac if OFF until the applied voltage of either polarity (i.e., whether MT2 is positive with respect to MT1 or MT2 is negative w.r.t. MT1) exceeds the breakover voltage.
- As the applied voltage of either polarity exceeds the breakover voltage the triac turns ON and the voltage drop across the triac decreases to a low value (indicated by VH). The triac current increases to a value determined by the supply voltage and load resistance.

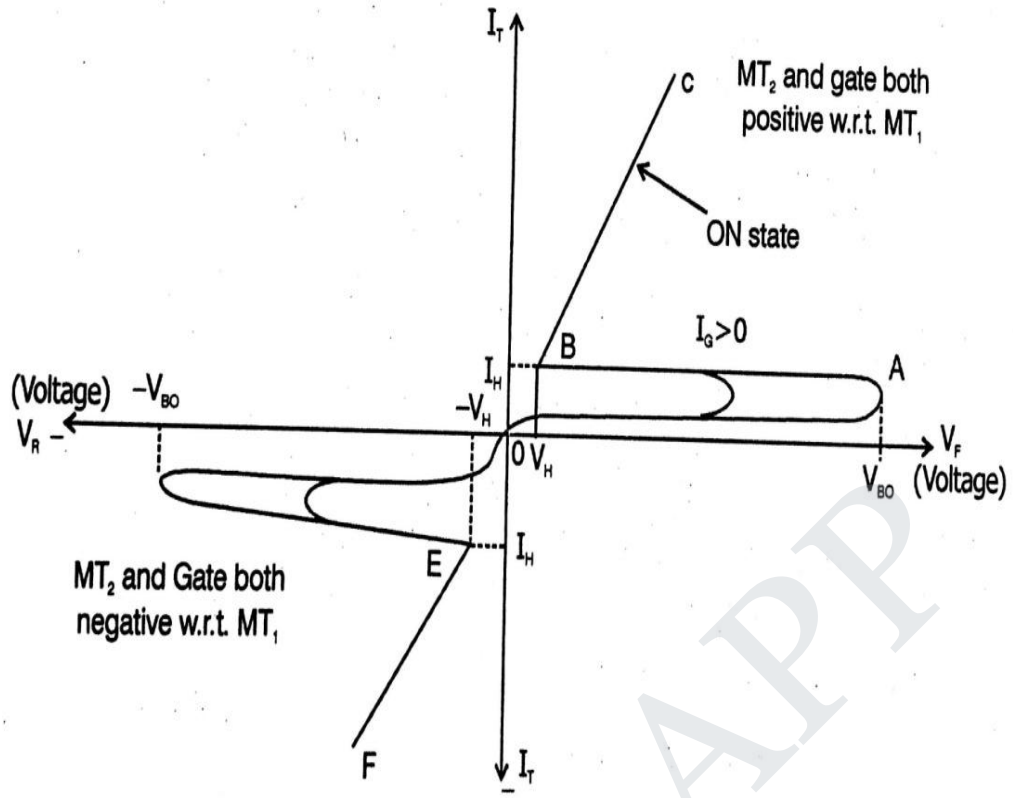


Fig. 2.158 VI Characteristics of TRIAC

- As the value of gate current is increased above zero ($I_G > 0$), the breakover voltage is lowered when the gate current of a suitable value is applied the triac turns ON at much lower breakover voltage.

APPLICATIONS:

- Phase control
- Motor speed control
- Heater control
- Light dimming control
- Static switch to turn AC power ON and OFF