EC8351 – ELECTRONIC CIRCUITS - I
- Bipolar Junction Transistor (BJT)

> Current Conduction: In Bipolar transistor because of both types of Charge carrier (Holes and electrons). Hence its called Bipolar Junction Transistor.

> 2 Basic types are NPN, PNP.

BJT Construction:

![BJT Diagram](attachment:image.png)

Base

i) Base Region is Very Thin and lightly doped.

ii) Emitter and Collector Region are heavily doped. But doping in emitter is greater than that of collector.

BJT Symbols:

![BJT Symbols](attachment:image.png)

Transistor Conventional Current Directions:

![Current Directions](attachment:image.png)
Electrons constitute the emitter current \( I_E \).

Assume that 100 electrons are injected into the base region.

The base region is very thin (say two electrons) and recombined with holes. This constitutes base current \( I_B \).

Remaining electrons, 98 appears in the collector. This constitutes collector current \( I_C \).

Emitter current \( I_E \) is always equal to the sum of base and collector currents \( I_B \) and \( I_C \).

\[
I_E = I_B + I_C
\]

Since \( I_B \) is very small, \( I_E = I_C \).

BJT Configurations:

1. Common Base
2. Common Collector
3. Common Emitter

Common Base Configuration:

\[
\alpha = \frac{I_C}{I_B}
\]
2. **Common Collector Configuration**

\[ y = \frac{I_E}{I_B} \]

3. **Common Emitter Configuration**

\[ B = \frac{I_C}{I_E} \]

- **CE Mode**
  - Input Resistance: Low, \( R_B \)
  - Output Resistance: High, \( R_C \)
  - Input Current: \( I_E \)
  - Output Current: \( I_C \)
  - Input Voltage: \( V_{BE} \)
  - Output Voltage: \( V_{CE} \)
  - Current Gain: High
  - Voltage Gain: High
  - Applications: Audio Signal Amplification

**Why CE Configuration is widely used in Amplifiers?**

- The CE Configuration is the only
configuration which provides both voltage gain as well as current gain greater than unity.
CB Configuration: Current gain less than unity.
CC Configuration: Voltage gain is less than unity.
Power gain is much greater than other two configurations.

Ratio of output resistance to input resistance is small, range from 10 to 100. This makes an ideal for coupling between transistor stages.

Topic 1: DC LOAD LINE & OPERATING POINT:

1) 8m
   What is DC loadline? How you will select the operating point, explain its Common Emitter Configuration with an example. (8m)

2) 8m
   Describe how DC load line is drawn? (8m)

Ans:

What is d.c. biasing of the transistor?
What is the Need for Biasing BJT?
What is called operating point?

1) D.C. Biasing:

→ In Active Region, Emitter Base junction is forward biased and Collector Base junction is reverse biased.

→ In order to operate transistor in the desired region (Active Region), we have to apply external d.c. voltage of correct polarity and magnitude to the two junctions of the transistor.

→ Because d.c. voltages are used to bias the transistor, biasing is known as d.c. biasing of the transistor.

→ In Transistor circuits, output signal
Power is always greater than input signal power.

→ The d.c. sources (d.c. biasing) supplies the power to the transistor circuit to get the output signal power greater than input signal power.

→ When we bias a transistor we establish a certain current and voltage conditions for the transistor. These conditions are known as operating conditions (or) d.c. operating point (or) quiescent point.

→ The operating point must be stable for proper operation of the transistor.

→ Operating point shifts with changes in transistor parameters such as β (current gain),
  \[ \times 2 \Delta \]
  \[ I_C \text{ [Reverse Saturation Current]} \]
  \[ V_{BE} \text{ [Base Emitter Voltage]} \]

→ As transistor parameters are temperature dependent, operating point also varies with changes in temperature.

→ For proper operation of transistor, fixed level of current and voltage in the transistor defined a point at which transistor operates. This point is called operating point (or) quiescent (or) Q-point or Active region.

Draw and explain "fixed bias" circuit.

Ans: → Let us consider fixed bias circuit.

For d.c. analysis, replace capacitor with an open circuit because reactance of a capacitor for d.c.

\[ X_C = \frac{1}{2\pi fC} \Rightarrow \frac{1}{2\pi (0)} = \infty \]
CIRCUIT ANALYSIS:

i) Base circuit of the fixed bias circuit:

Applying Kirchhoff's Voltage law to the base circuit,

\[ V_{CC} - I_B R_B - V_{BE} = 0 \]
\[ V_{CC} - V_{BE} = I_B R_B \]

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \]  \( \text{(1)} \)

\[ V_{BE} = 0.7 \text{V} \]
\[ V_{BE} = 0.3 \text{V} \]

\[ \begin{align*}
\text{Input Signal} & \rightarrow V_{BE} = 0.7 \text{V} \\
\text{Ground} & \rightarrow V_{BE} = 0.3 \text{V}
\end{align*} \]  \( \text{(2)} \)

ii) Collector circuit of the fixed bias circuit:

Applying Kirchhoff's Voltage law to the collector circuit,

\[ V_{CC} - I_C R_C - V_{CE} = 0 \]
\[ V_{CE} = V_{CC} - I_C R_C \]  \( \text{(3)} \)
\[ V_{CC} - V_{CE} = I_C R_C \]
\[ I_C = \frac{V_{CC} - V_{CE}}{R_C} \]  \( \text{(4)} \)
(iv) \[ V_{BE} = V_B - V_E \quad \rightarrow \quad (a) \]
\[ V_{CE} = V_C - V_E \quad \rightarrow \quad (b) \]

- \( V_B \rightarrow \text{Base Voltage} \)
- \( V_E \rightarrow \text{Emitter Voltage} \)
- \( V_C \rightarrow \text{Collector Voltage} \)

\[ V_E = 0 \quad (\text{in the circuit}) \]

- \( V_{BE} = V_B \quad (\text{from } \text{a}) \)
- \( V_{CE} = V_C \quad (\text{from } \text{b}) \)

- Base current \( I_B \) is controlled by \( R_E \).
- Collector current \( I_C \) is not a function of \( R_E \).
- Changing \( R_E \) to any level will not affect \( I_C \).

**Proper Biasing:**

Transistor is used as an amplifier, the Q point should be selected at the center of the DC loadline to prevent any possible distortion.

**What is meant by Loadline?**

A DC loadline of a transistor is the straight line drawn on the output characteristics of the transistor.

- In saturation region, \( I_C \) is a function of \( V_{CE} \) and \( I_B \) is constant.
- In active region, \( I_C \) is a function of \( I_B \) and \( V_{CE} \) is constant.
- In cutoff region, \( I_C \) is constant and \( V_{CE} \) is zero.
\[ I_c = \frac{V_{cc} - V_{ce}}{R_c} \]

\[ = \frac{V_{cc}}{R_c} - \frac{1}{R_c} V_{ce} \]

\[ I_c = -\frac{1}{R_c} V_{ce} + \frac{V_{cc}}{R_c} \quad \rightarrow \quad (A) \]

Equation of straight line, \( y = mx + c \) \( \rightarrow \quad (B) \)

To determine the two points \( A' \) and \( B' \), we assume

\[ I_c = \frac{V_{cc} - V_{ce}}{R_c} \quad \rightarrow \quad (C) \]

a) \( V_{ce} = V_{cc} \) \( \rightarrow \quad (C) \), \( I_c = \frac{V_{cc} - V_{cc}}{R_c} \), \( I_c = 0 \)

b) \( V_{ce} = 0 \) \( \rightarrow \quad (C) \), \( I_c = \frac{V_{cc} - 0}{R_c} \), \( I_c = \frac{V_{cc}}{R_c} \)

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**Ic (mA)**

- D.C. Load Line
- Active Region
- \( I_B = 0 \text{mA} \)
- \( I_B = 10 \text{mA} \)
- \( I_B = 20 \text{mA} \)

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**Fig:** CE-output characteristics with d.c. load line

Line drawn between points \( A' \) and \( B' \) is called d.c. Load Line.

\( \text{d.c.} \) indicates (i.e) input signal is assumed to be zero.
(a) Selection of Operating Point:

Case (i) Operating point near saturation region gives clipping at positive peaks.

Case (ii) Operating point near cut-off region gives clipping at negative peaks.

Case (iii) Operating point at the centre of active region is most suitable.

\[ V_{BE} \text{ for } S_i = 0.7\lambda, \ G_{fe} = 0.3\lambda \]
Designing the biasing circuit, care should be taken so that the operating point will not shift into an undesirable region (cut-off & saturation region). Hence biasing the circuit to stabilize the Q-point is known as bias stability.

- Two important factors are:
  1. Temperature
  2. \( \frac{h_{fe}}{\beta} \)

**Temperature:**

a) \( I_{co} \): Flow of current in the circuit produces heat at the junctions. This heat increases the temperature at the junctions.

\[
I_c = I_{BE} + I_{CO}
\]

Power dissipation, \( P_d = V_e I_c \)

Heat (Excess) produced at the collector-base junction may even burn and destroy the transistor. This situation is called Thermal Runaway.

b) \( V_{BE} \): \( V_{BE} \) changes with temperature at a rate of 2.5mV/°C. \( I_B \) depends on \( V_{BE} \), \( I_C \) depends on \( I_B \) and \( V_{BE} \).

c) \( B \): It is temperature dependent. \( B \) varies, \( I_C \) also varies. \( I_C = B I_B \). Change in \( I_C \) change the operating point.
Avoid the thermal instability by biasing the circuit. It should be designed to provide a degree of temperature stability.

1) Transistor current gain $\frac{hfe}{\beta}$:

- Changes in the transistor parameters among different units of the same type, same number.

(x) Advantages of fixed Bias:

- Simple circuit because of few components
- Operating point can be fixed anywhere in the Active Region
- Maximum flexibility in the design.

(x) AC LOAD LINE:

Explain AC Load Line with diagram. Draw it.

Ans: → position of Q-point is constant when we do AC Analysis (on) DC Analysis.
- Capacitive act as Short Circuit.
  \[ X_C = \frac{1}{2\pi f C} \quad f \uparrow \quad X_C \downarrow \]
- DC Source → Shunted
Problems

1. Ac/DC Loadline operation point

2. Triode bias circuit: $I_{B}, I_{C}$, $V_{BE}$

3. Effect of $V_{CE}$ on the load line

4. Effective resistance decreases, current increases

5. $V_{T} = kT/R$
From the above circuit, \( R_c = 8 \Omega \), \( R_L = 24 \Omega \) and \( V_{cc} = 24 \text{V} \). Draw the DC Load Line and determine the operating point values. Also find the AC Load Line.

**Solution:**

1. **DC Load Line**
   - Apply KVL to the collector circuit.
   - \( V_{cc} - I_c R_c - V_{ce} = 0 \) → (1)

   i) Find \( V_{ce} \): \([I_c \rightarrow 0]\)
   - From eqn (1): \( 24 - I_c \times 8000 - V_{ce} = 0 \)
   - \( 24 - 0 - V_{ce} = 0 \)
   - \( V_{ce} = 24 \text{V} \)

   ii) Find \( I_c \): \([V_{ce} \rightarrow 0]\)
   - From eqn (1): \( 24 - I_c \times 8000 - 0 = 0 \)
   - \( 24 = I_c \times 8000 \)
   - \( I_c = \frac{24}{8000} \)
   - \( I_c = 3 \times 10^{-3} \text{A} \)
   - \( I_c = 3 \text{mA} \)

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**Graph:**

- DC Load Line
  - \( I_c = 3 \text{mA} \)
  - \( V_{ce} = 24 \text{V} \)
i) \[ \text{Max } V_{ce} = V_{ceq} + I_{cq}.R_{ac} \]

\[ \text{Max } V_{ce} = 12 + 1.5 \ \text{mA} \times 6 \ \text{k} \Omega \rightarrow \text{(A)} \]

ii) \[ V_{ceq} = \frac{V_{ce}}{2} = \frac{12}{2} = 6 \ \text{V} \]

iii) \[ I_{cq} = \frac{I_c}{2} = \frac{3 \ \text{mA}}{2} = 1.5 \ \text{mA} \]

iv) \[ R_{ac} = R_e \parallel R_L \]

\[ R_e = 8 \ \text{k} \Omega, \ R_L = 24 \ \text{k} \Omega \]

\[ R_e = 6 \ \text{k} \Omega \]

Max \[ V_{ce} = 12 + 1.5 \times 6 \times 10^{-3} \]

\[ \text{Max } V_{ce} = 14 \ \text{V} \]

Max \[ I_c = I_{cq} + \frac{V_{ceq}}{R_{ac}} \]

\[ I_c = 1.5 \times 10^{-3} + \frac{6}{6 \times 10^{-3}} \]

\[ I_c = 1.5 \times 10^{-3} + 2 \times 10^{-3} \]

\[ \text{Max } I_c = 3.5 \times 10^{-3} \ \text{A} \]

\[ \text{Max } I_c = 3.5 \ \text{mA} \]
2) Draw the D.C. Load Line, find \( I_c \) and \( V_{CE} \)

Given \( R_c = 12k \Omega \), \( V_{CC} = 20V \) for fixed bias.

Solution:

From the Fixed Bias Circuit,

\[ V_{CC} - I_c R_c - V_{CE} = 0 \quad \Rightarrow \quad (1) \]

i) Put \( I_c = 0 \) in (1) \( [\text{pt } 'A' ] \)

\[ V_{CC} - 0 - V_{CE} = 0 \]

\[ V_{CC} = V_{CE} \]

\[ V_{CE} = 20V \]

ii) Find \( I_c \). Put \( V_{CE} = 0 \) in (1) \( [\text{pt } 'B'] \)

\[ V_{CC} - I_c R_c - 0 = 0 \]

\[ V_{CC} = I_c R_c \]

\[ I_c = \frac{V_{CC}}{R_c} \]

\[ I_c = \frac{20}{12 \times 10^3} \]

\[ I_c = 1.7 \times 10^{-3} A \quad (\text{or}) \quad 1.7 mA \]

Find the points \( 'A' \) and \( 'B' \) for the given fixed bias values, \( V_{CC} = 20V \), \( R_c = 10k \Omega \).

Solution:

i) Find \( V_{CE} \). (pt \( 'A' \)) \( I_c = 0 \)

\[ V_{CC} - V_{CE} - I_c R_c = 0 \]

\[ V_{CC} - V_{CE} = 0 \]

\[ V_{CC} = V_{CE} \Rightarrow V_{CE} = 20V \]
\[ \text{Find } I_C : \begin{align*}
I_C &= \frac{V_C}{R_C} \\
V_C - I_C R_C - V_{CE} &= 0
\end{align*} \]
\[ \text{Put } V_{CE} = 0 \]
\[ V_C - I_C R_C = 0 \]
\[ I_C = \frac{V_C}{R_C} = \frac{20}{10 \times 10^3} \]
\[ I_C = 2 \times 10^{-3} \text{ A (or) 2 mA} \]

\[ \text{Draw the Load Line for the fixed bias, then} \]
\[ I_B = 20 \mu A, \quad V_C = 20 \text{ V}, \quad R_C = 10 \text{ k}\Omega, \quad \beta = 100 \]

**Solution:**

1) \( \beta = \frac{I_C}{I_B} \)

\[ \beta \times I_B = I_C \]
\[ I_C = \frac{50 \times 20 \times 10^{-6}}{1000 \times 10^{-6}} \]
\[ I_C = 1000 \times 10^{-6} \]
\[ I_C = 1 \times 10^{-3} \text{ (or) 1 mA} \]

2) \( \text{Find } V_{CE} : \)

\[ V_C - I_C R_C - V_{CE} = 0 \]
\[ 20 - (1 \times 10^{-3}) \times (10 \times 10^3) = V_{CE} \]
\[ 20 - 10 = V_{CE} \]
\[ V_{CE} = 10 \text{ V} \]
\[ I_B = 30 \mu A, \beta = 50, V_{cc} = 20 V, R_c = 10 k\Omega. \]

\[ V_{ce} \text{ and } I_c ? \]

\( \text{Soln:} \)

\( i) \) Find \( V_{ce} \) at Point A

\[ V_{cc} - V_{ce} - I_c R_c = 0 \quad \text{(1)} \]

\( ii) \) \[ \beta = \frac{I_c}{I_B} \]

\[ I_c = \beta \cdot I_B \]

\[ = 50 \times 30 \times 10^{-6} \]

\[ I_c = 1.5 \times 10^{-3} \text{ (or) } 1.5 \text{ mA} \quad \text{(2)} \]

Sub (2) in (1)

\[ 20 - V_{ce} - (1.5 \times 10^{-3}) \times (10 \times 10^3) \]

\[ V_{ce} = 20 - 15 \]

\[ V_{ce} = 5 V \]

\( \text{(b) Design a fixed bias circuit using a silicon transistor having } \beta \text{ value of 100. } V_{cc} \text{ is } 10 V \text{ and d.c. bias conditions are to be } V_{ce} = 5 V \text{ and } I_c = 5 \text{ mA.} \]

\( \text{Soln:} \)

Given: \( \beta = 100 \)

\[ V_{cc} = 10 V \]

\[ V_{ce} = 5 V \]

\[ I_c = 5 \text{ mA} \]

\( i) \) Apply KVL in collector circuit,

\[ V_{cc} - I_c R_c - V_{ce} = 0 \]

Find \( R_c \)

\[ R_c = \frac{V_{cc} - V_{ce}}{I_c} \]

\[ = \frac{10 - 5}{5 \times 10^{-3}} \Rightarrow \frac{5}{5 \times 10^{-3}} \]

\[ R_c = 1 k\Omega \]
(11) Applying KVL in the Base circuit,

\[ V_{cc} - I_B R_B - V_{BE} = 0 \]

\[ R_B = \frac{V_{cc} - V_{BE}}{I_B} \]

\[ = \frac{10 - 0.7}{50 \times 10^{-6}} \]

\[ = \frac{10 - 0.7}{50 \times 10^{-6}} \]

\[ R_B = 186 \times 10^3 \text{ (ohm) } 186 \text{ k}\Omega \]

**Fixed Bias Circuit**

- \( V_{cc} = 10 \text{V} \)
- \( I_B = 50 \mu\text{A} \)
- \( R_B = 186 \text{k}\Omega \)
- \( R_c = 1 \text{k}\Omega \)
- \( V_{CE} \)
- \( V_{BE} \)

The fixed biased circuit in Fig is subjected to an increase in junction temperature from 25°C to 75°C. If \( \beta = 100 \) at 25°C and \( \beta = 125 \) at 75°C, determine percent change in Q point values (\( V_{CE}, I_c \)) over the temperature range. Neglect any change in \( V_{BE} \).
At 25°C,

1) Apply KVL to Base Ckt.

\[ V_{cc} - I_B R_B - V_{BE} = 0 \]

\[ I_B = \frac{V_{cc} - V_{BE}}{R_B} \]

\[ I_B = \frac{12 - 0.7}{100 \times 10^3} \]

\[ I_B = 113 \times 10^{-6} \text{ (cm)} \]

\[ I_B = 113 \text{ mA} \]

2) Apply KVL to Collector Ckt.

\[ V_{cc} - I_C R_C - V_{CE} = 0 \]

\[ V_{CE} = V_{cc} - I_C R_C \]

\[ V_{CE} = 12 - (11.3 \times 10^{-3}) \times 600 \]

\[ V_{CE} = 5.22 \text{ V} \]

\[ \beta = \frac{I_C}{I_B}, \quad I_C = \beta I_B \]

\[ I_C = 100 \times 113 \times 10^{-6} \]

\[ I_C = 11.3 \times 10^{-3} \text{ (cm)} \]

\[ I_C = 113 \text{ mA} \]

\[ \% \text{ change in } I_C = \frac{I_C(75°C) - I_C(25°C)}{I_C(25°C)} \times 100 \% \]

\[ = \frac{(14.125 \times 10^{-3}) - (11.3 \times 10^{-3})}{(11.3 \times 10^{-3})} \times 100 \% \]

\[ = 25 \% \text{ (an increase)} \]

\[ \% \text{ change in } V_{CE} = \frac{V_{CE}(75°C) - V_{CE}(25°C)}{V_{CE}(25°C)} \times 100 \% \]

\[ = \frac{3.525 - 5.22}{5.22} \times 100 \% \]

\[ = -32.47 \% \text{ (a decrease)} \]
Given in the fig.

\[ I_c = \frac{V_{cc}}{R_c} = 10 \]  

A point

\[ I_{Bq} = 40 \, \mu A \]

\[ 20 \, V = V_{CE} = V_{cc} \]

**Solution:**

i) **Fixed Bias Ckt, \( V_{cc} \)**

\[ V_{CE} = V_{cc} = 20 \, V \]

\[ I_c = \frac{V_{cc}}{R_c} = 10 \times 10^{-3} \]

\[ 10 \times 10^{-3} = \frac{20}{R_c} \]

\[ R_c = \frac{20}{10 \times 10^{-3}} \]

\[ R_c = 2 \, k \Omega \]

ii) **Find \( R_c \):**

\[ V_{CE} = V_{cc} = 20 \, V \]

\[ I_c = \frac{V_{cc}}{R_c} = 10 \times 10^{-3} \]

\[ 10 \times 10^{-3} = \frac{20}{R_c} \]

\[ R_c = \frac{20}{10 \times 10^{-3}} \]

\[ R_c = 2 \, k \Omega \]

iii) **Apply KVL at Base Ckt**

\[ V_{cc} - \theta R_B - V_{BE} = 0 \]

\[ R_B = \frac{V_{cc} - V_{BE}}{\theta} = \frac{20 - 0.7}{40 \times 10^{-6}} \]

\[ R_B = 482.5 \, k \Omega \]

\[ \theta V_{BE} = 0.7 \]

\[ I_B = 40 \, \mu A \]

from fig.
For the circuit shown in the fig, calculate $I_E$, $I_C$, $V_C$, $V_B$, $V_C$, $V_B$, $V_{CC}$. Assume $V_{BE} = 0.7V$ and $\beta = 50$.

### Solution:

1. **Applying KVL to the Base Circuit**, \( V_{CC} - I_B R_B - V_{BE} = 0 \)
   
   \[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \]
   
   \[ I_B = \frac{10 - 0.7}{220 \times 10^{-3}} = \frac{9.3 \times 10^{-3}}{220} = 42.27 \times 10^{-6} \text{ (or) } 42.27 \text{ mA} \]

2. **$\beta$**, \( \beta = \frac{I_C}{I_B} \)
   
   \[ I_C = \beta \times I_B \]
   
   \[ I_C = 50 \times (42.27 \times 10^{-6}) = 2.1135 \times 10^{-3} \text{ (or) } 2.135 \text{ mA} \]

3. **Applying KVL to the Collector Circuit**, \( V_{CC} - I_C R_C - V_{CE} = 0 \)
   
   \[ V_{CE} = V_{CC} - I_C R_C \]
   
   \[ = 10 - (2.1135 \times 10^{-3})(1.2 \times 10^3) \]
   
   \[ V_{CE} = 10 - 2.5362 \]
   
   \[ V_{CE} = 7.4638 \text{ V} \]
\[ V_{EB} = 0 \]
\[ V_{BE} = V_{B} \]
\[ V_{B} = 0.7 \text{V (for Si)} \]

\[ V_{C} = \]
\[ V_{CE} = V_{C} - V_{E} \]
\[ V_{E} = 0 \]
\[ V_{c} = 7.4638 \text{V} \]

\[ V_{BC} = V_{B} - V_{C} \]
\[ = 0.7 - 7.4638 \]
\[ = -6.7638 \text{V} \]

**Negative sign indicates base collector junction is reverse biased.**

**In the circuit showing:**

**i)** \( R_{B} = 300 \text{k}\Omega \)

Apply KVL at Base,
\[ V_{CC} - I_{B}R_{B} - V_{BE} = 0 \]
\[ I_{B} = \frac{V_{CC} - V_{BE}}{R_{B}} \]
\[ I_{B} = \frac{10 - 0.7}{300 \times 10^{-3}} \]
\[ I_{B} = 0.031 \text{mA} \]
\[ \text{(Si)} \]
\[ I_{B} = 0.31 \text{mA} \]

**ii)** \( R_{B} = 150 \text{k}\Omega \)

Apply KVL at Base,
\[ V_{CC} - I_{E}R_{B} - V_{BE} = 0 \]
\[ I_{B} = \frac{V_{CC} - V_{BE}}{R_{B}} \]
\[ I_{B} = \frac{10 - 0.7}{150 \times 10^{-3}} \]
\[ I_{B} = 0.062 \text{mA} \]
\[ \text{(Si)} \]
\[ I_{B} = 62 \mu\text{A} \]
\[ I_c = \beta I_B \]
\[ I_c = 100 \times 3.1 \mu A \]
\[ I_c = 3.1 \text{mA} \]

Apply KVL at collector,
\[ V_{cc} - I_c R_C - V_{ce} = 0 \]
\[ V_{ce} = V_{cc} - I_c R_C \]
\[ = 10 - (3.1 \times 10^{-3}) \times (2 \times 10^3) \]
\[ V_{ce} = 10 - 6.2 \]
\[ V_{ce} = 3.8 \text{V} \]

Comment:
\[ V_{ce} \text{(active)} > V_{ce} \text{(sat)} \]
Assumption that transistor is in active region.

\[ \text{iii) Apply KVL to base,} \]
\[ V_{cc} - I_B R_B + V_{BE(sat)} \]
\[ I_B = \frac{V_{cc} - V_{BE(sat)}}{R_B} \]
\[ I_B = \frac{10 - 0.8}{150 \times 10^3} \]
\[ I_B = 61.33 \mu A \]

Apply KVL to collector,
\[ V_{cc} - I_c R_C - V_{ce} \text{(sat)} \]
\[ I_c = \frac{V_{cc} - V_{ce(sat)}}{R_c} \]
\[ I_c = \frac{10 - 0.2}{2 \times 10^3} \]
\[ I_c = 4.9 \text{mA} \]

\[ \text{Justify transistor in saturation, } I_B > I_c / \beta \]
\[ \frac{I_c}{\beta} = \frac{4.9 \times 10^{-3}}{100} = 0.049 \mu A \]

\[ I_B = 10 \text{mA} \]
\[ I_c = 6.2 \text{mA} \]

Apply KVL at collector,
\[ V_{cc} - I_c R_C - V_{ce} = 0 \]
\[ V_{ce} = V_{cc} - I_c R_C \]
\[ = 10 - (6.2 \times 10^{-3}) \times (2 \times 10^3) \]
\[ V_{ce} = 10 - 12.4 \]
\[ V_{ce} = -2.4 \text{V} \]

Assumption that transistor is in saturation region.
The Various types of Biasing Circuits Are:
1. Fixed Bias Circuit (or) Base Resistance Method
2. Collector to Base Bias Circuit
   - Modified Collector to Base Bias Circuit
3. Voltage divider (or) Self-Bias Circuit
4. Emitter Stabilized Bias Circuit

1. Fixed Bias Circuit - Stability:

- Derive an expression for the stability factor for fixed bias method.
- Draw and explain fixed bias method.
- Describe the stability in fixed bias.
- What are the methods of BJT Biasing?
   - All Methods
- Different types of Biasing circuit methods.
- Explain the method of stabilizing Q-point

\[ \text{Ans:} \]

![Image of fixed bias circuit](image_url)

**Fig (a): Fixed Bias Circuit**
As temperature increases, collector current increases and hence base current decreases.

\[ \text{Temp} \uparrow, \ I_c \uparrow, \ I_B \downarrow \]

→ \(R_B, \ R_e, \ V_{cc}\) are fixed. As they have fixed value, \(I_B\) is maintained constant. When \(I_c\) increases, so we cannot achieve the good stabilization. So, it is called as "fixed bias".

i) Input side loop [Base]

\[ V_{cc} \]
\[ \downarrow I_B \]
\[ R_B \]
\[ V_{BE} \]
\[ + \]
\[ B \]
\[ \uparrow \]
\[ E \]

Apply Kirchhoff's Voltage law on base circuit,

\[ V_{cc} - I_B R_B - V_{BE} = 0 \]

\[ I_B = \frac{V_{cc} - V_{BE}}{R_B} \]

Base current \((I_B)\):

\[ I_B = \frac{V_{cc} - V_{BE}}{R_B} \]

\(R_B \rightarrow \text{Constant}, \ V_{cc} \rightarrow \text{Constant} \)

ii) Output side loop [Collector]

\[ V_{cc} \]
\[ \downarrow I_c \]
\[ R_c \]
\[ V_{CE} \]

\[ V_{BE} = \begin{cases} 0.3 \rightarrow \text{Gpe} \\ 0.7 \rightarrow 8 \text{p} \end{cases} \]
(CON ON condition)
Apply Kirchhoff’s Voltage law on collector circuit:

\[ V_{cc} - I_c R_e - V_{ce} = 0 \]
\[ V_{cc} - V_{ce} = I_c R_c \]

Collector current (I_c):

\[
I_c = \frac{V_{cc} - V_{ce}}{R_c} \rightarrow (a)
\]

\[ V_{ce} = V_{cc} - I_c R_c \rightarrow (b) \]

When we take biasing circuit, the Q-point does not lie exactly at the centre of the Active Region.

\[ B = \frac{I_c}{I_B} \]

\[ I_c = B I_B \]

\[ V_{ce} = V_c - V_e \]
\[ V_{be} = V_B - V_e \]
\[ V_e = 0 \] (Emitter Voltage)

\[ V_{ce} = V_c \]
\[ V_{be} = V_b \]

**Stability Factors:**

Definition: Stability factor, which indicates degree of change in operating point due to variation in temperature.

Stability factors are:

\[
S = \frac{\delta I_c}{\delta I_c_0} \quad | \quad V_{be}, B \text{ constant} \\
S' = \frac{\delta I_c}{\delta V_{be}} \quad | \quad I_c, B \text{ constant} \\
S'' = \frac{\delta I_c}{\delta B} \quad | \quad V_{be}, I_c \text{ constant}
\]
Ideally, Stability factor should be perfectly zero to keep operating point stable.

Practically, stability factor should have value as minimum as possible.

Thermal stability of a circuit is assessed by defining a stability factor, $S$.

\[ S = \frac{\Delta I_c}{\Delta I_{CEO}} \]

1. **Stability factor, $S$** - **Fixed Bias**

For a CE configuration, $I_C$ is given as,

\[ I_C = \beta I_B + I_{CEO} \]

Diff on both sides,

\[ \Delta I_C = \beta \Delta I_B + (1+\beta) \Delta I_{CEO} \]

\[ \frac{\Delta I_C}{\Delta I_C} = \frac{\beta \Delta I_B + (1+\beta) \Delta I_{CEO}}{\Delta I_C} \]

\[ 1 = \beta \frac{\Delta I_B}{\Delta I_C} + (1+\beta) \frac{\Delta I_{CEO}}{\Delta I_C} \]

\[ 1 - \beta \frac{\Delta I_B}{\Delta I_C} = (1+\beta) \frac{\Delta I_{CEO}}{\Delta I_C} \]

\[ \frac{\Delta I_{CEO}}{\Delta I_C} = \frac{1-\beta \left[ \frac{\Delta I_B}{\Delta I_C} \right]}{1+\beta} \]

\[ S = \frac{1+\beta}{1-\beta \left[ \frac{\Delta I_B}{\Delta I_C} \right]} \]
\[ \text{from eqn} \ 1 \Rightarrow I_c = \beta I_B + (1+\beta) I_{CBO} \]

\[ I_c = \beta \left( \frac{V_{cc} - V_{BE}}{R_B} \right) + (1+\beta) I_{CBO} \]

\[ \therefore I_B = \frac{V_{cc} - V_{BE}}{R_B}, \text{ for fixed bias} \]

\[ I_c = \frac{\beta V_{cc}}{R_B} - \frac{\beta V_{BE}}{R_B} + (1+\beta) I_{CBO} \]
Diff w.r.t. $V_{BE}$,
\[
\frac{dI_C}{dV_{BE}} = \frac{0 - \beta}{R_B} + 0
\]
\[
S = -\frac{\beta}{R_B} \quad \rightarrow (6)
\]

\[s'' = \frac{dI_C}{\beta} \bigg|_{V_{BE}, I_{C0} \text{ constant}}
\]

From eqn (5),
\[
I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + \frac{(1 + \beta) I_{C0}}{R_B}
\]
Diff w.r.t. $\beta$,
\[
\frac{dI_C}{d\beta} = \frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B} + \frac{I_{C0}}{R_B}
\]
\[
= \frac{V_{CC} - V_{BE}}{R_B} + \frac{I_{C0}}{R_B}
\]
\[
\frac{dI_C}{d\beta} = I_B + I_{C0}
\]
\[
\frac{dI_C}{d\beta} = \frac{I_C}{\beta} \quad \left( \therefore \frac{V_{CC} - V_{BE}}{R_B} = I_B \right)
\]
\[I_B \gg I_{C0}
\]
\[I_B = \frac{I_C}{\beta} \]

(\text{A}) Relation between $s$ and $s'$:
\[
s = 1 + \beta
\]
\[
s' = -\frac{\beta}{R_B}
\]
Multiply $(1 + \beta)$ in $s'\!$, \[
-\frac{\beta (1 + \beta)}{R_B (1 + \beta)}
\]
\[
s' = -\beta s
\]
Relation between $s$ and $s''$:

\[ s = 1 + \beta \]

\[ s'' = \frac{I_c}{\beta} \]

Multiply $(1 + \beta)$ in $s''$ in Eq. 2 or

\[ s'' = \frac{I_c (1 + \beta)}{\beta (1 + \beta)} \]

\[ s'' = \frac{I_c s}{\beta (1 + \beta)} \]

**Diagram Explanation:**

- It shows the d.c. bias with voltage feedback.
- It is also called the Collector to base bias circuit.
- It is an improvement over the fixed bias.
- Biasing resistor is connected between collector and base of the transistor to provide a feedback path.
- Thus, $I_B$ flows through $R_B$ and $(I_C + I_B)$ flows through the $R_e$. 
Disadvantages of fixed bias:

(*) This circuit does not provide any check on the collector current which increases with the rise in temperature i.e. thermal stability is not provided by this circuit. So, operating point is not maintained.

\[ I_c = \beta I_B + I_{CEO} \]

(*) Since \( I_c = \beta I_B \) and \( I_B \) is already fixed, \( I_c \) depends on \( \beta \) which changes unit to unit and shifts the operating point.

(*) Thus, stabilization of operating point is very poor in the fixed bias circuit.

Circuit Analysis:

→ As temperature increases, \( I_c \) increases. Result, drop across the collector resistance increases, so \( V_{CE} \) drop decreases.

→ When \( V_{CE} \) decreases, \( I_B \) also decreases → drop across decreases \( R_B \).

\[ V_{CE} = V_{BE} + V_{CB} \]

It provides good stability.

\[ \text{Temp} \uparrow \rightarrow I_c \uparrow \rightarrow V_{BC} \uparrow \rightarrow V_{CE} \downarrow \]

When \( I_B \downarrow \), \( I_C \downarrow \), \( \downarrow R_B \) \[ \rightarrow V_{CB} \downarrow \]

*Input Side Loop - Base Circuit:

\[ V_{CC} \]

\[ R_B \downarrow \rightarrow I_C + I_B = I_C \]
Applying the voltage divider rule, we have:

\[ V_{CC} - (\frac{1}{R_C+R_B}) V_{CE} - V_{BE} = 0 \]

The feedback loop around the collector circuit results in a reflection of the resistance \( R_C \) to the input circuit.

The difference only for fixed bias will be this topic.

\[ \begin{align*}
\text{I}_B &= \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C} \\
\text{I}_C &= \frac{V_{CC} - V_{BE}}{R_B + R_C} \\
\text{V}_{CE} &= \frac{(R_C + R_B) \text{I}_B + \text{R}_C + V_{BE}}{R_B + R_C} \\
\text{V}_{BE} &= \frac{(R_C + R_B) \text{I}_B + \text{R}_C + V_{BE}}{R_B + R_C}
\end{align*} \]
\[
V_{cc} - I_c R_c - I_B R_c - V_{ce} = 0
\]
\[
V_{ce} = V_{cc} - (I_c + I_B) R_c
\]
\[
I_B = \frac{V_{cc} - V_{ce} - I_B R_c}{R_c}
\]

The result is that the circuit tends to maintain a stable value of collector current, keeping the Q-point fixed.

Rb appears directly across input (base) and output (collector), output is feedback to the input, and increase in collector current decreases the base current. Negative feedback exists in the circuit, so this circuit is called voltage feedback bias circuit.

Q2: (*) Prove that collector to base bias circuit is better than fixed bias circuit.

3m) (*) Draw and explain "Collector to Base Bias" circuit

Ans: (Above)

(*) MODIFIED COLLECTOR TO BASE BIAS CIRCUIT

\[
\text{Fig. - }
\]

To further improve the level of stability, the emitter resistance is connected in this circuit.
Applying KVL,
\[ V_{cc} - (I_c + I_B)R_C - I_BR_B - V_{BE} - I_{ERE} = 0 \]
\[ V_{cc} - V_{BE} = I_B (1 + \beta) R_C + I_BR_B + (1 + \beta) R_C I_B \]
\[ I_B = \frac{V_{cc} - V_{BE}}{R_B + (1 + \beta)(R_C + R_E)} \]
\[ \beta > 1 \]

Difference is \( \beta (R_C + R_E) \) from fixed Bias.

\[ \text{Collector Circuit:} \]

Applying KVL,
\[ V_{cc} - (I_c + I_B)R_C - V_{CE} - I_{ERE} = 0 \]
\[ V_{CE} = V_{cc} - I_E (R_C + R_E) \]

(iii) Explain Modified Collector to Base Bias circuit.

Ans. (Above)

*) STABILITY FACTORS COLLECTOR TO BASE BIAS:

(i) Derive the stability factor for the Collector to Base Bias.

\[ V_{cc} - I_c R_C - I_B [R_C + R_B] + V_{BE} = 0 \]
\[ V_{cc} = I_c R_C + I_B [R_C + R_B] + V_{BE} \rightarrow (1) \]

Diff on both sides \( \text{eqn} (1) \)
\[ 0 = \frac{\partial I_c R_C + \partial I_B (R_C + R_B) + 0}{\partial V_{cc}} \]
\[ -I_c R_C = \frac{\partial I_B (R_C + R_B)}{\partial V_{cc}} \]
\[ \frac{\partial I_B}{\partial I_c} = \frac{-R_C}{R_C + R_B} \]
Stability factor, \( S = \frac{1 + B}{1 - B} \left[ \frac{\frac{-R_c}{R_c + R_b}}{\frac{dI_B}{dI_c}} \right] \)

\[ S = \frac{1 + B}{1 + B} \left[ \frac{R_c}{R_c + R_b} \right] \]

Collector to bias circuit is having lesser stability factor than for fixed bias circuit. Hence this circuit provides better stability.

ii) Stability factor, \( S' \):

\[ S' = \frac{dI_c}{dV_{BE}} \]

from the CKT, \( (\frac{I_c}{I_B}) \):

\[ V_{cc} - (I_c + I_B) R_c - I_B R_b - V_{BE} = 0 \]

\[ V_{cc} - I_c R_c - I_B R_c - I_B R_b - V_{BE} = 0 \]

\[ V_{cc} - I_c R_c - (R_c + R_b) I_B - V_{BE} = 0 \]

\[ I_B = \frac{V_{cc} - V_{BE} - I_c R_c}{R_c + R_b} \]

\[ I_B = \frac{I_c}{B} \]

\[ \frac{I_c}{B} = \frac{V_{cc} - I_c R_c - V_{BE}}{R_c + R_b} \]

\[ \frac{I_c}{B} + \frac{I_c R_c}{R_c + R_b} = \frac{V_{cc} - V_{BE}}{R_c + R_b} \]

\[ I_c \left( \frac{1}{B} + \frac{R_c}{R_c + R_b} \right) = \frac{V_{cc} - V_{BE}}{R_c + R_b} \]

\[ I_c \left( \frac{R_c + R_b + R_c R_b}{B (R_c + R_b)} \right) = \frac{V_{cc} - V_{BE}}{R_c + R_b} \]
\[
\frac{\text{d}I_C}{\text{d}V_{BE}} = 0 - \frac{\beta}{R_B + (1+\beta)R_C}
\]

\[S'' = \frac{\text{d}I_C}{\text{d}V_{BE}} \frac{1}{\beta}
\]

From the circuit \((0\, \text{V})\):

\[V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0\]

\[V_{CC} - V_{BE} = (I_C + I_B)R_C - I_B R_B = 0\]

\[V_{CC} - V_{BE} = (\beta I_B + I_B)R_C - I_B R_B = 0\]

\[V_{CC} - V_{CE} = I_B [\beta + 1]R_C + R_B\]

\[I_B = \frac{V_{CC} - V_{CE}}{(\beta + 1)R_C + R_B}
\]

\[I_C = \frac{\beta [V_{CC} - V_{CE}]}{(\beta + 1)R_C + R_B}
\]

\[\Rightarrow \quad I_C = \beta I_B\]
\[
\begin{align*}
\left[ \frac{u'}{v'} - \frac{u}{v^2} \right] \\
\text{Diff w.r.t. } \beta \\
\frac{dI_C}{d\beta} &= \frac{[(B+1)RC + RB][Vcc - VBE] - \beta [Vcc - VBE]RC}{(B+1)RC + RB}^2 \\
&= \frac{Vcc - VBE(RB + RC)}{(B+1)RC + RB}^2 \\
&= \frac{Vcc - VBE}{RB + (1+\beta)RC} \\
&= \frac{I_C}{RB + (1+\beta)RC} \\
S'' &= \frac{I_C}{B} \left[ \frac{RB + RC}{RB + (1+\beta)RC} \right] \\
(\times) \quad \text{Relation between } S \text{ and } S' \\
2m) \quad S &= \frac{1+\beta}{1+\beta} \left[ -\frac{RC}{RC + RB} \right] \\
S' &= -\beta \frac{RB + (1+\beta)RC}{RB + (1+\beta)RC} \\
&= -S \frac{B}{(1+\beta)(RC + RB)} \\
&\Rightarrow S' = -S \frac{B}{(1+\beta)(RC + RB)}
\end{align*}
\]
$S = \frac{1 + \beta}{1 + \beta \left[ \frac{R_c}{R_c + R_b} \right]}$

$S'' = \frac{I_c}{\beta} \frac{[R_c + R_b]}{[\beta + 1] R_c + R_b}$

$\Rightarrow S' = \frac{I_c}{\beta} \left[ \frac{S}{1 + \beta} \right]$

**Advantages of Collector-Base Bias:**

(i) $R_c$ must be large for good stabilization.

(ii) It produces better degree of stabilization.

"If $S$ is small, $S''$ will also be small. Thus, if we provide stability against $I_c$ variations we get stability against $\beta$ variations also."

3. **Voltage Divider Bias** (or) **Self-Bias Circuit**

![Diagram of Voltage Divider Bias]

**Diagram Explanation:**

- It is the more stable biasing circuits.
- Biasing is provided by three resistors $R_1, R_2$ & $R$.
Resistors $R_1$ and $R_2$ act as a potential divider on the voltage divider circuit.

If collector current increases due to change in

temperature or change in $V_B$.

The emitter current $I_E$ also increases and voltage
drop across $R_E$ increases, reducing voltage difference
between base and emitter ($V_{BE}$).

Due to reduction in $V_{BE}$, base current $I_B$ and
hence $I_C$ also reduces.

Hence, negative feedback exists in the emitter bias
circuit.

This reduction in $I_C$ compensates for original value
change in $I_C$.

**Table:**

<table>
<thead>
<tr>
<th>Temp</th>
<th>$I_C$</th>
<th>$I_C$</th>
<th>Voltage drop across $I_E$</th>
<th>$I_E$</th>
<th>$I_C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$+$</td>
<td>$+$</td>
<td>$+$</td>
<td>$+$</td>
<td>$+$</td>
<td>$+$</td>
</tr>
</tbody>
</table>

**Circuit Analysis:**

The Voltage Divider Rule, total voltage $\times$ particular resistor

Sum of all resistors

Apply Voltage divider rule,

$$V_B = \frac{V_{CC} \times R_C}{R_1 + R_2} \quad \rightarrow \quad (1)$$

1) Apply KVL to the base side (input circuit)

**Fig(2):**

$$V_B - V_{BE} - V_E = 0 \quad \rightarrow \quad (2)$$

$$V_E = I_E \times R_E \quad \rightarrow \quad (3)$$

$$V_E = V_B - V_{BE} \quad \rightarrow \quad (4)$$

(from eqn(2))

Equate (3) and (4):

$$I_E \times R_E = V_B - V_{BE}$$

$$P_E = V_B - V_{BE} \quad \rightarrow \quad (5)$$
i) Apply KVL at the input side [Base circuit]

\[ V_{th} - R_B I_B - V_{BE} - R_E I_E = 0 \]  \[ A \]

\[ V_{th} = \frac{R_2}{R_1 + R_2} V_{cc} \]  \[ B \]

\[ R_{th} = \frac{R_1 R_2}{R_1 + R_2} \]

\[ R_B (\text{ohm}) \]

\[ \frac{R_2}{R_1 + R_2} V_{cc} = R_B I_B + V_{BE} + R_E I_E \]

\[ I_E = I_c + I_B \]

\[ V_{th} = R_B I_B + V_{BE} + R_E (I_c + I_B) \]

\[ V_{th} = R_B I_B + V_{BE} + I_c R_E + I_B R_E \]

\[ V_{th} - V_{BE} = R_B I_B + R_E (I_c + I_B) \]

\[ I_c = \beta I_B \]

\[ V_{th} - V_{BE} = I_B [R_B + R_E + R_E] \]

\[ I_B = \frac{V_{th} - V_{BE}}{R_B + (1+\beta) R_E} \]  \[ C \]

Difference in \((1+\beta)\) compared to other techniques.

ii) Apply KVL at the output side [Collector circuit]

from the below fig:

\[ V_{cc} - I_c R_c - V_{CE} - I_E R_E = 0 \]

\[ V_{CE} = V_{cc} - I_c R_c - I_E R_E \]
Fig(4):

\[ V_{CE} = V_{CC} \cdot Ic \cdot R_e - Ic \cdot R_e \]

\[ V_{CE} = V_{CC} - Ic \left[ R_e + R_e \right] \]

\[ I_c = \frac{V_{CC} - V_{CE}}{R_e + R_e} \]

**Qn:** (x) Explain Voltage divider bias (Self Bias)

(8m)

(x) Draw the circuit of a Voltage divider bias circuit. Explain its operation and discuss how it stabilizes against VBE Changes.

(x) Draw a Voltage divider bias BJT. Derive the expressions for \( I_c \) and \( V_{CE} \) and describe the method of drawing d.c. loadline on the output characteristics of transistor.

(x) Comment the performance of self-bias with fixed bias.

(x) Draw the circuit diagram of self-bias circuit using CE configuration.

**Ans:** [Above Answer] 
[D-13, D-18, M-12, M-14, M-15, D-15, D-02, M-08, D-04, D-14, D-12, M-11]
Stability Factor - Voltage Divider / Self Bias

\[ S = \frac{1 + \beta}{1 - \beta \left[ \frac{dI_B}{dI_C} \right]} \]

Fig: Thevenin's Equivalent Circuit

\[ R_1 || R_2 \]

\[ R_{E(\text{er})} \]

\[ R_{\text{th}} \]

\[ V_{th} \ (\text{or}) \]

\[ V_B \]

\[ \rightarrow R_1 \text{ and } R_2 \text{ is replaced by } R_{B(\text{er})} \text{, } R_{\text{th}} \text{ and } V_{th} \]

\[ \rightarrow R_E \text{ is parallel combination of } R_1 \text{ and } R_2 \]

\[ V_{th} \text{ is the Thevenin's Voltage} \]

Apply KVL to the input circuit

\[ V_{th} - I_B R_B - V_{BE} - I_C R_E = 0 \quad \rightarrow (1) \]

\[ V_{th} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0 \]

\[ (\therefore I_E = I_B + I_C) \quad \rightarrow (2) \]

\[ V_{th} - I_B R_B - V_{BE} - I_B R_E - I_C R_E = 0 \quad \rightarrow (3) \]

\[ V_{th} - V_{BE} - I_C R_E = I_B R_B + I_B R_E \quad \rightarrow (4) \]

\[ V_{th} - V_{BE} - I_C R_E = I_B \left[ R_B + R_E \right] \]

\[ I_B = \frac{V_{th} - V_{BE} - I_C R_E}{R_B + R_E} \quad \rightarrow (5) \]

Stability factor,

\[ S = \frac{1 + \beta}{1 - \beta \left[ \frac{dI_B}{dI_C} \right]} \]
\[ I_B = \frac{V_{BE}}{R_B + R_E} - \frac{V_{BE}}{R_B + R_E} - \frac{I_C R_E}{R_B + R_E} \]

Diff w.r.t \( I_c \)

\[ \frac{dI_B}{dI_c} = 0 - \frac{R_E}{R_B + R_E} \]

\[ \frac{dI_B}{dI_c} = \frac{-R_E}{R_B + R_E} \rightarrow (7) \]

Sub (7) in eqn (6)

\[ s = \frac{1 + \beta}{1 - \beta \left[ \frac{-R_E}{R_B + R_E} \right]} \]

\[ s = \frac{1 + \beta}{1 + \beta \left[ \frac{R_E}{R_B + R_E} \right]} \]

\[ = \frac{1 + \beta}{(R_B + R_E + \beta R_E)} \]

\[ = \frac{(1 + \beta)}{(R_B + R_E + \beta R_E)} \]

\[ \frac{1}{\text{each terms by } R_E} \]

\[ s = \frac{(1 + \beta)}{(1 + \frac{R_E}{R_B})} \]

\[ \frac{\frac{R_B}{RE}}{1 + \frac{R_E}{R_B}} \]

\[ s = \frac{(1 + \beta)}{(1 + \frac{R_E}{R_B})} \cdot \left( \frac{\frac{R_B}{R_E}}{1 + \frac{R_E}{R_B}} \right) \]

\[ (\because \frac{R_B}{R_E} \ll \ll \ll \ll \ll) \]

\[ s = \frac{(1 + \beta)}{(1 + \frac{R_E}{R_B})} \cdot \left( \frac{(1 + \frac{R_E}{R_B})}{1 + \frac{R_E}{R_B}} \right) \]

\[ s = \frac{(1 + \beta) \cdot (1)}{(1 + \frac{R_E}{R_B})} \]

\[ s = \frac{(1 + \beta)}{(1 + \frac{R_E}{R_B})} \]

\[ = 1 \rightarrow (12) \]
\[
\begin{align*}
\frac{\partial I_c}{\partial V_{BE}} & \quad I_c, \beta \text{ are constant} \\
\text{General expression,} \\
I_c &= \beta I_B + (1 + \beta) I_c \quad (14) \\
I_c &= \beta I_B \quad (15) \\
I_c &= \beta \cdot I_B \\
\text{from eqn (5),} \\
I_B &= \frac{V_{th} - V_{BE} - I_c R_E}{R_B + R_E} \\
I_c &= \beta \left[ \frac{V_{th} - V_{BE} - I_c R_E}{R_B + R_E} \right] \\
\frac{I_c}{\beta} &= \frac{V_{th} - V_{BE} - I_c R_E}{R_B + R_E} \\
\frac{I_c}{\beta} &= \frac{V_{th} - V_{BE} - I_c R_E}{R_B + R_E} \\
\frac{I_c + I_c R_E}{\beta} &= \frac{V_{th} - V_{BE}}{R_B + R_E} \\
I_c \left[ \frac{1}{\beta} + \frac{R_E}{R_B + R_E} \right] &= \frac{V_{th} - V_{BE}}{R_B + R_E} \\
I_c \left[ \frac{R_B + R_E + R_E}{\beta (R_B + R_E)} \right] &= \frac{V_{th} - V_{BE}}{R_B + R_E} \\
I_c &= \frac{(V_{th} - V_{BE}) (\beta (R_B + R_E))}{(R_B + R_E) (R_B + R_E + R_E)} \\
I_c &= \frac{\beta (V_{th} - V_{BE})}{R_B + R_E (1 + \beta)} \\
I_c &= \frac{\beta V_{th}}{R_B + R_E (1 + \beta)} - \frac{V_{BE} \beta}{R_B + R_E (1 + \beta)} \quad (19)
\end{align*}
\]
\[ s' = \frac{dI_c}{dV_{BE}} \]

Differentiating w.r.t. \( V_{BE} \) on eqn (19):

\[ \frac{dI_c}{dV_{BE}} = \frac{0 - \beta}{R_B + R_E(1+\beta)} \]

\[ s' = \frac{-\beta}{R_B + R_E(1+\beta)} \quad \rightarrow (20) \]

\[ s'' = \frac{dI_c}{\frac{d}{d\beta}} |_{I_{C0}, V_{BE} \rightarrow \text{constant}} \quad \rightarrow (21) \]

\[ 2q_{n(19)} \Rightarrow I_c = \beta \left[ \frac{V_{th} - V_{BE}}{R_B + R_E(1+\beta)} \right] \]

Differentiating \( I_c \) with \( \beta \):

\[ \frac{dI_c}{d\beta} = \frac{R_B + R_E(1+\beta)(V_{th} - V_{BE}) - \beta(V_{th} - V_{BE})R_E}{[R_B + R_E(1+\beta)]^2} \]

\[ = \frac{(V_{th} - V_{BE})(R_B + R_E)}{[R_B + R_E(1+\beta)]^2} \quad \rightarrow (22) \]

On \( \beta \rightarrow \) \[ I_B = \frac{V_{th} - V_{BE}}{R_B + R_E(1+\beta)} \]

\[ \frac{dI_c}{d\beta} = \frac{I_B (R_B + R_E)}{[R_B + R_E(1+\beta)]^2} \quad \rightarrow (23) \]
\[ \frac{\Delta I_C}{\Delta \beta} = \frac{I_C}{\beta} \frac{(R_B + R_E)}{R_B + R_E(1 + \beta)} \rightarrow (25) \]

\[ x'y' = \frac{s''}{s} \text{ by } (1 + \beta) \]

\[ S'' = \frac{I_C}{\beta} \frac{(1 + \beta)}{R_B + R_E(1 + \beta)} \]

\[ \text{from eqn (9), } S = \frac{(1 + \beta)(R_B + R_E)}{R_B + R_E(1 + \beta)} \]

\[ S'' = \frac{I_C}{\beta} \frac{s}{1 + \beta} \]

Advantages of Voltage divider Bias:

(i) Stability factor \( S' \) for Voltage divider bias is less compared to other Biasing circuits. It is known as Self Biasing circuits.

(ii) If Self Bias Circuit, when \( R_B/R_E \) is small, \( S' \) is large, which provides good stability.

(iii) It is more stable, popular for stability.

\[ \text{Derive the Stability factor of Self bias circuit of BJT.} \]

\[ \text{Derive all Stability factors, } S, S', S'' \text{ for Voltage divider bias.} \]

\[ \text{Derive Stability factor } \frac{\Delta I_C}{\Delta \beta} \text{ in Self bias circuit.} \]

\[ \text{What are the design considerations to make Stability factor independent of } h_{FE} \text{ Variation?} \]

\[ \text{Prove that Self bias of Stability factors} \]

\[ \text{[Above Answer] [D-04, D-05, D-02, D-14, D-13, M-13, M-12, D-11, M-15, D-15, M-14]} \]
**PROBLEMS**

**FIXED BIAS**

**SELF BIAS**

**VOLTAGE DIVIDER BIAS**

**COLLECTOR TO BASE BIAS**

1) In fixed bias method, a Si transistor with $B=100$ is used. $V_{cc} = 6\text{V}$, $R_c=3k\Omega$, $R_b=530k\Omega$. Draw the DC load line and determine the operating point. What is the stability factor?

**Solution:**

**Given:**

- $B = 100$
- $R_c = 3k\Omega$
- $R_b = 530k\Omega$
- $V_{cc} = 6\text{V}$

**To Draw DC Load Line:**

- $V_{cc} - I_c R_c - V_{CE} = 0$
- $6 - I_c (3k) - V_{CE} = 0$ → $i$
  
  **a) To find $V_{CE}$:** ($I_c = 0$
- $b) To find $I_c$:** ($V_{CE} = 0$

\[ I_c = \frac{6}{3 \times 10^3} \]

**$I_c = 2mA$**

**To Find $Q$-point:**

- $I_B = \frac{V_{cc} - V_{BE}}{R_B}$ → $6 - 0.7 (V_{BE} = 0.7\text{V})$

\[ = \frac{5.3}{530 \times 10^3} \Rightarrow 1 \times 10^{-5} \]

**$I_B = 10 \mu\text{A}$**

**Output side:**

- $V_{CE} = V_{cc} - I_c R_c$
- $V_{CE} = 6 - (1 \times 10^{-3})(3 \times 10^3)$

**$V_{CE} = 3\text{V}$**

**Stability Factor:**

\[ S = 1 + B \ [for \ fixed \ Bias] \]

\[ S = 1 + 100 \Rightarrow S = 101 \]
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**Voltage Divider Bias (or) Self Bias**

### Expressions

- $I_{CQ} = \beta I_B$
- $I_B = \frac{V_{CE} - V_{BE}}{R_B}$
- $V_{CE} = V_{CC} - I_C R_C$
- $I_C = \frac{V_{CC}}{R_C}$
- $S = \frac{I_C}{I_B}$
- $S' = -\frac{\beta}{R_B}$
- $S'' = \frac{I_C}{\beta}$

### Collector to Base Bias

- $I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(1+\beta)}$
- $V_{CE} = V_{CC} - I_C R_C$
- $I_C = \frac{V_{CC}}{R_C}$
- $S = \frac{1+\beta}{1+\beta \left(\frac{R_C}{R_B + R_C}\right)}$
- $S' = -\frac{\beta}{R_B + R_C(1+\beta)}$
- $S'' = \frac{I_C}{\beta}$

### Voltage Divider Bias

- $I_B = \frac{V_{th} - V_{BE}}{R_B + R_C(1+\beta)}$
- $V_{CE} = V_{CC} - I_C (R_C + R_E)$
- $I_C = \frac{V_{CC}}{R_C + R_E}$
- $S = \frac{1+\beta}{1+\beta \left(\frac{R_E}{R_B + R_E(1+\beta)}\right)}$
- $S' = -\frac{\beta}{R_B + R_E(1+\beta)}$
- $S'' = \frac{I_C}{\beta}$
Problems Continuation,

12) Design a fixed bias circuit to have operating point of (10 V, 3 mA). The circuit is supplied with 20 V and uses a silicon transistor of $hfe = 25$. 

\[
\begin{align*}
I_C &= 3 \times 10^{-3} \text{A} \\
\beta &= 250 \\
V_{BE} &= 0.7 \\
V_{CE} &= 10 \text{V}
\end{align*}
\]

**Solution** -

\[
\begin{align*}
I_C &= \beta I_B \\
I_B &= \frac{V_{CC} - V_{BE}}{R_B} \\
V_{CE} &= V_{CC} - I_C R_C \\
V_{BE} &= V_{CC} - I_C R_C \\
R_C &= \frac{V_{CC} - V_{CE}}{I_C} \\
R_C &= \frac{20 - 10}{3 \times 10^{-3}} \\
R_C &= \frac{10}{3 \times 10^{-3}} \\
R_C &= 3.33 \times 10^3 \\
R_C &= 3.33 \text{ k}\Omega
\end{align*}
\]

\[
\begin{align*}
R_B &= \frac{V_{CC} - V_{BE}}{I_B} \\
R_B &= \frac{V_{CC} - V_{BE}}{(I_C/\beta)B} \\
R_B &= \frac{20 - 0.7}{(3 \times 10^{-3}/250)} \\
R_B &= 250(20 - 0.7) \times 3 \times 10^{-3} \\
R_B &= \frac{4825}{3 \times 10^{-3}} \\
R_B &= 160833.333 \text{M}\Omega
\end{align*}
\]

**Answer** -

\[
\begin{align*}
R_C &= 3.33 \text{ k}\Omega \\
R_B &= 1.6 \text{ M}\Omega
\end{align*}
\]
3) Design the circuit shown in the Fig. Given Q-point values are to be $I_C = 1mA$, $V_{CEQ} = 2V$
Assume that $V_{CC} = 10V$, $\beta = 100$, $V_{BE\text{ (ON)}} = 0.7V$

\[ I_C = \beta I_B \]
\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \]
\[ V_{CC} = V_{CC} - I_C R_C \]

This is fixed bias circuit.

\[ Rc = \, ? \quad RB = \, ? \]

Find:

\[ \begin{align*}
\text{(i) To Find } & \quad R_C = \, ? \\
& \quad V_{CE} = V_{CC} - I_C R_C \\
& \quad R_C = \frac{V_{CC} - V_{CE}}{I_C} \\
& \quad R_C = \frac{10 - 6}{1 \times 10^{-3}} \\
& \quad R_C = 4 \times 10^3 \\
& \quad R_C = 4K\Omega
\end{align*} \]

\[ \text{Ans: } R_C = 4K\Omega \]

\[ \text{RB = 930K\Omega} \]

\[ \text{RB = 930K\Omega} \]

(iii) To Find $R_B$:

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \]
\[ R_B = \frac{V_{CC} - V_{BE}}{I_B} \]
\[ R_B = \frac{10 - 0.7}{(I_C/\beta)} \]
\[ R_B = 1 \times 10^{-3} \]
\[ R_B = 930 \times 10^3 \]

14) In a CE configuration, Germanium transistor amplifier circuit the bias is provided by self...
The various parameters are $V_{cc} = 16V$, $R_c = 8k\Omega$, $R_E = 2k\Omega$, $R_1 = 56k\Omega$, $R_2 = 20k\Omega$, $\alpha = 0.985$. Determine:

i) the co-ordinates of operating point.

ii) Stability factor $S$.

**Hint:** (Self Bias)

**Formula:**

$$I_c = \frac{\beta \left[ V_{th} - V_{BE} \right]}{R_B + (1 + \beta) R_E}, \quad \beta = \frac{\alpha}{1 - \alpha}$$

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$

$$I_E = I_c + I_B$$

$$V_{th} = \frac{R_2 \cdot V_{cc}}{R_1 + R_2}$$

$$V_{CE} = V_{cc} - I_c \left[ R_c + R_E \right]$$

$$S = \frac{[R_B + R_E][1 + \beta]}{R_B + (1 + \beta) R_E}$$

**Solution:**

i) Co-ordinates of operating point: $(I_c, V_{CE})$

a) To find $I_c$:

$$I_c = \frac{\beta \left[ V_{th} - V_{BE} \right]}{R_B + (1 + \beta) R_E}$$

Want to find $\beta$, $V_{th}$, $R_B$:

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\beta = \frac{0.985}{1 - 0.985} = 65.067$$

$$V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{cc} = \frac{(56 \times 10^3)(16)}{(56 \times 10^3) + (20 \times 10^3)}$$

$$= 0.015$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{56 \times 10^3}{56 \times 10^3 + 20 \times 10^3}$$

$$= 14.736, 84.2 \Omega$$
\[ V_{th} = 4.210 \text{V} \]

\[ \alpha \beta, V_{th}, R_B, I_C \]

\[ I_C = \frac{\beta \left( V_{th} - V_{BE} \right)}{R_B + (1 + \beta) R_E} \]

\[ = \frac{65.667 \left[ 4.210 - 0.3 \right]}{14736.842 + \left[ 1 + 65.667 \right] \left( 2 \times 10^3 \right)} \]

\[ = \frac{256.757}{148070.842} \]

\[ = 1.734 \times 10^{-3} \]

\[ I_C = 1.734 \text{mA} \]

b) To Find \( V_{CE} \):

\[ V_{CE} = V_{CC} - I_C \left( R_C + R_E \right) \]

\[ V_{CE} = 16 - (1.734 \times 10^{-3}) \left[ 3 \times 10^3 + 2 \times 10^3 \right] \]

\[ V_{CE} = 16 - 1.734 \times 10^{-3} \times 10^3 \times [3 + 2] \]

\[ = 16 - 1.734 \times 5 \]

\[ V_{CE} = 7.33 \text{V} \]

The coordinates of operating point are:

\[ Q \left[ 1.734 \text{mA}, 7.33 \text{V} \right] \]

(ii) Stability Factor \( S \):

\[ S = \frac{R_B + R_E}{R_B + [1 + \beta]} \left( \frac{1 + \beta}{1 + \beta \left( \frac{R_E}{R_B + R_E} \right)} \right) \]

\[ = \frac{[14736.842 + 2 \times 10^3] \left[ 1 + 65.667 \right]}{14736.842 + \left[ 1 + 65.667 \right] \left( 2 \times 10^3 \right)} \]
15) A Series Amplifier with Voltage divider bias is designed to establish Q-point at $V_{CE} = 12\text{V}$, $I_c = 2\text{mA}$ and Stability factor $S = 5.1$ if $V_{cc} = 24\text{V}$ $V_{BE} = 0.7\text{V}$, $\beta = 50$ and $R_c = 4.7\text{k}\Omega$. Determine the values of resistors $R_E$, $R_1$ and $R_2$.

**Hint:**

Voltage divider bias

**Formula:**

i) $V_{CE} = V_{cc} - I_c (R_c + R_E)$, find $R_E$

ii) $S = \frac{[R_B + R_E][1+\beta]}{R_B + R_E[1+\beta]}$, find $R_B$, $R_B = \frac{R_1 R_2}{R_1 + R_2}$

**Solution:**

i) To find $R_E$:

Given:

$V_{CE} = V_{cc} - I_c (R_c + R_E)$

$V_{CE} = 12 - 2 \times 10^{-3} [4.7 \times 10^3 + R_E]$

$V_{CE} = 12 - 9.4 - 2 \times 10^{-3} R_E$

$2 \times 10^{-3} R_E = 24 - 9.4 - 12$

$R_E = \frac{24 - 9.4 - 12}{2 \times 10^{-3}}$

$R_E = 1.3 \times 10^3 \Omega$

(ii) To find $R_1$ and $R_2$ ($R_E$):

Given:

$\beta = 50$

$S = 5.1$

$R_E = 1.3 \Omega$

$S = \frac{[R_B + 1.3 \times 10^3][1+50]}{R_B + 1 + 50[1.3 \times 10^3]}$
\[ R_B + 66300 \]
\[ 5.1R_B + 338130 = 5.1R_B + 66300 \]
\[ 5.1R_B - 5.1R_B = 66300 - 338130 \]
\[ T45.9R_B = 271830 \]
\[ R_B = \frac{271830}{45.9} \]
\[ R_B = 5922.22\, \Omega \]

Find \( R_1 \) and \( R_2 \):

\[ R_B = R_1 \parallel R_2 \]
\[ R_B = \frac{R_1 R_2}{R_1 + R_2} \rightarrow (B) \]
\[
\begin{align*}
R_2 &= 0.1 \times 50 \times 1.3 \times 10^3 \\
R_2 &= 6500\, \Omega \rightarrow (A)
\end{align*}
\]

Substitute \((A)\) in \((B)\):

\[ 5922.22 = \frac{R_1 (6500)}{R_1 + 6500} \]
\[ 5922.22 R_1 + 5922.22 (6500) = 6500R_1 \]
\[ 38494430 = 6500R_1 - 5922.22 R_1 \]
\[ 38494430 = 577.78R_1 \]
\[ R_1 = \frac{38494430}{577.78} \]
\[ R_1 = 66622.71 \]
\[ R_1 = 6.66\, \text{K}\, \Omega \]

\[ R_B = 5922.22\, \Omega \]
\[ R_1 = 6.66\, \text{K}\, \Omega \]

Ans:

\[ R_B = 1.3\, \text{K}\, \Omega \]
\[ R_1 = 6.66\, \text{K}\, \Omega \]
(b) An NPN Transistor, if $B = 50$ is used in Series and Circuit with $V_{CC} = 10V$ and $R_C = 2K\Omega$. The Bias is obtained by connecting $100K\Omega$ resistor from Collector to Base; find the Q-point and Stability Factor $s$.

**Collector to Base Circuit**

**Formulae:**

\[
I_C = \frac{B (V_{CC} - V_{BE})}{\beta R_C + R_B + R_C}
\]

\[
V_{CE} = V_{CC} - I_C R_C
\]

\[
s = \frac{1 + \beta}{R_B + (1 + \beta) R_C}
\]

**Given:**

- $V_{CC} = 10V$
- $R_C = 2K\Omega = 2 \times 10^3 \Omega$
- $\beta = 50$
- $V_{BE} = 0.7V$

**Solution:**

1) **Q-point:** $[V_{CE}, I_C]$

a) **Find $I_C$:**

\[
I_C = \frac{50 \times [10 - 0.7]}{(50[2 \times 10^3] + (100 \times 10^3) + (2 \times 10^3)}
\]

\[
= \frac{465}{(100 \times 10^3) + (100 \times 10^3) + (2 \times 10^3)}
\]

\[
= 2.32 \times 10^{-3}
\]

\[
I_C = 2.32mA
\]

b) **Find $V_{CE}$:**

\[
V_{CE} = V_{CC} - I_C R_C
\]

\[
= 10 - (2.32 \times 10^{-3})(2 \times 10^3)
\]

\[
= 10 - 4.64
\]

\[
V_{CE} = 5.36V
\]

Q-Point is $[V_{CE}, I_C] \rightarrow (5.36V, 2.32mA)$
i) Stability Factor $S$:

$$ S = \frac{1 + \beta [R_B + R_C]}{R_B + [1 + \beta] R_C} $$

$$ = \frac{1 + 50 \left[ \frac{100 \times 10^3 + 2 \times 10^3}{100 \times 10^3 + [1 + 50](2 \times 10^3)} \right]}{100 \times 10^3 + 100 \times 10^3} $$

$$ = \frac{1 + 50 \left[ \frac{102 \times 10^3}{100 \times 10^3 + 102 \times 10^3} \right]}{(100 + 102) \times 10^3} $$

$$ S = 25.75 $$

4) In the circuit shown in Figure, where $V_{cc} = 10V$

$R_B = 220k\Omega$. Calculate $I_B$, $I_C$, $V_{ce}$

Assume $V_{BE} = 0.7V$

$\beta = 50$

Hint: fixed bias circuit

Normal form:

$$ I_B = \frac{V_{cc} - V_{BE}}{R_B} $$
ii) \( I_c = \beta I_b \)

(iii) \( V_{ce} = V_{cc} - I_c R_e \)

(i) Find \( I_b \):

\[
I_b = \frac{V_{cc} - V_{be}}{R_b} = \frac{10 - 0.7}{(220 \times 10^3)} = \frac{9.3}{220000} = 4.227 \times 10^{-6}
\]

\[
I_b = 4.227 \mu A
\]

(ii) Find \( I_c \):

\[
I_c = \beta I_b = 50 \times 4.227 \times 10^{-6} = 2.1135 \times 10^{-3}
\]

\[
I_c = 2.1135 mA
\]

(iii) Find \( V_{ce} \):

\[
V_{ce} = V_{cc} - I_c R_e = 10 - (2.1135 \times 10^{-3})(1.2 \times 10^8)
\]

\[
V_{ce} = 7.4638 V
\]

Ans:

\[
\begin{align*}
I_b &= 4.227 \mu A \\
I_c &= 2.1135 mA \\
V_{ce} &= 7.4638 V
\end{align*}
\]

18) Estimate the value of the resistor in the fixed biasing circuit using the following specification:

\[
V_{ce} = 4.4 V, \quad V_{be} = 0.7 V, \quad I_{co} = 9 mA
\]

\[
\beta = 115, \quad V_{cc} = 9 V
\]

Find \( R_e, I_b, R_b \)?
(i) $V_{ce} = V_{cc} - I_c R_c$

(ii) $I_c = \beta I_B$

(iii) $I_B = \frac{V_{cc} - V_{BE}}{R_B}$

(i) **Find $R_c$:**

\[
V_{ce} = V_{cc} - I_c R_c \\
R_c = \frac{V_{cc} - V_{ce}}{I_c} \\
R_c = \frac{9 - 4.4}{(9 \times 10^{-3})} \\
R_c = \frac{4.6 \times 10^3}{9} \\
R_c = 0.5111 \times 10^3 \\
R_c = 511.11 \Omega
\]

(ii) **Find $I_B$:**

\[
I_B = \frac{I_c}{\beta} \\
I_B = \frac{9 \times 10^{-3}}{115} \\
I_B = 78.26 \times 10^{-6} A \\
I_B = 78.26 |\mu| A
\]

(iii) **Find $R_B$:**

\[
I_B = \frac{V_{cc} - V_{BE}}{R_B} \\
R_B = \frac{V_{cc} - V_{BE}}{I_B} \\
R_B = \frac{9 - 0.7}{78.26 \times 10^{-6}} \\
R_B = \frac{8.3 \times 10^6}{78.26} \\
R_B = 0.106056 \times 10^6 \\
R_B = 106 \times 10^3 \Omega \\
R_B = 106 \text{ k}\Omega
\]

**Ans:**

\[
R_c = 511.11 \Omega \\
I_B = 78.26 |\mu| A \\
R_B = 106 \text{ k}\Omega
\]
Determine the Bias transistor $R_B$ for fixed Bias and collector to base bias and compare the stability factor $S$ for both of them.

**Hint:**

1. **Fixed Bias**
   - (i) **Find $R_B$**
     \[
     V_{cc} = V_{BE} + I_{B} R_B \\
     R_B = \frac{V_{cc} - V_{BE}}{I_{B}} \\
     R_B = \frac{12 - 0.7}{(0.3 \times 10^{-3})} \quad \text{Ans: } R_B = 37.67 \, k\Omega
     \]
   - (ii) **Stability Factor $S$**
     \[
     S = 1 + \beta \\
     S = 1 + 100 \\
     S = 101
     \]

2. **Collector to Base Bias**
   - (i) **Find $R_B$**
     \[
     V_{cc} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0 \\
     I_C = \beta I_B \\
     = 100 \times 0.3 \times 10^{-3} \quad \text{Ans: } I_C = 0.03 \, mA
     \]
\[ 12 = 9.99 + 0.3 \times 10^{-3} R_B + 0.7 \]

\[ 12 - 9.99 - 0.7 = 0.3 \times 10^{-3} R_B \]

\[ R_B = \frac{1.31}{0.3 \times 10^{-3}} \]

\[ R_B = 4.3367 \times 10^3 \Omega \]

\[ R_B = 4.3367 \text{ k}\Omega \]

\[ S = \frac{1 + R}{1 + \beta} \left[ \frac{R_C}{R_C + R_B} \right] \]

\[ = \frac{1 + 100}{1 + 100 \left[ \frac{380}{380 + 4.3367} \right]} \]

\[ = \frac{101}{1 + 100 \left[ 0.00708 \right]} \]

\[ = \frac{101}{8} \]

\[ S = 12.5 \]

\[ R_B = 4.3367 \text{ k}\Omega \]

\[ S = 12.5 \]

For good stabilization, S value will be low.
Collector to Base bias shows good stabilization.
S (Fixed Bias) 101 > S (Collector to Base bias) 12.5

For the circuit shown in the figure, find I_c, V_C, and S_2.
**Hint:** Fixed Bias

**Formula:**

i) \( I_B = \frac{V_{cc} - V_{BE}}{R_B} \)

ii) \( I_C = \beta I_B \)

iii) \( V_{CE} = V_{cc} - I_C R_C \)

iv) \( S = 1 + \beta \)

**Solution:**

i) To find \( I_B \):

\[
I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{10 - 0.7}{500 \times 10^3} = \frac{0.3 \times 10^{-3}}{500} = 18.6 \times 10^{-6} \text{ A} = 18.6 \mu A
\]

ii) To find \( I_C \):

\[
I_C = \beta I_B = 100 \times 18.6 \times 10^{-6} = 1.86 \times 10^{-3} \text{ A} = 1.86 \text{ mA}
\]

\[
S = 1 + \beta = 1 + 100 = 101
\]

\[
\text{Ans:} \ I_C = 1.86 \text{ mA, } V_{CE} = 4.42 \text{ V, } S = 101
\]

**Given:**

- \( R_C = 3 \text{ k}\Omega = 3 \times 10^3 \)
- \( R_B = 500 \text{ k}\Omega = 50 \times 10^3 \)
- \( \beta = 100 \)
- \( V_{cc} = 10 \text{ V} \)
- \( V_{BE} = 0.7 \text{ V} \)

**In the circuit given:**

Determine \( R_B, I_C, V_C \) if \( V_C = 6 \text{ V} \).
For the circuit in Fig. find $I_C$, $V_{CE}$, $S$

Hint: Collector to Base Bias
Given:
\[ \beta = 100 \]
\[ R_C = 3k \Omega = 3 \times 10^3 \]
\[ R_B = 500k \Omega = 5 \times 10^5 \]
\[ V_{BE} = 0.7V \]
\[ V_{cc} = 10V \]

1. \[ I_C = \beta \cdot I_B \]
2. \[ I_B = \frac{V_{cc} - V_{BE}}{R_B + (1+\beta)R_C} \]
3. \[ V_{CE} = V_{cc} - (I_B + I_C)R_C \]
4. \[ S = \frac{1 + \beta}{1 + \beta} \left( \frac{R_C}{R_C + R_B} \right) \]

\[ \text{Find } I_C : \]
\[ V_{cc} - R_c [I_C + I_B] - I_B R_B - V_{BE} = 0 \]

On simplification,
\[ I_B = \frac{V_{cc} - V_{BE}}{R_B + (1+\beta)R_C} \]
\[ I_B = \frac{10 - 0.7}{500 \times 10^3 + [1 + 100] 3 \times 10^3} \]
\[ I_B = 11.58 \times 10^{-6} \]
\[ I_B = 11.58 \mu A \]

\[ I_C = \beta \cdot I_B \]
\[ = 100 \times 11.58 \times 10^{-6} \]
\[ I_C = 1.158 \times 10^{-3} \]
\[ I_C = 1.158 mA \]

\[ \text{Find } V_{CE} : \]
\[ V_{ce} = V_{cc} - (I_c + I_b) R_c - V_{ce} = 0 \]

\[ V_{ce} = V_{cc} - (I_c + I_b) R_c \]

\[ = 10 - \left[ (1.58 \times 10^{-6} + 1.158 \times 10^{-3}) \right] \left[ 3 \times 10^3 \right] \]

\[ V_{ce} = 10 - \left[ 1.169 \times 10^{-3} \right] \left[ 3 \times 10^3 \right] \]

\[ = 10 - 3.507 \]

\[ V_{ce} = 6.493 \text{V} \]

(iii) \[ S = \frac{1 + \beta}{1 + \beta} \left( \frac{R_c}{R_c + R_B} \right) \]

\[ S = \frac{1 + 100}{1 + 100} \left( \frac{3 \times 10^3}{3 \times 10^3 + 500 \times 10^3} \right) \]

\[ = \frac{101}{101} \left( \frac{3 \times 10^3}{3 \times 10^3 + 503 \times 10^3} \right) \]

\[ = \frac{101}{101 + 0.005964} \]

\[ = 101 \]

\[ S = 68.2673 \]

Ans: \[ V_{ce} = 6.493 \text{V}, \]
\[ S = 68.2673 \]
\[ I_B = 11.584 \text{mA} \]

Q3) Determine \( V_{ce} \) and \( I_c \) in the Voltage divider Bias

fig is below...

int: Voltage divider bias
i) \[ V_{CE} = V_{CC} - I_C R_C - I_E R_E \]

ii) \[ I_C = \beta \cdot I_B \]

\[ I_B = \frac{V_{TH} - V_{BE}}{R_B + (1 + \beta)R_E} \]

\[ V_{TH} = \frac{R_2}{R_1 + R_2} \cdot V_{CC} \]

\[ R_B = \frac{R_1 \cdot R_2}{R_1 + R_2} \]

---

i) Find \( I_C \):

a) \[ V_{TH} = \frac{R_2}{R_1 + R_2} \cdot V_{CC} \]

\[ V_{TH} = \frac{5 \times 10^3}{(5 \times 10^3) + (10 \times 10^3)} \times 10 \]

\[ V_{TH} = \frac{5 \times 10^3 \times 10}{15 \times 10^3} \]

\[ V_{TH} = \frac{10}{3} \]

\[ V_{TH} = 8.33 \text{V} \]

b) \[ R_B = \frac{R_1 \cdot R_2}{R_1 + R_2} \]

\[ R_B = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{(10 \times 10^3)(5 \times 10^3)}{(10 \times 10^3) + (5 \times 10^3)} \]

\[ R_B = \frac{50 \times 10^6}{15 \times 10^3} \]

\[ R_B = 3.33 \times 10^3 \text{\Omega} \]
\[ e) \quad I_B = \frac{V_{TH} - V_{BE}}{R_B + (1 + \beta) R_E} \]
\[ = \frac{3.33 - 0.7}{3.8 \times 10^3 + [1 + 100] \times 500} \]
\[ = \frac{2.63}{3.8 \times 10^3 + 50500} \]
\[ I_B = 4.886 \times 10^{-6} \]
\[ I_B = 48.86 \mu A \]

\[ d) \quad I_C = \beta \cdot I_B \]
\[ = 100 \times 4.886 \times 10^{-6} \]
\[ = 4.886 \times 10^{-3} \]
\[ I_C = 4.886 mA \]

\[ f) \quad \text{Find } V_{CE} - \]
\[ V_{CE} = V_{cc} - I_C R_C - I_E R_E \quad \rightarrow (\) \]
\[ I_E = I_B + I_C \]
\[ = (4.886 \times 10^{-6}) + (4.886 \times 10^{-3}) \]
\[ I_E = 4.935 mA \]
\[ \therefore (\) \Rightarrow V_{CE} = 10 - (4.886 \times 10^{-3})(1 \times 10^3) - \]
\[ (4.935 \times 10^{-3})(500) \]
\[ V_{CE} = 10 - 4.886 - 2.467 \]
\[ V_{CE} = 2.647 V \]

\[ \text{Ans!} \quad V_{CE} = 2.647 V \]
\[ I_C = 4.886 mA \]
24) The PNP transistor in a circuit of fig. has $\beta = 50$. Find the values of $R_c$ to obtain $V_c = 5 \text{V}$. What happens if the transistor is replaced with another $\beta = 100$?

**Solution:**

(i) $\beta = 50$:

- $I_c = \beta I_B = 50 \times 9.3 \times 10^{-6}$
- $I_c = 4.65 \times 10^{-3}$
- $I_c = 4.65 \text{mA}$

- $R_c = \frac{V_c}{I_c} = \frac{5}{4.65 \times 10^{-3}}$
- $R_c = 1075 \Omega$

(ii) $\beta = 100$:

- $I_c = \beta I_B = 100 \times 9.3 \times 10^{-6}$
- $I_c = 9.3 \times 10^{-3}$
- $I_c = 9.3 \text{mA}$

- $R_c = \frac{V_c}{I_c} = \frac{5}{9.3 \times 10^{-3}}$
- $R_c = 537.6 \Omega$

25) Calculate the Q point $V_a$ ([Ic and Vce]) for the circuit in the fig. [Diagram]
1) To find \( I_B \):

\[
I_B = \frac{V_{cc} - V_{BE}}{R_B + (1+\beta)R_C}
\]

\[
= \frac{12 - 0.7}{(100 \times 10^3) + (1+100)(10 \times 10^3)}
\]

\[
I_B = 10.18 \mu A
\]

2) \( I_C \):

\[
I_C = \beta I_B
\]

\[
= 100 \times 10^{-18} \times 10^{-6}
\]

\[
I_C = 1.018 \times 10^{-3}
\]

\[
I_C = 1.018 mA
\]

3) \( V_{CE} \):

\[
V_{CE} = V_{cc} - (I_B + I_C)R_C
\]

\[
= 12 - (10^{-18} \times 10^{-6} + 1.018 \times 10^{-3})(10 \times 10^3)
\]

\[
V_{CE} = 1.7182V
\]

\[\therefore \text{QPT } [1.018mA, 1.7182V]\]

---

Calculate the minimum and maximum values of \( I_C \) and \( V_{CE} \) for the collector to base bias when \( hfe(\text{min}) = 50 \) and \( hfe(\text{max}) = 60 \). For circuit, \( V_{cc} = 12V, R_C = 2K \) and \( R_B = 150K \). Assume Si Transistor. Hint: Collector to Base Bias

<table>
<thead>
<tr>
<th>( I_B )</th>
<th>( I_C = \beta I_B )</th>
<th>( V_{CE} = V_{cc} - \frac{V_{CE}}{I_B R_C} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{min} )</td>
<td>44.84 mA</td>
<td>2.243 mA</td>
</tr>
<tr>
<td>( \text{max} )</td>
<td>41.54 mA</td>
<td>2.4924 mA</td>
</tr>
</tbody>
</table>
27) Design a collector to base bias circuit for the specified conditions: \( V_{cc} = 15V, V_{ce} = 5V, I_c = 5mA \), \( \beta = 100 \).

**Hint:** Collector to Base Bias

\[ \text{Formula} \]

\[
\begin{align*}
(1) \quad I_B &= \frac{I_c}{\beta} \\
(2) \quad R_c &= \frac{V_{cc} - V_{ce}}{I_B + I_c} \\
(3) \quad R_B &= \frac{V_{cc} - V_{BE}}{I_B}
\end{align*}
\]

**Ans:**

\[
\begin{align*}
I_B &= 50k\Omega \\
R_c &= 1.98k\Omega \\
R_B &= 86k\Omega
\end{align*}
\]

28) Design a collector to base bias circuit to have an operating point of \((10V, 4mA)\). The circuit is supplied with 20V and uses a Si transistor of \( hfe = 250 \).

**Hint:** Collector to Base Bias

\[ \text{Formula} \]

\[
\begin{align*}
(1) \quad R_c &= \frac{V_{cc} - V_{ce}}{I_B + I_c} \\
(2) \quad I_B &= \frac{I_c}{\beta} \\
(3) \quad R_B &= \frac{V_{cc} - V_{BE}}{I_B}
\end{align*}
\]

**Ans:**

\[
\begin{align*}
R_c &= 2.49k\Omega \\
I_B &= 16\mu A \\
R_B &= 581.25k\Omega
\end{align*}
\]

Draw the circuit diagram.
for the circuit shown in fig. Determine \( I_{BQ}, I_{CQ}, V_{CEQ} \)

Formulas:

i) \( I_{BQ} = \frac{V_{cc} - V_{BE}}{R_B + (1 + \beta)R_C + R_E} \)

ii) \( I_{CQ} = \beta I_{BQ} \)

iii) \( I_{EQ} = I_{BQ} + I_{CQ} \)

iv) \( V_{CEQ} = V_{cc} - I_{E}(R_E + R_C) \)

Answers:

26.95 mA

1.347 mA

1.3737 mA

6.07 V

Hint: Modified Collector to Base Bias

for the circuit shown in the fig. Calculate the operating points.
1) \[ \text{Find } I_{bq} : \]
\[ I_{bq} = \frac{V_{cc} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)} \]
\[ = \frac{10 - 0.7}{(200 \times 10^3) + (1+50)(1 \times 10^3 + 100)} \]
\[ I_{bq} = 36.31 \mu A \]

2) \[ \text{Find } I_{cq} : \]
\[ I_{cq} = \beta I_{bq} \]
\[ = 50 \times 36.31 \times 10^{-6} \]
\[ I_{cq} = 1.8155 \text{ mA} \]

3) \[ \text{Find } I_{eq} : \]
\[ I_{eq} = I_{cq} + I_{bq} \]
\[ = (36.31 \times 10^{-6}) + (1.8155 \times 10^{-3}) \]
\[ I_{eq} = 1.85181 \text{ mA} \]

4) \[ \text{Vceq} : \]
\[ \text{Vceq} = V_{cc} - \frac{I_{eq} R_C + R_E}{10} \]
\[ = 10 - \frac{1.85181 \times 10^{-3} \times 1 \times 10^3 + 100}{1 \times 10^3 + 100} \]
\[ \text{Vceq} = 7.963 \text{ V} \]

Operating point is \([1.8155 \text{ mA}, 7.963 \text{ V}]\)

31) Determine the Bias Resistor \(R_B\) for fixed

Try it

Where \(V_{cc} = 20 \text{ V}, I_{b} = 2 \text{ mA}\)

Answer:
\[ R_B = \frac{V_{cc} - V_{BE}}{I_{b}} \]

32) Locate the operating point of the circuit

Shown in Fig. \(V_{cc} = 15 \text{ V}, h_{fe} = 200\)

Hint: (Modified Collector to Base Bias)
Operating point

i) \( I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + [(1 + \beta) \cdot (R_C + R_E)]} \)

\[ I_{BQ} = \frac{15 - 0.7}{630 \times 10^3 + [(1 + 200) \cdot (4.7 \times 10^3 + 680)]} \]

\[ I_{BQ} = 8.356 \times 10^{-6} \]  
\[ I_{BQ} = 8.356 \ mA \]

ii) \( I_{CQ} = \beta \cdot I_{BQ} \)

\[ I_{CQ} = 200 \cdot (8.356 \times 10^{-6}) \]

\[ I_{CQ} = 1.6712 \times 10^{-3} \]  
\[ I_{CQ} = 1.6712 \ mA \]

(iii) \( I_{EQ} = I_{CQ} + I_{BQ} \)

\[ I_{EQ} = (1.6712 \times 10^{-3}) + (8.356 \times 10^{-6}) \]

\[ I_{EQ} = 1.68 \times 10^{-3} \]  
\[ I_{EQ} = 1.68 \ mA \]
(iv) \[ V_{CEQ} = V_{cc} - \frac{IE}{RC + RE} \]
\[ = 15 - \frac{1.68 \times 10^{-3} \times (4.7 \times 10^3 + 680)}{4.3} \]
\[ V_{CEQ} = 5.9816V \]

33) For the circuit, find the q-point, \( V_{cc} = 15V \) and \( \beta = 100, \ V_{BE} = 0.7V \).

Hint: Voltage Divider Bias

Q point \([V_{CE}, I_c]\)

i) Find \( I_c \):
\[ I_c = \beta I_B \]

a) \( I_B = \frac{V_{th} - V_{BE}}{R_B + (1+\beta)RE} \) → (i)

b) \[ V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{cc} \]
\[ = \frac{6.8 \times 10^3}{(100 \times 10^3) + (100 \times 10^3)} \times 15 \]
\[ V_{th} = 7.5V \]

c) \[ R_B = R_1 \left( \frac{R_2}{R_1 + R_2} \right) \]
\[ = \frac{R_1 R_2}{R_1 + R_2} \]
$I_B = \frac{7.5 - 0.7}{(50 \times 10^3) + (1+100)(6.8 \times 10^3)}$

$= 9.23 \times 10^{-6}$

$= 9.23 \text{ mA}$

Solve $I_B$ in $I_C$.

i) $I_C = \beta \cdot I_B$

$= 100 \times 9.23 \times 10^{-6}$

$I_C = 0.923 \text{ mA}$

ii) $I_E = I_C + I_B$

$= (0.923 \times 10^{-3}) + (9.23 \times 10^{-6})$

$I_E = 0.932 \text{ mA}$

iii) $V_{CE}$:

$V_{CE} = V_{cc} - I_C R_C - I_E R_E$

$= 15 - 0.923 \times 4.3 - 0.932 \times 6.8$

$V_{CE} = 4.6935 \text{ V}$

- Operating Q point $[I_{CQ} = 0.932 \text{ mA};$
  $V_{CEQ} = 4.6935 \text{ V}]$

34) Draw the d.c. load line for the following transistor configuration. Obtain the equivalent point.

\[
\begin{align*}
V_c &= +12 \text{ V} \\
R_1 &= 5.2 \text{ K} \\
R_2 &= 1.24 \text{ K} \\
R_E &= 100 \text{ ohm} \\
R_C &= 330 \text{ ohm}
\end{align*}
\]
**Voltage Divider Bias**

i) **Find $I_c$**

a) $V_{th}$

$$V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{cc}$$

$$= \frac{12 \times 1.24 \times 10^3}{\left(1.24 \times 10^3\right) + \left(5.2 \times 10^3\right)}$$

$$V_{th} = 8.31V$$

cia) $I_B$

$$I_B = \frac{V_{th} - V_{BE}}{R_B + (1 + \beta)R_E}$$

$$= \frac{8.31 - 0.7}{\left(1 \times 10^3\right) + \left(1 + 100\right)\left(100\right)}$$

$$= 14.5 \times 10^{-6}$$

$$I_B = 14.5\mu A$$

ii) **Find $V_{CE}$**

$$V_{CE} = V_{cc} - I_cR_C - I_E R_E$$

$$= 12 - \left[14.5 \times 10^{-3} \times 330\right] - \left[100 \times I_E\right]$$

$$= 12 - 4.785 - 100 \times I_E$$

$$V_{CE} = 5.7505V$$

$\therefore I_E = I_B + I$
Calculate the minimum and maximum values of $I_c$ and $V_{ce}$ for the voltage divider bias, when $hfe\text{(min)} = 50$ and $hfe\text{(max)} = 60$. For circuit $V_{cc} = 12$, $R_1 = 10\, k\Omega$, $R_2 = 2\, k\Omega$, $R_E = 470\, \Omega$, $R_c = 2\, k\Omega$.

### Formulas

1. $V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{cc}$
2. $R_B = \frac{R_1 R_2}{R_1 + R_2}$
3. $I_B = \frac{V_{th} - V_{BE}}{R_B + (1 + hfe) R_E}$
4. $I_C = \beta I_B$
5. $I_E = I_C + I_B$
6. $V_{CE} = V_{cc} - I_C R_C - I_E R_E$

### Answers

- $hfe\text{(min)} = 50$
- $V_{th} = 2\, V$
- $R_B = 1.67\, k\Omega$
- $I_B = 50.7\, \mu A$
- $I_C = 2.535\, mA$
- $I_E = 2.585\, mA$
- $V_{CE} = 5.715\, V$
- $2.613\, mA$
- $5.632$

For a circuit shown in fig, $V_{cc} = 20\, V$, $R_c = 2\, k\Omega$, $\beta = 50$, $V_{BE} = 0.2\, V$, $R_1 = 100\, k\Omega$, $R_E = 100\, \Omega$. Calculate $I_B$, $V_{CE}$, $I_C$ and Stability Factor $s$.

### Formulas

1. $V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{cc}$
2. $R_B = \frac{R_1 R_2}{R_1 + R_2}$
3. $I_B = \frac{V_{th} - V_{BE}}{R_B + (1 + hfe) R_E}$
4. $I_C = \beta I_B$
5. $V_{CE} = V_{cc} - I_C R_C - (1 + \beta) I_E R_E$
6. $s = \frac{1 + \beta}{1 + \beta \frac{R_E}{R_E + R_B}}$

### Answers

- $1.818\, V$
- $9.09\, k\Omega$
- $114\, mA$
- $5.7\, mA$
- $8\, V$
- $33$
4. Emitter Feedback Bias (or)

Emitter Stabilized Bias Circuit:

\[ +Vcc \]

\[ \downarrow \]

\[ I_B \]

\[ R_B \]

\[ I_C \]

\[ R_c \]

\[ \downarrow \]

\[ V_C E \]

\[ I_E \]

\[ R_E \]

\[ V_{O} \]

\[ C_2 \]

\[ \uparrow \]

\[ V_B E \]

\[ J_1 \]

\[ J_2 \]

\[ J_3 \]

\[ J_4 \]

**Fig.: Emitter bias circuit**

→ To improve the stability of the biasing circuit over fixed bias stability, the emitter resistance is connected in the biasing circuit. Such biasing circuit is known as Emitter bias circuit.

**Circuit Analysis:**

1. **Base Circuit [Input Side]**
   
   Apply KVL to the base circuit,
   
   \[ Vcc - I_B R_B - V_{BE} - I_E R_E = 0 \quad (1) \]
   
   \[ I_E = I_C + I_B \quad (2) \]
   
   \[ = I_B + \beta I_B \]
   
   \[ I_E = (\beta + 1) I_B \quad (3) \]
   
   Substituting (3) in (1),
   
   \[ Vcc - I_B R_B - V_{BE} - (1 + \beta) I_B R_E = 0 \]
   
   \[ Vcc - V_{BE} = I_B R_B + (1 + \beta) I_B R_E \]

   | \[ I_B = \frac{Vcc - V_{BE}}{R_B + (1 + \beta) R_E} \] |
   | \[ (\because \beta \gg 1) \]
   |
   | \[ I_B = \frac{Vcc - V_{BE}}{R_B + B R E} \] |
only difference is $V_R$ with fixed Bias.

$$V_B = V_{BE} + V_E$$

$$V_E = I_{RE}$$

$$V_B = V_{BE} + I_{RE}$$

(ii) Collector Circuit (output side):

Apply KVL to the collector circuit

$$V_{cc} - I_{c}R_c - V_{CE} - I_{RE} = 0$$

$$V_{CE} = V_{cc} - I_{c}R_c - I_{RE}$$

$$V_{CE} = V_{cc} - V_E$$

$$V_c = V_{cc} - I_{c}R_c$$

---

**Problems Continuation:**

37) For a Voltage divider Bias, $V_{cc} = 5V$, $\beta = 100$ and $R_c = 1.2k\Omega$. Obtain the values of $R_E$, $R_1$, and $R_2$ such that the circuit is considered bias stable at $V_{ceq} = 3V$.

**Hint:** Voltage divider Bias

**Given:**

- $V_{cc} = 5V$
- $\beta = 100$
- $V_{ceq} = 3V$
- $R_c = 1.2k\Omega$
- $R_E, R_1, R_2 = ?$

**Solution:**

i) $I_{cq}$:

$$I_{cq} = \frac{V_{cc} - V_{ceq}}{R_c + R_E}$$

$$= \frac{5 - 3}{1.2 + 0.68} = 0.64 mA$$

ii) $R_E$:

$$R_E = \frac{I_{cq} \times R_E}{I_{cq}} = \frac{1.064 \times 10^{-3} \times 0.68 \times 10^3}{0.64}$$
\[ R_E = 0.7235V \]

\[ I_B = \frac{I_C \cdot f}{\beta} \]
\[ = \frac{1.064 \times 10^{-3}}{100} \]
\[ I_B = 1.064 \mu A \]

\[ R_B = 0.6 \text{K} \]

\[ I_e = \frac{V_{th} - V_{BE}}{R_B + (1 + \beta)R_E} \]

\[ V_{th} = I_e \left[ R_B + (1 + \beta)R_E \right] + V_{BE} \]
\[ = 0.64 \times 10^{-6} \left[ 6.868 \times 10^3 + (1 + 100) \times 680 \right] + 0.7 \]
\[ V_{th} = 1.5V \]

\[ \frac{V_{th}}{V_{cc}} = \frac{R_2}{R_1 + R_2} \]
\[ R_a = \frac{V_{th}}{V_{cc}} \Rightarrow \frac{1.5}{5} \Rightarrow 0.3 \]
\[ R_B = \frac{R_1 R_2}{R_1 + R_2} \Rightarrow R_1 \left[ \frac{R_2}{R_1 + R_2} \right] = 0.3 R_1 \]
\[ R_1 = \frac{R_B}{0.3} = \frac{6.868 \text{K}}{0.3} \]
\[ R_1 = 22.86 \text{K} \]

\[ R_2 = \frac{1}{\frac{1}{R_E} - \frac{1}{R_1}} \Rightarrow \frac{1}{6.868 \times 10^3 - \sqrt{2.866 \times 10^5}} \]
Design a Voltage divider Bias circuit for the specified conditions: $V_{cc} = 12V$, $V_{ce} = 6V$, $I_C = 1mA$, $\beta = 100$, $V_E = 1V$. 

**Voltage divider Bias**

1. $I_B = \frac{I_C}{\beta} \Rightarrow 10\mu A$
2. $I_E = I_B + I_C = 1.01mA$
3. $R_E = \frac{V_E}{I_E} = 990\Omega$
4. $R_C = \frac{V_{cc} - V_{ce} - V_E}{I_C} = 5k\Omega$
5. $S = \frac{1 + \beta}{1 + \beta \left[ \frac{R_E}{R_B + R_E} \right]} , \quad R_B = 2345\Omega$

(i) $V_B = V_E + V_{BE} = 1.7V$
(ii) $R_1 = \frac{V_{cc} - V_B}{I + I_B} \Rightarrow R_1 = 1454.86\Omega$
(iii) $R_2 = \frac{1.7}{I} \Rightarrow (I = 60.797mA)$

39) Determine the resistor values of the circuit shown in fig. for given operating point and supply voltage: $P = 100$, $V_{ceq} = 10V$, $I_{eq} = 1.5mA$

**Hint:** Emitter Bias
Let us assume \( V_E = \frac{1}{10} \) of \( V_{cc} \).

\[ V_E = \frac{1}{10} \cdot (20) \Rightarrow V_E = 2V \]

\[ I_{Bq} = I_{Cq} = \frac{I_{Cq}}{\beta} = \frac{1.5 \times 10^{-3}}{100} \]

\[ I_{Bq} = 15\mu A \]

\[ R_E = \frac{V_E}{I_E} = \frac{VE}{IB+IC} = \frac{2}{(15 \times 10^{-6}) + (1.5 \times 10^{-3})} \]

\[ R_E = 1.32k\Omega \]

\[ R_C = \frac{V_{cc} - V_{CE} - V_E}{IC} \]

\[ = \frac{20 - 10 - 2}{1.5 \times 10^{-3}} \Rightarrow R_C = 5.33k\Omega \]

\[ R_B = \frac{V_{cc} - V_{BE} - V_E}{IB} \]

\[ R_B = 1.15M\Omega \]

---

Try by yourself:

(iV) \( V_{CE} = V_{CC} - I_C R_C - I_E R_E \)

\( V_{CE} = 13.94V \)

(iV) \( V_C = V_{CC} - I_C R_C \)

\( V_C = 15.9875V \)

(vi) \( V_E = I_E R_E = 2.0462 \)

(vii) \( V_B = V_E + V_{BE} \)

\( V_B = 2.746375 \)

(viii) \( V_{BC} = V_B - V_C \)

\( V_{BC} = -1.84V \)
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Problems Continuation:

41) For the circuit shown in the figure, β = 100. Calculate Vc, Ic, Ic and Vce.

- i) Vc = Vb - VBE = 3.3V
- ii) Ic = \frac{Vc}{RE} = 1mA
- iii) Ic = \frac{Ic + Ib}{1 + \beta}
- iv) Vc = VCE - Ic RE = 3.84V
**Topic 3:** Bias Compensation

**Method of Stability of 8-Point Compensation**

- Compensation → temperature sensitive device. Such as Thermistor, Diode, Sensor.
- To maintain the operating point constant.
- It provides constant voltage.
- This device provides compensating voltage and current to stabilize the variation in $I_c$, $V_{BE}$ & $I_e$.

**Need:**

- Collector to Base Bias and the Voltage follower bias.
- Use negative feedback to do stabilization action.
- This negative feedback reduces the Amplification of the signal.
- If this loss in signal amplification is intolerable and extremely stable biasing conditions are required, then it is necessary to use Compensation Techniques.

Various Compensation techniques involved are,

1. Diode Compensation for $V_{BE}$ and $I_c$.
2. Thermistor Compensation.

**1. Diode Compensation for $I_c$:**

![Diode Compensation Diagram]

In case of Germanium Transistors, changes in $I_c$ with temperature are comparatively larger than...
As $I_B$ is constant, the collector current $I_C$ remains constant, and any change in $I_C$ with temperature are compensated by $I_C$.

\[
I_C = \frac{I_C}{B+I}
\]

\[
I_C = B I_B + (1+\beta) I_C
\]

If $\beta > 1$, we get:

\[
I_C = B I_B + (1+\beta) I_C
\]

\[
I = \frac{V_{EE}}{R_1} = \frac{I_B + I_C}{R_1}
\]

\[
V_{EE} = 0.2 \text{V}
\]

\[
I_C = \frac{I_C}{B+I_C}
\]

\[
V_{EE} = 0.2 \text{V}
\]

The current flowing through the diode is kept in reverse bias.

\[
I_C = \frac{I_C}{B+I_C}
\]

The leakage current $I_C$ is small compared to $I_C$. Leakage current at the same gate of the collector leakage of the diode, and the transistor are of the same type.

\[
I_C = \frac{I_C}{B+I_C}
\]

The changes in the $V_{EE}$ as important role in collector current stability.
2. DIODE COMPENSATION FOR VBE:

(a) Diode compensation in emitter circuit:

\[ V_{cc} \]
\[ Rc \]
\[ RB \]
\[ V_b \]
\[ V_d \]
\[ V_{BE} \]
\[ IE = IB + Ic \]
\[ RE \]
\[ RD \]
\[ D \]

\[ V_{bb} \]

\[ V_{DD} \] is used to keep diode in forward biased.

\[ V_{BB} \] changes by \( \Delta V_{BB} \) with change in temperature.

\[ V_d \] changes by \( \Delta V_d \) and \( \Delta V_d = \Delta V_{BB} \), the changes tend to cancel each other.

Apply KVL to the base circuit,

\[ V_{th} - IE \cdot RB - V_{BE} - (IB + IC) \cdot RE + V_d \longrightarrow (1) \]

\[ V_{th} = IB [RB + RE] + IC \cdot RE + V_{BE} - V_d \longrightarrow (2) \]

Leakage current:

\[ IC = \beta IB + (1 + \beta) I_{C0} \longrightarrow (3) \]

\[ IB = \frac{IC}{\beta} + \frac{(1 + \beta) I_{C0}}{\beta} \longrightarrow (4) \]

\[ IB \longrightarrow (5) \]
\[
\begin{align*}
I_C &= \frac{I_C}{B} \left[ \beta (R_B + R_E) \right] + \frac{I_C}{\beta} \left[ \beta (R_B + R_E) + V_{BE} - V_D \right] \\
&= \frac{I_C}{\beta} \left[ R_B + (1+\beta)R_E \right] = V_{th} - V_{BE} + V_D + \frac{R_B + R_E}{(1+\beta)I_C} \\
\end{align*}
\]

For voltage divider bias:

(b) Diode is connected in series with resistance \(R_2\) in the voltage divider bias and it is forward biased.

\[
I_E = \frac{V_B - V_{BE}}{RE} = \frac{V_E}{RE}
\]

\[
I_C = \frac{V_B - V_{BE}}{RE}
\]
When \( V_{BE} \) changes with temp, \( I_c \) also changes.
Diode is used to compensate,
\[
V_B = V_{R2} + V_D
\]
\[
I_c = \frac{V_{R2} + V_D - V_{BE}}{R_E}
\]

\( \rightarrow \) Diode is used as same type as Transistor,
Voltage across diode have same temp coefficient
\([-2.5\text{mV/°C}]\) as \( V_{BE} \).
\( \rightarrow \) \( V_{BE} \) changes by \( \delta V_{BE} \) with change in temp,
\( V_D \) changes by \( \delta V_D \) \([\delta V_D = \delta V_{BE}]\)
\[
I_c = \frac{V_{R2}}{R_E}
\]

\( \rightarrow \) Change in \( V_{BE} \) due to temp temperate are
Compensated by changes in the diode voltage
Which keeps \( I_c \) stable at a point.

3. **SENSITIVITY COMPENSATION TECHNIQUE**

**Fig(a):**

\( V_{cc} \)

\( R_T \)

\( R_c \)

\( R_E \)

\( R_2 \)

\( V_{BE} \)

\( \rightarrow \) This method of Transistor Compensation uses
temperature sensitive Resistive element, Sensors
rather than diode and transistors.
1. It has a positive temp coefficient. Resistance increases exponentially with increasing temp.

\[ \text{Slope of this curve} = \frac{\Delta R_T}{\Delta T} \]

\[ R_T \uparrow \]

\[ \text{Temp} \rightarrow \]

\[ \text{Fig (b): Temp Vs Resistance of Sensitiv} \]

\[ \Rightarrow \frac{\Delta R_T}{\Delta T} \rightarrow \text{Temp. coeff for thermistor} \]

\[ \Rightarrow \text{Slope is positive} \]

\[ \alpha \text{, Sensitiv has positive temp of resistance (PTC)} \]

\[ \Rightarrow \text{from fig (a): } R_1 \text{ is replaced by Sensitiv } R_T \text{ in self bias circuit} \]

\[ \Rightarrow R_T \text{ and } R_2 \text{ are two resistors of the potential divider} \]

\[ \Rightarrow \text{As temp increases, } R_T \text{ increases which decreases current flowing through it} \]

\[ \Rightarrow \text{Current through } R_2 \text{ decreases which reduces the voltage drop across it} \]

\[ \Rightarrow \text{Voltage drop across } R_2 \text{ is the voltage between base and ground} \]

\[ \Rightarrow \text{VBE reduces which decreases } I_B \]

\[ \Rightarrow \text{When } I_{CBO} \text{ increases with increase in temp, } I_B \text{ reduces due to reduction in VBE, maintaining } I_c \text{ constant} \]

4. THERMISTOR COMPENSATION:

\[ \Rightarrow \text{This Method of transistor Compensation} \]
uses temperature-sensitive resistive elements, thermistors, rather than diodes or transistors.

- It has a negative temperature coefficient; its resistance decreases exponentially with increasing temperature.

\[ \frac{\Delta R}{\Delta T} = \frac{dR}{dT} \]

**Fig (a)**: Temp Vs Resistance

Slope is Negative;

- Thermistor has a negative temperature coefficient of resistance (NTC)

**Fig (b)**:

- **Eqn (a)**: R2 is replaced by the thermistor RT in S.

  Bias circuit

- With increase in temp, RT decreases;

- Voltage drop across also decreases;

- Voltage drop is the Voltage at the Base with respect to ground.

- VBE decreases which reduces Ie;

- Behaviour will tend to offset the increase.
\[ I_c = \beta I_B + (1+\beta)I_{co} \]

There is an increase in \( I_{co} \) and decrease in \( I_B \) which keeps \( I_c \) almost constant.

**Fig (b):** Another thermistor compensation technique.

- The thermistor is connected between emitter and \( Vcc \) to minimize the increase in collector current due to changes in \( I_{co}, V_{BE} \) or \( \beta \) with temperature.
- \( I_c \) increases with temp and \( RT \) decreases with increase in temp.
- Current flowing through \( R_e \) is increased, which increases the voltage drop across it.
- \( E\!\!B \) junction is forward biased.
- But due to increase in voltage drop across \( R_e \), emitter (N-type NPN) is made more positive, which reduces \( V_{BE} \). \( I_B \) reduces.

\[ I_c = \beta I_B + (1+\beta)I_{co} \]

As \( I_{co} \) increases, \( I_B \) decreases & \( I_c \) is constant.

(x) Explain the method of stabilizing the Q-point (16m)

(x) Explain the circuit which uses a diode to compensate for changes in \( V_{BE} \) and \( I_{co} \).

(x) Discuss the operation of thermistor compensation.

(x) Explain Bias Compensation.

(x) Explain Sensors Compensation.

[M-10, D-10, D-12, D-09, D-13, D-04, M-03]
Topic 4: THERMAL STABILITY

- Maximum average power $P_d(\text{max})$ which a transistor is able to dissipate depends upon the transistor construction and may lie in the range from a few milliseconds to 200 kW.
- Power dissipated within a transistor is predominantly the power dissipated at its collector-base junction.
- Maximum power is limited by the temperature that the collector-base junction can withstand.
- For Si transistor this temp is in the range 150 to 225°C
- Ge transistor it is between 60 to 100°C.
- Collector-base junction temperature may rise because of reasons:
  a) due to rise in Ambient temperature
  b) due to self-heating

**Definition:**
Increase in collector current increases the power dissipated at the collector junction.
- Further increases the temp of the junction and hence increase in the collector current.
- Process is cumulative and it is referred to as self heating.
- Excess heat produced at the collector-base junction may even burn and destroy the transistor. This situation is called "thermal runaway" of the transistor.

**Thermal Resistance:**
- Steady state temp rise at the collector junction is proportional to the power dissipated at the junction $\Delta T = T_j - T_a = \Theta P_d$
- $T_j$ → Junction temp °C
- $T_a$ → Ambient temp °C
- $P_d$ → Power in Watts dissipated at collector junction.
- $\Theta$ → constant of proportionality
- $\Theta$, is called as Thermal Resistance $\Theta = \frac{T_j - T_a}{P_d}$
- Unit of $\Theta$ is °C/Watt.
A high-power transistor with an efficient heat sink to 1000°C/W for a low-power transistor.

Maximum collector power $P_c$ allowed for safe operation is specified at 25°C:

$$ P_c (W) \uparrow $$

It shows that above 25°C, collector power must be decreased, and at the extreme temp. at which the transistor may operate, $P_c$ is reduced to zero.

**Fig.** Power temp curve (Gle)

__(x)__ Condition for thermal stability__:

Thermal runaway may even burn and destroy the transistor. It is necessary to avoid thermal runaway.

Required condition to avoid thermal runaway is that the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated.

It is given by, $\frac{dP_c}{dT_J} < \frac{dP_D}{dT_J}$  \[\rightarrow (1)\]

\[\text{Diff:} \quad T_J - T_A = \theta P_D \]

\[1 = \theta \frac{dP_D}{dT_J} \Rightarrow \frac{dP_D}{dT_J} = \frac{1}{\theta} \quad \rightarrow (2)\]

\[\Rightarrow (2) \text{ in (1)} \quad \frac{dP_c}{dT_J} < \frac{1}{\theta}\]

This condition must be satisfied to prevent thermal runaway.

By proper design of biasing circuit, it is possible to ensure that the transistor cannot runaway below a specified ambient temperature or even under any conditions.

Let us consider voltage divider bias CRT for Analysis:

$$ P_c = Vcc \times I_c - I_c^2 R_c - I_e^2 R_e $$

$$ [P_c = \text{Heat at Collector} - \text{Power loss in } R_c \& R_e] $$

$$ I_c = I_e \quad P_c = Vcc I_c - I_c^2 (R_e + R_e) $$
\[
\frac{\Delta P_c}{\Delta I_c} = V_{cc} - 2I_c \left[ R_c + R_e \right]
\]

\[
\frac{\Delta P_c}{\Delta I_c} \cdot \frac{\Delta I_c}{\Delta T_j} < \frac{1}{8}
\]

\[
\frac{\Delta I_c}{\Delta T_j} = s \frac{\Delta I_c}{\Delta T_j} + s \frac{\Delta V_{BE}}{\Delta T_j} + s \frac{\Delta B}{\Delta T_j}
\]

\[\text{Fig.} \quad \text{Voltage Divider Bias}
\]

Junction temp affects collector current by affecting \( I_{cc} \). But doing Analysis for thermal Runaway the affection \( I_{co} \) dominates.

\[
\frac{\Delta I_c}{\Delta T_j} = \frac{\Delta I_{co}}{\Delta T_j}
\]

As Reverse Saturation current for both Si and Ge increase about 7 percent per°C,

\[
\frac{\Delta I_{co}}{\Delta T_j} = 0.07 I_{co}
\]

\[
\frac{\Delta I_c}{\Delta T_j} = s \times 0.07 I_{co}
\]

\[
\text{Substitute} \quad \frac{\Delta I_c}{\Delta T_j}, \frac{\Delta P_c}{\Delta I_c}, \text{in,} \quad V_{cc} - 2I_c \left[ R_c + R_e \right] < 0.07 I_{co}
\]

\[\text{As} \quad s, I_{co}, \theta \rightarrow +ve, \text{is always satisfied provided the quantity in bracket is } -ve; \]

\[V_{cc} < 2I_c \left[ R_c + R_e \right] \Rightarrow \frac{V_{cc}}{2} < I_c \left[ R_c + R_e \right]
\]

Apply KVL at collector CKT

\[V_{CE} = V_{cc} - I_c \left[ R_c + R_e \right]
\]

\[I_c \left[ R_c + R_e \right] = V_{cc} - V_{CE}
\]

\[\text{Substitute} \quad I_c \left[ R_c + R_e \right], \quad \frac{V_{cc}}{2} < V_{cc} - V_{CE} \Rightarrow V_{CE} < V_{cc}
\]

Thus if \( V_{CE} < \frac{V_{cc}}{2} \), the stability is ensured. But if Transformer coupled circuit, \( R_c \) and \( R_e \) are quite Small and \( V_{CE} = V_{cc} \). Hence it is Necessary to design Transformer coupled circuits with Stability Factor as close to 1 as possible to Avoid thermal Runaway.

STM: (W) DESIRE and Explain the Condition to Avoid thermo Runaway? [Ans: Above] (8m)
For the circuit shown in Fig, emitter voltage is \(-0.7\text{V}\). If \(\beta = 50\), find \(I_E, I_B, I_C\) and \(V_E\).

\[ \begin{align*}
I_C &= 10^5 \text{V} \\
5k\Omega &= \text{V} \\
I_B &= 10^7 \text{V} \\
10k\Omega &= \text{V} \\
10V &= \text{V} \\
-10V &= \text{V}
\end{align*} \]

**Solution:**

1) \[ I_E = \frac{V_E}{R_E} = \frac{V_E}{R_E} \]

2) To find \(V_E\): Using Nodal Analysis,

\[ \begin{align*}
V_E &= -0.7 \\
V_E &= -0.7 \text{V} \\
I_E &= 9.3 \times 10^{-3} \\
I_E &= 9.3 \times 10^{-3} \text{A} \\
I_E &= 0.93 \text{mA} \\
\end{align*} \]

3) \[ I_B = \frac{I_E}{1 + \beta} = \frac{9.3 \times 10^{-3}}{1 + 50} \]

\[ I_B = 18.2 \text{mA} \]

4) \[ I_C = I_E + I_B \]

\[ I_C = 9.3 \times 10^{-3} + 18.2 \times 10^{-6} \]

\[ I_C = 9.1 \text{mA} \]

5) \[ V_C = V_{\text{drop across } R_C} \Rightarrow I_C R_C = 0.91 \times 10^{-3} \times 5 \times 10^3 \]

\[ V_C = 10 - 4.55 \text{V} \]

\[ V = 5.45 \text{V} \]
For the circuit shown in Fig. calculate $I_B$, $I_C$, $I_E$, $V_{CE}$.

(i) $I_B$:

Apply KVL on Base Side

$9V - (1000)RB - V_{BE} = 0$

$9V - 100 \times 10^3 RB - 0.7 = 0$

$I_B = \frac{9.7 - 0.7}{100 \times 10^3} = 83 \times 10^{-6} A$

$i) I_B = 83 \mu A$

(ii) $I_C$:

$I_C = \beta I_B$

$= 45 \times 83 \times 10^{-6}$

$I_C = 3.735 \times 10^{-3}$

$I_C = 3.735 mA$

(iii) $I_E$:

$I_E = I_B + I_C$

$I_E = (83 \times 10^{-6}) + (3.735 \times 10^{-3})$

$I_E = 3.818 \times 10^{-3}$

$II) I_E = 3.818 mA$

(iv) $V_{CE}$:

Apply KVL on Collector Side,

$9V - (1.2K)R_C - V_{CE} = 0$

$V_{CE} = 9 - (1.2 \times 10^{-3}) \times (3.735 \times 10^{-3})$

When grounded $\Rightarrow V_{CE} = (-1.2 \times 10^{-3}) \times (3.735 \times 10^{-3})$

$V_{CE} = 9 - 4.82 V$

44) For the circuit shown in Fig. Determine $I_E$, $V_C$.

$R_E = 2.2K$

$b = 100; V_{BE} = 0.7 V$
\[ E = 2.2 \text{k} \]

**i) [Nodal Analysis]**

\[ I_E = \frac{V_B - V_A}{R} \Rightarrow \frac{V_E - V_{EE}}{2.2 \times 10^{-3}} \]

\[ V_E = V_B - V_{BE} \]

\[ V_{BE} = 0.7 \]

\[ V_E = -0.7 \text{V} \]

\[ I_E = \frac{-0.7 - (-8)}{2.2 \times 10^{-3}} \Rightarrow I_E = 3.3182 \times 10^{-3} \]

\[ I_E = 3.3182 \text{mA} \]

\[ V_C = V_{cc} - \text{Voltage drop across } R_C \]

\[ a) \text{ Voltage drop across } R_C, V = I_C R_C \]

\[ b) I_C = \beta I_B \]

\[ c) I_B = \beta I_B, I_E = I_B + I_C \]

\[ I_B = I_E - I_C \]

\[ I_B = I_E - \beta I_B \]

\[ I_B + \beta I_B = I_E \]

\[ I_B = \frac{I_E}{1 + \beta} \Rightarrow \frac{3.3182 \times 10^{-3}}{1 + 100} \]

\[ I_B = 3.285 \times 10^{-6} \]

\[ I_B = 32.85 \mu A \]

\[ \text{Solved in (b).} \]

\[ I_C = 100 \times 3.285 \times 10^{-6} \Rightarrow I_C = 3.285 \text{mA} \]
\[ V = (2.85 \times 10^{-3}) \times (1.8 \times 10^{-3}) \]
\[ V = 5.913V \]
\[ V_c = 10 - 5.913 \]
\[ V_c = 4.087V \]

**(iii)\[ V_{CE} = V_c - V_E \]
\[ V_{CE} = 4.087 - (-0.7) \]
\[ V_{CE} = 4.787V \]

---

For the circuit shown in Fig. 2,
Determine \( I_c, V_E \) and \( V_{CE} \).

**45.**

\[ V_{CC} = 6V \]
\[ R_B = 330 \Omega \]
\[ \beta = 120 \]
\[ R_E = 1.2 \Omega \]
\[ V_{EE} = -6V \]

\text{Apply KVL to Base, } V_{CC} - I_B R_B - V_{BE} - I_E R_E \Rightarrow V_{EE}

\[ I_E = I_c + I_B \]
\[ = \beta I_B + I_B \]
\[ I_E = (1 + \beta) I_B \]

\[ V_{CC} - 1 \times 330 \times 10^3 - 0.7 \times 1.2 \times 10^3 \]
\[ V_{CC} - (1 + \beta) I_B R_E - V_{EE} = 0 \]
\[ V_{CC} - V_{BE} - V_{EE} - I_B \left( R_B + (1 + \beta) R_E \right) = 0 \]

\[ I_B = \frac{V_{CC} - V_{BE} - V_{EE}}{R_B + (1 + \beta) R_E} \]
\[ I_B = \frac{6 - 0.7 - (-6)}{(330 \times 10^3) + (1 + 120)(1.2 \times 10^3)} \]
\[ I_B = 23.78 \mu A \]

\[ I_E = (1 + 120) \times 23.78 \times 10^{-6} \Rightarrow I_E = 2.877 mA \]
Voltage drop across $R_E$, $V_E = V_{EE} - V_{R_E}$

$$V = 3.452856 \text{V}$$

$$V_E = 6 + 3.452856$$

$$V_E = 2.547144 \text{V}$$

(iii) $V_{CE} = -V_E$

$$V_{CE} = 2.547144 \text{V}$$

For the circuit shown in Fig. calculate $I_E$, $I_C$, and $V_{CE}$.

**Solu Ans:**

i) Apply KVL on Base Side:

$$V_{EE} - I_B R_B - V_{BE} - V_{R_E} = 0$$

$$I_B = 25.06 \text{mA}$$

ii) Apply KVL on Collector Side:

$$V_{EE} - I_C R_C - V_{CE} - V_{R_E} = 0$$

$$V_{CE} = 4.961 \text{V}$$

For the circuit shown in Fig. $\beta = 100$, calculate $V_E$, $I_E$, $I_C$, and $V_C$.

**Ans:**

i) $V_{BE} = V_B - V_E$

$$V_E = 3.37 \text{V}$$

ii) $V_E = I_{R_E}$

$$R_E = 3.3k\Omega$$

$$I_E = 1 \text{mA}$$

iii) $I_C = \beta I_B$

$$I_C = 0.999 \text{mA}$$

iv) $I_B = \frac{I_E}{1 + \beta}$

$$I_B = 9.96 \text{mA}$$

v) $V_C = V_{CC} - I_C R_C$

$$V_C = 5.347 \text{V}$$
Calculate Values for \( I_B \), \( I_C \) and \( V_C \).

i) \( I_B : \)
\[
I_B = \frac{V_{th} - V_{BE}}{R_B + (1 + \beta) R_E}
\]
\[
I_B = 32.71 \text{mA}
\]

ii) \( V_{th} = \frac{20 + 20 \times 2.2 \text{K}}{8.2 \text{K} + 2.2 \text{K}} = 8.44 \text{V}
\]

(iv) \( I_C = \beta \cdot I_B = 4.25 \text{mA} \)

(v) \( V_C = V_{cc} - I_C R_E = 8.52 \text{V} \)

49) CB transistor is biased using single DC source. The transistor is \( SI \) with \( V_{BEQ} = 0.7 \text{V} \), \( \beta = 99 \) and \( I_{BO} = 80 \mu \text{A} \).

Find (a) \( R_2 \) (b) \( V_{CEQ} \).

\( i \) \( R_2 \) :-

Apply KVL on Base:
\[
V_{th} - I_{BRB} - V_{BE} - I_{E_{RE}} = 0. \quad (1)
\]

(a) \( V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{cc} \)
\[
= \frac{V_{cc} \cdot R_1 R_2}{R_1 (R_1 + R_2)} = \frac{R_2}{R_1} \cdot \frac{15 R_B}{10 \text{K}} = \frac{15 R_B}{10 \times 10^3} \]
\[
V_{th} = 15 \times 10^{-3} \cdot R_B \quad (2)
\]

SVB \( V_{th} \) in (1)

(1) \( \Rightarrow \)
\[
V_{th} = I_{BRB} + V_{BE} + I_{E_{RE}}
\]
\[
15 \times 10^{-3} R_B = (3 \times 10^{-6}) R_B + 0.7 + (3 \times 10^{-3}) \times 1 \times 10^{-3}
\]
\[
R_B = 2.517 \text{K} \Omega
\]
\[
V_{th} = 1.5 \times 10^{-3} \times 2.517 \times 10^{-3} = 3.7155 \text{V}
\]
\[
\frac{V_{BE}}{R_1+R_2} = 3.7755 = \frac{15 \times R_2}{10 \times 10^3 + R_2} \Rightarrow 3.7755 \left[ 10 \times 10^3 + R_2 \right] = 15 R_2 \\
\Rightarrow R_2 = 3.363 \text{k} \Omega 
\]

(i) \(V_{CEQ}\):

Apply KVL on collector,

\[ V_{CC} - I_{CQ} R_C - V_{CEQ} - V_{ERE} = 0 \]

\[ V_{CEQ} = V_{CC} - I_{CQ} R_C - V_{ERE} \]

\[ V_{CEQ} = 15 - (2.97 \times 10^{-3})(2 \times 10^3) - (3 \times 10^{-3})(1 \times 10^3) \]

\[ V_{CEQ} = 6.06 \text{V} \]

\[ I_{CQ} = 13 \times I_{EQ} = 2.99 \times 3 \times 10^{-6} \Rightarrow 2.99 \text{mA} \]

\[ I_E = I_C + I_B \Rightarrow (2.97 \times 10^{-3}) + (3 \times 10^{-6}) = 3 \text{mA} \]

**Topic 5: Design of Biasing for JFET**

**Introduction:**

- Parameters of FET are temperature dependent.
- As temperature increases, drain resistance also increases, reducing drain current.
- Thermal runaway does not occur with FET.
- Differences in maximum and minimum transfer characteristics make it necessary to keep drain current \(I_D\) stable at its quiescent value.

The general relationships that can be applied to the dc analysis of all FET amplifiers are:

\[
I_{EQ} = 0 \\
I_D = I_C
\]
Relationship between input and output quantities is non-linear due to squared term in Shockley's equation.

For JFET:

\[ I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_T} \right)^2 \]

(Biasing Methods):

Different biasing circuits of FET are:

1. Fixed Bias Circuit [Gate Bias]
2. Self Bias Circuit
3. Voltage Divider Bias Circuit

(Fixed Bias Circuit): [Gate Bias Circuit]

Diagram Explanation:

- The simplest of biasing arrangements for the n-channel JFET is fixed bias method.
- Coupling capacitors are open circuit for the d.c. analysis and low impedances [short circuit] for the a.c. analysis.
- To make gate-source junction reverse biased, a separate supply \( V_{GQ} \) is connected such that...
More Negative than the Source.

\[ V_i \] is present to ensure that \( V_i \) appears at
the input to the FET Amplifier for the AC Analysis.

For DC Analysis,

\[ I_G = 0 \]

\[ I_D = I_S \]

The negative terminal of the battery is connected
directly to the defined positive potential of \( V_{GS} \) as
indicates that the polarity of \( V_{GS} \) is directly opposite
that of \( V_{GG} \).

\[ (1) \quad \text{Input Circuit \[ Gate \ Side \] -} \]

\[ V_G \]

Apply KVL at the \[ Gate \ Side \],

\[ -V_{GG} - I_G R_G - V_{GS} = 0 \]

\[ I_G = 0 \]

\[ -V_{GG} = V_{GS} \]

\[ V_{GS} = -V_{GG} \]

\( V_{GG} \) is fixed DC supply, voltage \( V_{GS} \) is fixed in
magnitude, \( V_{GS} \) is "fixed bias configuration",

\[ \text{Shockley's equation: -} \]

Resulting level of drain current \( I_D \)

is said by,
\[ I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \rightarrow (2) \]

- \( V_{GS} = -V_{G1} \)

Substitute \( V_{GS} \) in (2)

\[ I_D = I_{DSS} \left[ 1 - \left( -\frac{V_{G1}}{V_P} \right) \right]^2 \]

\[ I_D = I_{DSS} \left[ 1 + \frac{V_{G1}}{V_P} \right]^2 \rightarrow (3) \]

### (iii) Output Side

#### Drain Circuit

![Circuit Diagram]

Apply KVL on the drain circuit,

\[ V_{DD} - I_D R_D - V_{DS} = 0 \]

\[ V_{DD} - I_D R_D = V_{DS} \]

\[ V_{DS} = V_{DD} - I_D R_D \]

### (iv) \( V_{DS} = V_D - V_S \)

\[ V_{DS} = V_D - 0 \] [Voltage at a point w.r.t. ground, \( V_S = 0 \)]

\[ V_{DS} = V_D \]

\[ V_{G1S} = V_{G1} - V_S \]

\[ V_{G1S} = V_{G1} - 0 \]

\[ V_{G1S} = V_{G1} \]
Fig: Voltage divider bias arrangement

Diagram Explanation:

→ It is p-channel JFET with voltage divider bias.
→ Voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse biased.
→ Coupling capacitors C₁ and C₂; Bypass capacitors Cs are assumed to be open circuit for DC Analysis.

(i) Input Side

Apply KVL on the input side,

\[ V_G - R_G I_G - V_G S - I_s R_S = 0 \]
\[ V_G - 0 - V_G S - I_s R_S = 0 \]
\[ I_G = 0 \]
\[
V_{G1} - V_{GS} - I_{DRS} = 0 \\
V_{G1} - I_{DRS} = V_{GS} \\
V_{GS} = V_{G1} - I_{DRS} \\
\text{\rightarrow (1)}
\]

\[
V_{G2} = \left( \text{Thevenin Voltage} \right) \\
V_{G2} = \frac{\text{Particular Resistor} \times \text{Voltage}}{\text{Sum of Resistor}} \\
V_{G2} = \frac{R_2 \times V_{DD}}{R_1 + R_2} \\
\text{\rightarrow (2)}
\]

\[
\text{Strockley's equation:} \\
I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 \\
\text{\rightarrow (3)}
\]

\[
SVB (1) \text{ to (3)} \\
I_D = I_{DSS} \left[ 1 - \frac{(V_{G1} - I_{DRS})}{V_P} \right]^2 \\
\text{\rightarrow (4)}
\]

\[
\text{Output Circuit} \left[ \text{Drain Side} \right] \\
\text{Apply KVL at the Drain Side,} \\
V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0
\]
\[ V_{DD} - I_{DRD} - I_{DRS} = V_{DS} \]

\[ V_{DS} = V_{DD} - I_{D}(R_{D} + R_{S}) \]  \( \text{(5)} \)

The DC-point of a JFET Amplifier is given by

\( I_{D}, V_{DS}, V_{GS} \)

**SELF BIAS**

- It is most common type of JFET Bias.
- This configuration eliminates the need for two d.c. supplies.

**Fig:** JFET Self Bias Configuration

**Diagram Explanation:**

- Controlling gate-to-source Voltage is determined by the Voltage across a resistor \( R_{S} \) in source.
- For d.c. Analysis, the capacitors can be replaced by open circuits, and resistor \( R_{G} \) replaced by a short circuit \( I_{G} = 0A \).
- \( R_{G} \) does not affect the bias.
- \( R_{G} \) is necessary only to isolate an a.c. signal.
from ground in Amplifier Applications

\( V_{DS} \) is Gate Source Junction Reverse Biased

**Fig: DC Analysis**

\[
\begin{align*}
V_{DD} & \downarrow \quad I_D \\
R_D & \downarrow \\
I_G = 0 & \quad V_{DS} \\
I_S & \quad (I_S = I_D) \\
V_{GS(0)} & \quad V_{RS}
\end{align*}
\]

**Input Circuit (Gate Side)**

\[
\begin{align*}
G_s & \quad D \\
I_G & \quad R_G \\
V_{gs} & \quad I_S \\
R_s & \quad (I_S = I_D)
\end{align*}
\]

Apply KVL at the input side,

\[-I_G R_G - V_{gs} - I_S R_S = 0
\]

\[0 - V_{gs} - I_D R_S = 0
\]

\[
\begin{align*}
\therefore I_G = 0 & \quad I_S = I_D \\
-V_{gs} & \quad -I_D R_S = 0
\end{align*}
\]

\[V_{gs} = -I_D R_S
\]

\[V_{gs} = -I_D R_S \quad \rightarrow (1)
\]

**Hperley's equation:**

\[
I_D = I_{DSS} \left[ 1 - \frac{V_{gs}}{V_P} \right]^2 \quad \rightarrow (2)
\]

\[
2D = I_{DSS} \left[ 1 - \frac{(-I_D R_S)}{V_P} \right]^2
\]
\[ I_D = \frac{V_{DS}}{V_P} \left( 1 + \frac{I_{DRS}}{V_P} \right)^2 \rightarrow (3) \]

**iii. Output Circuit [Drain Side]**

\[ \begin{align*}
& V_{DD} \quad \downarrow \quad I_D \\
& \quad \downarrow \quad I_D \\
& R_D \\
& \quad \downarrow \\
& V_{DS} \\
& \quad \downarrow (I_S = I_D) \\
& \quad \downarrow R_S \\
& \quad \downarrow \\
& \end{align*} \]

Apply KVL at the Drain (output) side,

\[ V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0 \]

\[ V_{DD} - I_D R_D - V_{DS} - I_{DRS} = 0 \]

\[ V_{DD} - I_D R_D - I_{DRS} = V_{DS} \]

\[ V_{DS} = V_{DD} - I_D R_D - I_{DRS} \]

\[ V_{DS} = V_{DD} - I_D [R_D + R_S] \]

\[ V_{DS} = V_D - V_S \]

\[ V_D = V_{DS} + V_S \]

\[ = V_{DS} + I_S R_S \]

\[ \implies V_D = V_{DS} + I_{DRS} \]

\[ \implies V_S = I_S R_S \]

**uns**: (x) What are the different Methods of JFET?

(x) Explain Self Bias and Fixed Bias JFET?

(x) Explain Voltage divider Bias JFET Configuration?

(x) Explain the Circuit of gate Bias for providing of JFET.
(X)

**Comment on fixed Biasing in BJT and FET.**

**Explain the procedure for locating operating point**

\[ N-06, M-06, M-08, M-07, N-08, M-12, N-12, N-13, N-15 \]

**Ans:**

\[ \text{Above} \]

**PROBLEMS**

\[ \text{JFET, Fixed Bias, Self Bias, Voltage divider Bias} \]

50) **find the fixed Bias circuit Arrangement parameters** for the circuit shown in Fig.

**Given:**

\[ \begin{align*}
I_{ds} &= 15 \text{mA} \\
V_P &= -10 \text{V} \\
R_D &= 1 \text{k}\Omega \\
V_{dd} &= 15 \text{V} \\
V_{gg} &= -3 \text{V}
\end{align*} \]

**To find:**

\[ \begin{align*}
V_{gs} & \quad I_D & \quad V_{ds} & \quad V_D & \quad V_{g} \\
\end{align*} \]

**Hint:** fixed Bias

\[ \begin{align*}
(i) \quad V_{gs} & = - \frac{V_{gg}}{2} \\
& = - (-3) \\
& = 3 \text{V}
\end{align*} \]

\[ \begin{align*}
(ii) \quad I_D & = I_{ds} \left\{ 1 - \frac{V_{gs}}{V_P} \right\}^2 \\
& = (15 \times 10^{-3}) \left\{ 1 - \frac{3}{-10} \right\}^2 \\
& = 7.35 \times 10^{-3} \text{A} \\
& = 7.35 \text{mA}
\end{align*} \]

\[ \begin{align*}
(iii) \quad V_{ds} & = V_{dd} - I_D R_D \\
& = 15 - (7.35 \times 10^{-3})(1 \times 10^3) \\
& = 15 - 7.35 \\
& = 7.65 \text{V}
\end{align*} \]
\[ V_{DS} = V_D - V_S \]
\[ V_D = V_{DS} + V_S \]
\[ V_D = V_{DS} \]
\[ V_D = 7.65\,V \]  

\[ (V) \quad V_{G1} = V_{G1S} - V_S \]
\[ V_{G1S} = V_{G1} - V_S \]
\[ V_{G1} = V_{G1S} \]
\[ V_{G1} = -3\,V \]

\[ \text{Ans:} \]
\[ \begin{align*}
V_D &= 7.65\,V \\
V_{G1} &= -3\,V \\
I_D &= 7.35\,mA \\
V_{DS} &= 7.65\,V \\
V_{G1S} &= -3\,V.
\end{align*} \]

5) Determine the following for the network shown:

Find:
1) \( V_{GSQ} \)
2) \( I_{DQ} \)
3) \( V_{DS} \)
4) \( V_D \)
5) \( V_{G1} \)
6) \( V_S \)

\[ V_{GSQ} = -V_{G1}G_1 \]
\[ V_{GSQ} = -2\,V \]

\[ I_{DQ} = I_{DSS} \left[ 1 - \frac{V_{GSQ}}{V_P} \right]^2 \]
\[ = 10 \times 10^{-3} \left[ 1 - \frac{-2}{-8} \right]^2 \]
\[ = 10 \times 10^{-3} \left[ 1 - \frac{8}{8} \right]^2 \]
\[ = 5.625 \times 10^{-3} \Rightarrow I_{DQ} = 5.625\,mA \]
\( V_{DS} = V_{DD} - I_{DRD} \)
\[ = 16 - (5.625 \times 10^{-3})(2 \times 10^{3}) \]
\[ = 16 - 11.25 \]
\[ V_{DS} = 4.75 \text{V} \]

(iv) \( V_D \):
\[ V_{DS} = V_D - V_s \quad (\therefore V_s = 0) \]
\[ V_D = V_{DS} \]
\[ V_D = 4.75 \text{V} \]

(v) \( V_G \):
\[ V_{GS} = V_G - V_s \quad (\therefore V_s = 0) \]
\[ V_G = V_{GS} \]
\[ V_G = -2 \text{V} \]

(vi) \( V_s \):
\[ V_s = 0 \text{V} \]

5.2) Determine the operating point values for the given fixed bias circuit in Fig. 1b. 

\( V_p = -6 \text{V} \)
\( I_{DSS} = 12 \text{mA} \)

Hint: (Fixed Bias)

Operating point \([V_{GS}, I_D, V_{DS}]\)

(i) \( V_{GS} \):
\[ V_{GS} = -V_G \]
\[ V_{GS} = -3 \text{V} \]

(ii) \( I_D \):
\[ I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2 \]
\[ = (12 \times 10^{-3}) \left[ 1 - \frac{-3}{-6} \right]^2 \]
\[ = 12 \times 10^{-3} \left[ 1 - 0.5 \right]^2 \]
\[ = 3 \times 10^{-3} \text{mA} \]

(iii) \( V_{DS} \):
\[ V_{DS} = V_{DD} - I_D R_D \]
\[ = 18 - (3 \times 10^{-3})(3 \times 10^3) \]
\[ = 4.75 \text{V} \]
53) Determine drain voltage $V_D$ for a fixed bias JFET circuit shown in fig. Given $V_{DD} = 15V$, $R_D = 1k\Omega$.

Try by yourself.

Hint: Fixed Bias

\[ V_{DD} - I_D R_D = V_{DS} \]

\[ V_{DS} = V_{DD} - I_D R_D \]

\[ V_{DS} = 7V \]

\[ V_D = V_{DS} = 7V \]

54) For the bias JFET, determine $I_D$ and $V_{GS}$. Given $V_{DD} = 14V$, $R_D = 1.4k\Omega$, $V_{DS} = 9V$, $I_{DS} = 8mA$ 

Try by yourself.

Hint: Fixed Bias

\[ I_D = \frac{V_{DD} - V_{DS}}{R_D} \]

\[ I_D = 3.13mA \]

55) Determine the following for the network of fig. 

Find $V_{GSQ}$, $I_{DQ}$, $V_{DS}$, $V_{S}$, $V_{D}$.

Hint: Self Bias

$I_{DS} = 8mA \Rightarrow 8 \times 10^{-3} A$

$V_p = -6V$. 

(i) $V_{G_T} = V_{T_S} - I_D R_S$

$$V_{T_S} = -I_D x 10^3$$

\[ a) \]

$$I_D = I_{DSS} \left[ 1 - \frac{V_{G_T}}{V_F} \right]^2$$

$$= (8 \times 10^3) \left[ 1 + \frac{(1 \times 10^3) I_D}{-b} \right]^2$$

$$= 8 \times 10^{-3} \left[ 1 - \frac{1000 I_D}{b} \right]^2$$

\[ b)\]

$$I_D = 8 \times 10^{-3} \left[ b - 1000 I_D \right]^2$$

$$= 8 \times 10^{-3} \left[ 36 - 1 \cdot I_D + 10^6 I_D^2 \right]$$

\[ c) \]

$\therefore (a - b)^2 = a^2 + b^2 + 2ab$

$$8 \times 10^3 I_D^2 - 132 I_D + 0.288 = 0$$

$$I_D = \frac{132 \pm \sqrt{(132)^2 - 4 \times 8 \times 10^3 \times 0.288}}{2 \times 8 \times 10^3}$$

$$I_D = 13.2 \pm \sqrt{132^2 - 4 \times 8 \times 10^3 \times 0.288}$$

$$a = 8 \times 10^3 \quad b = -132 \quad c = 0.288$$

$$I_D = 13.9 \text{ mA (OK)} \quad 2.5 \text{ mA}$$

$I_D$ cannot be higher than $I_{DSS}$. \therefore $I_D = 2.5 \text{ mA}$

\[ d) \]

$$V_{G_T} = -(2.5 \times 10^{-3}) \times 10^3$$

$$V_{G_T} = -2.5 V$$

\[ e) \]

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

$$= 20 - 2.5 \times 10^{-3}[3.3] \times 10^3$$

$$V_{DS} = 9.25 V$$

\[ f) \]

$$V_S = I_D R_S$$

$$= (2.5 \times 10^{-3}) \times (10^3)$$

$$V_S = 2.5 V$$

\[ g) \]

$V_G = 0 V$

\[ h) \]

$V_D = V_D = V_{DD} + V_S$

$$= 9.25 + 2.5$$
\[ V_{DS} = V_{DD} - I_D \left[ R_D + R_S \right] \]
\[ = 20 - 6 \times 10^{-3} \left[ 2 \times 10^3 + 500 \right] \]
\[ V_{DS} = 5 \text{V} \]

\[ V_D = V_{DS} + V_S \]
\[ = (5 + 3) \text{V} \]
\[ V_D = 8 \text{V} \]

3) A Voltage divider bias is provided to an N-Channel JFET circuit as shown in Fig. To establish \( I_{DSS} = 10 \text{mA} \)
\( V_P = -3.5 \text{V} \), \( R_1 + R_2 = 20 \text{k} \Omega \), \( I_D = 5 \text{mA} \) and \( V_{DS} = 5 \text{V} \), determine the values of \( R_1, R_2 \) and \( R_D \).

\[ V_{GS} \]
\[ I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 \]
\[ 5 = 10 \left[ 1 - \frac{-1.008}{(-3.5)} \right]^2 \]
\[ \therefore V_{GS} = -1.008 \text{V} \]

\[ V_S = V_D - V_{DD} \]
\[ = (5 \times 10^{-3})(0.5 \times 10^3) - 5 \]
\[ \Rightarrow V_S = -2.5 \text{V} \]
\[
V_G = V_{GS} - V_s \\
V_{GS} = V_G - V_s \\
\therefore V_G = \frac{-R_2}{R_1 + R_2} (10) - 5 \\
-3.508 = \frac{R_2}{20 \times 10^3} \\
R_2 = 2.984K \Omega \\
R_1 + R_2 = 20K \Omega \\
R_1 = 20 \times 10^3 - 2.984 \times 10^3 \\
R_1 = 17.016K \Omega \\
V_{DS} & RD = 5 - I_D R_D - I_D R_S (\text{-5}) \\
I_D = \frac{10 - V_{DS} - I_D R_S}{5} \\
R_D = 0.5K \Omega \\
\]

60) A JFET Amplifier with a Voltage divider biasing circuit has the following parameters: \( V_p = -2V, I_{DS} = 4\text{mA}, R_D = 910 \Omega, R_S = 5K \Omega, R_1 = 12M \Omega, R_2 = 8.57M \Omega \) and \( V_{DD} = 24V \). Find the value of the drain current \( I_D \) at the operating point. Verify the FET will operate in the pinch-off region.

**Hint:** Voltage divider bias

**Soh:**
\[
V_G = \frac{R_2}{R_1 + R_2} \\
V_{DD} = \frac{8.57 \times 10^6 \times 24}{(12 + 8.57) \times 10^6} \\
V_G = 10V
\]
\[ I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right] \]
\[ = I_{DSS} \left[ 1 - \left( \frac{V_{GS} - I_{DRS}}{V_P} \right) \right] \]
\[ = 4 \times \left[ 1 - \left( \frac{10 \times I_D + 3}{2} \right) \right]^2 \]
\[ = 9 \left( I_D \right)^2 - 78I_D + 144 = 0 \]
\[ \therefore I_D = 3.39 \text{mA}, \quad \text{and} \quad 4.72 \text{mA} \]

\[ I_D < I_{DSS}, \quad \therefore I_D = 3.39 \text{mA} \]

\[ V_{GS} = V_{eq} - I_{DRS} \]
\[ = 10 - \left[ 3.39 \times 10^{-3} \times 3 \times 10^3 \right] \]
\[ V_{eq} = -0.17 \text{V} \]

\[ V_{DS} = V_{DD} - I_D \left[ R_D + R_S \right] \]
\[ = 24 - 3.39 \times 10^{-3} \left[ 0.91 + 3 \right] \times 10^3 \]
\[ V_{DS} = 10.745 \text{V} \]

\[ V_{DG} = V_{DS} - V_{eq} \]
\[ = 10.745 + 0.17 \]
\[ V_{DG} = 10.915 \text{V} \]

\[ V_{DG} \approx \left| V_P \right| = 2 \text{V}. \quad \therefore \text{Hence FET in pinch-off region.} \]

6. \text{Determine } I_D, V_{GS}, V_D, V_{DS}, V_{DG} \text{ for the given network shown in Fig.}

\[ I_{DSS} = 8 \text{mA} \]
\[ V_P = -4 \text{V} \]

\text{Note: Voltage divider bias.
\[ V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD} \]
\[ = \frac{270 \times 10^3}{(2100 + 270) \times 10^3} \times 20 \]
\[ V_G = 2.28 \text{V} \]

\[ V_{G1} = V_G - V_S \]
\[ = 2.28 - 1.5 \times 10^3 \text{I}_D \]

\[ I_D = I_{DSS} \left[ 1 - \frac{V_{G1}}{V_P} \right]^2 \]
\[ = 8 \left[ 1 - \left( \frac{2.28 - 1.5 \text{I}_D}{1} \right) \right]^2 \]
\[ I_D = \frac{8}{16} \left[ 4 + 2.28 - 1.5 \text{I}_D \right]^2 \]
\[ = 0.5 \left[ 6.28 - 1.5 \text{I}_D \right]^2 \]
\[ 2 \text{I}_D = 39.44 - 18.84 \text{I}_D + 2.25 \text{I}_D^2 \]
\[ 2.25 \text{I}_D^2 - 20.84 \text{I}_D + 39.44 = 0 \]
\[ I_D = \frac{-20.84 \pm \sqrt{(20.84)^2 - 4 \times 2.25 \times 39.44}}{2 \times 2.25} \]
\[ I_D = 6.6 \text{mA} \text{ (or) } 2.6 \text{mA} \]

\[ V_{DS} \rightarrow \text{Negative, Value may be Neglected.} \]

Choose \[ I_D = 2.65 \text{mA} \]

\[ I_{DQ} = 2.65 \text{mA} \]

\[ V_{G1} = 2.28 - 1.5 \times \text{I}_{DQ} \]
\[ = 2.28 - (1.5 \times 2.65) \times 10^{-3} \]
\[ V_{G1} = -1.695 \text{V} \]
\[ V_{DSQ} = V_{DD} - I_{DQ} \left( R_D + R_S \right) \]
\[ = 20 - 2.65 \times 10^{-3} \left( 4.7 + 1.5 \right) \times 10^3 \]
\[ V_{DSQ} = 3.57 \text{V} \]

(vi) \[ V_S = \frac{I_{DRS}}{R_S} \]
\[ = 2.65 \times 10^{-3} \times 1.5 \times 10^3 \]
\[ V_S = 3.975 \text{V} \]

(vii) \[ V_{DS} = V_D - V_S \]
\[ V_D = V_{DS} + V_S \]
\[ = 3.975 + 3.57 \]
\[ V_D = 7.55 \text{V} \]

(viii) \[ V_{DG} = V_D - V_{EQ} \]
\[ = 7.55 - 2.08 \]
\[ V_{DG} = 5.265 \text{V} \]

Obtain the values of \( V_{DSQ}, I_{DQ}, \) and \( V_{DS} \) for the voltage divider bias circuit shown in fig.

\[
V_{EQ} = \frac{R_2 \times V_{DD}}{R_1 + R_2}
\]
\[ V_{EQ} = 3.836 \text{V} \]

\[ I_{DSQ} = 6 \text{mA} \]
\[ V_P = -4 \text{V} \]

Try it yourself

Hint: Voltage divider bias

\[
V_{EQ} = \frac{R_2 \times V_{DD}}{R_1 + R_2}
\]
(ii) \( V_{gs} = V_{g} - V_{s} \implies V_{gs} = 3.84 - 1 \times 10^{-3} I_{D} \)

(iii) \( I_{D} = \frac{I_{Ds} \left( 1 - \frac{V_{gs}}{V_{p}} \right)^{2}}{\left[ A_{DQ} < I_{Ds} \right]} \), \( I_{D} = 18.94 \text{mA} \) or \( 4.41 \text{mA} \)

(iv) \( V_{gs} = 3.84 - 1 \times 10^{-3} I_{D} \implies V_{gs} = -0.57 \text{V} \)

(v) \( V_{DS} = V_{DD} - I_{D} \left[ R_{D} + R_{S} \right] \implies V_{DS} = 0.975 \text{V} \)

An N-channel JFET having \( V_{p} = -4 \text{V} \) and \( I_{Ds} = 10 \text{mA} \) is used in the circuit of Fig. The parameter values are \( V_{DD} = 18 \text{V} \), \( R_{S} = 2 \text{K} \Omega \), \( R_{1} = 450 \text{K} \Omega \), \( R_{2} = 90 \text{K} \Omega \). Determine \( I_{D} \) and \( V_{D} \)

**Hints:**

**Ans.**

(i) \( V_{gs} = V_{g} - I_{D} R_{S} \)

\[ V_{g} = \frac{R_{2}}{R_{1} + R_{2}} \cdot V_{DD} \]

\[ V_{g} = 3 \text{V} \]

\[ V_{gs} = \left[ 3 - 2 \times 10^{-3} I_{D} \right] \]

(ii) \( J_{D} = \frac{I_{D} \left[ 1 - \frac{V_{gs}}{V_{p}} \right]}{\left[ 1 - 3 - 2 \times 10^{-3} I_{D} \right]^2} \)

\[ J_{D} = 4.9 \text{mA} \] or \( 2.5 \text{mA} \)

(iii) \( V_{DS} = V_{DD} - I_{DQ} \left[ R_{D} + R_{S} \right] \)

\[ V_{DS} = 8 \text{V} \]
Advantages:
1. Input resistance is high.
2. Thermal stability is high.
3. Less noisy than BJT.

FET is a unipolar device, voltage controlled device [output ID current is controlled by input voltage Vgs].

Drain characteristics

\[ I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \]

\( i) \) N-channel
\[ G \rightarrow \text{P} \rightarrow D \]
\[ S \]

\( ii) \) P-channel
\[ G \rightarrow \text{N} \rightarrow D \]
\[ S \]

FET parameters:

i) Transconductance \( (g_m) \), \[ g_m = \frac{\Delta I_D}{\Delta V_{GS}} | V_{DS} \text{ const} \]

ii) Drain Resistance \( (R_d) \), \[ r_d = \frac{\Delta V_{DS}}{\Delta I_D} | V_{GS} \text{ const} \]

iii) Amplification factor \( (\mu) \), \[ \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} | I_D \text{ const} \]

\( \Theta \)-Point:

\[ I_D \rightarrow \Theta \rightarrow \text{Operating Point} \rightarrow \text{Loadline} \]

\[ \Theta \rightarrow V_{GS} \rightarrow V_{DS} \]
Biases

(2m) In JFET, drain current \( I_D \) changes with temp. Hence \( Q \)-point changes. In order to obtain the stable \( Q \)-point JFET is biased for zero temp drift. The \( Q \)-point is selected in the middle of the transfer characteristics (or) drain characteristics.

\[ I_D = K \left( V_{GS} - V_{TH} \right) \]

\[ K = I_D \left( \delta N \right) / \left( V_{GD} - V_{TH} \right)^2 \]

\( * \) JFET Biassing - MOSFET

(2m) The similarities in appearance between the transfer curves of JFET and depletion-type MOSFET permit a similar analysis in the d.c. domain.

→ The primary difference between the list is the fact that depletion-type MOSFET permit operating points with positive values of \( V_{GS} \) and levels of \( I_D \) that exceeds \( I_{DS} \).

→ The analysis is the same if the JFET is replaced by a depletion-type MOSFET.

→ The procedure followed for analysis of DMOSFET biasing circuits is exactly same as the one followed for the JFET biasing circuits.

<table>
<thead>
<tr>
<th>N-channel D-MOSFET</th>
<th>P-channel D-MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>( G_1 ) [ \rightarrow ] ( D ) [ \rightarrow ] ( S ) [ \rightarrow ] ( G_1 ) [ \rightarrow ] ( D ) [ \rightarrow ] ( S )</td>
<td></td>
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</tbody>
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<table>
<thead>
<tr>
<th>N-channel E-MOSFET</th>
<th>P-channel E-MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>( G_1 ) [ \rightarrow ] ( D ) [ \rightarrow ] ( S ) [ \rightarrow ] ( G_1 ) [ \rightarrow ] ( D ) [ \rightarrow ] ( S )</td>
<td></td>
</tr>
</tbody>
</table>

\( D \) = Depletion type
\( E \) = Enhancement type

\( V_{GS} \) must be more than \( V_{TH} \), \( V_{GS} > V_{TH} \)

\( \rightarrow \) Threshold Voltage Must be 2x
IC 6: DESIGN OF BIASING FOR MOSFET

1) D-MOSFET Biasing
   1. Gate Bias [Fixed Bias]
      2. Self Bias
      3. Voltage Divider Bias

2) E-MOSFET Biasing
   1. Voltage Divider Bias
      2. Drain Feedback Bias

3) D-MOSFET Biasing
   1. Fixed Bias / Gate Bias Method:
for d.c. Analysis

\[ I_G = 0 \]
\[ I_D = I_S \]  

Input circuit:

Apply KVL at the Gate Side:

\[ -V_{GG} - I_G R_G - V_{GS} = 0 \]
\[ I_G = 0 \]
\[ -V_{GG} - 0 - V_{GS} = 0 \]
\[ -V_{GG} = V_{GS} \]

\[ I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 \]
\[ V_{GS} = -V_{GG} \]
\[ I_D = I_{DSS} \left[ 1 + \frac{V_{GS}}{V_P} \right]^2 \]

Output circuit:

Apply KVL at Drain Side:

\[ V_{DD} - I_{DRS} - V_{DS} = 0 \]
\[ V_{DS} = V_{DD} - I_{DRS} \]
\[ V_{DS} = V_D - V_S \]
\[ V_{GS} = V_G - V_S \]
\[ V_S = 0 \]
\[ V_{DS} = V_D, V_{GS} = V_G \]

Voltage divider Bias Method:

The N-channel JFET like

N-channel D-MOSFET is given by,

Same derivation as JFET Voltage divider Bias.
i) Input Side [Gate Method]

Apply KVL at input:

\[ V_G - R_G I_G - V_G S - I_S R_S = 0 \]

\[ \therefore I_G = 0 \]

\[ V_G - V_G S - I_D R_S = 0 \]

\[ \therefore I_D = I_S \]

\[ V_G S = V_G - I_D R_S \]

ii) Shockley's equation

\[ I_D = I_{DSS} \left[ 1 - \frac{V_G S}{V_P} \right]^2 \]

\[ I_D = I_{DSS} \left[ 1 - \frac{(V_G - I_D R_S)}{V_P} \right]^2 \]

iii) Output Side [Drain Side]

Apply KVL at output,

\[ V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0 \]

\[ V_{DD} - 2I_D R_D - V_{DS} - I_D R_D = 0 \]

\[ V_{DS} = V_{DD} - I_D \left[ R_D + R_S \right] \]

The Q-point of D-MOSFET are \( I_D, V_{DS}, V_G S \)
3. **Self Bias Method**

\[ 
\begin{align*}
V_{DD} \downarrow & I_D \\
I_D \downarrow & R_D \\
\downarrow & I_S = I_D \\
\end{align*}
\]

This is the most common type of Biasing.

(i) **Input Side**: [Gate]

Apply KVL at input
\[ I_{G} R_G = V_{G_{SS}} - I_S \]

\[ I_S = I_D \]

(ii) **Shockley's equation**:

\[ I_D = I_{DSS} \left[ 1 - \frac{V_{G_{SS}}}{V_P} \right] \]

\[ I_D = I_{DSS} \left[ 1 + \frac{I_{DRS}}{V_P} \right] \]

(iii) **Output Side**:

Apply KVL at output
\[ V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0 \]

\[ V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0 \]

\[ V_{DS} = V_{DD} - I_D (R_D + R_S) \]
1. **Voltage divider Bias**

\[ V_{DD} \]

\[ R_1 \]

\[ I_{Q} = 20A \]

\[ V_{GQ} \]

\[ R_D \]

\[ V_{GS} \]

\[ R_S \]

\[ V_{DS} \]

\[ V_{IS} = I_D \]

\[ I_D = K \left[ V_{GS} - V_{GS(TH)} \right]^2 \]

\[ K = \frac{I_D(ON)}{\left[ V_{GS(ON)} - V_{GS(TH)} \right]^2} \]

2. **Input Side [Gate Circuit]**

Apply KVL at gate side,

\[ V_{GQ} = R_G I_Q - V_{GS} - I_D R_S = 0 \]

\[ I_Q = 0, I_S = I_D \]

\[ V_{GQ} = 0 - V_{GS} - I_D R_S = 0 \]

\[ V_{GS} = V_{G} - I_D R_S \]

3. **Shockley's equation**

\[ I_D = K \left[ V_{GS} - V_{GS(TH)} \right]^2 \]

\[ K = \frac{I_D(ON)}{\left[ V_{GS(ON)} - V_{GS(TH)} \right]^2} \]

4. **Output Side [Drain Circuit]**

Apply KVL at output side,

\[ V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0 \]

\[ V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0 \]

\[ V_{DS} = V_D - I_D R_D \]

\[ V_{DS} = V_D - I_D [R_D + R_S] \]
2. **Drain Feedback Bias Circuit**

A popular Biasing Arrangement for E-typed MOSFET

\[ V_{GS} = V_{DD} - V_{DS} \]

\[ I_G = 0 \]

\[ V_{RG} = 0 \]

\( j \) **Input Side [Gate Side]**

Apply \( V_{DD} \) at Gate Side

\[ V_{DD} - (I_D + I_G)(R_D) - V_{DS} = 0 \]

\[ (I_G = 0) \]

\[ V_{DD} - I_D R_D - I_D R_G - V_{GS} = 0 \]

\[ V_{DD} - I_D R_D - I_D R_G - V_{GS} = 0 \]

\[ V_{DD} - I_D R_D = V_{GS} \]

\( ii \) **Shockley's Eqn**

\[ I_D = K \left[ V_{GS} - V_{GS(TH)} \right]^2 \]

\[ K = \frac{I_D(ON)}{\left[ V_{GS(ON)} - V_{GS(TH)} \right]^2} \]

\( iii \) **Output Side [Drain Side]**

Apply \( V_{DD} \) at Output Side

\[ V_{DD} - (I_D + I_G)(R_D) - V_{DS} = 0 \]

\[ V_{DD} - R_D I_D - R_D I_G - V_{DS} = 0 \]

\[ (I_G = 0) \]

\[ V_{DD} - R_D I_D = 0 - V_{DS} = 0 \]

\[ V_{DD} - R_D I_D = V_{DS} \]

\[ V_{DS} = V_{DD} - R_D I_D \]
(x) Explain D-MOSFET Biasing Methods.
(x) Explain D-MOSFET Voltage divider Bias
(x) Explain Self Bias of D-MOSFET, and E-MOSFET
(x) Explain Gate Bias (Fixed bias) of E-MOSFET and D-MOSFET
(x) Explain E-MOSFET drain feedback Bias
(x) Explain E-MOSFET Voltage divider Bias

\[ V_{G1} = \frac{R_2}{R_1 + R_2}, \quad V_{DD} \]
\[ V_{G1S} = V_{G1} - I_D R_S \]
\[ V_{DS} = \frac{V_{DD} - I_D (R_D + R_S)}{R_D} \]

\[ V_{GS} = \frac{V_{DD}}{R_D} \]
\[ V_{DS} = V_{DD} - I_D \]

\[ V_{G1} = \frac{R_2}{R_1 + R_2}, \quad V_{DD} \]
\[ V_{G1S} = V_{G1} - I_D R_S \]
\[ V_{DS} = \frac{V_{DD} - I_D (R_D + R_S)}{R_D} \]
- MOSFET
  Voltage divider Bias

- MOSFET
  Source Bias

- MOSFET
  Fixed bias

- MOSFET - Drain feedback Bias, Voltage divider Bias

\[
\begin{align*}
V_{GS} &= \frac{V_{g3} - V_{DS}}{R_1 + R_2} \\
V_{DS} &= V_{DD} - \frac{V_{g3} - V_{IDR}}{R_D + R_S} \\
V_{g3} &= V_{G} - V_{IDR}
\end{align*}
\]

\[
\begin{align*}
V_{DS} &= V_{DD} - \frac{V_{g3} - V_{IDR}}{R_D + R_S} \\
V_{g3} &= \frac{V_{g3}}{R_D + R_S} - V_{IDR}
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\end{align*}
\]
Calculate the value of feedback resistor (Rs) required to self bias an N-channel JFET with $I_{DS} = 40\,mA$, $V_p = -10\,V$, and $V_{GSQ} = -5\,V$.

**Hint:** Self Bias - JFET

c) $I_D$:

a) $V_{GS} = -I_D R_S$

b) $R_S = \left| \frac{V_{GS}}{I_D} \right| = \frac{-5}{I_D} \rightarrow (1)$

c) $I_D = I_{DS} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2$

\[
= 40 \times 10^{-3} \left[ 1 - \frac{-5}{-10} \right]^2
= 40 \times 10^{-3} \left[ 1 - 0.5 \right]^2
= 40 \times 10^{-3} \left[ 0.5 \right]^2
\]

$I_D = 10 \times 10^{-3}$

$I_D = 10\,mA$ \hspace{1cm} (2)

c) $V_{GSQ}$ in (1):

$$Rs = \left| \frac{-5}{10 \times 10^{-3}} \right| \implies Rs = 500\,\Omega$$

65) For the circuit shown in Fig. calculate $I_{DS}$ and $V_{DSQ}$.

- $V_{DD} = 18\,V$
- $I_{DS} = 6\,mA$
- $V_p = -3\,V$

d) **Voltage divider bias** - D-MOSFET
\[ V_{G1} = \frac{V_{DD}}{R_1 + R_2} \]
\[ = \frac{10 \times 10^6}{(10 + 110) \times 10^6} \times 18 \]
\[ V_{G1} = 1.5\text{V} \]

\[ I_D = I_{DS} \left[ 1 - \frac{V_{G1} - V_{TH}}{V_P} \right]^2 \]
\[ = 6 \times 10^{-3} \left[ 1 + 0.5 - 250 I_D \right]^2 \]
\[ = 6 \times 10^{-3} \left[ 1 - 50 I_D \right]^2 \]
\[ = 6 \times 10^{-3} \left[ 2.25 - 150 I_D + 62500 I_D^2 \right] \]
\[ I_D = 0.0135 - 5.5 I_D + 375 I_D^2 \]
\[ 375 I_D^2 - 5.5 I_D + 0.0135 = 0 \]
\[ I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \]
\[ = \frac{-5.5 \pm \sqrt{(5.5)^2 - 4(375 \times 0.0135)}}{2 \times 375} \]
\[ I_D = 0.0135 \text{mA} \text{ (or) 8.11mA} \]
\[ I_D = 11.55\text{mA} \]

\[ V_{DS} = V_{DD} - I_D (R_D + R_S) \]
\[ = 18 - 11.55 \times 10^{-3} [1.8 + 0.75] \times 10^3 \]
\[ = -11.45\text{V} \]

\[ V_{DS} \text{ is practically Not Acceptable. Choose} \]
\[ I_D = 3.11\text{mA} \]

\[ V_{DS} = V_{DD} - I_D (R_D + R_S) \]
\[ = 18 - 3.11 \times 10^{-3} [1.8 + 0.75] \times 10^3 \]
\[ V_{DS} = 10.07\text{V} \]
ii) \( V_{GSQ} \text{ and } V_{DS} \):

\[ V_{GSQ} = -2.4 \text{ ID} \]

\[ \text{Hint: D-Mosfet Self Bias} \]

\[ \text{IDSS} = 8 \text{ mA} \]
\[ V_p = -8 \text{ V} \]

\[ V_{ds} = V_{dd} - \text{IDRD} \]
\[ V_{ds} = 20 - (1.77 \times 6.2) \]
\[ V_{ds} = 9.026 \text{ V} \]

67) The circuit shown in Fig. represents a small signal such that \( V_o \) is 20 times \( V_{x} \) Amplitude. 
Find the necessary...
68) Determine the source to drain voltage required to bias a p-channel enhancement-mode MOSFET in the saturation region. Given $K_P = 0.2 mA/V^2$, $V_{TP} = -0.50 V$, and $I_D = 15 mA$.

To find $V_{SD}$:

\[
I_D = K_P \left( V_{GS} - V_{TP} \right)^2
\]

\[
0.5 \times 10^{-3} = 0.2 \times 10^{-3} \left( V_{GS} - 0.50 \right)^2
\]

\[
2.5 = V_{GS} - V_{GS1} + 0.25
\]

\[
V_{GS} = 2.25
\]

\[
V_{GS} = - (1) \pm \sqrt{(1)^2 - 4(1)(-2.25)}
\]

\[
2(1)
\]

\[
V_{GS} = 2.08 V \text{ (OV)} - 1.08 V
\]

\[
V_{GS} = 2.08 V
\]

To find p-channel MOSFET in Saturation region,

\[
V_{SD} > V_{GS} \text{ (sat)} \Rightarrow V_{GS} + V_{TP} \Rightarrow 2.08 - 0.5
\]

\[
V_{SD} = 1.58 V
\]
Consider the given circuit. Assume that \( I_1 = 0 \). 

\[ R_2 = 20 \text{K}\Omega, \quad R_D = 10 \text{K}\Omega, \quad V_{DD} = 6 \text{V}, \quad V_{gS}(T_2) = 1 \text{V} \]

\[ K = 0.2 \text{mA/V}^2 \]

\[ V_{gS} = V_{gs} + V_{gS}(T_2) \]

\[ = \frac{R_2}{R_1 + R_2} \times V_{DD} \]

\[ = \frac{20 \times 10^3}{(30 + 20) \times 10^3} \times 6 \]

\[ V_{gS} = 2.4 \text{V} \]

(i) \( I_D \):

\[ I_D = K \left( V_{gS} - V_{gS}(T_2) \right)^2 \]

\[ = 0.2 \times 10^{-3} \left( 2.4 - 1 \right)^2 \]

\[ = 0.2 \times 10^{-3} \left( 1.4 \right)^2 \]

\[ I_D = 0.392 \text{mA} \]

(ii) \( V_{DS} \):

\[ V_{DS} = V_{DD} - I_D \times R_D \]

\[ = 6 - (0.392 \times 10^{-3}) (10 \times 10^3) \]

\[ V_{DS} = 6 - 3.92 \]

\[ V_{DS} = 2.08 \text{V} \]

(iii) \( P_T \):

\[ P_T = I_D \times V_{DS} \]

\[ = (0.392 \times 10^{-3}) (2.08) \]

\[ P_T = 0.82 \text{mW} \]

X) Comparison of BJT and FET

<table>
<thead>
<tr>
<th>Parameter</th>
<th>BJT</th>
<th>FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control element</td>
<td>Current Controlled device</td>
<td>Voltage controlled dev</td>
</tr>
<tr>
<td>Input current</td>
<td>( I_e ) controls ( I_a )</td>
<td>Input Voltage ( V_{gs} ) controls current ( I_d )</td>
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Biase of Discrete BJT, JFET and MOSFET

- \( R_1 \) is replaced by resistor \( R_s \) in voltage divider circuit.
- Now \( R_s \) and \( R_2 \) are the two resistors of the potential divider circuit.
- Temperature increases, \( R_s \) increases which decreases the current flowing through it. Hence current through \( R_s \) decreases which reduces the voltage drop across it.
- \( V_B \) voltage reduces due to that \( V_{BE} \) which decreases \( I_B \). This decreases the \( I_C \).

Flow diagram: \( T \uparrow, R_s \uparrow, V_{RS} \uparrow, V_B \downarrow, V_{BE} \downarrow, I_B \downarrow, I_C \downarrow \)

1.11 Biasing BJT switching Circuits

The application of transistors is not limited solely to the amplification of signals. Through proper design it can be used as a switch for computer and control application.

1.11.1 Direct – Coupled Switching Circuit

When a transistor is used as a switch, it is either biased off to \( I_C = 0 \) or biased on to its maximum collector current level. Fig 1.32 illustrates the two conditions.

![Diagram of Direct coupled transistor switching circuit](image-url)
Note that the circuit 1.32 is termed as *direct-coupled switching circuit*, because the signal source is directly connected to the circuit.

**Condition 1: OFF-biased transistor**

In Fig 1.32(a) the negative polarity of the base input voltage ($V_s$) biases the transistor ($Q_i$) off. In this case, the only current flowing is the collector base leakage current ($I_{CBO}$) which is normally so small that it can be neglected.

The transistor collector-emitter voltage is

$$V_{CE} = V_{CC} - (I_C R_C)$$

With $Q_i$ off

$$V_{CE} = V_{CC}$$

**Condition 2: ON-biased transistor**

In Fig 1.32(b) $V_s$ is positive, and if biases $Q_i$ on to the maximum possible $I_C$ level. The collector current is limited only by the collector supply voltage ($V_{CC}$) and the collector resistor ($R_C$).

Therefore, $I_C R_C = V_{CC}$

$$V_{CE} = V_{CC} - I_C R_C = 0$$

**DC load line for a transistor switching circuit**

Now consider figure 1.33 which shows the output characteristics and dc load line for the switching circuit in Fig 1.32.

![DC load line for a transistor switching circuit](image)

Fig. 1.33 DC load line for a transistor switching circuit
The load line is drawn by the usual process of plotting point A at \( I_c = 0 \) and \( V_{ce} = V_{cc} \) and point B at \( V_{ce} = 0 \) and \( I_c = V_{cc}/R_c \).

From the graph, when on, the transistor is operating in the saturation region when off, it is in the cut off region.

The 1k\( \Omega \) load line shows that when \( I_B = 0 \), \( I_c \) is close to zero at \( I_c = I_{cbo} \).

At this point the transistor is cut off. The region of the characteristics below \( I_B = 0 \) is termed the cut-off region. When \( I_c \) is at its maximum level, the transistor is said to be saturated and the collector-emitter voltage is the saturation voltage \( V_{CE(sat)} \).

The region of the transistor characteristics at \( V_{CE(sat)} \) is termed the saturation region. The region between saturation and cut-off is the active region which is where a transistor is normally biased for amplification. From the load line, it is seen that \( V_{CE(sat)} \) is dependent on the \( I_c \) level.

For 2k\( \Omega \) load line shown dashed in Figure 1.33, \( V_{CE(sat)} \) is smaller than for \( R_C = 1k\Omega \).

From Fig 1.32(b) it is seen that \( I_B \) is a constant quantity

\[
I_B = \frac{V_R - V_{BE}}{R_B}
\]  
\[\hline\]

Also, the level of \( I_c \) depends upon \( I_B \)

\[ I_c = h_{FE} \times I_B \]

The collector current can be determined from equation

\[ I_c R_C = V_{cc} \]

and the base current can be calculated from equation

\[ I_B = \frac{V_R - V_{BE}}{R_B} \]

Then the minimum required current gain for the transistor is

\[ h_{FE}(1) = \frac{I_c}{I_B} \]  
\[\hline\]
$h_{FE}$:

- If the transistor $h_{FE}$ value is less than the calculated $h_{FE}(1)$ value, $I_C$ will be lower than the level required for transistor saturation.
- If the actual $h_{FE}$ value of the transistor is greater than the calculated $h_{FE}(1)$, $I_C$ tends to be greater than the current level required to saturate the transistor.
- However, $I_C$ cannot exceed $V_{CC}/R_C$.
- Consequently an $h_{FE}$ value larger than $h_{FE}(1)$ will adjust down to $h_{FE}(1)$. An $h_{FE}$ value lower than $h_{FE}(1)$ cannot adjust up. So, to ensure that the transistor in the switching circuit saturates, it must have an $h_{FE}$ value equal to or greater than the calculated $h_{FE}(1)$ for the circuit.

$V_{CE(sat)}$:

$V_{CE(sat)}$ is typically 0.2V for a low current silicon transistor, while $V_{BE}$ is typically 0.7V. Consider the circuit in Fig. 1.32(b); if $V_{BE} = 0.7V$ and $V_{CE(sat)} = 0.2V$ the transistor base is 0.5V more positive than the collector. This means that the collector base junction which is usually reverse biased, as forward biased when the transistor is in saturation.

With the collector-base junction forward biased, fewer charges carriers from the emitter and drawn across to the collector, and the device current gain is lower than normal.

### 1.11.2 Capacitor Coupled Switching Circuit

![Capacitor-coupled switching Circuit with the transistor biased on into saturation](image)

The fixed bias circuit in Fig. 1.34 is similar to circuits of that type that have already been considered, with exception that the transistor is biased into saturation.
Basing of Discrete BJT, JFET and MOSFET

The base bias current is quite satisfactory for switching circuits. The transistor in Fig 1.34 is in normally on state with \( V_{CE} = V_{CE(sat)} \).

The capacitor-coupled (pulse waveform) input turns the device off, giving \( V_{CE} = V_{CC} \).

The transistor base current is

\[
I_B = \frac{V_{CC} - V_{BE}}{R_B} 
\]

(1.54)

The collector current can be determined from equation \( I_C R_C = V_{CC} \) and then the minimum required \( h_{FE} \) value can be calculated from equation

\[
h_{FE(min)} = \frac{I_C}{I_B} 
\]

Another type of capacitor-coupled switching circuit is illustrated in Fig 1.35. In this case, resistor \( R_B \) keeps the transistor base emitter voltage at zero, to ensure that the device is in a normally off state. The capacitor-coupled input voltage biases the transistor on into saturation.

![Fig 1.35 Capacitor-coupled switching circuit with the transistor biased OFF.](image)

1.11.3 Switching Circuit Design

- The resistance of \( R_C \) for any one of the switching circuits discussed can be calculated by using the specified \( V_{CC} \) and \( I_C \) level with the equation
  \[
  I_C R_C = V_{CC}
  \]
- The transistor \( h_{FE(min)} \) value can used with \( I_C \) to determine the minimum \( I_B \) level required for transistor saturation.
Actual transistor current gain can be avoided by using an $h_{fe}$ value of 10.

The resistance $R_b$ for the direct coupled circuit in Fig 1.32 is calculated from the equation

$$I_B = \frac{V_S - V_{BE}}{R_b}$$

For capacitor coupled switching circuit shown in Fig 1.34(a) resistance $R_b$ is calculated using the equation

$$I_B = \frac{V_{CC} - V_{BE}}{R_b}$$

A different approach must be taken for calculating a suitable resistance for $R_b$ in the normally-off capacitor coupled circuit in Fig 1.35(b). The current that flows through $R_b$ when the transistor is off, and the allowable voltage drop across $R_b$ must be considered. The resistor current is the collector-base leakage current ($I_{cbo}$) and the maximum voltage drop produced by $I_{cbo}$ must be smaller than the normal transistor $V_{BE}$ level when the device is on.

- $I_{cbo}$ at maximum transistor temperature is unlikely to exceed 5 μA. So the maximum resistance value for $R_b$ is

$$R_b = \frac{0.1V}{5\mu A} = 20 k\Omega$$

Normally, as allowable $R_b$ value is 22kΩ or lower is suitable for keeping the transistor biased OFF.

**Example 1.15:**

Calculate the minimum $h_{fe}$ for the transistor in the circuit in Fig. 1.32 when $V_{CC} = 10 V$, $R_c = 1 k\Omega$, $R_b = 6.8 k\Omega$ and $V_s = 5V$. Also determine the transistor $V_{ce}$ level when $h_{fe} = 100$.

**Solution:**

$h_{fe(i)}$ Calculation

$$I_C = \frac{V_{CC}}{R_c} = \frac{10V}{1k\Omega}$$

$$I_C = 10 mA$$
Step 2:

Calculate \( g_m \)

\[
g_m = -\frac{2I_{DS}}{V_p} = -\frac{-2 \times 1.65}{-2} = 1.65 \text{ mS}
\]

\[
g_m = g mo \left[ 1 - \frac{V_{GS}}{V_p} \right]
\]

\[
= 1.65 \left( 1 - \frac{0.6074}{2} \right) \times 10^{-3}
\]

\[
= 1.65 \times 10^{-3} \times 0.6963
\]

\[
= 1.15 \text{ mS}
\]

Step 3:

Calculate \( R_S \)

\[
0 = V_{GS} + I_D R_S
\]

\[
R_S = -\frac{V_{GS}}{I_D} = -\left( \frac{0.6074}{0.8 \text{ mA}} \right)
\]

\[
= 759.25 \Omega
\]

1.16 BIASING FET SWITCHING CIRCUITS

1.16.1 JFET Switching

A field effect transistor in a switching circuit is manually in an off state with zero drain current or in an on state with a very small drain-source voltage \( V_{DS} \).

When FET is off, there is a drain-source leakage current so that it can almost always be neglected.

When FET is on, the drain-source voltage drop depends on the channel resistance \( r_{DS(on)} \) and the drain current \( I_D \).
Biasing of Discrete BJT, JFET and MOSFET

\[
V_{DS(on)} = I_D r_{DS(on)} \quad \text{(1.97)}
\]

FET is mainly designed for switching applications have very low channel resistances. For example, the 2N4856 has \( r_{DS(on)} = 25 \Omega \). With low \( I_D \) levels, \( V_{DS(on)} \) can be much smaller than the 0.2V typically \( V_{CE(sat)} \) for BJT. This is an important advantage of a FET switch over a BJT switch.

### 4.16.2 Direct Coupled JFET switching circuit

A direct coupled JFET switching circuit in Fig. 1.61(a) and a circuit waveforms are illustrated in Fig. 1.61(b).

**Fig. 1.61** Direct coupled JFET switching circuit, and the waveforms of the circuit input and output voltages.

**Case 1:** When \( V_i = 0 \), the FET gate and source voltages are equal, and there is no depletion region penetration into the channel.

The output voltage is now \( V_o = V_{DS(on)} \).

**Case 2:** When \( V_i \) exceeds the FET gate-source cutoff voltage, the device is switched off and the output voltage goes to \( V_{DD} \).

Assuming that \( V_{DS(on)} \) is very small, the drain current level is determined from the equation

\[
V_{DD} = I_D R_D \quad \text{(1.98)}
\]

Equation (1.98) can be used to determine \( R_D \) when \( V_{DD} \) and \( I_D \) are specified or to calculate \( I_D \) when \( R_D \) is known. The \( I_D \) level can then be employed to determine \( V_{DS(on)} \). The lowest drain current that can be used must be very much greater than the specified drain source leakage current for the device.
Case 3: To switch the FET off, $V_i$ should exceed the maximum gate-source cutoff voltage. However, $V_i$ must not be so large that the drain-gate voltage ($V_{DG} = V_{DD} + V_i$) approaches the breakdown voltage.

A rule-of-thumb is to select the off input voltage $1\text{V}$ larger than $V_{GS(\text{off})\text{(max)}}$

$$V_i = -(V_{GS(\text{off})\text{(max)}} + 1\text{V})$$

The gate resistor ($R_g$) in the circuit in Fig 1.61 is provided solely to limit any gate current in the event that the gate-source functions become forward biased. The circuit might operate satisfactorily with $R_g$ selected as $1\text{M} \Omega$, however, high value resistors can slow the switching speed of the circuit, so quite small resistance values are often used for $R_g$.

1.16.3 Capacitor-coupled JFET switching circuits

Fig 1.62 (a) and (b) shows the Normally-on circuit and Normally-off circuit of two capacitor-coupled JFET switching circuit.

The FET in Fig 1.62(a) is normally-on because it has $V_{GS} = 0$ and the device in the fig 1.62 (b) is normally-off with $V_{GS}$ greater than the pinch-off voltage. In both circuits, the FET is switched on or off by a capacitor-coupled input pulse.

1.16.4 MOSFET Switching

Fig 1.63 shows two capacitor-coupled MOSFET switching circuits. In Fig 1.63(a), the FET is biased off because $V_{GS} = 0$. A positive-going input signal is required to turn the device on. The FET in Fig 1.63(b) is biased on by the positive $V_{GS}$ provided by $R_1$ and $R_2$. In this case, a negative-going input voltage must be applied to turn the FET off. Equations 1.97 and 1.98 can be applied to these circuits to calculate $I_D$ and $V_{DS(\text{on})}$. 
Biased of Discrete BJT, JFET and MOSFET

Fig 1.63 MOSFET normally-on and normally-off capacitor-coupled switching circuits.

To set the device on to a desired level of drain current, the transfer characteristics can be employed for determining $V_{GS}$ if they are available.

To ensure that the FET is off, the gate-source voltage must be driven below the minimum voltage for the device.

Example 1.27

Design the JFET switching circuit in Fig 1.61 to have $V_{DS(on)}$ not greater than 200mV, a 2N4856 FET is to be used with a 12V supply.

Solution:

From specification $r_{DS(on)} = 25$V $V_{GS(off)} = 10V_{(max)}$

$$I_D = \frac{V_{DS(on)}}{r_{DS(on)}} = \frac{200mV}{25\Omega}$$

$$I_D = 8mA$$

$$R_D = \frac{V_{DD}}{I_D} = \frac{12V}{8mA} = 1.5k\Omega \text{ (Standard Value)}$$

$$V_i = -(V_{GS(off)_{(max)}} + 1V)$$

$$V_i = -11V$$
2. What is meant by transistor?
A: A transistor is a three terminal device: base, emitter and collector which can be operated under three modes of operation common base, common emitter and common collector.

3. Why are common emitter amplifiers more popular? Dec-11
A: (i) The CE configuration provides both voltage gain and current gain greater than unity. (ii) In a CE circuit, the ratio of output resistance to input resistance is small ranging from 100 to 1000.

4. Why biasing is necessary in BJT amplifiers? Dec-06, 07, 08, 09, 12
A: In order to operate the transistor in the desired region we have to apply external dc voltages of correct polarity. This is called biasing of the transistor.

5. Define biasing. May-13, Nov-15
A: It is the phenomenon of applying dc voltage of correct polarity to the transistor in order to operate in the desired region.

6. Define dc operating point. May-15, 16, Nov-14, 16
A: When a transistor is biased, certain current and voltage conditions are established for the transistor. These conditions are known as operating conditions or dc operating point or quiescent (q) point.

7. What is the use of stability factor?
A: Stability factor indicates the degree of change in operating point due to variation in $V_{BE}$ and $I_C$.

8. What is the function of $Q$-point? Dec-13
A: The function of $Q$-point is to establish certain dc current and voltage conditions to operate transistor in a particular operating region at zero signal level.
8. Define all the three stability factors. 

A. Stability factor $s$ is defined as the rate of change of collector current to the change in reverse saturation current with $V_{BE}$ and $\beta$ as constant.

$$s = \frac{\Delta I_C}{\Delta I_{CO}} \quad V_{BE} \& \beta \text{ constant}$$

B. Stability factor $s'$ is defined as the rate of change of collector current to change in the base-emitter voltage with $I_{CO} \& \beta$ as constant.

$$s' = \frac{\Delta I_C}{\Delta V_{BE}} \quad I_{CO} \& \beta \text{ as constant}$$

C. Stability factor $s''$ is defined as the rate of change of collector current to the change in gain when $I_{CO} \& V_{BE}$ are constant.

$$s'' = \frac{\Delta I_C}{\Delta \beta} \quad I_{CO} \& V_{BE} \text{ as constant}$$

9. Mention the methods of biasing of BJT. Dec-07-01, 11

A. Fixed bias
   i. Collector to base bias (con base with feedback bias)
   ii. Voltage divider (self bias / emitter bias)

10. Draw a fixed bias circuit. Vcc: May-06-04

The line drawn between the points $A$ and $B$ is called the dc load line. Dc indicates that only dc conditions are considered. It shows the relationship between $I_C$ and $V_{CC}$. Dec-02.
why do you put the point at the middle of the dc load line?  
the point should always be stable. a shift with temperature

what is meant by stabilization techniques?  
Stabilization techniques refer to the use of temperature sensitive devices such as diodes, transistors, thermistors, etc. which provides compensating voltages and currents to maintain the point stable.

what is meant by stabilization?  
Stabilization techniques refer to the use of resistive biasing circuits which allow $I_B$ to vary so as to keep $I_C$ relatively constant with variations in $I_{co}, \beta$, and $V_{BE}$.

differentiable bias stabilization and compensation techniques, 

why fixed bias circuit is not used in practice?  
the stability $s = 1 + \beta$ for a fixed bias is very less and $s$ is of larger quantity. so, it is not used in amplifying circuits.

rewritten for the stability factor $s$ for a fixed bias circuit 

$\frac{I_C}{I_{co}} = \beta I_B + (\beta+1)I_{co}$

differentiated wrt $I_C$,

$1 = \beta \frac{\partial I_B}{\partial I_C} + (\beta+1) \frac{\partial I_{co}}{\partial I_C}$

$1 = \beta \frac{\partial I_B}{\partial I_C} + (\beta+1) \frac{\partial I_{co}}{\partial I_C}$

$s = \frac{\partial I_C}{\partial I_{co}} = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$

hence, $I_B = \frac{V_{ec} - V_{BE}}{R_B}$

$\frac{\partial I_B}{\partial I_{co}} = 0 \quad \Rightarrow \quad s = 1 + \beta \quad \Rightarrow \quad s = 1 + \beta$
18. Draw the single stage self-biased circuit using Pnp transistor. [Figure]

19. How can collector current be stabilized with Ico variations? Dec-10
   a. The rate of change of Ico with temperature in case of Germanium is greater than that of Silicon transistor. \( \frac{\partial I_c}{\partial T} \) is important to stabilize. \( \frac{\partial I_c}{\partial T} > 0 \) since the diode is connected in reverse bias condition in this compensation, leakage current Ic flows through it. When temperature increases, Ic increases. As a result, Ic also increases, thereby increasing the collector current Ic.

20. What is bias compensation using thermalistor? Dec-10
   a. This method involves a temperature sensitive resistive element, the thermalistor, rather than diodes or transistors. It has a negative temperature coefficient, its resistance decreases exponentially with increasing temperature.

21. Why is bias compensation required? Dec-12
   a. Collector to bias and self-bias use negative feedback which reduces the amplification of the signal. So to make the operating point stable, compensation techniques are needed.

22. What is thermal runaway? Dec-08, 06, 17
    a. When temperature increases, the collector current increases, the voltage across CB junction increases to excess heat is produced at CB junction which destroy or burn the transistor. This is called thermal runaway.
18. What is the condition for thermal stability? Dec-07

The rate at which the heat released at collector junction must not exceed the rate at which the heat can be dissipated.

\[ \frac{\partial P}{\partial t} < \frac{\partial Q}{\partial t} \]

The condition for thermal stability is \( V_{CE} < \frac{V_{CC}}{2} \).


- FET has positive temperature coefficient of resistivity.
- As temperature increases, its drain resistance increases, reducing the drain current. Thus, thermal runaway does not exist in FET unlike BJT.

5. List the different types of FET biasing circuits: May-12, 16

(i) Fixed Bias
(ii) Voltage divider bias
(iii) Self Bias

6. What are the requirements for biasing circuits? May-12, 16

(i) The point must be taken at the middle of the line or active.
(ii) The point should be made independent of transistor parameters.
(iii) Emitter diode should be forward biased and the collector diode must be reverse biased.
(iv) The collector current should be stabilized against the temperature variations.

7. What are the basic relationships of a BJT amplifier?

\[ V_{BE} = 0.7V \]
\[ I_c = \beta I_B \]
\[ I_e = (\beta + 1) I_B \]

Why FET is known as voltage variable resistor? Dec-08.

In the region before pinch off, where \( V_{OS} \) is small, the drain to source resistance \( R_d \) can be controlled by bias voltage \( V_{GS} \). Therefore, FET is known as voltage variable resistor.
39. Name the two techniques involved in the stability of a point-
A: (i) Stabilization techniques
(ii) Compensation techniques

30. What is thermal stability? Dec-13
A: The maximum power dissipation depends upon the concentration of the transistor. The power varies from 1mW to 200W. The CB junction dissipates more amount of power because of two reasons: i. Increase in ambient/room temperature ii. Self-heating. This compensation is called thermal stability.

31. What are the factors against which an amplifier needs to be stabilized? Dec-14
A: (i) Reverse saturation current - Ic0
(ii) Gain - \( \beta \)
(iii) Emitter to base voltage - VBE

2. Determine the value of \( R_B \) and \( R_C \) for a collector to base bias circuit with \( V_{CC} = 15V, \ V_{CE} = 5V, \ I_C = 5mA \) and \( \beta = 100 \). Dec-09.

\[ I_B = \frac{I_C}{\beta} = \frac{5 \times 10^{-3}}{100} = 50 \mu A \]

Output side:
\[ I_C = \frac{V_{CC} - V_{BE} - I_B R_C}{R_C} = \]

\[ R_C = \frac{V_{CC} - V_{CE}}{I_B + I_C} = \frac{15 - 5}{50 \mu A + 5mA} \]
\[ R_C = 1.98 K\Omega \]

Input side:
\[ I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C} \]
\[ R_B = \frac{V_{CC} - V_{BE} - I_C R_C - I_B R_C}{I_B} \]
\[ = 15 - 0.07 - (5 \times 10^{-3} \times 1.98 \times 10^3) - (50 \times 10^{-6} \times 1.98 \times 10^3) \]
\[ = 8.6 - 0.2 K\Omega \]
3. Find the collector and base current of the circuit given in Fig.

$h_f = 80, \ V_{BE \text{on}} = 0.7 \ V$.

![Circuit diagram]

At is a fixed bias circuit.

From input side: $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$= \frac{5 - 0.7}{10k}$

$I_B = 0.43 \ mA$

$I_C = \beta I_B$

$= 80 \times 0.43 \times 10^{-3}$

$= 34.4 \ mA$

What is the impact of temperature on drain current of MOSFET? Dec-16

When temperature increases in MOSFET, the drain resistance increases, thereby decreasing the drain current.

Draw a DC load line of the circuit shown in Figure. May-15

$\Rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_C}$

(a) When $V_{CE} = V_{CC}$, $I_C = 0 \Rightarrow \text{Point A is obtained}$
(b) When \( V_{CE} = 0 \), \( I_C = \frac{V_{CC}}{R_C} = \frac{10}{18 \times 10^3} \)

\[ I_C = 0.555 \text{mA} \]

It is a fixed bias circuit

From Input side, \( I_B = \frac{V_{CC} - V_{BE}}{R_B} \)

\[ = \frac{5 - 0.7}{20k} \]

\[ I_B = 0.215 \text{mA} \]

\[ I_C = \beta I_B \]

\[ = 100 \times 0.215 \times 10^3 \]

\[ I_C = 21.5 \text{mA} \]

What are the operating regions of N-channel MOSFET and how do you find the operating region? **Inc-14**

N-channel MOSFET operates in the saturation region. Operating point should always be at the centre of the dc load line of saturation region.
What do you mean by punch through? May-14

Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. Punch through causes a rapidly increasing current with drain-source voltage increase. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of devices.

1. Calculate the value of $R_s$ required to self-bias an N-channel JFET with $I_{DS} = 40mA$, $V_p = -10V$ and $V_{GS} = -5V$. May-10

For a self-bias circuit,

$$I_D = I_{DS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$$

$$= 40 \times 10^{-3} \left( 1 - \left( \frac{-5}{-10} \right) \right)^2$$

$$I_D = 0.01A$$

$V_{GS} = -I_D R_s$

$$R_s = \frac{-V_{GS}}{I_D} = \frac{-(-5)}{0.01} = 500 \Omega$$

$$R_s = 0.5 \Omega$$
UNIT - II

BJT AMPLIFIERS

Small Signal Hybrid π Equivalent Circuit of BJT

To develop a small signal equivalent circuit of the transistor, we can treat the bipolar transistor as a two port network as shown in Fig. 1. BJT as a two port network.

Now consider the base current versus base-emitter voltage characteristic with small time-varying signals superimposed at the Q-point. Since the sinusoidal signal is small, we can treat the slope at the Q-point as a constant, which has units of conductance. The inverse of this conductance is the small-signal resistance defined as $r_x$.

Now we can relate the small signal input base current to the small signal input voltage by:

$$v_{be} = i_b r_x \quad \text{(1)}$$

From equation (1) we can write:

$$\frac{1}{r_x} = \frac{i_b}{v_{be}}$$

From the characteristic curve, from the characteristic curve, we can write:

$$\frac{1}{r_x} = \left| \frac{d i_b}{d v_{be}} \right|_{Q-point} \quad \text{eqn (2)}$$

In the CE configuration, the B-E junction is forward biased therefore we expect the current through this junction to be an exponential function of B-E voltage.
we can write current at the emitter terminal as 
\[ i_E = I_{EO} \left( e^{\frac{V_{BE}}{V_T}} - 1 \right) \approx I_{EO} e^{\frac{V_{BE}}{V_T}} \quad \ldots \, 3 \]

Similarly collector current can be written using the relation
\[ \alpha = \frac{i_C}{i_E} \Rightarrow i_E = \frac{i_C}{\alpha} \]

Now substitute \( i_E \) in equ \( 3 \)
\[ \frac{i_C}{\alpha} = I_{EO} \left( e^{\frac{V_{BE}}{V_T}} - 1 \right) \Rightarrow i_C = \alpha I_{EO} \left( e^{\frac{V_{BE}}{V_T}} - 1 \right) \]

Let us assign \( \alpha I_{EO} = I_S \)
\[ i_C = I_S \left( e^{\frac{V_{BE}}{V_T}} - 1 \right) \approx I_S \left( e^{\frac{V_{BE}}{V_T}} \right) \quad \ldots \, 4 \]

To find \( i_B \) consider the relation 
\[ \beta = \frac{i_C}{i_B} \Rightarrow i_B = \frac{i_C}{\beta} \quad \ldots \, 5 \]

The base current can be written as
\[ i_B = I_{BO} e^{\frac{V_{BE}}{V_T}} \]

Now substitute equ \( 4 \) in \( 5 \) we get
\[ i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{\frac{V_{BE}}{V_T}} \quad \ldots \, 6 \]

Substitute equ \( 6 \) in equ \( 2 \) and differentiate it w.r.t \( V_B \)
\[ \Rightarrow \frac{1}{r_X} = \frac{\partial}{\partial V_B} \left[ \frac{I_S}{\beta} e^{\frac{V_{BE}}{V_T}} \right] \bigg|_{V_B = 0} = \frac{1}{V_T} \left[ \frac{I_S}{\beta} e^{\frac{V_{BE}}{V_T}} \right] \bigg|_{V_B = 0} \]

\[ \frac{1}{r_X} = \frac{I_{BO}}{V_T} \quad \text{(using equation} \, 6) \]

we can write above relation as
\[ r_X = \frac{V_{BE}}{i_B} = \frac{V_T}{I_{BO}} = \frac{\beta V_T}{I_{CBO}} \quad \ldots \, 7 \]

The resistance \( r_X \) is called the diffusion resistance or base-emitter input resistance and it is a function of
- Q-point parameters.

Now we consider the output terminal characteristics of the bipolar transistor. Here output collector current is independent of the collector-emitter voltage, then the collector current is a function only of the base-emitter voltage. Therefore we can write

\[
\frac{\Delta I_C}{\Delta V_{BE}} = \frac{\partial I_C}{\partial V_{BE}} \bigg|_{Q\text{-point}} \Rightarrow \Delta I_C = \frac{\partial I_C}{\partial V_{BE}} \bigg|_{Q\text{-point}} \cdot \Delta V_{BE} \quad (8)
\]

(8a) \[ i_C = \frac{\partial I_C}{\partial V_{BE}} \bigg|_{Q\text{-point}} \cdot V_{BE} \quad (9) \]

Substitute equ. (4) in equ. (9)

\[
\frac{i_C}{v_{BE}} = \frac{\partial I_C}{\partial V_{BE}} \bigg|_{Q\text{-point}} \cdot \frac{1}{v_{BE}} = \frac{\beta}{v_{BE}} \left[I_s \exp \left(\frac{V_{BE}}{V_T}\right)\right] \bigg|_{Q\text{-point}} \quad (10)
\]

\[
\frac{i_C}{v_{BE}} = \frac{I_s}{v_T} \exp \left(\frac{V_{BE}}{v_T}\right) \bigg|_{Q\text{-point}} = \frac{I_{CA}}{v_T} \quad (11)
\]

\[
i_C = \frac{I_{CA}}{v_T} \cdot v_{BE} = g_m v_{BE} \quad (11)\]

where \( g_m = \frac{I_{CA}}{v_T} \) The term \( \frac{I_{CA}}{v_T} \) is a conductance since this conductance relates a current in the collector to a voltage in the B-E circuit, the parameter is called transconductance. It is also a function of Q-point parameter.

Using these new parameters we can develop a simplified small signal hybrid-\( \Pi \) equivalent circuit for the
npn transistor as shown below.

Fig. 2.7 as a small signal two-port network.

Similarly, we can draw the simplified small signal hybrid $\alpha$-equivalent circuit of npn transistor using above selection as

$$i_c = \beta i_b$$  (13)
Common Emitter Current Gain:

The common emitter current gain $\beta$ as beta does not include dc leakage currents, whereas dc beta includes the leakage current. However, we will assume in our analysis the leakage current are negligible therefore.

$$\beta_{dc} = \beta_{ac} \quad \text{[when leakage current is "0"]}$$

The small signal hybrid $\pi$ parameters $r_x$ and $g_m$ are multiplied we get current gain as:

$$r_x g_m = \left( \frac{\beta V_T}{I_C} \right) \left( \frac{V_C}{V_T} \right) = \beta$$

Small Signal Voltage Gain:

When incorporating the small signal hybrid $\pi$ model of the transistor into the ac equivalent circuit, it is generally helpful to start with the three terminals of the transistor as shown below:

![Diagram of transistor](image)

The small signal voltage gain, $A_v = \frac{V_o}{V_s}$ of the circuit is defined as the ratio of output signal voltage to input signal voltage. The conventional phasor notation for the small signal base to emitter voltage is $V_{be}$ it is called the Control Voltage.
The output voltage can be written as

\[ V_o = V_{ce} = -I_c R_c \quad \text{(1)} \]

\[ V_o = -g_m V_i R_c \quad \text{(2)} \]

From the input position of the circuit, we can write

\[ V_i = \frac{V_x}{R_x + R_B} \]

The small signal voltage gain can be obtained by substituting eqn (1) in eqn (2) we get

\[ V_o = -g_m \frac{V_x}{R_x + R_B} \]

\[ A_v = \frac{V_o}{V_i} = -g_m R_c \frac{V_x}{R_x + R_B} \quad \text{(3)} \]

Hybrid \( \pi \) Equivalent Circuit Including the Early Effect:

So far in the small signal equivalent circuit, we have assumed that the collector current is independent of the collector - emitter voltage. Since an in early effect the collector currents will vary with collector - emitter voltage. The relationship between \( I_c \) with \( V_{ce} \) can be written as

\[ I_c = I_s \left( e^{\frac{V_{ce}}{V_A}} - 1 \right) \quad \text{(4)} \]

where \( V_A \) is the Early voltage and it is a positive number.

The output resistance \( R_o \) is defined as
\[ V_o = \frac{\Delta V_{ce}}{\Delta I_C} \text{ Q-point} \]  

\[ \frac{1}{V_o} = \frac{dI_C}{dV_{ce}} \text{ Q-point} \]
Now substitute \( I_C \) and differentiate it with respect to \( V_{ce} \) we get:

\[ \frac{1}{V_o} = \frac{d}{dV_{ce}} \left[ I_s \left( e^{(V_{be}/V_t)} \right) \left( 1 + \frac{V_{ce}}{V_A} \right) \right] \text{ Q-point} \]

Differentiating the above equation we get:

\[ \frac{1}{V_o} = I_s e^{(V_{be}/V_t)} \frac{d}{dV_{ce}} \left[ \left( 1 + \frac{V_{ce}}{V_A} \right) \right] = I_s e^{(V_{be}/V_t)} \frac{1}{V_A} \]

\[ \frac{1}{V_o} \geq \frac{I_{ce}}{V_A} \Rightarrow \]

\[ V_o = \frac{V_A}{I_{ce}} \]  

where \( V_o \) is called the small signal transistor output resistance. This resistance can be thought of as an equivalent Norton resistance, which means that \( V_o \) is in parallel with the dependent current source.

The hybrid \( T \) equivalent circuit of a CE amplifier can be drawn as:

The small signal model of the BJT including output resistance due to Early effect.
Combining the hybrid-\( \pi \) model of a transistor with the ac equivalent circuit, we obtain the small signal equivalent circuit shown below, then the output voltage is given by:

\[
V_o = -(g_m V_x) (\frac{R_{o1} R_c}{R_B + r_x})
\]

Similarly, the control voltage \( V_x \) can be expressed in terms of the input signal voltage \( V_i \) using voltage divider equation as:

\[
V_x = V_i \left[ \frac{r_x}{R_B + r_x} \right]
\]

Combining the equation (5) and (6) we obtain the small signal voltage gain:

\[
A_v = \frac{V_o}{V_i} = \frac{-g_m V_x (\frac{R_{o1} R_c}{R_B + r_x})}{R_B + r_x}
\]

We get \( g_m r_x = \beta \), therefore equation (7) becomes

\[
A_v = \frac{-\beta (\frac{R_{o1} R_c}{R_B + r_x})}{R_B + r_x}
\]

The voltage gain contains a negative sign indicating a 180-degree phase shift between the input and output signal.

**Small Signal Analysis of Common Emitter Amplifier:**

The basic common-emitter circuit with voltage divider biasing and its small signal equivalent circuit is given in the next page.

The signal from source is coupled into the base.
q) the transistor through the coupling capacitors Cc.

\[ V_{cc} \]

\[ R_s \]

\[ R_1 \]

\[ R_c \]

\[ V_n \]

\[ V_0 \]

\[ I_b \]

\[ R_i \]

\[ R_i \]

\[ R_{l1}R_{l2} \]

\[ V_{R} \]

\[ V_{R} \]

\[ V_{o} \]

\[ V_{o} \]

\[ V_{s} \]

\[ V_{c} \]

\[ V_{c} \]

\[ I_c \]

\[ C_c \]

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Now substitute eqn (2) in (1) to find voltage gain.

\[ V_o = -g_m \left( \frac{R_1 R_2 R_3 R_4}{R_1 R_2 R_3 R_4 + R_s} \right) V_s \cdot (R_0 H R_6) \]

\[ A_v = \frac{V_o}{V_s} = -g_m (R_0 H R_6) \left[ \frac{R_1 R_2 R_3 R_4}{R_1 R_2 R_3 R_4 + R_s} \right] \]  \hspace{1cm} (3)

From the small signal equivalent circuit we can also calculate \( R_i \) which is the resistance to the amplifier.

\[ i.e \quad R_i = R_1 R_2 R_3 R_4 \]  \hspace{1cm} (4)

The output resistance \( R_o \) is found by setting the independent source \( V_s \) equal to zero. In this case, there is no excitation to the input portion of the circuit so \( V_{ix} = 0 \), which implies that \( g_m V_s \).

Then the output resistance looking back into the output terminals

\[ R_o = R_0 H R_6 \]  \hspace{1cm} (5)

The input resistance to the amplifier is not very much greater than the signal source resistance, the actual input vol to the amplifier is reduced due to signal voltage. This is called “loading effect.”

The loading effect can be minimized by making \( R_i >> R_s \) which means \( V_{ix} \approx V_s \), \( V_{ix} \approx V_s \).

Small Signal Analysis of CE Amplifier with emitter resistor:

We know that Q-point was stabilized again.

Variations in \( \beta \) if an emitter resistor were included in the circuit as shown in next page. we will find a
Similar property for the ac signals, in which the voltage gain of a circuit with \( R_E \) will be less dependent on the transistor current gain \( 
abla \). \( R_i : R_{ib} \)

\[ \frac{R_i}{R_{ib}} \]

In the small signal equivalent circuit we are assuming that the early voltage is infinite so the transistor output resistance \( V_o \) can be neglected. The ac output voltage is

\[ V_o = -(\beta I_b) R_C \quad \text{--- 1} \]

From the small signal equivalent circuit we can consider the \( V_{in} \) as sum of voltage across \( R_C \) and \( R_E \) that is

\[ V_{in} = I_b R_C + (\beta + 1) I_b R_E \]

\[ V_{in} = I_b [R_C + (1 + \beta) R_E] \]

\[ R_{ib} = \frac{V_{in}}{I_b} = R_C + (1 + \beta) R_E \quad \text{--- 2} \]

where as \( R_{ib} \) is input resistance, to the amplifier, input resistance \( R_i \) can be written as

\[ R_i = R_{ib} \frac{R_1 R_2}{R_1 + R_2} \quad \text{--- 3} \]

In common emitter configuration that includes an emitter resistance, the small signal input resistance, looking into
the base of the transistor is \( V_x \) plus the emitter resistance multiplied by the factor \((1+\beta)\) as shown in eqn(3). This effect is called resistance addition rule.

Apply voltage divider rule to the small signal equivalent circuit we can write

\[
V_{\text{in}} = \left[ \frac{R_i}{R_i+R_s} \right] V_s \quad \cdots (4)
\]

Now divide eqn (4) by equation (1) we get voltage gain

\[
A_V = \frac{V_o}{V_{\text{in}}} = \frac{-R_s R_b}{V_s} \quad \cdots (5)
\]

The small signal voltage gain can be obtained as

\[
A_V = \frac{V_o}{V_s} = \frac{-R_s R_b}{V_s} \quad \cdots (5)
\]

Using ohms law we can write \( I_b = \frac{V_{\text{in}}}{R_{ib}} \) the result equation (5) become

\[
A_V = -\frac{R_s R_b}{V_s} \cdot \frac{V_{\text{in}}}{R_{ib}} \quad \cdots (6)
\]

Now substitute equ (5) and (4) in equ (6) we get

\[
A_V = -\frac{R_s R_b}{V_s} \cdot \left[ \frac{R_i}{R_i+R_s} \right] V_s \cdot \frac{1}{V_x + (1+\beta) R_E}
\]

\[
A_V = -\frac{R_s R_b}{V_s} \cdot \frac{R_i}{R_i+R_s} \quad \cdots (7)
\]

In the above equation if \( R_i \gg R_s \) and \((1+\beta)R_E \gg R_x\), then the small signal voltage gain is approximately

\[
A_V = -\frac{R_s}{R_E} \quad \cdots (8)
\]
The previous equation shows that the voltage gain is less dependent on the current gain $h_{fe}$, which means that there is a smaller change in voltage gain when the transistor's current gain changes, but this advantage is at the expense of a smaller gain.

**Small signal equivalent circuit of CE amplifier with Bypass Capacitor:**

When the emitter resistor $R_e$ must be large for the purpose of dc design, but degrades the small signal voltage gain too severely, we can use an emitter bypass capacitor to effectively short out a position of all the emitter resistance as seen by the ac signal.

Consider the circuit diagram shown in Fig. 2, biased with positive and negative voltages. Both emitter resistors $R_{e1}$ and $R_{e2}$ are factors in the dc design of the circuit, but only $R_{e1}$ is part of the ac equivalent circuit, since $C_e$ provides a short circuit to ground for ac signal, whereas here ac gain stability is due only to $R_{e1}$ and most of the dc stability is due to $R_{e2}$.

**Ac load line:**

A dc load line shows the relationship between the $Q$-point and the transistor characteristic, when capacitors are included in a transistor circuit. A new effective load line called an ac load line exist. It gives the relationship between the small signal response and the...
Transistor characteristics.

(a) DC Amplifier Circuit.

From \( V_{CC} \) (a) the collector circuit resistance seen by the d.c. bias current \( I_{C0} \) is \( R_{dc} = R_c + R_L \) from \( V_{CC} \) (b) the collector resistance \( R_{ac} = R_c + R_L \) since \( R_{ac} \neq R_{dc} \), the concept of ac load line arises.

Apply KVL to the collector circuit of ac equivalent circuit.

\[
V_{CC} = I_{C0} R_{ac} \quad \text{--- (1)}
\]

where \( V_{CC} \) = a.c. collector to emitter voltage,

\( I_{C0} \) = a.c. collector current.

Since \( I_c = I_{C0} - I_{C0} \) and \( V_{CC} = V_{CE0} - V_{CE} \)

Substitute in equ (1) we get:

\[
V_{CE0} - V_{CE} = (I_c - I_{C0}) R_{ac} \quad \text{--- (2)}
\]

\[
= I_{C0} R_{ac} - I_{C0} R_{ac}
\]

\[
I_c = \frac{V_{CE0} - V_{CE} + I_{C0}}{R_{ac}} \quad \text{--- (3)}
\]

Let us find the points at which the a.c. load line intersects the axes of the output characteristics of the common emitter amplifier.

Assign \( I_c = 0 \) in equ (2) we get:

\[
V_{CE}(\text{max}) = V_{CE0} + I_{C0} R_{ac} \quad \text{--- (4)}
\]

Assign \( V_{CE} = 0 \) we get:

\[
I_{C0}(\text{max}) = \frac{V_{CE0} + I_{C0}}{R_{ac}} \quad \text{--- (5)}
\]
Small Signal Analysis of Common Collector Amplifier: [Emitter Follower]

The dc analysis of the circuit is exactly the same as we have already seen, so we will concentrate on the small signal analysis. The hybrid π model of the bipolar transistor can also be used in the small signal analysis of this circuit. Assuming the coupling capacitor $C_{c}$ act as a short circuit. The below fig shows the small signal equivalent circuit.

**Fig.** Output Signal is at the emitter terminal with ground.

**Fig.** Small signal equivalent circuit of the emitter follower.

**Fig.** Small signal equivalent circuit of the emitter follower with all signal grounds connected together.

The Collector terminal is at the signal ground and the transistor output resistance $r_o$ is in parallel with the dependent current source. From this circuit we can write:

$$I_o = I_E$$  \(\text{[1]}\)

where as we know that $I_E$ in terms of $I_b$ as

$$I_E = (1 + \beta)I_b$$  \(\text{[2]}\)
Substitute equation 2 in 1 we get:

\[ I_0 = (1+\beta) I_b \]  \[ \text{(3)} \]

The output voltage can be written as:

\[ V_o = I_o (r_{\text{oll}} R_e) \]  \[ \text{(4)} \]

Now substitute eqn 3 in 2 we get output voltage as:

\[ V_o = (1+\beta) I_b (r_{\text{oll}} R_e) \]  \[ \text{(5)} \]

Applying KVL equation around the base-emitter loop then:

\[ V_{\text{in}} = V_x + V_o \]  \[ \text{(6)} \]

where \[ V_x = I_b r_x \]

Now substitute \[ V_x \] and \[ V_o \] in eqn 6 we get:

\[ V_{\text{in}} = I_b r_x + (1+\beta) I_b (r_{\text{oll}} R_e) \]

\[ V_{\text{in}} = I_b \left[ r_x + (1+\beta) (r_{\text{oll}} R_e) \right] \]

\[ R_{ib} = \frac{V_{\text{in}}}{I_b} = r_x + (1+\beta) (r_{\text{oll}} R_e) \]  \[ \text{(7)} \]

Where \[ R_{ib} \] is input resistance to the base terminal.

Apply voltage divider rule at the input to we get:

\[ V_{\text{in}} = \left[ \frac{R_i}{R_i + R_s} \right] V_s \]  \[ \text{(8)} \]

Substitute \[ V_{\text{in}} \] in eqn 8 we get:

\[ I_b \left[ r_x + (1+\beta) (r_{\text{oll}} R_e) \right] = \left[ \frac{R_i}{R_i + R_s} \right] V_s \]

\[ I_b = \left[ \frac{R_i}{R_i + R_s} \right] V_s \left[ r_x + (1+\beta) (r_{\text{oll}} R_e) \right] \]  \[ \text{(9)} \]

Substitute \[ I_b \] in eqn 6 we get:
\[ V_o = \frac{(1+\beta) (\alpha R_e)}{\left[ \alpha + (1+\beta) (\alpha R_e) \right]} \left[ \frac{R_i}{R_i + R_s} \right] \]

\[ A_v = \frac{V_o}{V_s} = \frac{(1+\beta) (\alpha R_e)}{\left[ \alpha + (1+\beta) (\alpha R_e) \right]} \left[ \frac{R_i}{R_i + R_s} \right] \]

**Input Resistance:**

The input resistance looking into the base is denoted \( R_{ib} \) and is indicated in the small signal equivalent circuit shown in Fig. We already derived the equation for input resistance \( R_i \) consider eq. (7)

\[ R_{ib} = \frac{\alpha}{\alpha + (1+\beta)} (\alpha R_e) \]

Since the emitter current is \((1+\beta)\) times the base current, the effective impedance in the emitter is multiplied by \((1+\beta)\). This multiplication by \((1+\beta)\) is called resistance degradation rule.

**Output Resistance:**

To find the output resistance of emitter follower circuit, we will assume that the input signal source is ideal and that \( R_s = 0 \). The small signal equivalent circuit can be redrawn as given in next page. The circuit is derived from the small signal equivalent circuit by setting the independent voltage source \( V_e \) equal to zero, which means that \( V_e \) acts as a short circuit.

A base voltage \( V_b \) is applied to the output terminal and the resulting base current is \( I_b \). Therefore, output resistance \( R_o \) is given by
Fig. (Small signal equivalent circuit of emitter follower used to determine the output resistance.)

\[ R_o = \frac{V_x}{I_x} \quad \text{(1)} \]

The control voltage \( V_x \) is not zero, but is a function of applied base voltage, therefore \( V_x = -V_{xb} \) summing the currents at the output node we can write

\[ I_x = \frac{V_x}{R_E} + \frac{V_x}{r_o} + g_m V_{xb} + \frac{V_x}{r_c} \quad \text{(2)} \]

Substituting \( V_{xb} = -V_x \) in eqn (2) we get

\[ I_x = V_x \left[ g_m + \left( \frac{1}{R_E} + \frac{1}{r_o} + \frac{1}{r_c} \right) \right] \]

\[ \frac{R_{ox}}{R_o} = \frac{I_x}{V_x} = g_m + \left( \frac{1}{R_E} + \frac{1}{r_o} + \frac{1}{r_c} \right) \]

\[ R_o = \frac{1}{g_m + \left( \frac{1}{R_E} + \frac{1}{r_o} + \frac{1}{r_c} \right)} \]

The output resistance can be written in terms of \( B \) as

\[ \frac{1}{R_o} = g_m + \frac{1}{r_c} + \left( \frac{1}{R_E} + \frac{1}{r_o} \right) \]

\[ = \left( \frac{g_m V_x + 1}{r_c} \right) + \left( \frac{1}{R_E} + \frac{1}{r_o} \right) \]

\[ = \left( \frac{1 + B}{r_c} \right) + \left( \frac{1}{R_E} + \frac{1}{r_o} \right) \]

\[ R_o = \left( \frac{V_x}{\frac{1 + B}{r_c}} \right) \frac{1}{11 R_E R_0} \]

\[ \text{\textbullet\textbullet\textbullet\textbullet\textbullet} \]

\[ \text{\textbullet\textbullet\textbullet\textbullet\textbullet} \]
The output resistance looking back into the output terminals is the effective resistance in the emitter, $R_\text{E} || R_\text{o}$ in parallel with the resistance looking back into the emitter. It is the total resistance in the base circuit divided by $(1+\beta)$. This is an important result and is called the inverse resistanceagation rule.

Current gain:

From the small signal emitter follower equivalent circuit, the small signal current gain is defined as

$$ A_I = \frac{I_e}{I_i} \quad (5) $$

Using the current divida equation we can relate the base current to the input current as follows,

$$ I_b = \left[ \frac{R_1 || R_2}{R_1 || R_2 + R_\text{ib}} \right] I_i \quad (6) $$

Since we know that $I_0 = (1+\beta) I_b$, now substitute $I_b$ in $I_0$, we get,

$$ I_0 = (1+\beta) \left[ \frac{R_1 || R_2}{R_1 || R_2 + R_\text{ib}} \right] I_i \quad (7) $$

We can write the load current $I_e$ in terms of $I_0$ as

$$ I_e = \left[ \frac{R_0}{R_0 + R_E} \right] I_0 \quad (8) $$

Substitute equation (7) in (8) we get,

$$ I_e = \left[ \frac{R_0}{R_0 + R_E} \right] (1+\beta) \left[ \frac{R_1 || R_2}{R_1 || R_2 + R_\text{ib}} \right] I_i $$

Therefore,

$$ A_I = \frac{I_e}{I_i} = (1+\beta) \left[ \frac{R_0}{R_0 + R_E} \right] \left[ \frac{R_1 || R_2}{R_1 || R_2 + R_\text{ib}} \right] \quad (9) $$
If we assume that \( R_1R_2 \gg R_{ib} \) and \( V_o \gg V_E \) then

\[ A_2 \approx (1 + \beta) \quad \cdots \quad (2) \]

Although the small-signal voltage gain of the emitter follower is slightly less than 1, the small-signal current gain is normally greater than 1. Therefore, the emitter follower circuit produces a small signal power gain.

**Small Signal Analysis of Common Base Amplifier**

The basic common-base circuit in which the base at signal ground and the input signal is applied to the emitter. Assume a load is connected to the output through a coupling capacitor \( C_{cs} \).

![Diagram of the common base circuit](image)

The above circuit shows the small signal equivalent circuit of the common base circuit including the hybrid \( 
\begin{array}{c}
\text{p} \\
\text{g}
\end{array}
\) model of the transistor with the output resistance \( R_o \).

To be infinite.

From the small signal equivalent circuit, the output voltage is given by

\[ V_o = I_o \left( R_c || R_L \right) \quad \cdots \quad (3) \]

where as \( I_o = -g m V \)

\[ V_o = -g m V \left( R_c || R_L \right) \quad \cdots \quad (4) \]
Apply kcl to the emitter node we get

\[ \frac{V_S}{R_S} = -\frac{V_EX}{R_E} - \frac{V_X}{Y_E} - gmV_X \]  

\[ \frac{V_S}{R_S} + \frac{V_X}{R_S} = -\frac{V_EX}{R_E} - \frac{V_X}{Y_E} - gmV_X \]

\[ \frac{V_S}{R_S} = -V_X \left[ \frac{1}{R_S} + \frac{1}{R_E} + \frac{1}{Y_E} + gm \right] \]

\[ \frac{V_S}{R_S} = -V_X \left[ \frac{1}{R_S} + \frac{1}{R_E} + \frac{1+r_e gm}{Y_E} \right] \]

\[ \frac{1}{\left[ \frac{1}{R_S} + \frac{1}{R_E} + \frac{1+r_e gm}{Y_E} \right]} \frac{V_S}{R_S} = -V_X \]

\[ \therefore V_X = -\frac{V_S}{R_S} \left[ \left( \frac{r_E}{1+r_e gm} \right) \parallel \frac{R_E}{1} R_S \right] \]  

Now substitute equ 4) in equ 2) we get.

\[ V_o = gm \frac{V_S}{R_S} \left( R_{c1} || R_L \right) \left[ \left( \frac{r_E}{1+r_e gm} \right) || R_E \parallel R_S \right] \]

\[ A_v = \frac{V_o}{V_S} = gm \frac{R_{c1} || R_L}{R_S} \left[ \left( \frac{r_E}{1+r_e gm} \right) || R_E \parallel R_S \right] \]

when \( R_S \) approaches zero, the small signal voltage gain becomes

\[ A_v = gm \left( R_{c1} || R_L \right) \]

The small signal current gain can also be determined from the small signal equivalent circuit. To find the current gain apply kcl at the emitter node we get.

\[ \frac{A_v}{A_v} = gm \left( R_{c1} || R_L \right) \]
\[
I_i = -\frac{V_X}{R_E} - \frac{V_X}{V_{AX}} - g_m V_{AX} \quad (7)
\]

\[
= -V_{AX} \left[ \frac{1}{R_E} + \frac{1}{V_{AX}} + g_m \right] \quad (8)
\]

\[
I_i = -V_{AX} \left[ \frac{1}{R_{E11} \left( \frac{V_{AX}}{1+\beta} \right)} \right] \quad (9)
\]

\[
V_{AX} = -I_i \left[ R_{E11} \left( \frac{V_{AX}}{1+\beta} \right) \right] \quad (8)
\]

The load current \(I_0\) can be written as using current divider side.

\[
I_0 = -g_m V_{AX} \left( \frac{r_c}{r_c+r_L} \right) \quad (9)
\]

Substitute equation (8) in (9) we get:

\[
I_0 = -g_m I_i \left[ R_{E11} \left( \frac{V_{AX}}{1+\beta} \right) \right] \left[ \frac{R_C}{r_c r_L} \right] \quad (10)
\]

\[
A_{IV} = \frac{I_0}{I_i} = g_m \left[ R_{E11} \left( \frac{V_{AX}}{1+\beta} \right) \right] \left[ \frac{R_C}{r_c r_L} \right] \quad (10)
\]

when \(R_E\) approaches to infinity and \(R_L\) tends to zero, then the current gain becomes the short circuit current gain.

\[
A_{IV} = \frac{g_m V_{AX}}{1+\beta} = \frac{B}{1+\beta} = \alpha \quad (10)
\]

In common base circuit, the small signal voltage gain is usually greater than 1 and the small signal current gain is slightly less than 1. However, we still have a small power gain.

**Input impedance:**

The **fig** shown in next page is small - signal
equivalent circuit of the common base configuration looking into the emitter. For convenience we have reversed the polarity of the control voltage. The input resistance is

\[ R_{ie} = \frac{V_x}{I_i} \quad \text{(12)} \]

Apply KCL to the small signal equivalent circuit we get:

\[ I_i = I_b + g_m V_x = \frac{V_x}{Y_{ie}} + g_m V_x = V_x \left( \frac{1}{1+\beta} \right) \]

\[ R_{ie} = \frac{V_x}{I_i} = \frac{V_x}{V_x \left( \frac{1}{1+\beta} \right)} \quad \text{(13)} \]

when the input signal is a current source a small input resistance is desirable.

**Output Impedance**

The circuit diagram for output impedance calculation is shown in Fig. 4. The independent source \( V_x \) has been set equal to zero. Apply KCL to the emitter we get:

The output impedance looking back into the output terminals is then

\[ R_o = R_c \quad \text{(14)} \]

we have assumed to is infinite the output impedance looking back into the collector terminal is essentially infinite which means that the common base circuit looks like an ideal current source. The circuit is also referred to as a current buffer.
In most applications, a single transistor amplifier will not be meet the combined specifications of a given amplification factor, input resistance and output resistance. For example, the required voltage gain may exceed that which can be obtained in a single transistor circuit. Transistor amplifying circuits can be connected in series (as) cascaded as shown below.

![A generalized three stage amplifier.](image)

This may be done either to increase the overall small signal voltage gain or to provide an overall voltage gain greater than 1 with a very low output resistance. The overall voltage gain or current gain in general is not simply the product of individual amplification factors. For example, the gain of stage 1 is a function of the input resistance of stage 2. In other words, loading effects must have to be taken into account.

The overall voltage gain of the above block diagram is

\[ A_v = A_{v3} \times A_{v2} \times A_{v1} \]

Two stage cascade Amplifiers:

The series connected 'cascade configuration of two common emitter circuit is shown in the next page, in which both transistors are biased in the forward biased mode.
Two stage Common emitter amplifier in a Cascade configuration.

The above figure shows the Small signal equivalent circuit of cascade amplifier, assuming all capacitors act as short circuits and each transistor output resistance $r_o$ is infinite.

Let us consider the stage 2 amplifier where

Input resistance $R_{i2} = \frac{V_{i2}}{I_{i2}}$ \hspace{2cm} (1)

Voltage gain $= \frac{V_o}{V_{i2}}$ \hspace{2cm} (2)

From the small signal equivalent circuit at stage 2,

Output voltage

$V_o = G_{m2} V_{i2} \left( R_{c2} || R_L \right)$ \hspace{2cm} (3)

\[
\frac{V_o}{V_{i2}} = G_{m2} \left( R_{c2} || R_L \right)
\]

At stage 1:

Input resistance $R_{c1} = R_{11} R_{21} || V_{i1}$ \hspace{2cm} (4)

Voltage gain $= \frac{V_{i2}}{V_{i1}}$ \hspace{2cm} (5)

From the small signal equivalent circuit at stage 1,

Output voltage

$V_{i2} = G_{m1} V_{i1} \left( R_{c1} || R_{i2} \right)$ \hspace{2cm} (6)

\[
\frac{V_{i2}}{V_{i1}} = G_{m1} \left( R_{c1} || R_{i2} \right)
\]
Apply voltage divider rule at the input we get:
\[ V_{x1} = \left[ \frac{R_{c1}}{R_{c1} + R_S} \right] V_S \]  

Overall voltage gain \((A_v)\):
\[ A_v = \frac{V_o}{V_s} = \frac{V_0}{V_{x2}} \times \frac{V_{x2}}{V_{x1}} \times \frac{V_{x1}}{V_s} \]  

Substitute eqn 3, 5, and 7 in eqn 6 we get:
\[ A_v = g_m1 (Rc2 || R_L) \frac{g_m1 (Rc1 || R_{i2})}{R_{c1} + R_S} \]

where \(R_{i2} = R_{x2}\)

\[ A_v = g_m1 g_m2 (Rc2 || R_L) \frac{g_m1 (Rc1 || R_{x2})}{R_{c1} + R_S} \]

Output resistance:
To determine the output resistance, the independent source \(V_s\) is set equal to zero, which means that \(V_{x1} = 0\). Then \(g_m1 V_{x1} = 0\) which gives \(V_{x2} = 0\) and \(g_m2 V_{x2} = 0\). The output resistance is therefore \(R_{c2}\)

\[ R_o = R_{c2} \]

Multistage Darlington Pair Configuration:
In some applications, it would be desirable to have a bipolar transistor with a much larger current gain than can normally be obtained. The fig shown in the next page is a multistage bipolar configuration called a Darlington pair.
The small signal equivalent circuit in which the input signal is assumed to be a current source as shown below.

Fig. Darlington pair configuration

Fig. Small signal equivalent circuit

we will use the input current source to determine the current gain of the circuit. To determine the small signal current gain \( A_I = \frac{I_o}{I_i} \). From the small signal equivalent circuit we can write \( V_{r1} \) using Ohm's law as

\[ V_{r1} = I_i \cdot R_{s1} \]  \[ \text{(1)} \]

The current source at collector of transistor 2 as

\[ g_m I_i V_{x1} = g_m I_i R_{r1} = R_{r1} \cdot I_i \]  \[ \text{(2)} \]

Similarly using Ohm's law we can write \( V_{r2} \) as

\[ V_{r2} = (I_i + g_m V_{x1}) R_{r2} \]

\[ = (I_i + g_m R_{r1} I_i) R_{r2} \]

\[ V_{r2} = I_i (1 + \beta_i) R_{r2} \]  \[ \text{(3)} \]

The output current \( I_o \) can be written as

\[ I_o = g_m V_{x1} + g_m I_i V_{r2} \]  \[ \text{(4)} \]

Substitute eqn (2) and (3) in (4) we get:

\[ I_o = \beta_i I_i + g_m (1 + \beta_i) R_{r2} \cdot I_i \]
\[ i_o = \beta_1 i_c + \beta_2 (1+\beta_1) i_v \]
\[ = i_c \left[ \beta_1 + \beta_2 + \beta_1 \beta_2 \right] \]
\[ a_i = \frac{i_o}{i_c} = \beta_1 + \beta_2 + \beta_1 \beta_2 \]
\[ a_i \approx \beta_1 \beta_2 \]

From the above notation overall small signal current gain of the cascode pair is essentially the product of the individual current gain.

The input resistance can be written as \( R_i = \frac{V_i}{i}\) and the input voltage as

\[ V_i = V_{i1} + V_{i2} = i_c v_{i1} + i_v (1+\beta_1) v_{i2} \]

\[ V_i = i_c \left[ v_{i1} + (1+\beta_1) v_{i2} \right] \]

\[ R_i = \frac{V_i}{i_c} = \frac{v_{i1} + (1+\beta_1) v_{i2}}{i_c} \]

The base of transistor \( Q_2 \) is connected to the emitter of \( Q_1 \), which means that the input resistance to \( Q_2 \) is multiplied by a factor \((1+\beta_1)\) as we saw in a circuit with emitter resistor. We can write

\[ v_{i1} = \frac{\beta_1 V_T}{I_{c1}} \]

and

\[ I_{c1} + I_{c2} = \frac{I_{c2}}{\beta_2} \]

Therefore, substitute (2) in (3) we get,
\[
I_{x1} = \frac{P_1 V_T}{I_{CA2}} = \frac{P_1 P_2 V_T}{I_{CA2}} = P_1 \left( \frac{P_2 V_T}{I_{CA2}} \right)
\]

\[I_{x1} = P_1 I_{CA2} \quad \text{(10)} \]

Now substitute eq (10) in (9) we get,

\[R_i = P_1 R_{CA2} + R_{CA2} + P_1 R_{CA} \quad \text{(11)} \]

From the resultant equation we understand that the overall gain of the Darlington pair is large. At the same time, the input resistance tends to be large because of the \( P \) multiplication.

\[\begin{array}{c}
\text{Multistage Configuration} \\
\text{Cascade Configuration}
\end{array} \]

A slightly different multistage configuration called a Cascade configuration as shown below. The input is divided into a common emitter amplifier (Q1), which drives a common base amplifier (Q2). The ac equivalent circuit is also shown below.

\[\text{Fig. Small Signal Equivalent Circuit of Cascade Amplifier.}\]
we see that the output signal current of $Q_1$ is the input signal of $Q_2$, normally the input signal of a common base configuration is to be a current. One advantage of this circuit is that the output resistance looking into the collector of $Q_2$ is much larger than the output resistance of a simple common emitter circuit. Another important advantage of this circuit is in the frequency response.

Apply $\text{k}_{\text{CL}}$ to the $E_2$ of the small signal equivalent circuit we get:

$$9m_1V_{x1} = \frac{V_{x2}}{\text{r}_{x2}} + 9m_2V_{x2}.$$  

Solving the above equation for control voltage $V_{x2}$

Consider $V_{x1} = V_S$

$$9m_1V_S = \frac{V_{x2}}{\text{r}_{x2}} + 9m_2V_{x2}.$$  

$$V_{x2} = \frac{9m_1V_S}{9m_2 - \text{r}_{x2}}$$

(where $\beta_2 = \frac{9m_2}{9m_1\text{r}_{x2}}$)  

$$9m_2V_S = \frac{V_{x2}}{\text{r}_{x2}} 9m_1V_S$$

$$V_{x2} = \frac{\text{r}_{x2}V_{x2}}{9m_2 - \text{r}_{x2}}$$

From the small signal equivalent circuit the output voltage $V_O$ as

$$V_O = -9m_2V_{x2} (R_{CL} / R_L)$$  

Substitute eqn $\text{2}$ in eqn $\text{3}$ we get:
\[ V_o = -\frac{g_m R_x}{(1 + \beta_a)} \frac{g_{m1} V_s (R_e R_L)}{R_C} \quad (4) \]

\[ V_o = -\frac{\beta_a}{1 + \beta_a} g_{m1} V_s (R_e R_L) \]

When \( \beta_a \gg 1 \) then the above equation become

\[ V_o \approx -g_{m1} V_s (R_e R_L) \]

\[ A_v = \frac{V_o}{V_s} \approx -g_{m1} (R_e R_L) \quad (5) \]

which is same as for a single stage common emitter amplifier. This result is to be expected since the common base gain \( A_v \) of the Common base circuit is essentially unity.

**Differential Amplifier:**

The differential amplifier amplifies the difference between two input voltage signal, hence it is called a difference amplifier. The below Fig shows the block diagram of a differential amplifier.

[Diagram of Differential Amplifier]

where \( v_i \) and \( v_s \) are the two input signal while \( v_o \) is the output. In an ideal differential amplifier the output voltage \( v_o \) is proportional to the
The difference between the two input signal is:

\[ V_0 \propto (V_1 - V_2) \]  

**Differential Gain (\( A_d \))**:

where \( V_0 = A_d (V_1 - V_2) \)

\[ \text{At is the constant of proportionality. The } A_d \text{ is the gain with which differential amplifier amplifies the difference between two input signals. Hence it is called differential gain of differential amplifier.} \]

The difference between two input voltages \( (V_1 - V_2) \) is called difference voltage \( V_d \). These equations become

\[ V_0 = A_d V_d \]

\[ A_d = \frac{V_o}{V_d} \]

**Differential Gain in terms of decibel (dB)** as

\[ A_d = 20 \log_{10}(A_d) \text{ in dB} \]

**Common Mode Gain (\( A_{cm} \))**

The output voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of the two inputs. Such an average level of the two sig voltage is called common mode voltage denoted as \( V_{cm} \)

\[ V_{cm} = \frac{V_1 + V_2}{2} \]

The differential amplifier produces the output voltage proportional to such common mode signal is

\[ V_o = A_{cm} V_{cm} \]
If we apply two input voltages which are equal in all the respects to the differential amplifier i.e. $V_1 = V_2$, then ideally the output voltage $V_o = A_d (V_1 - V_2)$ becomes zero. However, there exists some finite output for $V_1 = V_2$ due to common mode gain $A_{cm}$.

So the total output of any differential amplifier can be expressed as

$$V_o = A_d V_d + A_{cm} V_{cm} \quad \text{(7)}$$

**Common mode rejection ratio** (CMRR)

when the same voltage is applied to both the inputs, the differential amplifier is said to be operated in a common mode configuration. Many disturbance signals, noise signal appear as a common input signal to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier.

The ability of a differential amplifier to reject common mode signal is expressed by a ratio called common mode rejection ratio denoted as CMRR.

It is defined as the ratio of differential voltage gain $A_d$ to common mode voltage gain $A_{cm}$.

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right| \quad \text{(8)}$$

CMRR is also expressed in dB as

$$\text{CMRR in dB} = 20 \log_{10} \left| \frac{A_d}{A_{cm}} \right| \text{ dB} \quad \text{(9)}$$
The output voltage can be expressed in terms of CMRR by considering equation (9):

\[ V_o = A_d V_d + A_{cm} V_{cm} \]

\[ = A_d V_d \left[ 1 + \frac{A_{cm} V_{cm}}{A_d V_d} \right] \]

\[ = A_d V_d \left[ 1 + \left( \frac{V_{cm}}{A_d V_d} \right) \right] \]

\[ V_o = A_d V_d \left[ 1 + \frac{1}{CMRR \frac{V_{cm}}{V_d}} \right] \]

---

Features of Differential Amplifier:

* High differential voltage gain
* Low common mode gain
* High input impedance
* Low output impedance
* Large bandwidth

BJT Differential Amplifier Operation:

The basic BJT differential pair configuration is shown in the next page. It consists of two identical transistors \( Q_1 \) and \( Q_2 \), whose emitters are connected together and biased by a constant current source \( I_e \), which is connected to a negative supply voltage \( V^- \). The collectors of \( Q_1 \) and \( Q_2 \) are connected through resistors \( R_c \) to a positive supply voltage \( V^+ \). By design, transistors \( Q_1 \) and \( Q_2 \) are to remain biased in the forward-active region.

We assume that the two collector resistors...
$r_c$ are equal and that $v_{b1}$ and $v_{b2}$, are ideal source meaning that the output resistance of these source are negligibly small.

Since both positive and negative bias voltages are used in the circuit the need for coupling capacitors and voltage divider biasing resistors at the inputs of $Q_1$ and $Q_2$ has been eliminated. If the input signal voltages $v_{b1}$ and $v_{b2}$ in the circuit are both zero, $Q_1$ and $Q_2$ are still biased in the active region by the current source $I_E$. The common emitter voltage $v_e$ would be on the order of $0.7$V. This circuit is referred to as a dc coupled differential amplifier. So difference in dc input voltages can be amplified.

**Common mode operation.**

The differential amplifier circuit in which the two base terminals are connected together and a common mode voltage $v_{cm}$ is applied as shown in Fig. 9. The transistors are biased on by the constant current source and the voltage at the common emitter is $v_E = v_{cm} - v_{BE(on)}$. Since $Q_1$ and $Q_2$ are identical, current $I_E$ splits evenly between two transistors

$$I_{E1} = I_{E2} = \frac{I_E}{2} \quad \cdots (1)$$

If base current are negligible then
then \( i_{c1} \approx i_{c1} \) and \( i_{c2} \approx i_{c2} \) and

\[
V_{c1} = V^+ - \frac{I_{c2}R_C}{\Delta V} = V_{c2} \quad \text{(2)}
\]

In the above equation for applied common mode voltage \( I_{c2} \) splits evenly between \( Q_1 \) and \( Q_2 \) and the difference between \( V_{c1} \) and \( V_{c2} \) is zero.

**Differential Mode Operation:**

Now if \( V_{c1} \) increases by a few millivolts and \( V_{c2} \) decreases by the same amount (Fig. 3) \( V_{B1} = V_{A1} \) and \( V_{B2} = -V_{A2} \). Since emitters are common B-E voltages on \( Q_1 \) and \( Q_2 \) are no longer equal.

Since \( V_{B1} \) increases and \( V_{B2} \) decreases then \( V_{B1} > V_{B2} \) which means that \( i_{c1} \) increases by \( \Delta I \) above its quiescent value and \( i_{c2} \) decreases by \( \Delta I \).

A potential difference now exist between two collector terminals.

\[
V_{c2} - V_{c1} = \left[ V^+ - \left( \frac{I_{c2}}{\Delta V} - \Delta \xi \right)R_C \right] - \left[ V^+ - \left( \frac{I_{c1} + \Delta \xi}{\Delta V} \right)R_C \right] = V^+ - \frac{I_{c2}}{\Delta V}R_C + \Delta \xi R_C \quad \text{(3)}
\]

\[
V_{c2} = 2 \Delta \xi R_C
\]

**DC Transfer Characteristics:**

The general analysis of differential pair configuration by using the exponential relationship between Collector Current and B-E Voltage

\[
I_{c1} = I_S \left[ e^{V_{BE1}/V_T} - 1 \right]
\]
and \( \textit{i}_{ca} = \textit{I}_s e^{\textit{V}_{ces}/\textit{V}_T} \)

we assume \( \textit{a}_1 \) and \( \textit{a}_2 \) are matched and are operating at the same temperature, so the coefficient \( \textit{I}_a \) is the same in each expression.

Neglecting base current and assuming \( \textit{I}_a \) is an ideal Constant current source,

\[
\textit{I}_{bo} = \textit{I}_c + \textit{I}_{ces} = \textit{I}_s e^{\textit{V}_{ces}/\textit{V}_T} + \textit{I}_s e^{\textit{V}_{ces}/\textit{V}_T}
\]

\[
\textit{I}_{bo} = \textit{I}_s \left[ e^{\textit{V}_{ces}/\textit{V}_T} + e^{\textit{V}_{ces}/\textit{V}_T} \right] \quad (16)
\]

Taking the ratio of \( \textit{I}_c \) to \( \textit{I}_{bo} \) we get:

\[
\frac{\textit{i}_{c1}}{\textit{i}_{bo}} = \frac{\textit{I}_s e^{\textit{V}_{ces}/\textit{V}_T}}{\textit{I}_s \left[ e^{\textit{V}_{ces}/\textit{V}_T} + e^{\textit{V}_{ces}/\textit{V}_T} \right]}
\]

\[
\frac{\textit{i}_{c1}}{\textit{i}_{bo}} = \frac{e^{\textit{V}_{ces}/\textit{V}_T}}{1 + e^{\textit{V}_{ces}/\textit{V}_T}} \quad (17)
\]

Similarly, taking the ratio of \( \textit{i}_{c2} \) to \( \textit{i}_{bo} \) we get:

\[
\frac{\textit{i}_{c2}}{\textit{i}_{bo}} = \frac{1}{1 e^{-(\textit{V}_{ces} - \textit{V}_{ces})/\textit{V}_T}} \quad (18)
\]

From the differential mode configuration we can write:

\[
\textit{V}_{ces} - \textit{V}_{ces} = \textit{V}_d \quad (19)
\]

Equation (17) and (18) can be written as:

\[
\textit{i}_{c1} = \frac{\textit{I}_{bo} - e^{\textit{V}_{ces}/\textit{V}_T}}{1 + e^{\textit{V}_{ces}/\textit{V}_T}} \quad (20)
\]
\[ i_{c_1} = \frac{I_0}{1 + e^{V_d/V_T}} \quad (21) \]

The above equations describe the basic current-voltage characteristic of the differential amplifier.

The normalized plot of the dc transfer characteristic for the differential amplifier is shown in Fig.

The gain of the differential amplifier is proportional to the slope of the transfer curve about the point \( V_d = 0 \).

The magnitude of \( V_d \) becomes sufficiently large, essentially all of current \( I_0 \) goes to one transistor and the second transistor effectively turns off.

Desired expression for \( V_d \):

The linear approximation for \( i_{c_1} \) versus \( V_d \) can be written as

\[ i_{c_1} = \frac{I_0}{2} + g_T V_d \quad (22') \]

The forward transconductance \( g_T \) can be written in terms of individual transconductance \( g_m \) as

\[ g_T = \frac{I_0}{4V_T} = \frac{1}{2} \frac{I_0}{V_T} = \frac{1}{2} g_m \quad (23) \]

Substitute equation (23) in (22') to get

\[ i_{c_1} = \frac{I_0}{2} + \frac{1}{2} g_m V_d \quad (24) \]

where \( I_0/2 \) is quiescent collector current in \( Q_1 \) and \( Q_2 \).

The magnitude of the small signal collector current in each transistor is then

\[ g_m V_d/2, \text{ i.e. } \Delta i = \frac{g_m V_d}{2} \quad (25) \]
Consider differential mode configuration circuit diagram and replace \( \Delta i \) by \( \frac{gmVd}{2i} \). Then the output signal voltage is

\[
V_o = V_{c2} - V_{c1} \quad \text{(26)}
\]

Substitute \( V_{c2} \) and \( V_{c1} \) in the above equation we get:

\[
V_o = \left[ V^+ - V_{c2}RC \right] - \left[ V^+ - V_{c1}RC \right] = V^+ - V_{c2}RC - V^+ + V_{c1}RC
\]

\[
V_o = (V_{c1} - V_{c2}) RC
\]

\[
= \left[ \frac{I_e}{2i} + \frac{gmVd}{2i} \right] RC
\]

\[
V_o = gmVdRC \quad \text{(27)}
\]

The ratio of output signal voltage to differential gain mode input signal is called differential mode gain \( A_d \). From equation (27) we can write:

\[
A_d = \frac{V_o}{V_{in}} = gmR_C = \frac{I_{e}RC}{2VT}. \quad \text{(28)}
\]

If the output voltage is the difference between the two collector terminal voltage, then neither side of the output voltage need at ground potential. In many cases the output voltage is taken at one collector terminal with respect to ground. The resulted voltage output is called a one-side output.

The differential gain for the one-side output is

\[
A_d = \frac{gmR_C}{2} = \frac{I_{e}RC}{2VT} = \frac{I_{e}RC}{4VT} \quad \text{(29)}
\]
Small signal equivalent circuit analysis:

The below fig. shows the small signal equivalent circuit of the bipolar differential pair configuration. We assume that the early voltage is infinite for the two emitter pair transistors, and the constant current source is not ideal but can be represented by a finite output impedance $R_o$. Resistance $R_B$ are also included. These represent the output resistance of the signal voltage source.

\[ V_{s1} + 2g_m V_{s2} + V_{s2} = V_e \]

\[ V_{r1} \left[ \frac{1 + g_m V_x}{V_x} \right] + V_{s2} \left[ \frac{g_m V_x + 1}{V_x} \right] = \frac{V_e}{R_o} \]

\[ V_{y1} \left[ \frac{1 + B}{V_x} \right] + V_{y2} \left[ \frac{1 + B}{V_x} \right] = \frac{V_e}{R_o} \]
Small signal equivalent circuit analysis:

The below fig shows the small signal equivalent circuit of the bipolar differential pair configuration. We assume that the early voltage is infinite for the two emitter pair transistors, and the constant current source is not ideal but can be represented by a finite output impedance $R_o$. Resistance $R_B$ are also included. These represent the output resistance at the signal voltage source.

![Circuit Diagram](image)

Fig. Small signal equivalent circuit, bipolar differential amplifier. Since the two transistors are biased at the same quiescent current we have:

\[ r_{sc1} = r_{sc2} = r_{sc} \text{ and } g_{m1} = g_{m2} = g_m \quad \text{(30)} \]

Apply KCL at node $V_e$ using phasor notation we can write:

\[ \frac{V_{x1}}{r_{sc}} + \frac{g_m V_{x1}}{r_{sc}} + \frac{g_m V_{x2}}{r_{sc}} + \frac{V_{x2}}{r_{c}} = \frac{V_e}{R_o} \quad \text{(31)} \]

\[ V_{x1} \left[ 1 + \frac{g_m V_{x1}}{r_{sc}} \right] + V_{x2} \left[ \frac{g_m V_{x1} + 1}{r_{sc}} \right] = \frac{V_e}{R_o} \quad \text{(32a)} \]

\[ V_{x1} \left[ 1 + \frac{1}{r_{sc}} \right] + V_{x2} \left[ \frac{1 + \beta}{r_{sc}} \right] = \frac{V_e}{R_o} \quad \text{(32b)} \]
Similarly from the circuit we can write,

\[ \frac{V_{x1}}{R_x} = \frac{V_{b1} - V_e}{R_x + R_B} \quad \text{and} \quad \frac{V_{x}\bar{a}}{R_x} = \frac{V_{b\bar{a}} - V_e}{R_x + R_B} \quad (33) \]

From the above equation,

\[ V_{x1} = \left( \frac{V_{b1} - V_e}{R_x + R_B} \right) R_x \quad \text{and} \quad V_{x}\bar{a} = \left( \frac{V_{b\bar{a}} - V_e}{R_x + R_B} \right) R_x \]

Substitute \( V_{x1} \) and \( V_{x}\bar{a} \) in (33) we get,

\[
\left[ \frac{V_{b1} - V_e}{R_x + R_B} \right] R_x \left( \frac{1 + \beta}{R_x} \right) + \left( \frac{V_{b\bar{a}} - V_e}{R_x + R_B} \right) R_x \left( \frac{1 + \beta}{R_x} \right) = \frac{V_e}{R_0}
\]

\[
\frac{(1 + \beta)}{R_x + R_B} \left[ V_{b1} - V_e + V_{b\bar{a}} - V_e \right] = \frac{V_e}{R_0}
\]

Solving the above equation for \( V_e \) we get,

\[
(1 + \beta) \left[ V_{b1} + V_{b\bar{a}} - 2V_e \right] = \frac{V_e (R_x + R_B)}{R_0 (1 + \beta)}
\]

\[
V_{b1} + V_{b\bar{a}} = \frac{V_e (R_x + R_B)}{R_0 (1 + \beta)} + \frac{2V_e}{R_0 (1 + \beta)}
\]

\[
V_{b1} + V_{b\bar{a}} = V_e \left[ \frac{(R_x + R_B) + 2}{(1 + \beta) R_0} \right]
\]

\[
V_e = \frac{V_{b1} + V_{b\bar{a}}}{\left[ \frac{(R_x + R_B) + 2}{(1 + \beta) R_0} \right]} \quad (35)
\]

**One Side Output**

If we consider a one-side output at the collector.
\[ V_0 = V_{ca} = -\left( g_m V_{ra} \right) R_c \]  

Substitute \( V_{ca} \) in above equation we get:

\[ V_0 = -g_m R_c \left[ \frac{V_{b2} - V_e}{R_n + R_B} \right] = -\beta R_c \left( \frac{V_{b2} - V_e}{R_n + R_B} \right) \]  

Substitute eqn (35) in (37) we get:

\[ V_0 = \frac{-\beta R_c}{R_n + R_B} \left[ V_{b2} - \frac{\left( V_{b1} + V_{b2} \right)}{\frac{R_n + R_B}{(1 + \beta)R_o} + 2} \right] \]

\[ = \frac{-\beta R_c}{R_n + R_B} \left[ \frac{V_{b2} \left( \frac{R_n + R_B}{(1 + \beta)R_o} + 2 \right)}{\frac{R_n + R_B}{(1 + \beta)R_o}} - V_{b1} - V_{b2} \right] \]

\[ = \frac{-\beta R_c}{R_n + R_B} \left[ \frac{V_{b2} \left( \frac{R_n + R_B}{(1 + \beta)R_o} + 1 \right)}{\frac{R_n + R_B}{(1 + \beta)R_o}} - V_{b1} \right] \]

In an ideal constant current source, the output resistance is \( R_o = \omega \) then above eqn (38) become:

\[ V_0 = \frac{-\beta R_c}{R_n + R_B} \left[ \frac{V_{b2} - V_{b1}}{\omega} \right] \]

The differential mode input is:

\[ V_d = V_{b2} - V_{b1} \quad V_{b1} - V_{b2} \]

\[ \therefore V_0 = \frac{+\beta R_c}{R_n + R_B} \frac{V_d}{\omega} \]
\[ A_d = \frac{V_o}{V_d} = \frac{B R_C}{2(R_o + R_B)} \quad \cdots \quad (40) \]

The differential and common mode voltage are given in equations below.

\[ V_d = V_{b1} - V_{b2} \quad \text{and} \quad V_{cm} = \frac{V_{b1} + V_{b2}}{2} \quad \cdots \quad (41) \]

Solving the above equation for \( V_{b1} \) and \( V_{b2} \) in terms of \( V_d \) and \( V_{cm} \) we get:

\[ V_{b1} = V_{cm} + \frac{V_d}{2} \quad \cdots \quad (42) \]

\[ V_{b2} = V_{cm} - \frac{V_d}{2} \quad \cdots \quad (43) \]

Since we are dealing with the linear amplifier, superposition applies. The above equation (42) and (43) state that the two input signals can be written as the sum of differential mode input signal component and common mode input signal component.

Substituting equations (42) and (43) in (40) and rearranging the term results in

\[ V_o = \frac{B R_C}{2(R_o + R_B)} V_d - \frac{B R_C}{2} \frac{V_{cm}}{R_o + R_B} \left[ i + \frac{1}{2} \frac{R_o}{R_o + R_B} \right] \quad \cdots \quad (44) \]

we can write the output voltage in general form as

\[ V_o = A_d V_d + A_{cm} V_{cm} \quad \cdots \quad (45) \]

where comparing equation (44) and (45) we can write

\[ A_d = \frac{B R_C}{2(R_o + R_B)} \quad \cdots \quad (46) \]
and common mode gain.

\[ A_{cm} = \frac{-\beta R_C}{(\gamma_N + R_B) \left[ 1 + 2(1+\beta)R_0 \right]} \]

Considering the base resistor \( R_B = 0 \) we can write

\[ A_d = \frac{R_C \beta}{\gamma_N} \frac{\beta}{\gamma_N} = \frac{R_C \beta}{\gamma_N} \]

where \( g_m = \frac{I_{CA}}{V_T} \) and \( \overline{I_{CA}} = \frac{I_{CA}}{2} \).

\[ A_d = \frac{R_C \overline{I_{CA}}}{\beta V_T} \]

Similarly

\[ A_{cm} = \frac{-g_m \gamma_N R_C}{\gamma_N \left[ 1 + 2(1+\beta)R_0 \right]} \]

where \( \frac{1}{\gamma_N} = \frac{g_m}{\beta} \).

\[ A_{cm} = \frac{-\overline{I_{CA}} \beta R_C}{\gamma_N \left[ 1 + 2(1+\beta)R_0 \overline{I_{CA}} \right]} \]

we again observe that common mode gain goes to zero for an ideal current source in which \( R_0 = \infty \). For a non-ideal current source \( R_0 \) is finite and common-mode gain is not zero.
Common mode rejection ratio:

The ability of a differential amplifier to reject a common mode signal is described in terms of the common mode rejection ratio (CMRR). The CMRR is a figure of merit for the differential amplifier and is defined as

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right| \quad (50)$$

For an ideal differential amplifier, $A_{cm} = 0$ and $\text{CMRR} = \infty$.

The one-sided differential and common mode gains are given by Equations (48) and (49) as

$$\text{CMRR} = \frac{\frac{R_c\xi \alpha/4V_T}{\phi}}{\frac{1}{2} \left[ \frac{1}{\frac{P V_T}{P V_T + (1+\beta)R_o I_0}} \right] \left[ \frac{P V_T + (1+\beta)R_o I_0}{P V_T} \right]} \quad (51)$$

The CMRR increases as $R_o$ increases.
UNIT III

SINGLE STAGE JFET AND MOSFET AMPLIFIERS

JFET AMPLIFIER:

JFET amplifiers provide an excellent voltage gain with the added advantages of a high input impedance because of their high input impedance and other characteristic JFET are often preferred over BJT for certain types of applications.

Most of the concepts that relate to amplifiers using BJT apply equally to FET. The three basic FET circuit configurations are:

(i) Common Source
(ii) Common Drain
(iii) Common Gate.

Small Signal AC Equivalent Circuit for JFET

We know that, drain to source current of JFET is controlled by gate to source voltage. The change in drain current due to change in gate to source voltage can be determined using the transconductance (g_m).

\[ g_m = \frac{\Delta I_D}{\Delta V_{gs}} \]

\[ \Delta I_D = g_m \Delta V_{gs} \]

Which in BJT the relation between an output and input quantity is given by amplification factor \( \beta \).
whereas in JFET this relation is given by

The another important parameter $g_d$ of JFET is drain

resistance $r_d$. It is given by

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \mid V_{GS} = \text{Constant}$$

The amplification factor $\mu$ of JFET is defined as

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \mid I_D = \text{Constant}$$

The parameters $g_m$, $r_d$ and $\mu$ are related by

$$\mu = r_d g_m$$

JFET low frequency a.c. equivalent circuit

The small signal low frequency a.c. equivalent circuit for n-channel JFET is shown below. The relation $A_f$ by $V_{gs}$ is included as a current source $g_m V_{gs}$ connected from drain to source. The input impedance is represented by the open circuit at its input terminals since gate current $I_G$ is zero. The output impedance is represented by $r_d$ from drain to source.

![Diagram](image-url)
when the value of external drain resistance $R_D$ is very small as compared to the value of output impedance represented by $r_d$ it is possible to replace $r_d$ by open circuit. This gives us approximate ac equivalent circuit for JFET amplifier as shown below.

Fig. Approximate ac equivalent circuit $V_{os}$ JFET amplifier.

Common Source Amplifier with Fixed Bias.

The common source amplifier with fixed bias is shown. The coupling capacitors $C_1$ and $C_2$ which are used to isolate the dc biasing from the applied ac signal act as short circuit for ac analysis.

Input Resistance $R_i$:

From the small signal equivalent circuit:

$$R_i = R_g.$$
The output resistance \( R_o \) is the impedance measured looking from the output side with input voltage \( V_i = 0 \). Therefore, \( V_{gs} = 0 \) and \( g_m V_{gs} = 0 \), this allows the current source to be replaced by an open circuit as shown below.

Therefore, output resistance

\[ R_o = R_d || R_d \] \hspace{1cm} (2)

If the resistance \( R_d \) is sufficiently large compared to \( R_o \), then we can say the output impedance is approximately equal to \( R_o \)

\[ R_o \approx R_d \] \hspace{1cm} (3)

Voltage Gain \( A_V \):

The voltage gain \( A_V = \frac{V_o}{V_i} \) from the small signal equivalent circuit.

\[ V_o = -g_m V_{gs} \left( R_d || R_d \right) \] \hspace{1cm} (4)

\[ V_i = V_{gs} \]

\[ V_o = -g_m V_i \left( R_d || R_d \right) \]

\[ A_V = \frac{V_o}{V_i} = -g_m \left( R_d || R_d \right) \] \hspace{1cm} (5)

If \( R_d \gg R_o \) then equation (5) becomes

\[ A_V = -g_m R_d \] \hspace{1cm} (6)
Common Source Amplifier with Self Bias: (Bypassed Rs)

The common source amplifier with self bias is shown below. The coupling capacitors $C_1$ and $C_2$, which are used to isolate the dc biasing from applied ac signal, act as short circuit for low frequency analysis. Bypass capacitors $C_S$ also act as a short circuit.

![Common Source FET Amplifier with Self Bias](image)

Fig. Common Source FET amplifier with self bias.

All capacitors and dc supply are short circuit and FET with its low frequency equivalent circuit.

Input Impedance Resistance ($R_i$):-

From the small signal equivalent circuit we can write:

$$Z_i = R_i = R_G$$ \[1\]

Output Resistance ($R_o$):-

$$R_o = R_D \parallel R_L$$ \[2\]

when $Y_d \gg R_D \parallel R_L$

$$R_o \approx R_D \parallel R_L$$ \[3\]
Voltage gain (A_v):

The output voltage can be written as

\[ V_o = -g_m \cdot V_{gs} \cdot (\frac{1}{R_{D11}}) \cdot R_{D11RL} \]  \[\text{Equation 4}\]

where \[ V_i = V_{gs} \] then equation 4 become

\[ V_o = -g_m \cdot V_i \cdot (\frac{1}{R_{D11}}) \cdot R_{D11RL} \]

ie. \[ A_v = \frac{V_o}{V_i} = -g_m \cdot (\frac{1}{R_{D11}}) \cdot R_{D11RL} \]  \[\text{Equation 5}\]

when \[ R_D >> R_{D11RL} \]

\[ A_v = -g_m \cdot (R_{D11RL}) \]  \[\text{Equation 6}\]

Common Source Amplifier with Self Bias (Unbypassed Rs)

The circuit diagram of a common source amplifier with self bias un bypassed Rs is shown below. Now Rs will be a part of the low frequency equivalent model as shown in Fig. The common source circuit with self bias having un bypassed Rs.

\[ \text{Fig. Small Signal equivalent circuit of common source with self bias having un bypassed Rs.} \]
Input Resistance ($R_i$):

From the small signal equivalent circuit

$$R_i = R_{in} \quad \text{(1)}$$

Output Resistance ($R_o$):

$$R_o = R'_o || R_{D1} || R_{L} \quad \text{(2)}$$

where as

$$R'_o = \frac{V_o}{I_D} \quad \text{when } V_i = 0.$$

Apply KVL on output circuit we can write:

$$V_o = (I_D - g_m V_{gs}) R_{D} + I_D R_s \quad \text{(3)}$$

$$V_o = I_D R_{D} - g_m V_{gs} R_D + I_D R_s \quad \text{(4)}$$

Apply KVL on input circuit we get:

$$V_{gs} = V_i - I_D R_s \quad \text{(5)}$$

when $V_i = 0$ then

$$V_{gs} = -I_D R_s \quad \text{(5)}$$

Now substitute $V_{gs}$ in equ. (4) we get:

$$V_o = I_D R_{D} + g_m I_D R_s R_D + I_D R_s \quad \text{(4)}$$

where $\mu = g_m R_D = \mu$

$$V_o = I_D \left[ R_D + g_m R_s R_D + R_s \right]$$

$$V_o = I_D \left[ R_D + \mu R_s R_D + R_s \right]$$

$$V_o = I_D \left[ R_D + R_s (\mu + 1) \right]$$

$$\therefore R'_o = \frac{V_o}{I_D} = R_D + R_s (\mu + 1) \quad \text{(5)}$$
Substitute equation 6 in 5 we get:

\[ R_0 = \left[ V_d + R_s (\mu + 1) \right] \frac{1}{R_D \parallel R_L} \]  

 Voltage Gain \((A_V)\):

From the circuit we can write: \( V_o = -I_D \left( R_D \parallel R_L \right) \)  

Apply KVL to output circuit as shown in Fig.

\[(I_D - g_m V_{gs}) V_d + I_D R_s + I_D \left( R_D \parallel R_L \right) = 0 \] \( (I_D - g_m V_{gs}) V_d + I_D R_s + I_D \left( R_D \parallel R_L \right) = 0 \)  

we know that \( V_{gs} = V_i - I_D R_s \). Now substitute \( V_{gs} \) in equation 7 we get:

\[ I_D - g_m (V_i - I_D R_s) V_d = -I_D R_s + I_D \left( R_D \parallel R_L \right) = 0 \]

\[ I_D - g_m V_i V_d + g_m I_D R_s V_d + I_D R_s + I_D \left( R_D \parallel R_L \right) = 0 \]

\[ I_D \left[ V_d + g_m R_s V_d + R_s + (R_D \parallel R_L) \right] = g_m V_i V_d \]

\[ I_D = \frac{g_m V_i V_d}{[v_d + g_m R_s v_d + R_s + (R_D \parallel R_L)]} \]  

Substitute equation 10 in 8 we get:

\[ V_o = \frac{-g_m V_i V_d \left( R_D \parallel R_L \right)}{[v_d + g_m R_s v_d + R_s + (R_D \parallel R_L)]} \]

\[ A_V = \frac{V_o}{V_i} = \frac{-g_m V_d \left( R_D \parallel R_L \right)}{[v_d + g_m R_s v_d + R_s + (R_D \parallel R_L)]} \]
Rearrange eqn 10 we get

$$A_v = \frac{-g_m \left(R_D \parallel R_L\right)}{1 + g_m R_s + R_s + \left(R_D \parallel R_L\right)}$$

(12)

Therefore

$$V_d \gg R_s + \left(R_D \parallel R_L\right)$$

then above equation become.

$$A_v = \frac{-g_m \left(R_D \parallel R_L\right)}{1 + g_m R_s}$$

(13)

**Common source amplifier with voltage divider Bias (unbypassed $R_s$).**

The common source amplifier with voltage divider bias having unbypassed $R_s$ is shown below.

Now $R_s$ will be the part of ac equivalent model as shown in Fig. 1. The derivation proceeded procedure is same as self bias.

**Fig.**: Common source amplifier with voltage divider bias having unbypassed $R_s$.
Input Resistance:
\[ R_i = R_1 R_2 \]  

Output Resistance:
\[ R_o = R_0' R_\text{D} R_{\text{L}} \]  

where as \[ R_0' = R_d + R_s (\mu + 1) \]
\[ R_o = \left[ R_d + R_s (\mu + 1) \right] R_{\text{D}} R_{\text{L}} \]

Voltage gain:
\[ A_v = \frac{V_o}{V_i} \]
\[ A_v = \frac{-g_m R_L'}{1 + g_m R_s + \frac{R_s + R_L}{R_d}} \]

where as \[ R_L' = R_{\text{D}} R_{\text{L}} \]
and when \[ R_d \gg R_s + R_L \] equation 4) become
\[ A_v = \frac{-g_m R_L'}{1 + g_m R_s} \]

Now substitute \( R_L' \) in above equation
\[ A_v = \frac{-g_m (R_{\text{D}} R_{\text{L}})}{1 + g_m R_s} \]

Since the resulting ac equivalent circuit is same
as ac equivalent circuit of fixed bias. The equation
for \( R_o \) and \( A_v \) are same.
Common Drain Amplifier: (Source follower)

The circuit diagram of a common drain configuration is shown below. In a common drain amplifier, circuit input is applied between gate and source, and output is taken between source and drain.

\[ V_{gs} = V_G + V_{GS} \quad \quad \quad (1) \]

When a signal is applied to the JFET gate via \( V_G \), it varies with the signal. As \( V_{GS} \) is constant, then \( V_G \) varies with \( V_i \).
**Input Resistance** ($R_i$)

From the small signal equivalent circuit, we can write:

$$R_i = R_G$$ ---- (1)

**Output Resistance** ($R_O$)

The output resistance is obtained by setting $V_i = 0$.

The resultant equivalent circuit is shown in Fig. A.

Apply KCL at node A, we can write:

$$I_0 + g_m V_{gs} = I_{rd} + I_{RL}$$ ---- (2)

$$I_0 + g_m V_{gs} = \frac{V_O}{R_d} + \frac{V_O}{R_L}$$ ---- (3)

When $V_i = 0$, then $V_o = -V_{gs}$, therefore:

Equation (3) we can write:

$$I_0 = \frac{V_o}{R_d} + \frac{V_o}{R_L} + g_m V_{gs}$$

$$I_0 = \frac{V_o}{R_d} + \frac{V_o}{R_L} + g_m V_{gs}$$

Hence:

$$R_o = \frac{V_o}{I_0} = \frac{1}{\frac{1}{R_d} + \frac{1}{R_L} + \frac{1}{g_m}}$$
The previous equation can be represented in parallel combination of three resistors.

\[ R_0 = \frac{1}{R_{d} \parallel R_{L} \parallel \frac{1}{g_m}} \tag{4} \]

when \( R_d \gg R_L \parallel \frac{1}{g_m} \) then eqn (4) becomes

\[ R_0 = R_L \parallel \frac{1}{g_m} = \frac{R_{L1} \parallel R_{L2}}{1/g_m} \tag{5} \]

\[ R_0 = \frac{R_{S1} \parallel R_{L1}}{1/g_m} \tag{5} \]

Voltage Gain \( A_v \):

From the small signal equivalent circuit can write.

\[ V_o = I_D \left( \frac{1}{R_{d} \parallel R_L} \right) \tag{6} \]

where as \( I_D = g_m V_{gs} \)

\[ V_o = g_m V_{gs} \left( \frac{1}{R_{d} \parallel R_L} \right) \tag{7} \]

Apply KVL to the small signal equivalent circuit can write.

\[ V_i = V_{gs} + V_o \tag{8} \]

Substitute eqn (6) in (8) we get:

\[ V_i = V_{gs} + g_m V_{gs} \left( \frac{1}{R_{d} \parallel R_L} \right) \]

\[ V_i = V_{gs} \left[ 1 + g_m \left( \frac{1}{R_{d} \parallel R_L} \right) \right] \tag{9} \]

Now divide eqn (7) by (9) we get:
\[ A_v = \frac{V_o}{V_i} = \frac{9m \times V_{gs}}{V_{gs} \left[ 1 + 9m \times \frac{R_d}{R_L} \right]} \]

\[ A_v = \frac{9m \times R_L}{1 + 9m \times R_L} \]  \hspace{1cm} (10)

If \( V_d \gg R_s \) then eqn (10) becomes

\[ A_v = \frac{9m \times R_L}{1 + 9m \times R_L} \]  \hspace{1cm} (11)

Similarly, if \( 9m \times R_L \gg 1 \) then eqn (10) becomes

\[ A_v \approx 1 \]  \hspace{1cm} (but it is always less than 1.)

From the above relation we understand that the common drain circuit does not provide voltage gain and there is no phase shift between input and output voltages.

**Common Gate Amplifier**

The circuit diagram of common gate amplifier is shown in Fig. In common gate amplifier circuit, input is applied between source and gate and output is taken between drain and gate.

In common gate configuration, gate voltage is at constant potential. Thus increase in input voltage \( V_i \).
in positive direction increase the negative gate-source bias voltage. Due to this drain current reduces, since 

\[ V_D = V_{DD} - I_D R_D \]

the reducing reduction in \( I_D \) results in an increase in output voltage.

\[ V_{jg} \text{ JFET Common Gate Amplifier.} \]

\[ V_{jg} \text{ Small Signal Equivalent Circuit of Common gate.} \]

**Input Resistance \( (R_i) \):**

From the small signal equivalent circuit we can write:

\[ R_i = R_s \parallel R_i' \quad (1) \]

From the circuit diagram we can write:

\[ R_i' = \frac{V_i}{I} \quad (2) \]

The current through resistance \( R_D \) can be written as

\[ I_{rd} = I + g_m V_{gs} \]

\[ \therefore I = I_{rd} - g_m V_{gs} \quad (3) \]

From the circuit diagram we can write:

\[ I_{rd} = \frac{V_i - I R_D}{R_D} \quad (4) \]

Now substitute equation (4) in (3) we can write.
\[ I = \frac{V_i - I R_D}{Y_d} - g_m V_{gs} \]  \hspace{1cm} (5)

From the circuit we can write

\[ V_i = -V_{gs} \]

\[ I = \frac{V_i}{Y_d} - \frac{I R_D}{Y_d} + g_m V_i \]

\[ I + \frac{I R_D}{Y_d} = \frac{V_i}{Y_d} + g_m V_i \]

\[ I \left[ \frac{R_d + R_D}{Y_d} \right] = \frac{V_i}{Y_d} \left[ \frac{1 + g_m Y_d}{Y_d} \right] \]

\[ V_i = \frac{V_i}{Y_d} \left[ \frac{R_d + R_D}{Y_d} \right] \]

\[ I = \frac{V_i}{Y_d} \left[ \frac{R_d + R_D}{1 + g_m Y_d} \right] \]

\[ R_i = \frac{R_d + R_D}{1 + g_m Y_d} \]  \hspace{1cm} (6)

Substitute eqn (6) in eqn (5) we get

\[ R_i = R_{s \parallel} \left[ \frac{R_d + R_D}{1 + g_m Y_d} \right] \]  \hspace{1cm} (7)

\[ \frac{1}{R_d} \gg \frac{1}{R_D} \quad \text{and} \quad g_m Y_d \gg 1 \]

Then eqn (7) can be written as

\[ R_i = R_{s \parallel} \frac{1}{g_m} \]  \hspace{1cm} (8)

**Output Resistance (R_o):**

It is the output resistance of the circuit when input is short circuit.
As input is short circuited, $R_s$ is also short circuited and $V_{gs}$ become zero. Therefore we can write

$$R_0 = \frac{V_d}{I_D}$$  \hspace{1cm} (9)

when $V_d \gg R_D$ then

$$R_0 = R_D$$

Voltage Gain ($A_V$):

From the small signal equivalent circuit we can write:

$$V_o = -I_D R_D$$  \hspace{1cm} (10)

Apply KVL to the outer loop we can write:

$$V_i + (I_D - g_m V_{gs}) R_D + I_D R_D = 0$$

as $V_i = -V_{gs}$

$$V_i + I_D R_D + g_m V_i R_D + I_D R_D = 0$$

$$V_i \left[ 1 + g_m R_D \right] = -I_D \left[ R_D + R_D \right]$$

$$V_i = -\frac{I_D (R_D + R_D)}{\left[ 1 + g_m R_D \right]}$$  \hspace{1cm} (11)

divide eq (10) by (11) we can write:

$$A_V = \frac{V_o}{V_i} = \frac{-I_D R_D \left[ 1 + g_m R_D \right]}{I_D \left[ R_D + R_D \right]}$$

$$A_V = \frac{R_D \left[ 1 + g_m R_D \right]}{(R_D + R_D)}$$  \hspace{1cm} (12)
MOSFET AMPLIFIER:

Small Signal Parameters:

The time varying signal source generates a time varying component of the gate to source voltage.

The instantaneous gate to source voltage is given by

\[ V_{gs} = V_{gsa} + V_t = V_{gsa} + V_{gs} \quad \text{(1)} \]

where \( V_{gsa} \) is the dc component and \( V_{gs} \) is the ac component.

The instantaneous drain current is

\[ i_D = k(n)(V_{gs} - V_t) \quad \text{(2)} \]

Now substitute eqn (1) in (2) we get

\[ i_D = k(n)[(V_{gsa} + V_{gs}) - V_t] \]

\[ = k(n)[(V_{gsa} - V_t) + V_{gs}] \]

\[ = i_D = k(n)(V_{gsa} - V_t) + k(n)V_{gs} + (k(n)V_{gs})(V_{gsa} - V_t) \quad \text{(3)} \]

For a sinusoidal input signal, the squared term produces undesirable harmonics or non-linear distortion in the output voltage. To minimize these harmonics, we must have

\[ V_{gs} \ll k(n)(V_{gsa} - V_t) \quad \text{(4)} \]

The above condition represents the small signal condition that must be satisfied for linear amplification.
Neglecting the $V_{gs}$ term we can write above relation as

$$i_D = I_{DQ} + i_d$$ — (5)

where as

$$I_{DQ} = Kn (V_{sat} - V_T)^2$$ — (6)

$$i_d = 2Kn (V_{sat} - V_T)V_{gs}$$ — (6)

The small signal drain current is related to the small signal gate to source voltage by the transconductance $g_m$.

$$g_m = \frac{I_d}{V_{gs}} = \frac{2Kn (V_{sat} - V_T)V_{gs}}{V_{gs}}$$

$$g_m = 2Kn (V_{sat} - V_T)$$ — (7)

The transconductance is a ratio of output current to input voltage and hence it represents the gain of the MOSFET.

Small Signal Equivalent Circuit.

The small signal low frequency ac equivalent circuit for a n-channel MOSFET is shown in Fig.

The relation of $I_d$ by $V_{gs}$ is included as a current source $g_m V_{gs}$ connected from drain to source.

The input impedance is represented.
by the open-circuit as its input terminals, since
gate current \( I_g \) is zero.

we know that the circuit has the finite output
resistance of a MOSFET biased in the saturation region
because of the nonzero slope in the \( i_D \) versus \( V_{DS} \) curve.

we know that

\[
\begin{align*}
    i_D &= k_n \left[ (V_{GS} - V_T)^2 (1 + 2V_{DS}) \right] \quad \text{(8)}
\end{align*}
\]

where \( \lambda \) is the channel length modulation.

The small signal output resistance is given by

\[
    r_0 = \left[ \frac{dV_D}{dV_{DS}} \right]^{-1}
\]

Now differentiate equation (8) with \( V_{GS} \) constant.

\[
    r_0 = \left[ \lambda I_D \right]^{-1}
\]

The above equation shows that the small signal
output resistance is a function of \( Q \)-point parameters.
**Common Source Amplifier:**

The Common Source circuit with voltage divider biasing and coupling capacitors. The MOSFET is biased near the middle of the saturation region by $R_1$ and $R_2$, resistors to work as an amplifier.

The signal frequency is sufficiently large for the coupling capacitors to act essentially as a short circuit. The resistance $R_{si}$ is the source resistance of the signal voltage source $V_i$.

![Circuit Diagram]

- **Input Resistance:** $R_i$ from the small signal equivalent circuit can be written as $R_i = R_{ii} \cdot R_2$.
- **Output Resistance:** $R_o = R_{D} \cdot R_o$.
- **Voltage Gain:** $A_V = \frac{V_o}{V_i}$

The output voltage can be written as $V_o = -g_m \cdot Vgs \cdot (\frac{R_i}{R_2})$. 
Using voltage divider rule, the input gate to source voltage is written as

\[
V_{gs} = \left[ \frac{R_i}{R_i + R_{si}} \right] V_i \quad \text{(4)}
\]

Now substitute equation (4) in (3) we get,

\[
V_o = -g_m \left[ \frac{R_i}{R_i + R_{si}} \right] V_i \left( R_{01}R_D \right)
\]

\[
A_v = \frac{V_o}{V_i} = -g_m \left( R_{01}R_D \right) \left[ \frac{R_i}{R_i + R_{si}} \right] \quad \text{(5)}
\]

Since \( R_{si} \) is not zero, the amplifier input signal \( V_{gs} \) is less than the signal voltage. This is known as loading effect. It reduces the voltage gain of the amplifier.

**Common Source Amplifier with Source Resistance:**

The common source amplifier with source resistance is shown below. The source resistance is introduced to stabilize the Q-point against variation in the MOSFET parameter.
From the small signal equivalent circuit we can write:

\[ V_o = -g_m V_{gs} R_D \quad \text{(6)} \]

Apply KVL between input to gate-source loop we can write:

\[ V_i = V_{gs} + g_m V_{gs} R_S \]

\[ V_i = V_{gs} \left[ 1 + g_m R_S \right] \quad \text{(8)} \]

\[ V_i = \frac{V_i}{g_m R_S} \quad \text{(8)} \]

Substitute equation (8) in (6) we can write:

\[ V_o = \frac{-g_m V_i R_D}{1 + g_m R_S} \]

\[ A_v = \frac{V_o}{V_i} = -g_m R_D \frac{1}{1 + g_m R_S} \quad \text{(10)} \]

Common Source Circuit with source bypass capacitor:

A source bypass capacitor connected across the source resistance in the common-source circuit will minimize the loss in the small signal voltage gain while maintaining Q-point stability.

We can further increase the Q-point stability replacing the source resistor with a constant current source.
From the small signal equivalent circuits, we can write:

**Input Resistance** \( R_i \):

\[ R_i = R_G \]

**Output Resistance** \( R_o \):

\[ R_o = R_D \]

**Voltage Gain** \( \Delta \):

The output voltage can be written as

\[ V_o = -g_m V_{gs} R_D \]

From the small signal equivalent circuit,

\[ V_i = V_{gs} \]

\[ V_o = -g_m V_i R_D \]

\[ \Delta V = \frac{V_o}{V_i} = -g_m R_D \]
MOSFET Source Follower Amplifier:

In source follower amplifier circuit, output is taken from the source with respect to ground, and drain is connected directly to VDD. The small signal equivalent circuit of source follower is shown below.

\[ V_{GS} = V_{GS0} - \frac{V_{DS}}{g_m} \]

Input Resistance \((R_i)\):

\[ R_i = R_1 || R_2 \]

Output resistance \((R_o)\):

To calculate the output resistance, we set all independent small signal source equal to zero by shorting them and apply the test voltage to output terminals and
measure the best current.

Apply KCL to the op node we can write:

\[ I_x = \frac{V_x}{R_o} + \frac{V_x}{R_s} - 9mVgs \quad \cdots \quad 2 \]

Since input current is zero we have

\[ Vgs = -V_x \quad \cdots \quad 3 \]

\[ I_x = \frac{V_x}{R_o} + \frac{V_x}{R_s} + 9mV_x \]

\[ V_x = \left[ \frac{1}{R_o} + \frac{1}{R_s} + 9m \right] \]

\[ R_o = \frac{V_x}{I_x} = \frac{\left[ \frac{1}{R_o} + \frac{1}{R_s} + 9m \right]}{1} \quad \cdots \quad 4 \]

Voltage Gain \((A_v)\):

From the small signal equivalent circuit the output voltage can be written as

\[ V_o = 9mVgs \left( \frac{R_o}{R_s} \right) \quad \cdots \quad 5 \]

Apply KVL to the output loop:

\[ V_{in} = Vgs + V_o \quad \cdots \quad 6 \]

Substitute eqn \((5)\) in \((6)\) we get

\[ V_{in} = Vgs + 9mVgs \left( \frac{R_o}{R_s} \right) \]

\[ V_{in} = Vgs \left[ 1 + 9m \left( \frac{R_o}{R_s} \right) \right] \]

\[ Vgs = \frac{V_{in}}{\left[ 1 + 9m \left( \frac{R_o}{R_s} \right) \right]} \quad \cdots \quad 7 \]
Apply voltage divider rule at input
\[ V_{in} = \left[ \frac{R_i}{R_i + R_s} \right] V_i \]  \( \quad \text{Eq. 8} \)

Now substitute Eq. 8 in Eq. 4 we get,
\[ V_{gs} = \frac{1}{1 + g_m (r_{o1} R_s)} \left[ \frac{R_i}{R_i + R_s} \right] V_{in} \]  \( \quad \text{Eq. 9} \)

Substitute equation 9 in Eq. 5 we can write
\[ V_o = \frac{g_m (r_{o1} R_s)}{1 + g_m (r_{o1} R_s)} \left[ \frac{R_i}{R_i + R_s} \right] V_{in} \]  \( \quad \text{Eq. 10} \)

**MOSFET Common Gate Amplifier:**

The circuit diagram of a common gate amplifier circuit is shown below. Here, a constant current source \( I_o \) is used to bias the MOSFET. The resistor \( R_o \) at the gate prevents the build-up of a static charge on the gate terminals and the bypass capacitor \( C_o \) ensures that the gate is at signal ground.

**Small Signal Equivalent Circuit:**
The coupling capacitor \( C_1 \) couples the signal to the source terminal and coupling capacitor \( C_2 \) couples the output voltage to the load resistor \( R_L \).

Input resistance \( (R_i) \):

From the small signal equivalent circuit we can write:

\[
R_i = \frac{-V_{gs}}{I_i} \quad \text{--- (1)}
\]

where \( I_i = -g_m V_{gs} \) (both are in opposite directions).

\[
R_i = \frac{-V_{gs}}{-g_m V_{gs}} = \frac{1}{g_m} \quad \text{--- (2)}
\]

Output resistance \( (R_o) \):

When input source voltage is zero, then the output resistance looking back from the load resistance is given by:

\[
R_o = R_D \quad \text{--- (3)}
\]

Voltage Gain \( (A_v) \):

The output voltage \( V_o \) can be written as:

\[
V_o = -g_m V_{gs} (R_D || R_L) \quad \text{--- (4)}
\]

Apply KVL to input side we can write:

\[
V_i = I_i R_s + V_{gs} \quad \text{--- (5)}
\]

Substitute \( I_i \) in eqn \( \text{(5)} \):

\[
V_i = -g_m V_{gs} R_s + V_{gs}
\]

\[
= -V_{gs} \left[ g_m R_s + 1 \right]
\]
\[ V_{gs} = \frac{-V_i}{1 + g_m R_s i} \]  

Substitute \( V_{gs} \) in equ (4) we get:

\[ V_o = -g_m \left[ \frac{-V_i}{1 + g_m R_s i} \right] (R_{D1} || R_L) \]

\[ A_v = \frac{V_o}{V_i} = \frac{g_m (R_{D1} || R_L)}{1 + g_m R_s i} \]  

**Current gain \( (A_i) \):**

The signal input to the common gate amplifier may be current.

Apply current divider rule at the node A we have:

\[ I_o = (-g_m V_{gs}) \left[ \frac{R_D}{R_D + R_L} \right] \]

Apply KCL at node A we have:

\[ I_c + X_{gs} = I_i = -\frac{V_{gs}}{R_s} - g_m V_{gs} \]

\[ I_i = -\frac{V_{gs}}{R_s} \left[ \frac{1 + g_m R_s i}{R_s} \right] \]

\[ V_{gs} = -\frac{I_i R_s}{1 + g_m R_s i} \]

Now substitute equ (9) in (8) we get:

\[ I_o = (-g_m) \left( -\frac{I_i R_s}{1 + g_m R_s i} \right) \left( \frac{R_D}{R_D + R_L} \right) \]

\[ A_i = \frac{I_o}{I_i} = \frac{g_m R_s i}{1 + g_m R_s i} \left( \frac{R_D}{R_D + R_L} \right) \]
Basic FET Differential Pair:

DC Transfer Characteristics:

The basic MOSFET differential pair with matched transistors $M_1$ and $M_2$ biased with a constant current $I_D$ is shown below. We assume that $M_1$ and $M_2$ are always biased in the saturation region.

Like the basic bipolar configuration, the basic MOSFET diff amp uses both positive and negative bias voltages, thereby eliminating the need for coupling capacitors and voltage divider biasing resistors at the gate terminal. Even with $V_{GS1} = V_{GS2} = 0$, the transistors $M_1$ and $M_2$ can be biased in the saturation region by the current source $I_D$. This circuit is also called dc-coupled diff amp.

The dc transfer characteristics of the MOSFET differential pair can be determined from the circuit above. Neglecting the output resistances of $M_1$ and $M_2$ and assuming the two transistors are matched, so we can write:

$$I_{D1} = k_n (V_{GS1} - V_{TH})^2$$  \hspace{1cm} (1)

$$I_{D2} = k_n (V_{GS2} - V_{TH})^2$$  \hspace{1cm} (2)

Taking square root of above equation 1 and 2 and then subtracting equation 2 from 1 we get:
\[ \sqrt{I_{D1}} - \sqrt{I_{D2}} = \sqrt{k_n} (V_{G_{S1}} - V_{G_{S2}}) = \sqrt{k_n} V_d \quad \text{--- (3)} \]

where \( V_d = V_{G_{S1}} - V_{G_{S2}} \) is the differential-mode input voltage.

If \( V_d > 0 \) then \( V_{G_{S1}} > V_{G_{S2}} \), which implies that \( I_{D1} > I_{D2} \) where as

\[ I_{D2} = I_{D1} + I_{D2} \quad \text{--- (4)} \]

From eqn (4) we can write \( I_{D2} = I_{D1} - I_{D1} \) substitute \( I_{D2} \) in eqn (3) we get

\[ \sqrt{I_{D1}} - \sqrt{I_{D1}} = \sqrt{k_n} V_d \quad \text{--- (5)} \]

Taking square on both sides we get

\[ \left[ \sqrt{I_{D1}} - \sqrt{I_{D1}} \right]^2 = k_n V_d^2 \]

\[ I_{D1} + (I_{D1} - I_{D1}) - 2 \sqrt{I_{D1} (I_{D1} - I_{D1})} = k_n V_d^2 \]

\[ I_{D1} - 2 \sqrt{I_{D1} (I_{D1} - I_{D1})} = k_n V_d^2 \]

Re-arranging the above equation we get

\[ \frac{1}{2} \left[ I_{D1} - k_n V_d^2 \right] \]

Taking square on both sides we get

\[ I_{D1} \left[ I_{D1} - I_{D1} \right] = \frac{1}{4} \left[ I_{D1} - k_n V_d^2 \right]^2 \]

Re-arranging the above equation we get

\[ I_{D1}^2 - I_{D1}^2 + \frac{1}{4} \left[ I_{D1} - k_n V_d^2 \right]^2 = 0 \quad \text{--- (7)} \]
Applying the quadratic formula, rearranging terms, and
noting that $I_{D1} > I_Q/2$, and $V_d > 0$ we obtain
from eq (7)
\[
I_{D1} = 
\frac{I_Q}{2} + \sqrt{\frac{k_n I_Q}{2}} \cdot V_d \sqrt{1 - \left(\frac{k_n}{2I_Q}\right)V_d^2}
\]

using equation (4) we can write,
\[
I_{D2} = 
\frac{I_Q}{2} - \sqrt{\frac{k_n I_Q}{2}} \cdot V_d \sqrt{1 - \left(\frac{k_n}{2I_Q}\right)V_d^2}
\]

from eq (8) and (9) we can write,
\[
\frac{I_{D1}}{I_Q} = \frac{1}{2} + \sqrt{\frac{k_n}{2I_Q}} \cdot V_d \sqrt{1 - \left(\frac{k_n}{2I_Q}\right)V_d^2}
\]
and
\[
\frac{I_{D2}}{I_Q} = \frac{1}{2} - \sqrt{\frac{k_n}{2I_Q}} \cdot V_d \sqrt{1 - \left(\frac{k_n}{2I_Q}\right)V_d^2}
\]
The above equations (10) & 11) describe the dc transfer
characteristic for this circuit. They are plotted in below
figure as a function of a normalized differential input
voltage, $V_d/\sqrt{2I_Q k_n}$

From equation (10) and (11) we see at a specific differential input
voltage, bias current $I_Q$ is switched entirely to one transistor
or the other. This occurs when
\[
|V_d|_{\text{max}} = \sqrt{\frac{I_Q}{k_n}}
\]
The forward transconductance is defined as the slope
of the dc transfer characteristic for $I_{D1}$ curve.
From the $\frac{d}{dV_d} \ln dip$ equation, we see that maximum forward transconductance occurs at $V_d = 0$.

\[ g_f(\text{max}) = \frac{d}{dV_d} \ln dip \mid V_d = 0. \]

Differentiating Eq. (3) with respect to $V_d$, we get

\[ g_f(\text{max}) = \sqrt{\frac{k_n I_a}{2}} = \frac{g_m}{2} \tag{3} \]

where $g_m$ is the transconductance of each transistor.

From the ac equivalent circuit of the diff amp configuration, showing only the differential voltage and signal current as a function of transistor transconductance $g_m$. The one-sided output voltage at $V_{oa}$ is given by

\[ V_{oa} = V_o = \left( \frac{g_m V_d}{2} \right) R_D \tag{14} \]

The differential voltage gain is then

\[ A_v = \frac{V_o}{V_d} = \frac{g_m R_D}{2} = \sqrt{\frac{k_n I_a}{2}} R_D \tag{15} \]

Small Signal Equivalent Circuit Analysis:

The small signal equivalent circuit of the MOSFET we assume for the differential pair configuration is shown in Fig. 14. Transistors are matched with $\lambda = 0$ for each transistor, and the constant-current source is represented by a finite output resistance $R_o$. All voltages are represented by their phasor components.
Apply KCL at $V_S$ we get

$$g_m V_{gs1} + g_m V_{gs2} = \frac{V_S}{R_0} \quad \text{(16)}.$$  

From the circuit we can write

$$V_{gs1} = V_i - V_S \quad \text{and} \quad (17a)$$
$$V_{gs2} = V_i - V_S \quad \text{and} \quad (17b)$$

Substitute equ. (17a) and (b) in equ. (16) we get

$$g_m (V_i - V_S) + g_m (V_i - V_S) = \frac{V_S}{R_0} \quad \text{(18)}$$

Re-arrange equ. (18) we get to obtain ($V_S$)

$$g_m (V_i - V_S) + g_m (V_i - V_S) = \frac{V_S}{R_0}$$

$$g_m (V_i + V_S) = \frac{V_S}{R_0} + 2g_m V_S$$

$$g_m (V_i + V_S) = V_S \left[ \frac{1}{R_0} + 2g_m \right] \quad \text{(19)}$$

$$V_i + V_S = \frac{V_S}{R_0} \left[ \frac{1}{g_m R_0} + 2 \right]$$

$$V_S = \frac{(V_i + V_S)}{2 + \frac{1}{g_m R_0}} \quad \text{(19)}$$

For a one-sided output at the drain of $M_2$, $V_D$,

$$V_o = V_D = -g_m V_{gs2} R_D \quad \text{(20)}$$

Substitute equ. (17b) in equ. (20) we get

$$V_o = -g_m (V_i - V_S) R_D \quad \text{(21)}$$
Substitute equation (3) in (20) we get:

\[ V_0 = -g_m R_D \left[ V_a - \left( \frac{V_1 + V_2}{2 + \frac{1}{g_m R_D}} \right) \right] \]

\[ = -g_m R_D \left[ \frac{V_a (2 + \frac{1}{g_m R_D}) - V_1 - V_2}{2 + \frac{1}{g_m R_D}} \right] \]

\[ V_0 = -g_m R_D \left[ \frac{V_a (1 + \frac{1}{g_m R_D}) - V_1}{2 + \frac{1}{g_m R_D}} \right] \] \quad \text{(22)}

Based on the relationship between the input voltages \( V_1 \) and \( V_2 \) and the differential and common mode voltages, we can write:

\[ V_1 = V_{cm} + \frac{V_a}{2} \quad , \quad V_2 = V_{cm} - \frac{V_a}{2} \] \quad \text{(23)}

Substitute equation (23) in \( V_1 \) and \( V_2 \) in equation (22) we get:

\[ V_0 = -g_m R_D \left[ \frac{(V_{cm} - \frac{V_a}{2}) (1 + \frac{1}{g_m R_D}) - (V_{cm} + \frac{V_a}{2})}{2 + \frac{1}{g_m R_D}} \right] \]

\[ = -g_m R_D \left[ \frac{V_{cm} + V_{cm} - \frac{V_a}{2} - \frac{V_a}{2} - \frac{V_a}{2g_m R_D} - V_{cm} - \frac{V_a}{2}}{(2 + \frac{1}{g_m R_D})} \right] \]
\[ V_o = -g_m R_D \left[ \frac{V_{cm}}{g_m R_o} - V_d (1 + \frac{1}{g_m R_o}) \right] \]

\[ = -g_m R_D \left( \frac{V_{cm}}{g_m R_o} \right) \times \frac{g_m R_o}{(2g_m R_o + 1)} + g_m R_D V_d \left( \frac{g_m R_o}{(2g_m R_o + 1)} \right) \]

\[ V_o = \frac{1}{2} g_m R_D V_d - g_m R_D \frac{V_{cm}}{(2g_m R_o + 1)} \]

The output voltage in general form is

\[ V_o = A_d V_d + A_{cm} V_{cm} \]

Compare equ. 24 and 25, we can write

\[ A_d = \frac{1}{2} g_m R_D \] \[ A_{cm} = -\frac{g_m R_D}{(1 + 2g_m R_o)} \]

The transconductance \( g_m \) of the Mosfet is

\[ g_m = 2 \sqrt{K_n I_{Da}} \] \[ \text{where } I_{Da} = \frac{I_a}{2} \]

Substitute \( g_m \) in \( A_d \) and \( A_{cm} \)

\[ A_d = \frac{1}{2} \left( \sqrt{2K_n I_a} \right) R_D \]

\[ A_{cm} = \frac{-\left( \sqrt{2K_n I_a} \right) R_D}{1 + \frac{g_m}{2} \left( \sqrt{2K_n I_a} \right) R_o} \]

From the above solution for an ideal current source, the common mode gain is zero since \( R_o = \infty \)

\[ \text{Common Mode Rejection Ratio (CMRR)} = \left| \frac{A_d}{A_{cm}} \right| \]

\[ \text{CMRR} = \left| \frac{1}{2} \left( \sqrt{2K_n I_a} \right) R_D \times \frac{1 + \frac{g_m}{2} \left( \sqrt{2K_n I_a} \right) R_D}{\sqrt{2K_n I_a} R_o} \right| \]
The basic JFET differential pair biased with a constant current source is shown in Fig. If a pure differential mode input signal is applied such that \( V_{01} = \frac{V_d}{2} \) and \( V_{02} = -\frac{V_d}{2} \), then drain currents \( I_{D1} \) and \( I_{D2} \) increase and decrease in the same way as in the NOSFET differential amplifier.

We can determine the differential-mode voltage gain by analyzing the small-signal equivalent circuit from the small-signal equivalent circuit when the current source output resistance is infinite. Then apply KCL we get:

\[
CMRR = \frac{1}{2} \left[ 1 + 2 \sqrt{\frac{2K_n I_D}{R_o}} \right]
\]
\[ g_m V_{gs1} + g_m V_{gs2} = 0 \quad \cdots \quad (1) \]

From the above equation we can write:

\[ g_m V_{gs1} = -g_m V_{gs2} \]
\[ V_{gs1} = -V_{gs2} \]

The differential mode input voltage is:

\[ V_d = V_i - V_o = V_{gs1} - V_{gs2} = -V_{gs2} - V_{gs2} = -2V_{gs2} \]

A one-sided output at \( V_{oa} \) is given by:

\[ V_{oa} = -g_m V_{gs2} R_D = -g_m \left( \frac{V_d}{2} \right) R_D \]
\[ V_{oa} = \frac{g_m V_d R_D}{2} \]

ie. \[ A_d = \frac{V_{oa}}{V_d} = \frac{g_m R_D}{2} \]

The expression for the differential mode voltage gain of the JFET differential amplifier is exactly the same as that of the MOSFET differential amplifier.
The bipolar junction transistors have a large transconductance than MOS transistors biased at the same current level and they have higher switching speed. Due to large transconductance they provide larger voltage gains.

On the other hand, MOS transistors have an essential infinite input impedance at low frequencies and have very high packaging density. Due to almost infinite input impedance, MOS transistors have zero input bias current.

The advantages of these two technologies can be utilized by combining bipolar and MOS transistors on the same substrate i.e. in the same integrated circuit. Such technology is known as BiCMOS technologies.

Basic Amplifier stages

The circuit shown below is a modified Darlington pair configuration. It uses the bias current $I_{bias}$ or some equivalent element to control the quiescent current in transistor Q1. The effective current gain of bipolar transistor is boosted in this circuit.

![Bipolar Darlington Pair Configuration](image)
The advantages of Bimeta technologies are:

(i) An infinite input resistance

(ii) A large transconductance due to the bipolar transistor.

Circuit Analysis:

Let us consider $r_0 = \infty$ in both transistors.

From the small signal, we can write output signal current as:

$$I_o = g_m V_{gs} + g_m a V_x$$ \hspace{1cm} (1)

Similarly,

$$V_i = V_{gs} + V_x$$ \hspace{1cm} (2)

where $a = \frac{V_x}{g_m V_{gs} r_x}$

$$V_{gs} = \frac{V_x}{g_m r_x}$$ \hspace{1cm} (3)

Substitute $V_x$ in equ (2) we get:

$$V_i = V_{gs} + g_m V_{gs} r_x$$

$$= V_{gs} [1 + g_m r_x]$$ \hspace{1cm} (4)

Similarly, substitute $V_x$ in equ (1) we get:

$$I_o = g_m V_{gs} + g_m a g_m V_{gs} r_x$$

$$I_o = g_m V_{gs} [1 + g_m a r_x]$$ \hspace{1cm} (5)

Substitute equ (4) in (5) we get:

$$I_o = \frac{g_m V_i [1 + g_m a r_x]}{[1 + g_m r_x]}$$
where $g_m$ is the composite transconductance. The $g_mA$ or the bipolar transistor is usually at least an order of magnitude greater than $g_m$ of the MOSFET.

**Bipolar Differential Amplifier:**

The basic bipolar differential amplifier with a constant current source bias and a bipolar active load.

The advantages of bipolar differential amplifier are:

* Infinite input resistance
* The zero input bias current.

The disadvantage of this circuit is, since MOSFET is used in the input stage the offset voltage is relatively high compared to that of a bipolar input circuit. The offset voltages are generated because of the mismatching of differential pair input transistor.

**Bipolar Inverter:**

The bipolar circuit consists of two bipolar transistors ($T_3$ and $T_4$). $V_{in}$.

One NMOS and one PMOS transistor (both enhancement type devices, off at $V_{in} = 0 V$).

**Bipolar Inverter:**
when \( V_{in} = 0 \):

- \( T_1 \) is off therefore \( T_3 \) is non-conducting.
- \( T_2 \) is on and supplies current to the base of \( T_4 \).
- \( T_4 \) base voltage is set to \( V_{dd} \).
- \( T_4 \) conducts and acts as a current source to charge the load \( C_L \) towards \( V_{dd} \). \( V_{out} \) rises to \( V_{dd} - V_{be} \) of \( T_4 \).

\( V_{be} \) is the base-emitter voltage of \( T_4 \). It is important to note that as the output approaches \( 8V - V_{be} \) of \( T_4 \), \( T_4 \) begins to turn off.

when \( V_{in} = V_{dd} \):

- \( T_2 \) is off therefore \( T_4 \) is non-conducting.
- \( T_1 \) is on and supplies current to the base of \( T_3 \).
- \( T_3 \) conducts and acts as a current sink to discharge the load \( C_L \) towards \( 0V \). \( V_{out} \) falls to \( 0V + V_{ce(sat)} \) of \( T_3 \).

The \( V_{ce(sat)} \) of \( T_3 \) is the saturation voltage from \( T_3 \) collector to emitter.

The \( T_3 \) and \( T_4 \) present low impedance when turned on into saturation and load \( C_L \) will be charged or discharged rapidly.

The output logic level will be good and will be close to \( 0 \) \& \( V_{dd} \) voltages since \( V_{ce(sat)} \) is quite small and \( V_{be} = 0.7V \). Therefore inverter has high noise margins.

The inverter has high input impedance and low output impedance.
For the circuit shown below the MOSFET parameters are \( V_T = 1.5 \) V, \( k_n = 0.8 \) mA/V\(^2 \) and \( \lambda = 0.01 \) V\(^{-1} \). Determine the small signal voltage gain \( R_i \) and \( R_o \).

**Solution:**

DC analysis:

\[
V_{GSQ} = \left[ \frac{R_D}{R_1 + R_2} \right] V_{DD}
\]

\[
= \left[ \frac{3 \times 10^3}{(8 \times 10^3 + 30 \times 10^3)} \right] (10) = 2.678 \text{ V}
\]

\[
I_{DSQ} = k_n \left[ V_{GSQ} - V_T \right] = 0.8 \times 10^{-3} \left[ 2.678 - 1.5 \right] = 1.11 \text{ mA}
\]

Apply KVL to output side and rearrange we get:

\[
V_{DSQ} = V_{DD} - I_{DSQ} \times R_D = 10 - \left[ 1.11 \times 10^{-3} \times 5 \times 10^3 \right] = 4.45
\]

Since \( V_{DSQ} > V_{GSQ} - V_T \) the MOSFET is biased in the saturation region.

Transconductance \( g_m \) is:

\[
g_m = 2k_n \left[ V_{GSQ} - V_T \right] = 2 \times 0.8 \times 10^{-3} \left[ 2.678 - 1.5 \right] = 1.88 \text{ mA/V}
\]

\[
\frac{1}{g_m} = \left[ \frac{1}{2 \times 0.8 \times 10^{-3} \times 5 \times 10^3} \right] = 90 \Omega
\]

\[
R_i = R_{11} R_D = 8 \Omega \times 11 \Omega = 88 \Omega \approx 90 \Omega
\]

\[
R_o = \frac{1}{\lambda} = \frac{1}{0.01 \times 1.11 \times 10^{-3}} = 90 \Omega
\]
\[ R_0 = R_{D1} V_0 = 5 \, k\Omega \, 11 \, 90 \, k\Omega = 4.737 \, k\Omega \]

\[ A_V = -g_m \left( \frac{R_C}{R_C + R_S} \right) \]

\[ = -1.88 \times 10^{-3} \left( 5 \, k\Omega \, 90 \, k\Omega \right) \left[ \frac{21.96 \, k}{21.96 \, k + 4 \, k} \right] \]

\[ A_V = -7.55 \]

For a NMOS common gate amplifier circuit: \( I_D = 2 \, mA \), \( R_S = 50 \, k\Omega \), \( V_{DD} = 5 \, V \), \( V_{SS} = -5 \, V \), \( R_G = 200 \, k\Omega \), \( R_D = 4.7 \, k\Omega \), and \( R_L = 10 \, k\Omega \). Calculate the output voltage with input current is \( 180 \sin(\omega t) \) and \( \lambda = 0 \).

**Solution:**

\[ I_{DEA} = K_n \left[ V_{GSQ} - V_{TN} \right] \]

Solve for it and find \( V_{GSQ} \).

\[ V_{GSQ} = \sqrt{\frac{I_{DEA}}{K_n}} + V_{TN} = \sqrt{\frac{2 \times 10^{-3}}{8 \times 10^{-3}}} + 1 \]

\[ V_{GSQ} = 2 \, V \]

\[ g_m = \frac{20}{K_n} \left[ V_{GSQ} - V_{TN} \right] \]

\[ g_m = 2 \times 2 \times 10^{-3} \left[ 2 - 1 \right] = 4 \, mA/V \]

\[ I_0 = \frac{I_C \left[ \frac{g_m R_S}{1 + g_m R_S} \right]}{R_D + R_L} \]

\[ V_0 = I_0 R_L \]
\[ V_0 = 0.382 \sin \omega t \ V \]

For the circuit shown in \( V^V \) calculate \( R_i \), \( A_v \) and \( R_0 \). The Norspot parameters are \( V_{TN} = 1.5 \text{ V} \), \( k_n = 8 \text{ mA/V}^2 \) and \( \lambda = 0.01 \text{ V} \).

Assume \( I_{DA} = 8 \text{ mA} \) and \( V_{GS\text{a}} = 2.5 \text{ V} \).

\[ R_i = R_1 \frac{1}{R_2} = 180 \times 10^{-3} \frac{1}{1470 \times 10^{-3}} \]

\[ R_i = 130.15 \text{ k}\Omega \]

\[ g_m = 2k_n \left[ V_{GS\text{a}} - V_{TN} \right] = 2 \times 8 \times 10^{-3} \left[ 2.5 - 1.5 \right] \]

\[ g_m = 16 \text{ mA/V} \]

\[ R_0 = \left[ \frac{1}{\lambda I_{DA}} \right] = \left[ \frac{1}{0.01 \times 8 \times 10^{-3}} \right]^{-1} = 125 \text{ k}\Omega \]

\[ A_v = \frac{g_m \left( R_s + r_o \right)}{1 + g_m \left( R_s + r_o \right)} \frac{R_i}{R_i + R_s} \]

\[ = \frac{16 \times 10^{-3} \left( 1 \times 10^{-3} \| 12.5 \times 10^{-3} \right)}{1 + 16 \times 10^{-3} \left( 1 \times 10^{-3} \| 12.5 \times 10^{-3} \right)} \left[ \frac{130 \times 10^3}{130 \times 10^3 + 12 \times 10^3} \right] \]

\[ = 4.7 \times 10^3 \]
\[ A_v = 0.92 \]

\[ R_0 = \frac{1}{11 R_o \parallel R_s} \]

\[ = \frac{1}{11 \times \frac{1}{2.9 \times 10^{-3}} \parallel 1 \times 10^{-3}} \]

\[ R_0 = 58.55 \Omega. \]

For the common drain amplifier as shown in Fig. \( g \). \( g_m = 3.5 \)

\[ r_d = 5k \Omega \]. Calculate \( z_0 \), \( z_0 \), and \( A_v \).

**Sol:**

\[ z_i = R_G = 1 \text{M} \Omega \]

\[ z_o = \frac{1}{g_m} R_s \parallel r_d \]

\[ = \frac{1}{2.9 \times 10^{-3} \parallel 3.3 \times 10^{-3} \parallel 2.5 \times 10^{-3}} \]

\[ z_o = 351.7 \Omega \]

\[ A_v = \frac{g_m (r_d \parallel R_s)}{1 + g_m (r_d \parallel R_s)} \]

\[ = \frac{2.5 \times 10^{-3}}{1 + 2.5 \times 10^{-3} (2.5 \times 10^{-3} \parallel 3.3 \times 10^{-3})} \]

\[ A_v = 0.819 \]

For common gate amplifier as shown in Fig. where \( g_m = 2.8 \text{MS} \), \( r_d = 50 \text{k} \Omega \). Calculate \( R_i, R_o \) and \( A_v \).
Solution:

\[ R_i = R_s \frac{V_D + R_D}{1 + g_m V_d} \]

\[ = 1 \times 10^3 \frac{V_D + 5.1 \times 10^3}{1 + 2.8 \times 10^{-3} \times 50 \times 10^3} \]

\[ R_i = 2.8 \Omega \]

\[ R_o = \frac{V_D}{1 + R_D} \]

\[ = 50 \times 10^{-3} \frac{5.1 \times 10^3}{1 + 2.8 \times 10^{-3} \times 50 \times 10^3} \]

\[ R_o = 4.63 \times 10^{-3} \]

\[ A_v = \frac{R_D (1 + g_m V_d)}{V_D + R_D} \]

\[ = 5.1 \times 10^3 \frac{1 + 2.8 \times 10^{-3} \times 50 \times 10^3}{50 \times 10^3 + 5.1 \times 10^3} \]

\[ A_v = 13.05 \]

For the amplifier shown in \( V^0 \). Calculate:

\( A_v, R_i \) and \( R_o \), also \( R_o' \) assume a JFET

with \( g_m = \text{amp/mV}, V_d = 10 \text{ KV} \).

\[ \text{Sol.:} \]

\[ A_v = \frac{-g_m R_L}{1 + g_m R_s + R_s + R_i} \]

\[ V_D \]

\[ 50 \text{ kV} \]

\[ g_m \]

\[ 1 \text{ M\Omega} \]

\[ 1 \text{ k} \]

\[ 50 \text{ kV} \]
where \[ R_L = 5 \times 10^{-3} \Omega \]
\[ \frac{1}{R_L} = 2 \times 10^{-8} \Omega. \]

and \[ A_V = \frac{2 \times 10^{-3} \times 2 \times 10^{-3}}{1 + (2 \times 10^{-3} \times 1 \times 10^{-3}) + (1 \times 10^{-3} + 2 \times 10^{-3})} \]
\[ A_V = -8.928 \]

Input resistance \[ R_i = R_G = 1 \text{M} \Omega \]

Output resistance \[ R_o = \left[ \frac{1}{R_d + 9m \cdot 8 \cdot R_d + R_s} \right] R_D \]
\[ = \frac{10 \times 10^3 + (2 \times 10^{-3} \times 1 \times 10^3 \times 10^3) + 1 \times 10^3}{1 \times 10^3} \text{M} \Omega \]
\[ R_o = 19.13 \times 10^3 \Omega, \]
\[ R_o^1 = R_0 \cdot R_L \]
\[ = 19.13 \times 10^3 \text{M} \Omega \]
\[ R_o^1 = 13.83 \times 10^3 \Omega. \]

Calculate the transconductance \( g_m \) of a MOSFET having following parameters. \( V_T = 1 \text{V} \), \( \frac{1}{A} \mu \text{m} \cdot \text{Cox} = 30 \text{mA/V}^2 \) and \( W/L = 50 \).

Assume the drain current \( I_D = 1.2 \text{mA} \).

Solution:

where \[ k_n = \left[ \frac{1}{A} \mu \text{m} \cdot \text{Cox} \right] \left[ \frac{W}{L} \right] \]
\[ = 3 \times 10^{-6} \text{mA} \cdot \text{V} \times 50 = 1.5 \text{mA} \cdot \text{V}. \]

\[ g_m = 2 \sqrt{k_n I_D} \]
\[ = 2 \sqrt{1.5 \times 10^{-3} \times 1.2 \times 10^{-3}} \]
\[ g_m = 2.68 \text{mA/V}. \]
UNIT-4: FREQUENCY RESPONSE OF AMPLIFIERS

**Topics:**
- Amplifier frequency response
- Frequency response of transistor amplifiers with circuit capacitors
- BJT Frequency Response
- Short circuit current gain
- cut-off frequency - f", f", & unity gain bandwidth
- Miller effect
- Frequency response of FET
- High frequency analysis of CE & HOSFET CS amplifier
- Transistor switching times

AMPLIFIER FREQUENCY RESPONSE: \( A_U(bm) \)

The response of any stage or multistage network is highly influenced by the frequency of the applied signal. At low frequency, the effect of coupling and bypass capacitors cannot be neglected due to their high value of capacitive reactance under certain conditions.

Any fluctuations in the number of stages of a cascaded system will also affect the frequency response of the system.

A general frequency response curve is shown as below:
Frequency response curve can be splitted into three regions:

- **Low frequency region**
- **Mid frequency region**
- **High frequency region**

The frequency response curve is a plot between the magnitude of gain and logarithmic frequencies. The main reason for the drop in gain at the low frequency region and the high frequency region is due to the increase in the capacitive reactance in the low frequency region and due to the parasitic capacitive elements on frequency dependence of the network gain on the active devices in the high frequency region.
Frequency boundaries of high gain region is determined by choosing \( \frac{1}{\sqrt{3}} \text{Av(mid)} \) to be the gain at cut-off level.

The frequencies corresponding to such values \( (f_1 \& f_2) \) are called cut-off frequencies or band frequencies or half power frequencies.

At cut-off frequencies, the output power is half the mid-band power output:

\[
P_{\text{out(mid)}} = \left| \frac{V_{\text{out}}}{V_{\text{in}}} \right|^2
\]

but, \( \text{Av(mid)} = \left| \frac{V_{\text{out}}}{V_{\text{in}}} \right| \)

\[
\therefore P_{\text{out(mid)}} = \frac{\text{Av(mid)} V_{\text{in}}^2}{R_0}
\]

At half power frequencies, \( f_1 \& f_2 \)

\[
P_{\text{out (HPF)}} = 10 \cdot 70.7 \frac{\text{Av(mid)} V_{\text{in}}^2}{R_0} = 0.5 \frac{\text{Av(mid)} V_{\text{in}}^2}{R_0}
\]

\[
P_{\text{out (HPF)}} = 0.5 P_{\text{out(mid)}}
\]

Bandwidth, \( = f_2 - f_1 \)

In most applications, normalised plot is used.

A normalised plot is a plot of gain vs log frequencies with the gain values divided by the gain in the mid-frequency range (i.e., maximum gain)

\[
\text{Normalised gain} = \left| \frac{\text{Av}}{\text{Av(mid)}} \right|
\]
NORMALISED PLOT FOR FREQUENCY RESPONSE

A dB plot can now be obtained by using the following transformation:

\[
\frac{A_v}{A_v(NID)} \bigg|_{dB} = 20 \log_{10} \left( \frac{A_v}{A_v(NID)} \right)
\]

The gain at half power frequency point becomes

\[20 \log_{10} \left( \frac{1}{\sqrt{2}} \right) = -3 \text{dB}\]

The plot is shown in the figure.
Ex. The voltage amplifier has voltage gain = 200 at cut-off. Find the maximum voltage gain.

5. We know that maximum voltage gain of voltage amplifier is given as

\[ \text{Maximum voltage gain} = \text{Gain at cut-off} \times \sqrt{2} \]

\[ = 200 \times \sqrt{2} \]

\[ \text{Maximum voltage gain} = 282.84 \]

4.2 Frequency Response of Transistor Amplifiers with Circuit Capacitors:

Generally, the frequency response involves low frequency response. The effect of capacitors in the circuit depends on the frequency response. There are certain terminologies to be discussed before low frequency analysis.

4.2.1 The Decibel Unit:

The basic for the decibel unit originates from the logarithmic response of the human ear to the intensity of sound. The decibel is a logarithmic measurement of the ratio of one power to another or one voltage to another. Usually, the voltage gain of the amplifier is represented in decibels (dB) and is given by

\[ \text{Voltage gain in dB} = 20 \log \text{Av} \]

The power gain in decibels (dB) is given by

\[ \text{Power gain in dB} = 10 \log \text{Ap} \]

When \( \text{Av} \) is greater than one, the dB gain is positive, and when \( \text{Av} \) is less than one, the dB gain is negative. The positive and negative signs of dB gain indicate the amplifier.
we have seen that the amplifiers exhibit a maximum gain over mid-frequency region and a reduced gain at frequencies below and above this range. Usually, the maximum gain called the mid-frequency range gain is assigned a 0 dB value. Any value of gain below mid-frequency region can be referred to as dB and expressed as a negative dB value. For example, assume that mid-frequency gain of a certain amplifier is 100, then

\[
\text{Voltage gain in dB} = 20 \log_{10} 100 = 20 \times 2 = 40 \text{dB}
\]

At \( f_1 \) and \( f_2 \),
\[
A_v = \frac{100}{\sqrt{2}} = 70.7
\]

Voltage gain in dB at \( f_1 \) = voltage gain at dB at
\[
= 20 \log_{10} 70.7
\]
\[
= 37 \text{dB}
\]

Now, if we assign maximum gain (40 dB) as 0 dB then gain at \( f_1 \) and \( f_2 \) becomes -3 dB (40 - 37), as shown in the figure.

It is shown that the voltage gain at \( f_1 \) and \( f_2 \) is less than 3 dB of the maximum voltage gain. Due to this, frequencies \( f_1 \) and \( f_2 \) are also called 3 dB frequencies.
42.2 Significance of Octaves and Decades

The octaves and decades are the measures of change in frequency. A ten times change in frequency is called a decade. On the other hand, an octave corresponds to a doubling or halving of the frequency. For example, an increase in frequency from 100 Hz to 200 Hz is called an octave. Likewise, a decrease in frequency from 100 Hz to 50 Hz is also an octave.

At lower and higher frequencies, the decrease in the gain of amplifiers is often indicated in terms of dB/decade or dB/octave. If the attenuation in the gain is 20 dB, for each decade, then it is indicated by the line having a slope of 20 dB/decade. This is illustrated in Fig.

A rate of 20 dB/decade is approximately equivalent to -6 dB/octave, a rate of 40 dB/decade is approximately equivalent to -12 dB/octave, and so on.

If the frequency is reduced to one hundredth of \( f_c \), i.e., from \( f_c \) to 0.01 \( f_c \), the drop in the voltage gain is -40 dB. In each decade, the voltage gain drops by 20 dB.
A.23. **Mid-band Gain:**

Midband gain of an amplifier is defined as the band of frequencies between 0.1f₁ and 0.1f₂. As shown in Fig., in the midband, the voltage gain of the amplifier is approximated maximum. It is designated as midband gain or Amid.

Although an amplifier normally operates in the midband, there are times when we want to know what the voltage gain is outside of the midband. The voltage gain of the amplifier outside the midband is approximately given as,

\[
A = \frac{\text{Amid}}{\sqrt{1 + (f/f₁)^2}} \sqrt{1 + (f/f₂)^2}
\]

In the midband, \( f/f₁ = 0 \) and \( f/f₂ = 0 \). Therefore,

**Midband:** \( A = \text{Amid} \)

**Below the midband:** \( f/f₂ = 0 \). As a result, the equation becomes

**Below midband:** \( A = \frac{\text{Amid}}{\sqrt{1 + (f/f₁)^2}} \)

**Above the midband:** \( f/f₁ = 0 \). As a result, the equation becomes

**Above midband:** \( A = \frac{\text{Amid}}{\sqrt{1 + (f/f₂)^2}} \)

**Problem:**

Ex. 2.1. For an amplifier, midband gain = 100, and lower cut-off frequency is 1 kHz. Find the gain of an amplifier at frequency = 20 kHz.

**Solution:**

We know that,

**Below midband:** \( A = \frac{\text{Amid}}{\sqrt{1 + (f/f₁)^2}} \)

\[
A = \frac{100}{\sqrt{1 + (20/1000)^2}} = \frac{100}{2} = 2
\]

\( A = 2 \)
Problem: \[ x = 2 \]

Ex. 4.22. For an amplifier, 3 dB gain is 200 and higher cut-off frequency is 20 kHz. Find the gain of an amplifier at frequency \( f = 100 \text{ kHz} \).

Solution: We know that, \[ \text{Amid} = 3 \text{ dB gain} \times \sqrt{2} \]

\[ = 200 \times \sqrt{2} = 282.84 \]

And above midband, \[ A = \frac{\text{Amid}}{\sqrt{1 + \left( \frac{f}{f_c} \right)^2}} \]

\[ A = \frac{282.84}{\sqrt{1 + \left( \frac{100 \times 10^3}{2 \times 10^3} \right)^2}} = 115.47 \]

\[ A = 115.47 \]

4.2.4. Effect of Various Capacitors on Frequency Response

4.2.4.1. Effect of Coupling Capacitors:

We know that the reactance of a capacitor is \( x_c = \frac{1}{2\pi f_c} \). At medium and high frequencies, the factor \( f \) makes \( x_c \) very small, so that all coupling capacitors behave as short circuits. At low frequencies, \( x_c \) increases. This increase in \( x_c \) drops the signal voltage across the capacitor and reduces the circuit gain. As signal frequency decreases, the capacitor reactances increase and the circuit gain continues to fall, reduces the output voltage.

4.2.4.2. Effect of Bypass Capacitors:

At lower frequencies, the bypass capacitors \( C_E \) is not a short. So, the emitter is not at the ground. \( x_c \) is in parallel with \( R_E \) (\( R_s \) in case of \( FET \)) creates an impedance. The signal voltage drops across this impedance reducing the circuit gain. This is illustrated in thefig.
4.2.4.3 EFFECT OF INTERNAL TRANSISTOR CAPACITANCES:

At high frequencies, the coupling and bypass capacitors act as short circuit and do not affect the amplifier frequency response. However, at high frequencies, the internal capacitances, commonly known as junction capacitances, do come into play, reducing the circuit gain.

Fig. shows the junction capacitances for both BJT and a JFET. In case of BJT, $C_{be}$ is the base-emitter junction capacitance and $C_{bc}$ is the base-collector junction capacitance. In case of JFET, $C_{gs}$ is the internal capacitance between gate and source and $C_{gd}$ is the internal capacitance between gate and drain.
At higher frequencies, the reactances of the junction capacitances are low. As frequencies increase, the reactances of the junction capacitances fall. When these reactances become small enough, they provide shunting effect as they are in parallel with junctions. This reduces the circuit gain and hence the output voltage.

4.2.44. HILLER THEOREM:

For the analysis purpose, in transistor amplifiers, it is necessary to split the capacitance between input and the output. This can be achieved by Hiller's theorem as shown in fig.

$A_v$ represents absolute voltage gain of the amplifier at midrange frequencies and $c$ represents either $c_{bc}$ or $c_{in}$ case of $n$ and $g_{dl}$ in case of $JFET$.

A.3. BJT FREQUENCY RESPONSE:

Generally, BJT frequency response involves the low frequency response of BJT. Let us consider a typical common emitter amplifier, as shown in fig.

The amplifier shown in fig. has three RC networks that affect its gain as the frequency is reduced below...
There are:

1. RC network formed by the input coupling capacitor and the input impedance of the amplifiers.
2. RC network formed by the output coupling capacitor, the resistance at the collector and the load resistance.
3. RC network formed by the emitter bypass capacitor and the resistance at the emitter.

**Typical RC Coupled CE Amplifier**

**1. Input RC Network:**

Fig. shows the input RC network formed by $C_1$ and the input impedance of the amplifiers. Note that $v_{out}$ shown in Fig. is the output voltage of the network.

Applying voltage divider theorem,

$$v_{out} = \left( \frac{R_i}{R_i + X_c} \right) v_{in}$$

We know that the critical point in the amplifier response is generally accepted to occur when the output voltage is 70.7 percent of the input ($v_{out} = 0.707v_{in}$). Thus, we can write at critical point:
\[
\frac{R_{in}}{\sqrt{R_{in}^2 + X_C^2}} = 0.707 = \frac{1}{\sqrt{2}}
\]

At this condition, \( R_{in} = X_C \)

The overall gain is reduced due to the attenuation provided by the input RC network. The reduction in overall gain is given by

\[
A_v = 20 \log \left( \frac{V_{out}}{V_{in}} \right) = 20 \log (0.707) = -3 \text{ dB}
\]

The frequency \( f_c \) at this condition is called the lower critical frequency and is given by

\[
f_c = \frac{1}{2\pi R_{in} C_1}
\]

where \( R_{in} = R_1 || R_2 || R_{in}(\text{base}) \)

\( R_{in}(\text{base}) = h_{ie} \)

If the resistance of the input source is taken into account, the above equation becomes

\[
f_c = \frac{1}{2\pi (R_1 || R_2 || h_{ie}) C_1}
\]

3. OUTPUT RC NETWORK:

Fig. shows output RC network formed by \( C_2 \), resistance at the collector and the load resistance.

The critical frequency for this RC network is given by

\[
f_c = \frac{1}{2\pi (R_c + R_L) C_2}
\]
The phase angle in the output RC network is given by

\[ \theta = \tan^{-1}\left( \frac{X_C}{R_C + R_L} \right) \]

(a) CURRENT SOURCE REPLACED BY (b) VOLTAGE SOURCE

3. Bypass Network:

Fig. shows RC network formed by the emitter bypass capacitor CE and the resistance looking in at the emitter.

\[ R = \left( \frac{R_{TH} + \frac{h_i_e}{\beta}}{\beta} \right) \parallel R_E \]

Here, \( R_{TH} + \frac{h_i_e}{\beta} \) is the resistance at the emitter. \( \frac{h_i_e}{\beta} \) is derived as follows:

\[ R = \frac{V_C}{I_C} + \frac{h_i_e}{\beta} = \frac{V_b}{\beta I_b} + \frac{h_i_e}{\beta} = \frac{I_{BRTH}}{\beta I_b} + \frac{h_i_e}{\beta} = R_{TH} + \frac{h_i_e}{\beta} \]

where \( R_{TH} = R_1 || R_2 || R_3 \).

The critical frequency at the bypass network is given by

\[ f_c = \frac{1}{2\pi R_C E} = \frac{1}{2\pi \left[ R_{TH} + \frac{h_i_e}{\beta} \right] || R_E} \]

Each network has its own critical frequency. It is not necessary all frequencies should be equal. The highest critical frequency is
4.31. Determine the low frequency response of the amplifier circuit shown.

**Solution:** It is necessary to analyze each network to determine the critical frequency of the amplifier.

(a) Input RC network:

\[ f_c \text{ (input)} = \frac{1}{2\pi \left( R_s + (R_1 || R_2) \right) c_1} \]

\[ = \frac{1}{2\pi \left( \frac{680 + (68k || 22k || 1.1k)}{0.1 \times 10^{-6}} \right)} \]

\[ = \frac{1}{2\pi \left( \frac{680 + 1031.4}{0.1 \times 10^{-6}} \right)} \times 0.1 \times 10^{-6} \]

\[ f_c \text{ (input)} = 92.98 \text{ Hz} \]

(b) Output RC network:

\[ f_c \text{ (output)} = \frac{1}{2\pi (R_e + R_L) c_2} \]

\[ = \frac{1}{2\pi \left( 2.2k + 10k \right) \times 0.1 \times 10^{-6}} \]

\[ f_c \text{ (output)} = 130.45 \text{ Hz} \]
(c) Bypass RE network:

\[ f_c (\text{bypass}) = \frac{1}{2\pi \left[ \frac{R_{TH} + R_{HE}}{R_{E}} \right] \text{CE}} \]

\[ R_{TH} = 68 \, \text{K} || 22 \, \text{K} || 680 \]
\[ = 653.28 \, \text{K} \]
\[ h_{ie} = 2 \, \text{K} \]

\[ f_c (\text{bypass}) = \frac{1}{2\pi \left[ \frac{1}{653.28 + \frac{1100}{100}} \right] \times 10 \times 10^{-6}} \]

\[ = \frac{1}{2\pi \left[ 1.723 \right] \times 10 \times 10^{-6}} \]

\[ f_c (\text{bypass}) = 923.7 \, \text{Hz} \]

\[ f_c (\text{input}) = 923.8 \, \text{Hz} \]
\[ f_c (\text{output}) = 130451 \, \text{Hz} \]
\[ f_c (\text{bypass}) = 923.7 \, \text{Hz} \]

From these equations, it is observed that input network produces the dominant lower critical frequency. The frequency response of the amplifier is drawn as:

![Low Frequency Response of the Amplifier](image-url)
Ex. 4.32: Calculate the cut-off frequencies due to $C_1$ and $C_2$ in the circuit shown in Fig. given $h_{fe} = 300$ and $h_{ie} = 32 k$. 

$$\text{Solution: (a) Cut-off frequency due to } C_1:\$$

$$f_c = \frac{1}{2\pi R_{\text{in}} C_1} \quad \text{where} \quad R_{\text{in}} = R_1 \parallel R_2 \parallel h_{ie}$$

$$R_{\text{in}} = 800 k \parallel 150 k \parallel 32 k$$

$$f_c = \frac{1}{2\pi (800 k \parallel 150 k \parallel 32 k) \times 1 \times 10^{-3}}$$

$$f_c = 6.565 \text{ Hz}$$

(b) Cut-off frequency due to $C_2$:

$$f_c = \frac{1}{2\pi (R_c + R_{L1} + R_{L2})}$$

$$f_c = \frac{1}{2\pi (7.5 \times 10^3 + 5 \times 10^3 + 1 \times 10^{-3})}$$

$$f_c = 1273.24 \text{ Hz}$$

Ex. 4.33: Determine the cut-off frequency due to the bypass capacitor in the Fig.

Given: $h_{ie} = 1 k$,

$h_{fe} = 200$
\[ f_{c (bypass)} = \frac{1}{2\pi \left( \frac{R_{th}}{\beta} \right) C_{E}} \]

\[ R_{th} = R_1 || R_2 || R_3 \]
\[ = 220k || 22k || 0 \]
\[ R_{th} = 0 \]

\[ f_{c (bypass)} = \frac{1}{2\pi \left( \frac{1000 || 1 \times 10^3}{200 \times 10^{-6}} \right) \times 4.7 \times 10^{-6}} \]
\[ = \frac{1}{2\pi (4.97) \times 4.7 \times 10^{-6}} \]

\[ f_{c (bypass)} = 6811 Hz \]

4.4: CE SHORT CIRCUIT CURRENT GAIN USING HYBRID-II MODEL

Consider a single stage CE transistor amplifier with load resistance \( R_L \).

HYBRID-II CIRCUIT FOR A SINGLE TRANSISTOR WITH \( R_L \).
HYBRID-\( \pi \) EQUIVALENT CIRCUITS OF BJT:

At low frequencies, we have assumed that the response of transistor to change of input voltage or current is instant and hence we have neglected the effect of shunt capacitance in the transistor. This is not in case of high frequencies.

At low frequencies, we analyse transistor using h-parameters. But for high frequencies, the h-parameter model is not suitable for following reasons:

(i) The values of h-parameters are not constant at high frequencies
(ii) At high frequencies, h-parameters are complex in nature.

Due to above reasons, hybrid-\( \pi \) models are used for high-frequency analysis of the transistor.

HYBRID-\( \pi \) COMMON EMITTER TRANSISTOR MODEL:

Common Emitter circuit is the most important practical configuration and hence, the circuit is chosen for analysis using hybrid-\( \pi \) model.

HYBRID-\( \pi \) MODEL FOR CE TRANSISTOR

ELEMENTS IN THE HYBRID-\( \pi \) MODELS:

\( C_{be} \) AND \( C_{bc} \):

The forward biased PN-junction exhibits a capacitance called diffusion capacitance. This capacitive effect is represented by \( C_{be} \) in the hybrid-\( \pi \) model. A typical value is 100 pf.
The reverse biased PN junction exhibits a capacitance effect called transition effect. This capacitance effect is represented by \( C_V \) in the hybrid-\( a \) model. Its typical value is 3pf.

(iii) \( Y_{bb'} \):

The bulk resistance between external base and the internal base \( B' \) is known as base spreading resistance \( Y_{bb'} \). Its typical value is 100\( \Omega \).

(iv) \( Y_{be} \):

The resistance \( Y_{be} \) is that portion of the base emitter which may be thought of as being in series with the collector junction. This establishes a virtual base \( B' \) for the junction capacitance to be connected to instead of \( B \). Its typical value is 1\( \mu \)F.

(v) \( Y_{bc} \):

Due to early effect, the varying voltages across the collector to emitter junction results in base width modulation. A change in effective width causes the emitter current to change. This feedback effect between input and output is taken into account by connecting \( Y_{be} \) between \( B' \) and \( C \). Its typical value is 4\( \mu \)F.

(vi) \( g_m \):

Due to small changes in voltage \( V_{be} \), there is excess minority carrier concentration injected into the base which is proportional to \( V_{be} \). This effect accounts for the current generator \( g_m V_{be} \). Where \( g_m \) is called transconductance, defined by \( g_m = \frac{\Delta I_C}{\Delta V_{be}} \) at a constant \( V_{ce} \).

(vii) \( Y_{ce} \):

It is the output resistance connected between collector and emitter. It is also the result of early effect. Its typical value is 800\( \Omega \).
HYBRID-π PARAMETERS:

in TRANSISTOR TRANS CONDUCTANCE, \( g_m \):

Let us consider a PNP transistor in CE configuration with \( V_{cc} \) bias in the collector circuit.

The transconductance is the ratio of change in the collector current due to the small change in \( V_{be} \) across the emitter junction. It is given as

\[
g_m = \frac{\Delta I_C}{\Delta V_{be}} \Bigg|_{V_{cc} = \text{constant}} \quad \rightarrow (1)
\]

We know that, the collector current \( I_C \) in the active region is given as

\[
I_C = I_{co} - \alpha I_E
\]

and therefore

\[
I_C = -\alpha I_E \quad \text{since } I_{co} = \text{constant}
\]

Neglect the sign and write in terms of differential terms,

\[
\delta I_C = \alpha \delta I_E
\]

Substituting the value of \( \delta I_C \) in equation (1), we get

\[
g_m = \alpha \frac{\delta I_E}{\delta V_{be}}
\]

From the circuit, \( V_E = V_{be} \)

\[
\therefore g_m = \alpha \frac{I_E}{V_E} \quad \rightarrow (2)
\]
The emitter diode resistance $r_e$ is given as

$$r_e = \frac{\partial V_e}{\partial I_e}$$

$$\frac{1}{r_e} = \frac{\partial I_e}{\partial V_e}$$

Substituting $r_e$ in eqn (2), we get

$$g_m = \frac{\partial I_e}{\partial V_e}$$

(3)

The emitter diode is a forward biased diode and its dynamic resistance is given as

$$r_e = \frac{V_T}{I_e}$$

(4)

where $V_T$ is the volt equivalent temperature given by $V_T = \frac{kT}{q}$ where $k =$ Boltzmann constant $= 1.38 \times 10^{-23} \text{ J/K}$, $q =$ electronic charge $= 1.6 \times 10^{-19} \text{ C}$

Substituting eqn (4) in eqn (3),

$$g_m = \frac{\partial I_e}{\partial V_e} = \frac{I_{co} - I_c}{V_T}$$

where $\frac{\partial I_c}{\partial I_e} = I_{co} - \alpha I_e$

since $|I_{co}| < |I_c|$, $I_{co}$ is neglected

$$g_m = \frac{|I_c|}{V_T q} \quad \text{where} \quad V_T = \frac{kT}{q}$$

$$= \frac{|I_c|}{1.6 \times 10^{-19}} \frac{1.38 \times 10^{-23}}{1.88 \times 10^{-23}} \times T$$

$$g_m = \frac{11600 |I_c|}{T} \quad \text{(5)}$$

At room temperature, $T = 300 \text{ K}$

$$g_m = \frac{11600 |I_c|}{300}$$

$$g_m = \frac{|I_c|}{25 \text{ mV}} \quad \text{(6)}$$
(iii) **INPUT CONDUCTANCE, g_{b'e}**:

At low frequencies, all capacitors are negligible and hence not drawn in the figure.

First consider the h-parameter model for CE configuration. Applying KCL to the output circuit, we get:

\[ I_c = h_{fe} I_b + \frac{V_{ce}}{h_{oe}} \]

Making \( V_{ce} = 0 \) by short circuiting, the short circuit current gain, \( h_{fe} \), is defined as

\[ h_{fe} = \frac{I_c}{I_b} \rightarrow (8) \]

Consider hybrid-n model, \( \gamma_{bc} > \gamma_{b'e} \). Hence, \( I_b \) flows into \( V_{b'e} \) and \( V_{be} = I_b \gamma_{b'e} \).

The short circuit collector current is given by

\[ I_c = g_m V_{b'e} = g_m I_b \gamma_{b'e} \]
\[ \frac{I_c}{I_b} = g_m \cdot \frac{\beta e}{v} \rightarrow (1) \]

Equating (8) & (9),

\[ h_{fe} = g_m \cdot \frac{\beta e}{v} \]

\[ \beta e = h_{fe} \cdot g_m \rightarrow (10) \]

\[ g_{be} = \frac{g_m}{h_{fe}} \]

From Equation (5), \[ g_m = \frac{1}{h_{fe} v} \]

\[ \beta e = \frac{h_{fe} v}{1} \]

\[ g_{be} = \frac{1}{h_{fe} v} \rightarrow (11) \]

(iii) **FEEDBACK CONDUCTANCE, \( g_{be} \):**

Let us consider h-parameter model for CE configuration with input open circuit, \( I_b = 0 \), then \( v_i \) given as

\[ v_i = h_{fe} v \rightarrow (12) \]

Now, let us consider hybrid-\( \pi \) model for CE configuration

With \( I_b = 0 \), \( v_{ce} \) can be given as

\[ v_{ce} = I_1 \left( \beta e + \beta e \right) \]

\[ I_1 = \frac{v_{ce}}{\beta e + \beta e} \rightarrow (13) \]
\[ V_{be} \text{ can be given as} \]
\[ V_{be} = I_1 \cdot V_{be} \]
\[ V_{be} = \frac{V_{re} \cdot V_{ce}}{\frac{1}{Y_{be}} + \frac{1}{Y_{re}}} \quad \text{(from Eqn 13)} \]

with \( I_b = 0 \),
\[ V_c = V_{be} \]
\[ V_{i} = \frac{V_{re} \cdot V_{ce}}{\frac{1}{Y_{be}} + \frac{1}{Y_{re}}} \]

Substituting the value of \( V_i \) in Eqn(12), we get

\[ h_{re} \cdot V_{ce} = \frac{V_{be} \cdot V_{ce}}{\frac{1}{Y_{be}} + \frac{1}{Y_{re}}} \]
\[ h_{re} = \frac{V_{be}}{\frac{1}{Y_{be}} + \frac{1}{Y_{re}}} \]
\[ Y_{be} = h_{re} \cdot Y_{re} + h_{re} \cdot Y_{be} \]
\[ Y_{be} \cdot (1-h_{re}) = h_{re} \cdot Y_{re} \]
\[ Y_{be}(1-h_{re}) = h_{re} \cdot Y_{re} \]
\[ Y_{be} = \frac{Y_{be}(1-h_{re})}{h_{re}} \quad \text{[1] \ \cdot \ \cdot \ 1-h_{re} = 1} \]
\[ Y_{be} = \frac{Y_{be}}{h_{re}} \]
\[ g_{bc} = \frac{h_{re}}{Y_{be}} \]

(iv) **BASE SPREADING RESISTANCE, \( Y_{bb}' \):**

Let us consider h-parameter model. The input resistance with output shorted (\( V_{ce} = 0 \)) is \( h_{ie} \) with hybrid \( \pi \) model, input resistance with output shorted in \( \frac{1}{Y_{bb}'} + Y_{be} \cdot \)

\[ h_{ie} = \frac{Y_{bb}'}{Y_{be} \cdot \frac{1}{Y_{re}} - \frac{1}{Y_{be}}} \]

\[ Y_{bb}' = \frac{h_{ie} - h_{re} \cdot V_i}{1} \]
Output Conductance, \( \beta_c \):

Using h-parameters, the output conductance is given by

\[
\beta_o = \frac{I_C}{V_{CE}}
\]

Apply KCL to the node \( 'y' \) at the output side:

\[
I_C = \frac{V_{CE}}{V_{CE}} + g_m V_{BE} + I_1
\]

From Eqn (13), \( I_1 = \frac{V_{CE}}{r_{BC} + r_{BE}} \)

\[
I_C = \frac{V_{CE}}{V_{CE}} + g_m V_{BE} + \frac{V_{CE}}{r_{BC} + r_{BE}}
\]

Substituting the value of \( V_{BE} \), we get

\[
I_C = \frac{V_{CE}}{V_{CE}} + g_m \frac{V_{BC} V_{CE}}{r_{BC} + r_{BE}} + \frac{V_{CE}}{r_{BC} + r_{BE}}
\]

\[
\frac{I_C}{V_{CE}} = \frac{1}{V_{CE}} + g_m \frac{V_{BC} V_{CE}}{r_{BC} + r_{BE}} + \frac{1}{r_{BC} + r_{BE}}
\]

\[
\beta_o = \frac{I_C}{V_{CE}} - \frac{g_m V_{BC} V_{CE}}{r_{BC} + r_{BE}} - \frac{1}{r_{BC} + r_{BE}}
\]

\[
\beta_c = \beta_o - \frac{1 + h_{fe}}{r_{BC} + r_{BE}}
\]

\[
V_{BC} > r_{BE}
\]

\[
\beta_c = \beta_o - h_{fe} r_{BC}
\]

\[
\beta_c = \beta_o - h_{fe} g_{BC}
\]

Summary:

\[
\begin{align*}
9_m &= \frac{I_C}{V_{T}} \\
\gamma_{BE} &= \frac{h_{fe}}{9_m} \\
\gamma_{BB} &= h_{ie} - \gamma_{BE} \\
\gamma_{BB} &= h_{ie} - h_{fe} g_{BC}
\end{align*}
\]
For the analysis of CE short circuit current gain, we have to assume $R_L = 0$. With $R_L = 0$, the output short circuiting $r_o$ becomes zero. $r_{be}$, $r_c$, and $r_{bc}$ appear in parallel. When $C_C$ coil appears between base and emitter, it is known as Miller capacitance ($C_M$).

The Miller capacitance is $C_M = C_C (1 + g_m R_L)$

Here, $R_L = 0$

$\therefore C_M = C_C (1 + g_m R_L)$

As $r_{bc} \gg r_{be}$, $r_{bc}$ is neglected. With these approximations, we get simplified hybrid-$\pi$ model for short circuit CE transistors.

The parallel combination of $r_{be}$ and $r_c + C_C$ is given by

$$Z = \frac{1}{r_{be} + \frac{1}{j\omega (r_c + C_C)}}$$

$$Z = \frac{r_{be}}{1 + j\omega r_{be} (r_c + C_C)} \quad \text{(1)}$$

This simplifies the hybrid-$\pi$ model as shown below:

The Simplified Hybrid-$\pi$ Model
From the figure, we can write

\[ V_{be} = I_b \cdot Z \]

\[ Z = \frac{V_{be}}{I_b} \quad \rightarrow (2) \]

The current gain can be given as

\[ A_i = \frac{I_C}{I_b} = -g_m V_{be} \quad \text{where } I_C = -g_m V_{be} \]

Substituting the value of \( \frac{V_{be}}{I_b} \) from Eqn (2), we get,

\[ A_i = -g_m \frac{V_{be}}{I_b} \]

\[ = -\frac{g_m V_{be}}{1 + j \omega (c_e + c) V_{be}} \quad \rightarrow (3) \]

\[ A_i = -\frac{h_{fe}}{1 + j \omega \left(c_e + c\right) V_{be}} \quad \rightarrow (4) \]

From Eqn (4), we can say that the current is not constant. It depends on frequency. When frequency is small, the term containing \( \omega \) is very small compared to 1 and hence at low frequency \( A_i = -h_{fe} \). But as frequency increases, \( A_i \) reduces.

4.5.1 Cut-Off Frequency - \( f_o \), \( f_b \) & Unity Gain Bandwidth (\( f_T \))

![Diagram showing current gain vs frequency]
Let us assume,

\[ f_p = \frac{1}{2\pi V_{be} (C_e + C_C)} \]

Substituting the value of \( f_p \) in \( A_i \),

\[ A_i = \frac{-h_{fe}}{1 + j\left(\frac{f}{f_p}\right)} \]

\[ |A_i| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_p}\right)^2}} \quad \rightarrow (5) \]

At \( f = f_p \),

\[ |A_i| = \frac{h_{fe}}{\sqrt{2}} \]

(i) \( f_p \) (cut-off frequency) is defined as the frequency at which the transistor short circuit CE current gain drops by 3dB or \( \frac{1}{\sqrt{2}} \) times from its value at low frequencies.

It is given as

\[ f_p = \frac{1}{2\pi V_{be} (C_e + C_C)} \]

\[ = \frac{\beta}{V_{be}} \]

\[ = \frac{\beta}{2\pi (C_e + C_C)} \]

\[ f_p = \frac{g_m}{2\pi h_{fe} (C_e + C_C)} \]

\[ = \frac{g_{fe}}{h_{fe}} \]

(ii) \( f_d \) (cut-off frequency) is defined as the frequency at which the transistor short circuit CB current gain drops by 3dB or \( \frac{1}{\sqrt{2}} \) times from its value at low frequencies.

The expression for \( f_d \) can be derived in the similar manner as for \( f_p \).
The current gain for CB configuration is given as

$$A_i = \frac{-h_{fe}}{1+j\frac{f}{f_d}}$$

where

$$f_d = \frac{h_{fe}}{2\pi \times h_c \times c_e}$$

$$|A_i| = \frac{h_{fe} b}{\sqrt{1 + \left(\frac{f}{f_d}\right)^2}}$$

At $f = f_d$,

$$|A_i| = \frac{h_{fe} b}{\sqrt{5}}$$

$$f_d = \frac{h_{fe} \times g_m}{2\pi h_{fe} c_e}$$

$$f_d = \frac{g_m}{2\pi c_e}$$

(iii) **Unity Gain** is defined as the frequency at which the CE short circuit current gain becomes unity.

At $f = f_1$, Eqn (5) becomes,

$$1 = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f_1}{f_p}\right)^2}}$$

The ratio $f_1/f_p$ is quite large compared to 1. Hence, the above equation becomes,

$$1 = \frac{h_{fe}}{f_1} \left(\frac{f_1}{f_p}\right)$$

$$1 = \frac{h_{fe} \times f_p}{f_1}$$

$$f_1 = h_{fe} \times f_p$$
Substituting value of $f_p$ from Eqn (b), we get

$$f_l = \frac{f_m}{2\pi h_{fe} (C_e + C_c)}$$

$$f_l = \frac{f_m}{2\pi} \frac{C_e + C_c}{C_e + C_c}$$

since $C_e \gg C_c$, we can write

$$f_l = \frac{f_m}{2\pi C_e}$$

Problem 45. At $I_C = 1mA$ and $V_{CE} = 10V$, a certain transistor data shows $C_E = 8pF$, $h_{fe} = 200$ and $\omega_T = -5000rad/sec$. Calculate $g_m$, $\gamma_{\pi}$, $C_E$, and $C_E$.

Solution (i) $g_m = \frac{I_C}{V_T} = \frac{1mA}{26mV} = 38.46mA/V$

(ii) $\gamma_{\pi} = \gamma_{be} = \frac{h_{fe}}{g_m} = \frac{200}{38.46 \times 10^{-3}} = 5200$K$

(iii) $C_E + C_E = C_{be} + C_{bc} = \frac{g_m}{\omega_T} = \frac{g_m}{\omega_T} = \frac{38.46 \times 10^{-3}}{-5000 \times 10^{-6}}$

$C_{be} + C_{bc} = 76.92pF$

$C_{be} = 76.92pF - 3pF$

$C_{be} = C_E = 73.92pF$

(iv) We know that, $f_l = h_{fe} f_p$

$$2\pi f_l = h_{fe} (2\pi f_p)$$

$$\omega_T = h_{fe} \omega_p$$

$$\omega_p = \frac{\omega_T}{h_{fe}}$$

$$= \frac{-500 \times 10^6}{200}$$

$$\omega_p = 2.5 \times 10^6 rad/sec$$
EX.45.2: Short circuit CE current gain of transistor is 25 at a frequency of 2 kHz if \( f_B = 200 \text{kHz} \). Calculate (i) \( f_T \) (ii) \( h_{fe} \) (iii) Find \(|A_{i1}|\) at frequency of 10 kHz and 100 kHz.

\[ f_T = \frac{1}{2\pi f_B} = 25 \times 2 \times 10^6 \]

\[ f_T = 50 \text{kHz} \]

\[ h_{fe} = \frac{f_T}{f_B} = \frac{50 \text{kHz}}{200 \text{kHz}} = 0.25 \text{kHz} \]

(iii) \[ |A_{i1}| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{2f_B}\right)^2}} \]

\[ |A_{i1}| = \frac{250 \text{kHz}}{\sqrt{1 + \left(\frac{10 \times 10^6}{200 \times 10^3}\right)^2}} \]

At \( f = 10 \text{kHz} \)

\[ |A_{i1}| = \frac{250}{\sqrt{1 + \left(\frac{100 \times 10^6}{200 \times 10^3}\right)^2}} = 5 \]

At \( f = 100 \text{kHz} \)

\[ |A_{i1}| = \frac{250}{\sqrt{1 + \left(\frac{1000 \times 10^6}{200 \times 10^3}\right)^2}} = 0.5 \]

4.5.2: Short circuit CE current gain with resistive load:

Consider a single stage CE transistor amplifier with load resistance \( R_L \) as shown in fig.

\[ V_{bc} = \frac{V_{be} - V_{ce}}{R_L} \]
In the output circuit, \( r_o \) is in parallel with \( R_L \). For high frequency amplifiers, \( R_L \) is very small compared to \( r_o \) and hence \( r_o \) can be neglected. Using Miller's Theorem, we split \( r_{be} \) and \( C_{be} \) to simplify the analysis.

Fig. shows the simplified hybrid-\( h \) model for a single transistor with resistive load.

On further simplification of the input circuit, amplifier's gain \( K \) is given as

\[
K = \frac{V_o}{V_{be}}
\]

where \( V_o = -g_m V_{be} R_L \)

\[
K = -g_m R_L
\]

The value \( \frac{r_{be}}{1-K} \gg r_{be} \) and hence \( \frac{r_{be}}{1-K} \) which is in parallel with \( r_{be} \) can be neglected.

\( C_{be} \) can be resolved by using Miller's Theorem,

\[
\frac{1}{j\omega C_{be}} = \frac{1}{j\omega C_{be} (1+g_m R_L)}
\]

\[
\frac{C_{be}}{1-K} = C = C_{be} (1+g_m R_L)
\]

where \( C_{be} = C \)
Parallel combination of $V_{be}$ and $C_{eq}$ is given as $Z$

\[
Z = \frac{V_{be}}{jwC_{eq}} \left( \frac{1}{V_{be}} + \frac{1}{jwC_{eq}} \right) = \frac{V_{be}}{jwC_{eq}V_{be}}
\]

From the above figure, we can write

\[
V_{be} = I_b \cdot Z
\]

\[
Z = \frac{V_{be}}{I_b}
\]

The current gain ($A_i$) can be given as

\[
A_i = \frac{I_L}{I_b} = \frac{-g_mV_{be}}{I_b}
\]

Substituting $\frac{V_{be}}{I_b}$ in this equation of $A_i$,

\[
A_i = -g_m Z
\]

Substituting the value of $Z$, we get,

\[
A_i = -g_m \frac{V_{be}}{I_b} = \frac{-h_f e}{1 + j \omega R_{be} C_{eq}} = \frac{-h_f e}{1 + j 2\pi f R_{be} C_{eq}}
\]

Consider, upper cut-off frequency $f_H = \frac{1}{2\pi \tau_{be} C_{eq}}$
\[ A_i = \frac{-h_{fe}}{1 + j\left(\frac{f}{f_H}\right)} \]

\[ |A_i| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} \]

At \( f = f_H \)

\[ A_i = \frac{h_{fe}}{\sqrt{2}} \]

Thus, \( f_H \) is defined as the frequency at which the transistor gain drops by 3dB or \( \frac{1}{\sqrt{2}} \) times from its value at lower frequency.

It is given as

\[ f_H = \frac{1}{2\pi \sqrt{h_{be} C_{eq}}} \]

\[ = \frac{1}{2\pi \sqrt{h_{be} \left[ C_{et} C_{cc} + g_m R_L \right]}} \]

At \( R_L = 0 \),

\[ f_H = \frac{1}{2\pi h_{be} (C_{et} + C_{cc})} = f_p \]

From the above equation, we can say that maximum possible value for \( f_H \) is \( f_p \). As \( R_L \) increases, \( C_{eq} \) increases, \( h_{be} \) decreases. \( f_H \)
4.5.3. CURRENT GAIN INCLUDING SOURCE RESISTANCE:

Fig. shows the equivalent circuit with source resistance, assuming current source.

\[
A_{is} = \frac{I_L}{I_s} = \frac{I_L}{I_b} \cdot \frac{I_b}{I_s}
\]

\[
: \quad \frac{I_b}{I_s} = \frac{R_s}{R_s + Y_{bb'} + Z}
\]

\[
: \quad A_{is} = -\frac{g_m Z R_s}{R_s + Y_{bb'} + Z}
\]

where \( Z = Y_{be} \frac{1}{1 + j\omega Y_{be} c_e}\).

At low frequency, we can neglect the capacitance and hence \( Z \) is given as \( Z = Y_{be} \).

Then \( A_{is} \), at low frequency, \( = \frac{I_L}{I_s} = -\frac{g_m Y_{be} R_s}{R_s + Y_{bb'} + Y_{be}} \).

\[
A_{is} (\text{low}) = -\frac{h_{fe} R_s}{R_s + Y_{bb'} + Y_{be}}
\]

\[
\therefore \quad h_{ie} = Y_{bb'} + Y_{be}
\]

\[
A_{is} (\text{low}) = -\frac{h_{fe} R_s}{R_s + h_{ie}}
\]

\[
\therefore \quad h_{ie} = Y_{bb'} + Y_{be}
\]
4.5.4. **Voltage Gain Including Source Resistance:**

Fig. shows the equivalent circuit with source resistance assuming voltage source.

\[ AV_s = \frac{V_o}{V_s} \]

\[ = \frac{I_L \cdot R_L}{I_s \cdot R_s} = -\frac{g_m Z \cdot R_s}{R_s + Y_{bb} + Z} \cdot \frac{R_L}{R_s} \]

\[ = -\frac{g_m Z \cdot R_L}{R_s + Y_{bb} + Z} \]

At low frequency,

\[ AV_s (\text{low}) = \frac{I_L \cdot R_L}{I_s \cdot R_s} = -\frac{h_{fe} R_s}{R_s + h_{ie}} \cdot \frac{R_L}{R_s} \]

\[ AV_s (\text{low}) = -\frac{h_{fe} R_L}{R_s + h_{ie}} \]

\[ AV_s (\text{low}) \text{ varies linearly with } R_L \]

45.5. **Cut-Off Frequency Including Source Resistance:**

\[ A_{is \ (\text{high})} = \frac{A_{is}}{1 + j \left( \frac{f}{f_{th}} \right)} \]

\[ A_{vs \ (\text{high})} = \frac{A_{vs}}{1 + j \left( \frac{f}{f_{th}} \right)} \]
where \( f_H = \frac{1}{2\pi R e_q C e_q} \)

where \( R e_q = \frac{1}{R} (\frac{1}{\beta} + R_s) \)

and \( C e_q = C e + (C e C 1 + g m R_L) \)

\( f_H \) increases as the load resistance decreases because \( C \) is a linear function of \( R_L \). At \( R_L = 0 \), the 3-dB frequency is finite. It is given as

\[
\frac{1}{2\pi R (C e + C c)} = \frac{f_l}{g m} \left( \frac{1}{2\pi (C e + C c)} \right) = \frac{h_{fe} \cdot f_p}{g m} \left( \frac{1}{2\pi (C e + C c)} \right)
\]

\[
\frac{f_H}{f_l} = \frac{f_p}{g h_{be} \cdot R} \left( \frac{1}{2\pi (C e + C c)} \right)
\]

4.5.6. GAIN BANDWIDTH PRODUCT:

45.6.1. GAIN BANDWIDTH PRODUCT FOR VOLTAGE:
The gain bandwidth product for voltage gain is given as

\[
|A_v(l w) \cdot f_H| = |A_{v 0} \cdot \frac{f_H}{f_l}| = \frac{-h_{fe} R L}{R_s + h_{ie}} \times \frac{1}{2\pi R e_q C e_q}
\]

\[
= \frac{-h_{fe} R L}{R_s + h_{ie}} \times \frac{1}{2\pi R e_q \left[ \frac{Y_{be} (Y_{bb} + R_s)}{Y_{be} + Y_{bb} + R_s} \right]}
\]

\[
= \frac{-h_{fe} R L}{R_s + h_{ie}} \times \frac{1}{2\pi R e_q \left[ \frac{Y_{be} (Y_{bb} + R_s)}{R_s + h_{ie}} \right]}
\]

\[
\frac{-h_{fe} R L}{2\pi R e_q T_{be} (Y_{bb} + R_s)} \left[ \frac{r_s \cdot h_{ie} = Y_{be} + Y_{bb} + R_s}{T_{be} (Y_{bb} + R_s)} \right]
\]
\[
\begin{align*}
|A_{vso} + fH| &= \frac{\frac{g_m}{2\pi C_{eq} (\frac{1}{R_s + Y_{bb}} + \frac{g_m}{2\pi C_{eq}})}}{2\pi C_{eq} (\frac{1}{R_s + Y_{bb}} + \frac{g_m}{2\pi C_{eq}})} \\
&= \frac{g_m}{2\pi (C_{eq} + \frac{g_m}{2\pi C_{eq}})} \frac{RL}{(R_s + Y_{bb})} \\
&= \frac{g_m}{2\pi C_{eq} (\frac{1}{R_s + Y_{bb}} + \frac{g_m}{2\pi C_{eq}})} \frac{RL}{(R_s + Y_{bb})} \\
&= \frac{RL}{2\pi C_{eq} (\frac{1}{R_s + Y_{bb}} + \frac{g_m}{2\pi C_{eq}}) R_l} \\
|A_{vso} \cdot fH| &= \frac{RL}{R_s + Y_{bb}'} \frac{1}{1 + 2\pi fT (C_{eq} R_l)} \\
\end{align*}
\]

45.6.2. GAIN BANDWIDTH PRODUCT FOR CURRENT:

The gain bandwidth product for current gain is given as

\[
|A_{islow} \cdot fH| = |A_{iso} \cdot fH| = \frac{-h_{fe} \cdot R_S}{R_{st} + h_{ie}} \frac{1}{2\pi \cdot R_{eq} \cdot C_{eq}}
\]

By similar analysis, with replacement of \(-h_{fe} R_s\) instead of \(-h_{fe} R_l\), we get

\[
|A_{iso} \cdot fH| = \frac{g_m R_S}{2\pi C_{eq} (R_s + Y_{bb})} \\
|A_{iso} \cdot fH| = \frac{fT}{1 + 2\pi fT (C_{eq} R_l)} \frac{R_S}{R_s + Y_{bb'}}
\]
Ex. 4.5-1: A high frequency amplifier uses a transistor which is driven from a source with $R_s = 0$. Calculate the value of $f_H$, if $R_L = 0$ and $R_L = 1$ kΩ. Assume typical values of hybrid-\(\pi\) parameters.

(i) \(f_H\):

For $R_L = 0$

\[
\frac{1}{2\pi \times b \times (C_{be} + C_{bc})} = \frac{1}{2\pi \times b \times (C_{bc} + C_{c})}
\]

Typical values: $v_{be} = 1k\Omega$, $C_{be} = 100pF$, $C_{bc} = 3pF$

\[
\frac{1}{2\pi \times 1 \times 10^3 \times \left[100 \times 10^{-12} + 3 \times 10^{-12}\right]}
\]

\[
f_H = 1.545 \text{ MHz}
\]

For $R_L = 1$ kΩ

\[
\frac{1}{2\pi \times b \times (C_{be} + C_{bc} (1 + gm R_L))}
\]

\[
g_m = 50 \text{ mV/\text{V}}
\]

\[
\frac{1}{2\pi \times 1 \times 10^3 \times \left[100 \times 10^{-12} + 3 \times 10^{-12} (1 + 50 \times 10^{-3} \times 1 \times 10^3)\right]}
\]

\[
f_H = 0.629 \text{ MHz}
\]
Problem: Determine the bandwidth of the amplifier shown.

\[ V_{bb} = 100 \text{V}, \quad V_{be} = 1.1 \text{k}\Omega, \quad C_{be} = 3 \text{pF}, \quad C_{bc} = 100 \text{pF}, \quad h_{fe} = 225 \]

We know that:

\[ h_{ie} = \gamma_{bb} + \gamma_{be} \]
\[ = 100 \times 1 + 1.1 \times 10^3 \]
\[ h_{ie} = 1.2 \text{k}\Omega \]

\[ f_c \text{ (input)} = \frac{1}{2\pi (R_s + (R_t \parallel R_{1} \parallel R_{12}) \cdot C) \cdot \omega} \]
\[ = \frac{1}{2\pi \left[ 0.1 \text{k}\Omega \parallel 10 \text{k}\Omega \parallel 1.2 \text{k}\Omega \right] \times 25 \times 10^{-6}} \]
\[ f_c \text{ (input)} = 6 \text{Hz} \]

\[ f_c \text{ (output)} = \frac{1}{2\pi (R_c \parallel R_L) C} \]
\[ = \frac{1}{2\pi (9 \times 15 \text{k}) \times 25 \times 10^{-6}} \]
\[ f_c \text{ (output)} = 0.454 \text{Hz} \]

\[ f_c \text{ (bypass)} = \frac{1}{2\pi \left[ \frac{10^{3} \times h_{fe}}{B}\right] \cdot C \cdot E} \]
\[ R_{TH} = R_1 \parallel R_2 \parallel R_3 \]
\[ = 110 \text{k}\Omega \parallel 10 \text{k}\Omega \parallel 0 = 0 \]
\[ = \frac{1}{2\pi \left[ \frac{1.2 \times 10^3}{225} \parallel 2 \times 10^3 \right] \times 5 \times 10^{-6}} \]
\[ = 5.98 \text{Hz} \]
The smallest of these is \( f_L = 0.454 \text{ Hz} \).

We know that, \( f_H = \frac{1}{2\pi \sqrt{Cc (Ce + C + 19\text{mF})}} \)

\[ C_{bc} = C_e = 3\text{pF} \]
\[ C_{b'c} = C_c = 100\text{pF} \]

\[ g_m = \frac{hfe}{\beta c} = \frac{225}{1.1 \times 10^3} = 204.5\text{mA/V} \]

\[ f_H = \frac{1}{2\pi \times 1\times 10^3 \times \left[ 3 \times 10^{-12} + 100 \times 10^{-12} \left( 1 + 204.5 \times 10^{-3} \times 5 \times 10^3 \right) \right]} \]

\[ f_H = 1.4136 \text{ KHz} \]

Bandwidth = \( f_H - f_L \)

\[ = 1.4136 \text{ KHz} - 0.454 \text{ Hz} \]

\[ BW = 1.4131 \text{ KHz} \]

4.6. **Miller Effect**:

In the high-frequency region, the inter-electrode capacitance and the wiring capacitance between the leads of the network are of importance. The large capacitance of the network are all replaced by their short-circuit equivalent due to their low reactance.

To reduce the effect of capacitor that exists between input and output terminals, Miller's Theorem is used. The Miller's Theorem states that the capacitance impedance connected between input and output can be split into two capacitance such as \( C_{hi} \) and \( C_{ho} \). It can be obtained as follows:
In Fig., the feedback capacitance is defined by $G$. Applying Kirchoff’s current law, we get

\[ I_L = I_1 + I_2 \]

Using Ohm’s law,

\[ I_1 = \frac{V_i}{Z_i}, \quad I_2 = \frac{V_i - V_o}{X_{cf}} \]

\[ I_2 = \frac{V_i}{Z_i} \cdot \frac{X_{cf}}{X_{cf}} = \frac{(1 - AV) V_i}{X_{cf}} \]

On substituting, we obtain,

\[ \frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{(1 - AV) V_i}{X_{cf}} \]

\[ \frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{cf} \left( \frac{1}{1 - AV} \right)} \]

But \[
\frac{X_{cf}}{1 - AV} = \frac{1}{2 \pi f (1 - AV) C_f} = X_{C_H} \]

\[ \frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_H}} \]

The Miller effect capacitance for input is given by

\[ C_{in} = (1 - AV) C_f \]
The importance to determine the output Miller effect are

\[ AV = \frac{V_o}{V_i} \]

**NETWORK FOR MILLER OUTPUT CAPACITANCE**

Applying Kirchhoff's Current Law, we get,

\[ I_0 = I_1 + I_2 \]

where, \( I_1 = \frac{V_o}{R_o} \) and \( I_2 = \frac{V_o - V_i}{x_{cf}} \)

The resistance \( R_o \) is generally large and therefore, the first term is ignored. Hence,

\[ I_0 = \frac{V_o - V_i}{x_{cf}} \]

Substituting, \( V_i = \frac{V_o}{AV} \)
\[ AV = \frac{V_o}{V_i} \] results in

\[ I_0 = \frac{V_o - \frac{V_o}{AV}}{x_{cf}} = \frac{V_o}{x_{cf}} \left[ 1 - \frac{1}{AV} \right] \]

\[ \frac{I_0}{V_o} = \frac{1 - \frac{1}{AV}}{x_{cf}} \]

\[ \cot V_o = \frac{x_{cf}}{I_0} = \frac{1 - \frac{1}{AV}}{x_{cf}} \]

\[ = \frac{1}{2\pi f} \int \left[ 1 - \frac{1}{AV} \right] x_{cf} \]

\[ = \int_{-\infty}^{\infty} \frac{1}{1 + \frac{1}{AV}} x_{cf} = C_h \]
where, \( C_{ho} = \left(1 - \frac{1}{AV}\right) C_f \) is the Miller output capacitance.

In general, if \( AV > 1 \), then the above equation reduces to
\[ C_{ho} \approx C_f \]

The Miller effect occurs only in the circuit where there is a 180° phase shift between the input and the output.

**Frequency Response of FET**

The drain current of FET is a function of drain to source voltage (\( V_{ds} \)) and gate to source voltage (\( V_{gs} \)). The linear small signal equivalent circuit for FET can be drawn analogous to the circuit. The input impedance of the FET amplifier is very high. So consider that gate current \( I_g = 0 \).

Assuming varying currents and voltages for a FET,
\[ I_D = f(V_{gs}, V_{ds}) \]

If both drain and gate voltages are varied, the change in drain current is given approximately by first term in the Taylor series expansion of equation.

\[ \Delta I_D = I_D \Delta V_{gs} + I_D \Delta V_{ds} \]

The small signal notation as for BJT,
\[ I_D = g_m V_{gs} + \frac{1}{r_D} V_{ds} \quad \rightarrow (1) \]

where \( g_m \) is the transconductance or mutual conductance of the FET.
\[ g_m = \left( \frac{\partial I_D}{\partial V_{GS}} \right)_{V_D} \Rightarrow \left( \frac{\Delta I_D}{\Delta V_{GS}} \right)_{V_D} = \left( \frac{I_D}{V_{GS}} \right)_{V_D} \]

Drain ion output resistance of the FET is given as

\[ r_d = \left( \frac{\partial V_D}{\partial I_D} \right)_{V_G} = \left( \frac{\Delta V_D}{\Delta I_D} \right)_{V_G} = \left( \frac{V_D}{I_D} \right)_{V_G} \]

Reciprocal of \( r_d \) is the drain conductance \( g_d \)

Amplification factor \( \mu \) for FET may be defined as

\[ \mu = \left( \frac{-\partial V_D}{\partial V_G} \right)_{I_D} \approx \left( \frac{\Delta V_D}{\Delta V_G} \right)_{I_D} = \left( -\frac{V_D}{V_G} \right)_{I_D} \]

Substitute \( I_D = 0 \) in \( g_m(\mu) \), we get the relation between \( \mu \), \( g_m \) & \( r_d \)

\[ \mu = g_m r_d \]

A small signal model for FET in common source configuration can be drawn by using equation (11),

![Small signal current source model for FET in CS configuration](image1)

![Small signal voltage source model for FET in CS configuration](image2)

**NOTE:**

The input resistance between the gate and source is infinite, since it is assumed that the reverse biased gate draws no current.
4.8. **High Frequency Analysis of CS MOSFET Amplifiers.**

Fig. shows the high frequency equivalent circuit model for MOSFET. In this model, the capacitance $C_{ds}$ can be neglected to simplify the analysis.

**High Frequency Model of FET**
- In the high frequency model of FET, the capacitances between nodes have to be added in the low frequency model.
- The resultant equivalent circuit is shown in Fig.

**Simplified High Frequency Model of FET**
- $C_{gs}$ represents the barrier capacitance between gate and source.
- $C_{gd}$ represents the barrier capacitance between gate and drain.
- $C_{ds}$ represents the drain to source capacitance of the channel.
- The internal capacitances lead to feedback from output to input and the voltage amplification decreases at high frequencies.
\[
\omega_T = \frac{g_m}{c_{gs} + c_{gd}} \\
\omega_T = \frac{g_m}{2\pi(c_{gs} + c_{gd})}
\]

4.8.2. **Frequency Response of Common Source Amplifier**

**High Frequency Cs Amplifier**

The circuit of configuration shows the Cs amplifier.

The equivalent circuit at high frequencies is shown in Fig. below.

**Small Signal Equivalent Circuit of Cs Amplifier**

At high frequencies

The equivalent circuit in terms of admittance is shown in Fig. below.
Applying Hillein's Theorem, Y_{gd} connected between input and output has been separated to input & output sides respectively.

**Hiller, Equivalent High Frequency, CO Amplifier**

(i) **Input Admittance, Y_i:**

It is given by the parallel combination of Y_{gs} and Y_{gd(1-Av)}.

\[ Y_i = Y_{gs} + Y_{gd(1-Av)} \]

(ii) **Output Admittance, Y_o:**

It is given by the parallel combination at the output side which includes Y_{gd(Av-1/Av)}, Y_{ds}, Y_{gd} and Y_{L}.

\[ Y_o = Y_{gd(Av-1/Av)} + Y_{ds} + Y_{gd} + Y_{L} \]

Since \( Y_{gd} \ll Y_{ds}, Y_{gd} \) can be neglected.

\[ Y_o = Y_{ds} + Y_{gd} + Y_{L} \]

(iii) **Voltage Gain, Av:**

Equivalent Circuit To Find Av.
Apply Kirchhoff’s current law at node $X$:

$$I_1 = g_m v_i + I \rightarrow (1)$$

By ohm’s law,

$$I = \frac{V}{R} = V_g$$

$$I_i = V_i Y_{gd} \rightarrow (2)$$

$$V_i Y_{gd} = g_m v_i + I$$

$$I = V_i \left(Y_{gd} - g_m\right) \rightarrow (3)$$

Voltage gain, $A_v = \frac{V_o}{V_i}$

$$= \frac{I Z}{V_i} = \frac{A_v}{V_i}$$

$$A_v = I \rightarrow (4)$$

From output admittance

$$Y_o = Y_{gd} \left(1 - \frac{1}{A_v}\right) + Y_{ds} + Y_d + Y_L$$

Since $\frac{1}{A_v} < 1$, it can be neglected.

$$Y_o = Y_{gd} + Y_{ds} + Y_d + Y_L \rightarrow (5)$$

Substitute (3) & (5) in (4),

$$A_v = \frac{V_i \left(Y_{gd} - g_m\right)}{V_i \left(Y_{gd} + Y_{ds} + Y_d + Y_L\right)}$$

$$A_v = \frac{Y_{gd} - g_m}{Y_{gd} + Y_{ds} + Y_d + Y_L}$$

This is the equation of voltage gain at high frequency.
At low frequency, capacitors are short-circuited

\[ AV = \frac{-gm}{\frac{1}{R_d} + \frac{1}{Z_L}} \]

\[ = \frac{-gm}{\frac{1}{R_d} + \frac{Z_L}{Z_L}} \]

\[ = \frac{-gmR_dZ_L}{R_d + Z_L} \]

Assume \( Z_L' = R_d' = Y_d || Z_L \)

\[ AV = \frac{-gmZ_L}{R_d' + Z_L} = \frac{-gmR_d}{Y_d' + Z_L} \]

**Input Capacitance, \( C_i \):**

From input admittance,

\[ Y_i = Y_{gs} + Y_{gd} (1 - AV) \]

We know that \( AV = \frac{-gmR_d}{Y_d' + Z_L} \)

\[ Y_i = Y_{gs} + Y_{gd} (1 + \frac{gmR_d}{Y_d' + Z_L}) \]

\[ \Rightarrow C = \frac{1}{Y_i}, \quad Y = \frac{1}{Y_i} \]

For \( C_i \),

\[ \frac{1}{C_i} = \frac{1}{C_{gs}} + \frac{1}{C_{gd} (1 + gmR_d)} \]

\[ C_i = \frac{C_{gs} C_{gd} (1 + gmR_d)}{C_{gs} + C_{gd} (1 + gmR_d)} \]
4.8.3 High Frequency Response:

Fig. shows the equivalent circuit for CS MOSFET Amplifier.

Let us consider the output node. The load current is
\[ g_m v_{gs} - I_{gd} \]
where \( g_m v_{gs} \) is the output current of MOSFET and \( I_{gd} \) is the current supplied through very small capacitance \( C_{gd} \).

At frequencies in the vicinity of \( f_H \), the \( I_{gd} \) is very small and can be neglected.

Hence, \[ V_o = -I_L R_L = -g_m v_{gs} R_L \]
where \( R_L = \frac{V_o}{I_{gd}} \).

**Equivalent Circuit of CS MOSFET Amplifier.**

Now, consider the input node. We can replace \( C_{gd} \) at the input with the equivalent capacitance \( C_{eq} \) using Hiller's Theorem.

By Hiller's Theorem, equivalent capacitance is given by
\[ C_{eq} = (1 + AV) C = (1 + AV) C_{gd} \]
The low frequency response of a MOSFET amplifier is affected by three RC networks as shown in the figure.

1. The first RC network is the input RC network due to input coupling capacitance, source resistance, and gate resistance. The corner frequency due to input RC network is given by:

   \[ f_1 = \frac{1}{2\pi C_1(R_{si} + R_{gs})} \]

2. The second RC network is the output RC network due to the output coupling capacitance, drain resistance, and load resistance. The corner frequency due to output RC network is given by:

   \[ f_1' = \frac{1}{2\pi (R_D + R_L) C_2} \]

3. The third RC network is due to the bypass capacitance in the source terminal. The corner frequency due to the bypass RC network is given by:

   \[ f_1'' = \frac{g_m}{2\pi C_b} \]

The highest among these frequencies is the lower 3 dB frequency. Hostile gain roll-off, higher than other low-frequency rolloff, and hence, a 'low-pass' response.

\[ V_1 \]

\[ R_4 \]

\[ C_1 \]

\[ R_{si} \]

\[ R_{gs} \]

\[ D \]

\[ C_2 \]

\[ R_D \]

\[ R_L \]

\[ C_b \]

\[ g_m \]

\[ f_0 \]
The parallel combination of \( r_o \), \( r_d \) & \( r_L \) is given by \( Z_L' \)

\[
Z_L' = \frac{Z_L}{Z_L + Z_{L'}}
\]

Apply K\(\text{u} \)lloff's current law at node \( 'Y' \),

\[
I_{gd} + I_L = g_m V_{gs}
\]

Since \( I_{gd} \ll I_L \), \( I_{gd} \) can be neglected

\[
I_L = g_m V_{gs} \quad \rightarrow (1)
\]

Voltage gain \( A_V \) is given by

\[
A_V = \frac{V_o}{V_i} = \frac{V_o}{V_{gs}} \quad \left[ V_{gs} = V_i \right]
\]

\[
= \frac{J_0 Z_L'}{V_{gs}}
\]

\[
= -\frac{1}{g_m} \frac{Z_L'}{V_{gs}}
\]

\[
= -\frac{g_m V_{gs} Z_L'}{V_{gs}}
\]

\[
A_V = -g_m Z_L'
\]

The total resistance at the input is given by

\[
R_{si}' = R_{si} || R_{Q}
\]

By considering input circuit as a simple time constant circuit

\[
T = \frac{1}{R_{si}' C_{in}}
\]

where \( C_{in} \) is the total input capacitance given by

\[
C_{in} = C_{gs} + C_{eq} = C_{gs} + C_{gd} \left( 1 + g_m Z_L' \right)
\]

\[
\omega_n = \frac{1}{T} = \frac{1}{R_{si}' C_{in}}
\]

\[
f_n = \frac{1}{2\pi R_{si}' C_{in}}
\]
4.8.1. For a CS MOSFET Amplifier, \( R_s = 120 \, k\Omega \), \( R_G = 4.7 \, M\Omega \), \( R_D = 10 \, k\Omega \), \( R_L = 15 \, k\Omega \), \( g_m = 1.2 \, mA/V \), \( V_o = 150 \, k\Omega \), \( C_{gs} = 1 \, pF \) and \( C_{gd} = 0.3 \, pF \). Find the midband gain, \( A_m \) and upper 3dB frequency, \( f_H \).

Gain:

\[
A_m = \frac{-R_G}{R_0 + R_s}
\]

where \( R'_L = R_0 || R_D || R_L \)

\[
= 150 || 10 \, k\Omega || 15 \, k\Omega
\]

\[
= 5.77 \, k\Omega
\]

\[
A_m = -\frac{4.7 \times 10^6}{(4.7 \times 10^6 + (120 \times 10^3)} \times 1.2 \times 10^{-3} \times 5.77 \times 10^3
\]

\[
A_m = -6.75
\]

\[
C_{eq} = C_{gd} \left( 1 + g_m R'_L \right)
\]

\[
= 0.3 \times 10^{-12} \times (1 + 1.2 \times 10^{-3} \times 5.77 \times 10^3)
\]

\[
C_{eq} = 2.377 \, pF
\]

\[ C_{in} = C_{eq} + C_{gs} \]

\[ = (2.377 + 1) \, pF \]

\[ C_{in} = 3.377 \, pF \]

\[
\frac{1}{2 \pi f \text{c}} R_s \]

where \( \text{cin} R_s' = R_s || R_G \)

\[
= 120 \, k\Omega || 4.7 \, k\Omega = 117 \, k\Omega
\]

\[
f_H = \frac{1}{2 \pi R_s' C_{in}}
\]
EX. 4.8.2. For a CS HOSFET amplifier, \( C_1 = C_s = C_2 = 1 \mu F, R_0 = 12 \Omega, R_s = 180 \Omega \), \( g_m = 1.2 \text{ mA/V} \), \( R_D = 10 \text{ k}\Omega \) and \( R_L = 15 \text{ k}\Omega \). Calculate \( A_H, f_1, f_1', f_1'' \) and \( f_L \).

**Solution**:

(i) \( A_H = \frac{g_m R_L}{R_s + R_L} \)

\[ R_L' = \frac{R_D}{R_L} \]

\[ R_L'' = \frac{R_D}{R_L} \]

\[ R_L = 10 \text{ k}\Omega \parallel 15 \text{ k}\Omega \]

\[ R_L' = 6 \text{ k}\Omega \]

\[ \frac{12}{12 + 0.18} \times 1.2 \times 6 = -7.09 \]

(ii) \( f_1 = \frac{1}{2\pi (R_s + R_D) C_1} \)

\[ f_1 = 0.013 \text{ Hz} \]

(iii) \( f_1' = \frac{1}{2\pi (R_D + R_L) C_2} \)

\[ f_1' = 0.366 \text{ Hz} \]

(iv) \( f_1'' = \frac{g_m}{2\pi C_s} \)

\[ f_1'' = \frac{1.2 \times 10^{-3}}{2\pi \times 1 \times 10^{-6}} \]

\[ f_1'' = 190.98 \text{ Hz} \]

Since, \( f_1'' \) is larger among all other frequencies,

\[ f_L = f_1'' = 190.98 \text{ Hz} \]
Ex. 4.83: Calculate the unity gain frequency with \( g_m = 3 \text{mA/\( V \)} \), 
\( C_{gs} = 8 \text{pF} \), \( C_{gd} = 4 \text{pF} \) and \( C_{ds} = 1 \text{pF} \).

Solv: Unity gain frequency of MOSFET,

\[
\begin{align*}
\nu_T &= \frac{g_m}{2\pi (C_{gs} + C_{gd})} \\
&= \frac{3 \times 10^{-3}}{2\pi (8+4) \times 10^{-12}} \\
&= 39.8 \text{Hz}
\end{align*}
\]

Ex. 4.84: Determine the low frequency response of the amplifier circuit shown in Fig.

**Fig:** It is necessary to analyse each network to determine the critical frequency of the amplifier.

(i) Input RC network:

\[
\begin{align*}
\nu_c &= \frac{1}{2\pi R_{in} C_1} \\
R_{in} &= R_G || R_{in}(\text{gate}) \\
&= R_G || \left( \frac{V_{gs}}{I_{gs}} \right) \\
&= 100 \Omega || \frac{8}{80 \times 10^{-9}} \\
&= 100 \Omega || 100 \Omega \\
R_{in} &= 50 \Omega, \\
\nu_c &= \frac{1}{2\pi \times 50 \times 10^{-12} \times 0.001 \times 10^{-6}} \Rightarrow \nu_c = 3.18 \text{Hz}
\end{align*}
\]
(ii) Output RC network:

\[ f_c = \frac{1}{2\pi \sqrt{(R_D + R_L) C_2}} \]

\[ = \frac{1}{2\pi (2 \times 2k + 28k) \times 1 \times 10^{-6}} \]

\[ f_c = 6.577 \text{ Hz} \]

(iii) Bypass network:

Since there is no bypass RC network, it is not considered.

We have calculated two critical frequencies:

(i) \( f_c \) (input) = 3.18 Hz
(ii) \( f_c \) (output) = 6.577 Hz

It shows that the output network produces a dominant lower critical frequency.

---

**Exercise 4.8.5:** Calculate the unity gain bandwidth (in Hz) with \( g_m = 1.5 \text{ mA/V} \), \( C_{gs} = 9 \text{ pF} \), \( C_{gd} = 3 \text{ pF} \) and \( C_{ds} = 1 \text{ pF} \)

**Solution:**

Unity gain frequency \( f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})} \)

\[ = \frac{1.5 \times 10^{-3}}{2\pi (9 + 3) \times 10^{-12}} \]

\[ f_T = 19.89 \text{ Hz} \]
Rise Time & Its Relation to Upper Cut-Off Frequency:

Upper 3-dB Frequency:

When a step input is applied, the amplifier's high frequency RC networks prevent the output from responding immediately to the step input. The output voltage starts from zero and rises towards the steady state value $V$, with time constant $R_2C_2$.

The output voltage is given by

$$V_0 = V \left(1 - e^{-t_1/R_2C_2}\right)$$

The time required for $V_0$ to reach $\frac{1}{10}$th of its final value

$$0.1V = V \left(1 - e^{-t_1/R_2C_2}\right)$$

$$0.1 = 1 - e^{-t_1/R_2C_2}$$

$$e^{-t_1/R_2C_2} = 0.9$$

$$\frac{t_1}{R_2C_2} = 0.1$$

$$t_1 = 0.1R_2C_2$$

Similarly, the time required for $V_0$ to reach $\frac{9}{10}$th of its final value is

$$0.9V = V \left(1 - e^{-t_2/R_2C_2}\right)$$

$$0.9 = 1 - e^{-t_2/R_2C_2}$$

$$\frac{t_2}{R_2C_2} = 2.3$$

$$t_2 = 2.3R_2C_2$$
The difference between \( t_1 \) and \( t_2 \) is called rise time \( t_r \) of the circuit:

\[ t_r = t_2 - t_1 \]
\[ = 2.3 R_2 C_2 - 0.1 R_2 C_2 \]
\[ t_r = 2.2 R_2 C_2 \]

The upper 3dB frequency is given as:

\[ f_H = \frac{1}{2 \pi R_2 C_2} \]

Therefore, upper 3dB frequency can be represented in terms of rise time as:

\[ f_H = \frac{2.2}{2 \pi t_r} = \frac{0.35}{t_r} \]
\[ f_H = \frac{0.35}{t_1} \]

This implies that upper 3dB frequency is inversely proportional to rise time.

**Relation between Bandwidth and Rise Time:**

The frequency range from \( f_L \) and \( f_H \) is defined as bandwidth. Usually, \( f_L \ll f_H \).

\[ BW = f_H - f_L \]

We know that:

\[ f_H = \theta \frac{2.2}{2 \pi t_1} = \frac{0.35}{t_1} \]

Therefore:

\[ BW = \frac{0.35}{t_1} \]

**Example:**

If the rise time of a BJT is \( 35 \mu s \), what is the bandwidth that can be obtained using BJT?

\[ f_L = \frac{0.35}{f_2} = \frac{0.35}{BW} \]
\[ BW = \frac{0.35}{t_1} \]

\[ BW = \frac{0.35}{35 \times 10^{-9}} \]
\[ BW = 10 \text{ MHz} \]
SAG AND ITS RELATION TO LOWER CUT-OFF FREQUENCY:

The amplifier's low frequency RC network consists of coupling and bypass capacitors make amplifier's output to decrease with large time constant. As a result, the output voltage has sag or tilt associated with it.

The tilt or sag at time $t_1$ is given by

$$X_{tilt} = P = \frac{V - V'}{V} \times 100$$

$$= \frac{t_1}{R_1 C_1} \times 100\%.$$

The lower 3dB frequency can be determined from the output response by carefully measuring the tilt:

We know that, the lower 3dB frequency is given as, $f_l = \frac{1}{2\pi R_1 C_1}$

Therefore, lower 3dB frequency can be represented in terms of tilt as given below:

$$P = \frac{T}{2 R_1 C_1} \times 100$$

$$= \frac{1}{2\pi f R_1 C_1} \times 100$$

$$= \frac{\pi f l}{2\pi f R_1 C_1} \times 100$$

$$= \frac{\pi f t}{f} \times 100$$

$$P = \frac{\pi f t}{f} \times 100$$
**Problem**

For the circuit shown in Fig. 1, calculate the percentage tilt. Assume approximate h-parameter circuit for transistor.

\[
\begin{align*}
\text{for} & \quad f_L = \frac{1}{2 \pi R_L C_L} \\
R_L & = R_C + R_L = 4k\Omega + 2k\Omega = 6k\Omega \\
f_L & = \frac{1}{2 \pi \times 6 \times 10^3 \times 10 \times 10^{-6}} \\
f_L & = 2.65 \text{Hz} \\
\text{We know that,} & \quad \text{P} = \frac{\text{kHzx}100}{f} \\
\text{Assume} & \quad f = 200 \text{Hz}, \quad \text{P} = \frac{\pi \times 2.65 \times 100}{200} \\
& = 4.17.
\end{align*}
\]

**Ex.** For the circuit shown above, what is the lowest frequency square wave which suffers less than 2% tilt.

Given: \( P = 2\% \), \( f_L = 2.65 \text{Hz} \)

\[
\begin{align*}
f & = \frac{PF}{100} \\
f & = \frac{100 \times 2.65}{P} \\
& = \frac{100 \times 2.65}{2} \\
f & = 416.25 \text{Hz}
\end{align*}
\]
PROBLEMS FOR PRACTICE:

1. Determine the bandwidth of the amplifier circuit shown in Fig. The transistor parameters are $h_{fe} = 100$, $h_{ie} = 1.1k$ and $h_{ce} = h_{re} = 0$, $C_b'c = 10pF$ and $C_b'e = 1pF$.

SOLUTIONS:

(a) Low frequency analysis:

(i) Input RC network:

$$f_c \text{ (input)} = \frac{1}{2\pi \left( R_s + \left( R_1 || R_2 \right) h_{ie} \right) C_1}$$

$$= \frac{1}{2\pi \left( 680 + (68k || 22k || 1k) \right) \times 0.1 \times 10^{-6}}$$

$$= \frac{1}{2\pi \left( 680 + 1031.7 \right) \times 0.1 \times 10^{-6}} = 929.8 \text{ Hz}$$

(ii) Output RC network:

$$f_c \text{ (output)} = \frac{1}{2\pi \left( R_c + R_L \right) C_2}$$

$$= \frac{1}{2\pi \left( 2.2k + (10k) \right) \times 0.1 \times 10^{-6}} = 130.45 \text{ Hz}$$

(iii) Bypass RC network:

$$f_c \text{ (bypass)} = \frac{1}{2\pi \left( R_{th} || h_{ie} \right) C_{b'e}}$$

$$R_{th} = R_1 || R_2 || R_s = 680 || 680k || 22k = 653.28 \Omega$$

$$f_c \text{ (bypass)} = \frac{1}{2\pi \left( 653.28 + 1M \right) \times 10^{-6}}$$
Between the three RC networks, the input RC network produces the dominant lower critical frequency.

**High Frequency Analysis**

(i) **Input RC Network**:

\[
\begin{align*}
\mathbf{S}_h (\text{Input}) &= \frac{1}{2\pi (R_s/R_1/R_2||\text{hie}) (C_{bb'}e + C_{ni})} \\
R_s/R_1/R_2||\text{hie} &= 680 || 68K || 22K || 1K = 1.03K \\
\text{Av} &= -h_{fe} \frac{(R_e||R_L)}{\text{hie}} = \frac{-100 (22K||10K)}{1K} = -163.93 \\
C_{hi} &= (1 - \text{Av}) C_{b'c} = \left[1 - \left(-\frac{163.93}{163.93}\right)\right] \times 10 \times 10^{-12} \\
&= 1.65 \times 10^{-9} \\
\mathbf{S}_h (\text{Input}) &= \frac{1}{2\pi (1.03K||1P + 10P)} \\
\mathbf{S}_h (\text{Input}) &= 221.9 \text{ MHz}
\end{align*}
\]

(ii) **Output RC Network**:

\[
\begin{align*}
\mathbf{S}_h (\text{Output}) &= \frac{1}{2\pi (R_{e||R_L}) C_{ho}} \\
C_{ho} &= \left(\frac{1}{\text{Av}}\right) C_{b'c} = \left(-\frac{163.93}{-163.93}\right) \times 10 \times 10^{-12} \\
&= 10 \text{ pF} \\
\mathbf{S}_h (\text{Output}) &= \frac{1}{2\pi (2.2K||10K) \times 10 \times 10^{-12}} \\
\mathbf{S}_h (\text{Output}) &= 8.84 \text{ MHz}
\end{align*}
\]

Among above two RC networks, the output produces dominant upper critical frequency.
Hence, Bandwidth = 8.84\,\text{Hz} - 929.8\,\text{Hz}

Bandwidth = 8.39\,\text{Hz}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{frequency_response.png}
\caption{Frequency Response of CE Amplifier}
\end{figure}

2. For the amplifier shown in Fig. obtain the high frequency response. Assume the values of internal capacitances as follows:

- \( C_{bc} = 10\,\text{pf} \)
- \( C_{be} = 1\,\text{pf} \)
- The h-parameters are \( h_{fe} = 100 \), \( h_{ie} = 1.1\,\text{K} \), \( h_{re} = h_{oe} = 0 \).

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{amplifier_circuit.png}
\caption{Amplifier Circuit}
\end{figure}

The voltage gain, \( A_v = \frac{-h_{fe}}{R_1\|R_2} \) = \(-100\ \frac{3.3\,\text{K}}{2.2\,\text{K}}\) \text{ since } \frac{h_{ie}}{1.1}\,\text{K}

Since it is a CE amplifier with bypassed \( R_E \):

\[ A_v = -261 \]

\[ C_{\text{hi}} = (1 - A_v) \, C_{bc} = \left(1 - 261\right) \times 10 \times 10^{-12} = 2620\,\text{pf} \]

\[ C_{\text{ho}} = \frac{1 - A_v}{A_v} \, C_{be} = \frac{1 - 261}{261} \times 10 \times 10^{-12} = 10\,\text{pf} \]
1. Input RC Network:

\[ S_H(\text{input}) = \frac{1}{2\pi (R_3 + R_1 + R_2 + \text{hie}) \left( \frac{1}{C_e} + \frac{1}{C_{hi}} \right)} \]

\[ R_3 || R_1 || R_2 || \text{hie} = 10 \, \text{k} || 40 \, \text{k} || 1 \, \text{k} = 490 \, \text{ohm} \]

\[ S_H(\text{input}) = \frac{1}{2\pi (490) \times (1 + 2 \times 10^5) \times 10^4} \]

\[ S_H(\text{input}) = 123.9 \, \text{KHz} \]

2. Output RC Network:

\[ S_H(\text{output}) = \frac{1}{2\pi (R_c || R_L) C_m} = \frac{1}{2\pi (3.3 \, \text{k} || 2.2 \, \text{k}) \times 10^6} \]

\[ S_H(\text{output}) = 5.56 \, \text{MHz} \]

The input RC network is the dominant network.

3. Find the midband gain \( A_H \) and the upper 3dB frequency \( f_H \) of a CS amplifier fed with a signal source having an internal resistance \( R_{ss} = 100 \, \text{kH} \). The amplifier has \( R_g = 47 \, \text{M} \), \( R_o = R_L = 15 \, \text{k} \), \( f_m = 1 \, \text{MHz} \), \( y_o = 150 \, \text{ps} \), \( c_{gs} = 1 \, \text{pF} \) and \( c_{gd} = 0.4 \, \text{pF} \).

\[ A_H = \frac{-R_g}{R_g + R_{ss}} \]

\[ Z_L = y_o || R_o || R_L = 150 \, \text{k} || 15 \, \text{k} || 15 \, \text{k} = 7.14 \, \text{k} \]

\[ R_m Z_L = 1 \times 10^{-5} \times 7.14 \times 10^3 = 7.14 \]

\[ A_H = \frac{-4.7 \times 10^5}{(4.7 + 1) \times 10^3} \times 7.14 = -7 \]

\[ A_H = -7 \]

\[ C_{eq} = (1 + g_m Z_L) c_{gd} \]

\[ C_{eq} = (1 + 7.14) \times 0.4 = 3.28 \, \text{pF} \]

\[ C_m = c_{gs} + C_{eq} \]

\[ R_{ss} = R_{ss} || R_g \]

\[ f_H = \frac{1}{2\pi (2.2 \times 9.7 \times 10^6 \times 4.2 \times 10^12) \times 10^3} \]

\[ f_H = 0.38 \, \text{MHz} \]
TWO MARKS:

1. Draw a hybrid-pi model for BJT.

A: 

[Diagram of BJT hybrid-pi model]

Dec-02, 06, 10, May-11, 16

2. What is the relationship between bandwidth and rise time? 

A: Bandwidth, \( BW = \frac{0.35}{t_r} \) where \( t_r \) = rise time

May-03, 02, 17

3. What does rise time indicate? How is it related to upper 3dB frequency? 

A: The rise time is an indication of how fast the amplifier can respond to a discontinuity in the input voltage.

\[ f_H = \frac{0.35}{t_r} \]

Dec-03

4. What are the high frequency effects? 

A: At high frequencies, the coupling and bypass capacitors act as short circuits which do not affect the frequency response. The junction capacitors/ internal capacitors come into play reducing the circuit gain.

May-04

5. Define \( f_t \) in a high frequency transistor. 

A: \( f_t \) is defined as the frequency at which CE short circuit current gain becomes unity.

May-06

6. Define rise time. 

A: It is the time required for the signal to change from 10% to 90% of its value.

Dec-07, 08, 0, 13, 14

7. Define say in an amplifier. 

A: Due to lack of low frequency response, the amplifier's output...
8. Draw a high frequency equivalent circuit for a BJT. **Sec-04, 12**
A: Refer Ch. 9.

9. If the rise time of a BJT is 0.5 ns, what is the bandwidth that can be obtained using this BJT? **May-05**
A: Refer Ex.

10. What is the significance of octaves and decades? **Dec-06**
A: The octaves and decades are the measures of change in frequency. A ten times change in frequency is called a decade. An octave corresponds to a doubling or halving of the frequency.

11. What is bandwidth of an amplifier? **Dec-07, 08, 09, May-09, 13**
A: The bandwidth of an amplifier is defined as the difference between the lower cut-off frequency and upper cut-off frequency.

   \[ BW = f_H - f_L \]

12. Draw the general frequency response of an amplifier. **Dec-07, 15**

   ![Frequency Response Curve]

13. Discuss the effect of bypass capacitor on frequency response of an amplifier. **May-09, 15, 17**
A: At low frequencies, the capacitor does not act as a short circuit. It creates an impedance \( Z_E \) in case of BJT and \( Z_S \) in case of JFET which reduces the circuit gain and overall voltage.

14. Give the expressions for gain bandwidth product for voltage and current. **May-10**
14. The gain-bandwidth product for voltage gain is given by
\[ |A_{\text{v low f}}| = \frac{R_L}{R_s + R_b} \times \frac{f_T}{1 + 2\pi f_T C_C R_L} \]
The gain-bandwidth product for current gain is given by
\[ |A_{\text{i low f}}| = \frac{f_T}{1 + 2\pi f_T C_C R_L} \times \frac{R_s}{R_s + R_b} \]

15. Why is it not possible to use h-parameters at high frequencies? Why?
A: The reasons why h-parameters are not used at high frequencies are
(i) The values of h-parameters are not constant at high frequencies.
(ii) It is necessary to analyze transistor at each and every frequency, which is impracticable.
(iii) h-parameters are complex at high frequencies.

16. If the rise time of a BJT is 40ns, what is the bandwidth that can be obtained using BJT?
A: \[ t_r = \frac{0.35}{f_2} \]
\[ f_2 = \frac{0.35}{t_r} = \frac{0.35}{40 \times 10^{-9}} \]
\[ f_2 = 8.75 \text{MHz} \]

17. What is meant by gain-bandwidth product? Dec-12, Hay-10
A: Refer 2 Marks Q14.

18. What is the effect of Miller's capacitance on the frequency response of amplifiers? Dec-14
A: The capacitance connected between input and output \( C_b'c \) cannot be split into separate input and output capacitance as \( C_b'c (1 - k) \) and \( C_b'c \frac{K}{K-1} \) respectively. As a result, input capacitance is increased, and the output capacitance is reduced.
19. Mention the effect of coupling capacitors on the bandwidth of an amplifier.

A: \[ X_c = \frac{1}{2\pi f C_c} \]

- \( C_c \) - coupling capacitor

When frequency increases, \( X_c \) decreases and vice versa.

So at lower frequencies, the coupling capacitors act as a short circuit and at high frequencies, it reduces the gain of an amplifier.


A: The frequency response can be defined as the variation of output quantity with respect to input signal frequency. In other words, it is defined as the graph drawn between input frequency and gain of an amplifier.

21. Define beta cut-off frequency

A: Beta cut-off frequency \( f_c \) is defined as the frequency at which the transistor \( CE \) current gain drops by 3dB or \( \frac{1}{\sqrt{2}} \) of its value at low frequencies.

\[ f_c = \frac{g_m}{2\pi f_c C_c (I_c)} \]

22. The midband gain of an amplifier is 100 and the half power frequencies are \( f_l = 40 \text{ Hz} \) and \( f_h = 16 \text{ kHz} \). Calculate amplifier gain at 20 kHz and 20 kHz.

A:

\[ A = \frac{100}{\sqrt{1 + \left(\frac{f}{f_l}\right)^2}} \]

At \( f = 20 \text{ Hz} \), below midband:

\[ A = \frac{100}{\sqrt{1 + \left(\frac{20}{40}\right)^2}} = \frac{100}{\sqrt{1 + 0.25}} = \frac{100}{1.5} = 66 \text{ dB} \]

At \( f = 20 \text{ kHz} \), above midband:

\[ A = \frac{100}{\sqrt{1 + \left(\frac{20}{16000}\right)^2}} \approx \frac{100}{\sqrt{1 + 0.0000625}} = 62.46 \text{ dB} \]
23. What is Miller effect? Dec-17 | May-14/15
A: Any internal electrode connected between input and output can be separated into input and output circuits separately. This effect is known as Miller effect (or) Miller's Theorem.

24. What is unity gain amplifier? Dec-17
A: An amplifier with gain is 1 is called as unity gain amplifier.

25. A bipolar transistor has parameters β = 150, Cc = 2pF, εp = 0.3pF and it is biased at Ic = 0.5mA. Determine β-cut-off frequency. May-16
A: \( f_b = \frac{g_m}{2 \pi f_h C} (C_{c+} C_{}) \)
\[ f_b = \frac{1.92 \times 10^{-3}}{2 \pi \times 150 (2+0.3) \times 10^{12}} \]
\[ f_b = 8.87 \text{ MHz} \]

26. What is the reason for reduction in gain at lower and higher frequencies of an amplifier? Dec-16
A: The coupling capacitor offers low impedance at high frequency thus reduces the input signal and so the gain falls. Similarly, at low frequency, it provides high impedance so it allows only a small signal from one to next stage. As a result, gain rolls off at low and high frequencies.

27. Find the unity gain bandwidth of MOSFET whose \( g_m = 6 \text{ mA/V} \), \( C_{gs} = 8 \text{ pF} \), \( C_{gd} = 4 \text{ pF} \) and \( C_{gb} = 1 \text{ pF} \). May-15
A: Unity gain frequency, \( f_t = \frac{g_m}{2 \pi (C_{gs} + C_{gd})} \)
\[ f_t = \frac{6 \times 10^{-3}}{2 \pi (8+4) \times 10^{12}} \]
\[ f_t = 49.57 \text{ MHz} \]
38. Why common base amplifiers are preferred for high frequency signal when compared to common emitter amplifiers? Sec-10

A: On grounding the base in CB makes the base act as shield between input emitter and output collector. This shield eliminates the capacitive coupling that cause oscillation whereas in CE there is no shielding, so capacitive coupling is not eliminated. So CB amplifiers is preferred at high frequency than CE amplifiers.

38. Calculate the amplification factor $\mu$ of FET if $V_{gd} = 4 \text{V}$ and $g_m = 4 \text{mS}$

\[ A = \frac{g_m V_{gd}}{\text{V}} \]

\[ A = \frac{4 \times 10^{-3} \times 4 \times 10^{-6}}{2} \]

\[ A = 0.6 \]

39. Two stage of a multistage amplifier have a gain of 50 and 20. What is the effective voltage gain in dB? Sec-15

A: Effective voltage gain $A_v = A_{v1} \cdot A_{v2}$

\[ A_v = 50 \times 20 \]

\[ A_v = 1000 \]

In dB, $A_v \text{ dB} = 80 \log 1000$

\[ A_v \text{ dB} = 60 \]

40. Two amplifiers having gain 20 dB and 40 dB are cascaded. Find the overall gain in dB. Sec-07

A: Overall gain in dB = $20 \text{ dB} \times 40 \text{ dB}$

\[ = 800 \text{ dB} \]

41. The ac schematic of an NMOS common source stage is shown in figure. Where part of biasing circuits has been omitted for simplicity for the n-channel MOSFET H1, the transconductance $g_m = 1 \text{ mA/V}$, and the body effect and the channel length modulation effect are to be neglected. Find the lower cut-off frequency. May-15
A: By low frequency analysis of FET,

(i) \( f_1 = \frac{1}{2\pi C_1 (R_1 + R_2)} \)

Since there is no capacitance effect across input, it can be neglected.

(ii) \( f_2 = \frac{1}{2\pi (R_D + R_L) C_2} \)

\[ f_2 = \frac{1}{2\pi (1x10^5) \times 1x10^6} \]

\( f_2 = 14.48 \text{ Hz} \)

(iii) \( f_3 = \frac{g_m}{2\pi C_S} \)

\[ f_3 = \frac{1x10^{-3}}{2\pi \times 1x10^{-6}} \]

\( f_3 = 159.15 \text{ Hz} \)

Since \( f_2 > f_1 \), \( f_L = f_1 = 159.15 \text{ Hz} \)
**Introduction:** This Rectifier circuit consists of Resistive load, rectifying element (i.e) P-N Junction diode and Source of a.c. Voltage, all connected in Series. To obtain the desired d.c. Voltage across the load, a.c. Voltage is applied to rectifier circuit using suitable Step-up or Step-down Transformer.

\[ E = E_{sm} \sin \omega t \quad \omega = 2\pi f \]

\[ \frac{N_2}{N_1} = \frac{E_{sm}}{E_{pm}} \]

\( E_{pm} \) = Peak Value of Secondary & Primary a.c. Voltage.

**Fig.(a): Forward Biased**

Operation:- +ve Half Cycle  
\( A \) Becomes +ve with B  
Diode - Forward Biased  
Current - Clockwise direction

**Fig.(b): Reverse Biased**

Operation:- -ve Half Cycle  
\( A \) is -ve with B  
Diode - Reverse Biased  
Current - No current flows

\[ I_m = \frac{E_{sm}}{R_f + R_L + R_d} \]

\( R_L \) = Resistance of Secondary winding of transformer  
\( R_d \) = Forward Resistance of diode
1) **Average (en) d.c. Value of Load**

\[ i_d = i_m \sin \omega t, \quad 0 \leq \omega t \leq \pi, \]
\[ i_d = 0, \quad \pi \leq \omega t \leq 2\pi \]

\[ i_{dc} = \frac{1}{2\pi} \int_0^{2\pi} i_d \, d(\omega t) \]

\[ = \frac{1}{2\pi} \int_0^{2\pi} i_m \sin(\omega t) \, d(\omega t) \]

As no current flows during

- We Half cycle \( \omega t = \pi \) to \( 2\pi \)

\[ i_{dc} = \frac{i_m}{2\pi} \int_0^{\pi} \sin \omega t \, d\omega t \]

\[ = \frac{i_m}{2\pi} \left[-\cos \omega t\right]_0^\pi \]

\[ i_{dc} = \frac{i_m}{2\pi} \left[-1 - 1]\right] \]

\[ \therefore \quad i_{dc} = \frac{i_m}{\pi} \]

\[ \boxed{\text{Current (I_{dc})}} \]

\[ \boxed{P_{dc} = E_{dc} \cdot I_{dc} = \frac{I_m^2}{\pi} \cdot R_L} \]

\[ = \frac{i_m^2}{\pi^2} \cdot R_L \Rightarrow \frac{i_m^2}{\pi^2} \cdot R_L \]

\[ P_{dc} = \frac{E_{sm} \cdot R_L}{\pi^2 \left[R_f + R_L + R_s\right]} \]

2) **A.C. Power Input \( (P_{ac}) \)**

\[ P_{ac} = 2IRms \left[R_L + R_f + R_s\right] \]

\[ IRms = \frac{i_m}{\sqrt{2}} \]

\[ P_{ac} = \frac{i_m^2}{4} \left[R_L + R_f + R_s\right] \]

3) **Rectifier Efficiency**

\[ \eta = \frac{P_{dc}}{P_{ac}} \Rightarrow \text{D.c. Output Power} \]

\[ \Rightarrow \frac{i_m^2}{\pi^2} \cdot R_L \Rightarrow \left(\frac{4}{\pi^2}\right) \cdot R_L \]

\[ \frac{i_m^2}{4} \left[R_f + R_L + R_s\right] \left[R_f + R_L + R_s\right] \]

\[ \therefore \quad R_L \Rightarrow \eta = \frac{0.406}{1 + \left(\frac{R_f + R_s}{R_L}\right)} \]

\[ \% \eta_{max} = 0.406 \times 100 \Rightarrow 40.6\% \]

4) **Ripple Factor**

Output of Halfwave rectifier is not pure d.c but pulsating d.c. The output contains pulsating components called ripples.

The measure of ripples present in the output is with the help of a factor called ripple factor, denoted by \( \gamma \).

Smaller the ripple factor closer is the output to a pure d.c.
Ripple factor: It is defined as the ratio of R.M.S. Value of the a.c. component in the output to the average or d.c. component present in the output.

\[ Y = \frac{\text{R.M.S. Value of a.c. Component of Output}}{\text{Average or d.c. Component of Output}} \]

\[ I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2} \]

\[ I_{rms} = \sqrt{I_{ac}^2 + I_{dc}^2} \]

\[ Y = \frac{I_{ac}}{I_{dc}} \]

\[ Y = \sqrt{\frac{I_{rms}^2}{I_{dc}^2}} - 1 \]

\[ Y = \sqrt{\left(\frac{I_m}{I_d}\right)^2 - 1} = \sqrt{\left(\frac{N_o}{N_i}\right)^2 - 1} \]

\[ Y \text{ is Very High.} \]

Peak Inverse Voltage (PIV): It is the peak voltage across the diode in the reverse direction (i.e., when the diode is reverse biased). This is called PIV rating of a diode.

PIV of diode = Esin for Half-Wave Rectifier

Voltage Regulation:

\[ \% \text{ Voltage Regulation} = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}} \times 100 \]

\[ (V_{dc})_{NL} = \frac{E_{sm}}{\pi} \]

\[ (V_{dc})_{FL} = I_{dc} \cdot R_L = \frac{I_m}{n} \cdot R_L \]

\[ E_{sm} \times R_L \]

\[ \frac{E_{sm}}{R_f + R_s + R_L} \]

\[ R = \frac{E_{sm} - R_L}{R_f + R_s + R_L} \times 10 \]

\[ R = \frac{R_f + R_s \times 100}{R_f + R_s + R_L} \]

Transformer Utilization Factor (T.U.F.):

\[ T.U.F. = \frac{D.C. \text{ Power Delivered to the Load}}{A.C. \text{ Power Rating of the Transformer}} \]

\[ P_{dc} = I_{dc}^2 R_L \Rightarrow (\frac{I_m}{\pi})^2 R_L \]

A.C. Power Rating of Transformer:

\[ E_{rms} \times I_{rms} = \frac{E_{sm}}{\sqrt{2}} \cdot I_{sm} = E_{sm} \cdot I_{sm} \]

\[ T.U.F. = \frac{I_m^2}{R_f^2 \cdot \frac{R_f}{2} + \frac{I_m^2}{R_L} \cdot R_L} \]

\[ T.U.F. = 0.287 \]

Advantages:

a) Only one diode is sufficient
b) Ckt is easy to design
c) No Centre Tap on Transformer is necessary

Disadvantages:

a) Ripple factor of Half-Wave Ckt is 1.21, which is high
b) Max. Rectification efficiency is 40%, which is low
c) T.U.F is low showing that transformer is not fully utilized
**FULL WAVE RECTIFIER**:

**Introduction**:
- It conducts during both positive and negative half cycles of input a.c. input, two diodes are used in this circuit.
- The diodes feed a common load $R_L$ with the help of a centre tap transformer. The a.c. voltage is applied through a suitable power transformer with proper turns ratio.

**Operation**:
- **(+)Half cycle**
  - $A$ is $+$ve, $B$ is $-$ve.
  - $(\text{Conduct})$ Diode $D_1 \rightarrow$ Forward biased
  - $(\text{Not Conduc})$ Diode $D_2 \rightarrow$ Reverse biased
  - Open C.Kts.

- **(-)Half cycle**
  - $A'$ is $-$ve, $B'$ is $+$ve.
  - $(\text{Conduct})$ Diode $D_2 \rightarrow$ Forward biased
  - $(\text{Not Conduc})$ Diode $D_1 \rightarrow$ Reverse biased

"Load current flows in both the half cycles of ac voltage and in the same direction through the load resistance."

**Maximum Load current**:
- $I_m = \frac{E_m}{R_s + R_f + R_L}$
- $R_f$ = Forward Resistance
- $R_s$ = Winding Resistance
- $I_m$ = Maximum Load current
- $E_m$ = Max. Value of a.c. i/p voltage of Secondary

**D.C. Load current**:
- $I_L = I_m \sin \omega t$, $0 \leq \omega t \leq \pi$
- $I_{av} = I_{DC} = \frac{1}{\pi} \int_{0}^{\pi} I_L \, d(\omega t) = \frac{1}{\pi} \int_{0}^{\pi} I_m \sin \omega t \, d\omega t$
- $= \frac{I_m}{\pi} \left[ -\cos \omega t \right]_0^\pi$
- $= \frac{I_m}{\pi} \left[ 1 - (-1) \right] = \frac{2I_m}{\pi}$

**Average D.C. Load Voltage** ($E_{dc}$):
- $E_{dc} = I_{DC} \cdot R_L = 2I_m R_L$
\[ E_{dc} = \frac{2 \alpha E_{sm} R_L}{R_L + R_f + R_s + R_L} = \frac{2 \alpha E_{sm}}{R_f + R_s + R_L} \]

\[ R_f + R_s < < \frac{1}{R_L} \]

\[ E_{dc} = \frac{2 \alpha E_{sm}}{R_f + R_s + R_L} \]

**RMS Load Current (I_{RMS}):**

\[ I_{RMS} = \sqrt{\frac{1}{\pi} \int_0^{2\pi} i_L^2 \, dt} \]

\[ = \sqrt{2 \times \frac{1}{\pi} \int_0^{\pi} \sin^2 \omega t \, dt} \]

\[ = \frac{I_m}{\sqrt{2}} \]

\[ E_{RMS} = I_{RMS} \cdot R_L = I_{RMS} \cdot R_L \]

**DC Power Output (P_{dc}):**

\[ P_{dc} = \frac{2 I_m^2}{\pi} R_L \]

\[ = \frac{4 E_{sm}}{\pi^2} \cdot \frac{R_L}{R_s + R_f + R_L} \]

\[ P_{dc} = \frac{4 E_{sm}}{\pi^2} \cdot \frac{R_L}{R_s + R_f + R_L} \]

**AC Power Input (P_{ac}):**

\[ P_{ac} = I_{RMS}^2 \left( R_f + R_s + R_L \right) \]

\[ \left( \frac{I_m}{\sqrt{2}} \right)^2 \left( R_f + R_s + R_L \right) = \frac{I_m^2 (R_f + R_s + R_L)}{2} \]

\[ P_{ac} = \frac{E_{sm}^2}{2} \cdot \frac{1}{R_f + R_s + R_L} \]

\[ P_{ac} = \frac{E_{sm}^2}{2} \cdot \frac{1}{R_f + R_s + R_L} \]

**Rectified Efficiency (\eta):**

\[ \eta = \frac{P_{dc} \text{ output}}{P_{ac} \text{ input}} = \frac{4 I_m^2 R_L}{2 \alpha E_{sm}^2} \]

\[ \frac{R_f + R_s}{R_L} < < 1 \]

\[ \frac{8 R_L}{\pi^2 (R_f + R_s + R_L)} \]

\[ \eta = \frac{8 R_L}{\pi^2 (R_f + R_s + R_L)} \]

\[ \Rightarrow \eta = 0.48 \]

**Ripple Factor:**

\[ y = \sqrt{2} \frac{I_{rms}}{I_{dc}} - 1 \]

\[ I_{rms} = I_m / \sqrt{2} \]

\[ I_{dc} = 2 I_m / \pi \]

\[ y = \sqrt{\left( \frac{I_m \pi}{2 I_m} \right)^2 - 1} \]

\[ y = 0.48 \]

**Peak Inverse Voltage (PIV):**

\[ PIV = \frac{2 \alpha E_{sm}}{\pi} \]

**Ripple Frequency:**

\[ f_r = f_0 \left( 1 + 1 \frac{1}{2} \right) \]

\[ \Rightarrow I_m \left[ \frac{2}{\pi} - \frac{4 \cos 2\omega t - 4 \cos 4\omega t}{15\pi} \right] \]

**Ripple Amplitude is at Hz:**

**Voltage Regulation:**

\[ V_{dc} \text{ (NL)} = \frac{2 \alpha E_{sm}}{\pi} \]

\[ V_{dc} \text{ (FL)} = \frac{I_{dc} R_L}{100} \]

\[ \% R = \frac{(V_{dc}) \text{ NL} - (V_{dc}) \text{ FL}}{(V_{dc}) \text{ NL}} \times 100 \]

\[ \% R = \frac{Q E_{sm} - I_{dc} R_L}{100} \]

\[ \left( \frac{I_m}{R_f + R_s + R_L} \right) \]

\[ E_{sm} = \frac{I_m}{R_f + R_s + R_L} \]

\[ I_{dc} = 2 I_m / \pi \]

\[ \frac{E_{sm}^2}{(R_f + R_s + R_L)} \]

\[ \frac{E_{sm}^2}{(R_f + R_s + R_L)} \]

\[ \frac{2 I_m}{\pi} \]
(X) Transformer Utilization Factor $(T.U.F.):$
\begin{align*}
\text{Secondary} &= \frac{\text{D.C. power to the load}}{\text{A.C. power rating of Secondary}} \\
&= \frac{I^2 \cdot RL}{E_{m} \cdot I_{m}} \Rightarrow \left(\frac{I}{I_{m}}\right)^2 \cdot \frac{RL}{E_{m}} \\
&= \frac{I^2 \cdot RL}{E_{m} \cdot I_{m}} \Rightarrow \frac{I^2}{I_{m}^2} \cdot \frac{RL}{E_{m}} \\
&= \frac{I^2 \cdot RL}{E_{m} \cdot I_{m}} \Rightarrow 2 \cdot 0.574 = 0.673
\end{align*}

(XII) Advantages:
- A) D.C. Load Voltage and current are more than H.T.E.
- B) No D.C. current through transformer windings
- C) T.U.F. is better as transformer losses are less.
- D) Efficiency is higher
- E) Ripple factor is less
- F) D.C. power output

(XIII) Disadvantages:
- A) Cost of centre tap transformer is higher.
- B) Higher D.P.R. diodes are larger in size and costlier.
- C) P.I.R. rating of diode is higher.

Bridge Rectifier:
It is essentially a full-wave rectifier circuit using four diodes forming the four arms of an electrical bridge.

To one diagonal of the bridge, the a.c. voltage is applied through a transformer if necessary, and the rectified d.c. voltage is taken from the other diagonal of the bridge.

Main advantage of this circuit is that it does not require a centre tap on secondary winding of the transformer.

\[ \text{Fig. Bridge Rectifier} \]

Operation: $+ve$ half of a.c. input voltage:
- Diode $D_1 \& D_2 \rightarrow$ forward biased
- Diode $D_3 \& D_4 \rightarrow$ reverse biased
- $D_1 \& D_2 \rightarrow$ Conduct in series with load & current
In Negative Half Cycle
B \rightarrow +ve, D_3 \& D_4 Diode - forward biased
D_1 \& D_3 Diode - reverse biased.
Diode D_3 \& D_4 conduct in series with load & current.

\( I_m = \frac{E_{sm}}{R_s + 2R_f + R_L} \)
\( P_{dc} = \frac{I_{dc}^2 R_L}{\sqrt{2}} = \frac{4}{\sqrt{2}} \frac{I_m^2 R_L}{(R_s + 2R_f + R_L)} \)
\( P_{ac} = \sqrt{2} I_{rms} \left[ \frac{R_s + 2R_f + R_L}{2} \right] = \frac{I_m^2 \left[ 2R_f + R_s + R_L \right]}{\sqrt{2}} \)
\( \eta = \frac{8RL}{\pi^2 \left[ R_s + 2R_f + R_L \right]} \)
\( \% \eta_{max} = 81.2 \% \)
\( \gamma = 0.48 \text{ T.U.F.} = 0.812 \)

Advantages:
(a) No Centre tap is required in the transformer secondary.
(b) Transformer gets utilized effectively.
(c) As 2 Diodes conduct in series in each half cycle, inverse voltage appearing across diode get shared.
(d) Current in both primary & secondary of power transformer is in either of the two half cycles & hence for a given power output, power transformer of small size & less cost.

Applications: In power supply circuits, in rectifiers type helps to convert a.c. voltage to be measured to d.c. used as rectifier in power circuits to convert a.c to d.c.

Question: Explain the working of bridge rectifier. Despite the expression for R.M.S. Current, pure Ripple factor & efficiency (\%\(\eta\))
What are the Adv & Dis Adv of Bridge Rectifier? 

1. Derive the expression for the Rectification efficiency, Ripple factor, Transformer utilization factor, form factor and peak factor of Halfwave Rectifier. 
2. Draw and explain the working of Halfwave Rectifier. 
3. Draw and explain the Blooming of Fullwave Rectifiers & derive all the parameters. 

**Answers:**
[above] 
[May-10, Dec-11, Dec-02, Dec-06, May-12, May-14]

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Parameter</th>
<th>Half Wave</th>
<th>Full Wave</th>
<th>Bridge Rectifier</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>No. of diodes</td>
<td>1</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>2.</td>
<td>Ripple frequency</td>
<td>50Hz</td>
<td>100Hz</td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td>PIV rating of diode</td>
<td>E_{Sm}</td>
<td>2E_{Sm}</td>
<td>E_{Sm}</td>
</tr>
<tr>
<td>4.</td>
<td>Avg D.C Current (I_{Dc})</td>
<td>(\frac{I_{m}}{\pi})</td>
<td>(\frac{2I_{m}}{\pi})</td>
<td>(\frac{2I_{m}}{\pi})</td>
</tr>
<tr>
<td>5.</td>
<td>Avg D.C Voltage (E_{Dc})</td>
<td>(\frac{E_{Sm}}{\pi})</td>
<td>(\frac{2E_{Sm}}{\pi})</td>
<td>(\frac{2E_{Sm}}{\pi})</td>
</tr>
<tr>
<td>6.</td>
<td>R.M.S Current (I_{rms})</td>
<td>(\frac{I_{m}}{\sqrt{2}})</td>
<td>(\frac{I_{m}}{\pi})</td>
<td>(\frac{I_{m}}{\pi})</td>
</tr>
<tr>
<td>7.</td>
<td>D.C power output (P_{Dc})</td>
<td>(\frac{I_{m}^2 R_{L}}{\pi^2})</td>
<td>(\frac{4I_{m}^2 R_{L}}{\pi^2})</td>
<td>(\frac{4I_{m}^2 R_{L}}{\pi^2})</td>
</tr>
<tr>
<td>8.</td>
<td>Tu.F</td>
<td>0.287</td>
<td>0.693</td>
<td>0.812</td>
</tr>
<tr>
<td>9.</td>
<td>A.C. power output (P_{AC})</td>
<td>(\frac{I_{m}^2 (R_{L}+R_{S}+R_{P})}{\pi^2})</td>
<td>(\frac{I_{m}^2 (R_{F}+R_{S}+R_{L})}{2})</td>
<td>(\frac{I_{m}^2 (R_{F}+R_{S}+R_{L})}{2})</td>
</tr>
<tr>
<td>10.</td>
<td>Maximum rectifier efficiency (\eta)</td>
<td>40.67%</td>
<td>81.27%</td>
<td>81.27%</td>
</tr>
<tr>
<td>11.</td>
<td>Maximum Load Current (I_{m})</td>
<td>(\frac{E_{Sm}}{R_{S}+R_{F}+R_{L}})</td>
<td>(\frac{E_{Sm}}{R_{S}+R_{F}+R_{L}})</td>
<td>(\frac{E_{Sm}}{R_{S}+2R_{F}+R_{L}})</td>
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<tr>
<td>12.</td>
<td>Ripple factor (\nu)</td>
<td>1.21</td>
<td>0.482</td>
<td>0.482</td>
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</table>

**Answer:**
Compare all the parameters with the Bridge Full Wave, Half Wave Rectifiers. 

[above]
A Bridge Rectifier is applied with output from a step down transformer having turns ratio 8:1 and input 230V, 50Hz. If the $R_f = 1.2$, $R_s = 10\Omega$ and $R_L = 2\Omega$, find each diode power output, (2) PIV across each diode, (3) % efficiency, (4) % regulation at full load.

\[ P_{dc} = \frac{I_{dc}}{R_L} = \left(12.859 \times 10^{-3}\right)^2 \times 2 \times 10^{-3} = 0.3357W \]

\[ \text{PIV} = E_{Sm} = 40.6586V \]

\[ P_{ac} = \left(\frac{I_{rms}}{\sqrt{2}}\right)^2 \left(2R_f + R_s + R_L\right) = \frac{20.12 \times 10^{-3}}{\sqrt{2}} \left(2012\right) = 0.406W \]

\[ \% \text{Efficiency} = \frac{P_{dc} \times 100}{P_{ac}} = 80.56\% \]

\[ V_{dc, no load} = \frac{2E_{Sm}}{25.884\Omega} = 2.82V \]

\[ V_{dc, full load} = I_{dc} \times R_L = 25.711V \]

\[ \% \text{Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = 0.645\% \]

A Full Wave Rectifier is fed from a transformer having a centre tapped secondary winding. The rms voltage from either end of the secondary is 20V. If the diode forward resistance is $5\Omega$ and that of half secondary is $5\Omega$, for a load of 1kW. Calculate $R_L = 10\Omega$.

\[ E_s = 20V, R_f = 3.9, R_s = 5\Omega \]

\[ a) E_{Sm} = E_s \times \sqrt{2} = 20V \times 2.82843V = 80.6V \]

\[ b) I_m = \frac{E_{Sm}}{R_f + R_s + R_L} = \frac{28.2843}{3 + 5 + 1000} = 0.0084\text{mA} \]

\[ i) I_{dc} = \frac{2I_m}{\pi} = \frac{2 	imes 0.0084}{\pi} = 17.8634\text{mA} \]

\[ \% \text{Regulation at full load} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{18 - 17.8634}{17.8634} \times 100 = 0.8\% \]

\[ \text{Efficiency at full load} = \frac{18}{17.8634} \times 100 = 80.56\% \]
\[ \eta = \frac{D \cdot C \cdot E_{dc} \cdot x \cdot 100}{A \cdot C \cdot f \cdot P} \]

\[ = \frac{8}{\pi^2} \times \frac{1}{1 + \frac{RF + RS}{RL}} \times 100 = 80.41\% \]

**TUF of Secondary:**

- **E rms \cdot I rms = 20 \times \frac{I_m}{\sqrt{2}}**
- **= 20 \times 2.86 \times 10^{-3} = 0.3968 \text{ W}**
- **\therefore \ TUF = \frac{D \cdot C \cdot E_{dc}}{A \cdot C \cdot f \cdot P} = 0.3968**
- **\text{A.C. Rating} = 0.8041**

**73.** In a *Full Wave Rectifier* a sign of 300V at 50Hz is applied at the input. Each diode has an internal resistance of 80Ω.

If the load is 2000Ω, calculate:

- **E_{dc} = 12 \times E_{rms} (\text{RMS}) = 300\sqrt{2} \text{ V}**
- **I_m = E_{rms} = \frac{300\sqrt{2}}{\sqrt{2}} = 0.1515 \text{ A}**
- **R_f + R_L = 800 + 2000 = 2800 \Omega**
- **\therefore I_{dc} = \frac{2 \times I_m}{\pi} = 2 \times 0.1515 = 0.303 \text{ mA}**
- **\therefore P_{dc} = I_{dc}^2 \cdot RL = (0.1515)^2 \times 2800 = 3.213 \text{ W}**
- **I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{0.1515}{\sqrt{2}} = 0.10712 \text{ A}**
- **\therefore P_{ac} = I_{rms}^2 \times (R_f + R_L) = (0.10712)^2 \times 2800 = 3.213 \text{ W}**
- **\therefore \eta = \frac{P_{dc} \times 100}{P_{ac}} = \frac{18.61 \times 100}{32.13} = 57.9152\%**

**74.** Assume *Full Wave Rectifier*:

- **A Diode has an internal resistance is 20Ω.**
- **Load from a 110V a.m.s. Source of Supply.**
- **Calculate R_f = 20 \Omega, R_L = 1000 - 2 \times E_{rms} (\text{RMS}) = 110V.**

**Efficiency of Rectification:**

- **E_{rms} = \sqrt{2} \times E_{rms} (\text{RMS}) = \sqrt{2} \times 110 = 155.56 \text{ volt}**
- **I_m = \frac{E_{rms}}{\sqrt{2}} = \frac{155.56}{\sqrt{2}} = 8.0812 \text{ mA}**
- **\therefore E_{dc} = I_{dc} \cdot RL = 8.0812 \times 10 = 80.812 \text{ V}**
- **\therefore E_{rms} = \frac{E_{dc}}{\sqrt{2}} = \frac{80.812}{\sqrt{2}} = 4.0406 \text{ mA}**
- **\therefore E_{rms} = 2892 \text{ V}**
- **\therefore I_{rms} = \frac{E_{rms}}{R_f + R_L} = 8.0812 \times 10 = 80.812 \text{ mA}**
- **\therefore I_{rms} = 2.5723 \times 10^{-3} \times 4 \times 10^3 = 10.2892 \text{ V}**
HALF-WAVE RECTIFIER POWER SUPPLY:

1. CAPACITOR FILTER CIRCUIT:

When a sinusoidal alternating voltage is rectified, the resulting waveform is a series of positive or negative half cycles of the input waveform; it is not direct voltage. To convert to direct voltage, a smoothing circuit or filter is needed.

\[ V_{c} = V_{pi} - V_{f} \]

The peak capacitor voltage when the instantaneous level of the input falls below \( V_{pi} \), the diode becomes reverse biased. The capacitor begins to discharge through the load resistor \( R_L \) when the diode is reverse biased, so \( V_c \) falls slowly as shown by the capacitor voltage in the Fig 1.
The diode remains reverse biased throughout the rest of the positive half cycle. Current flows through the diode to recharge the capacitor at this point, causing the capacitor to reach \((V_{pi} - V_f)\). The circuit output is then a direct voltage with a small ripple waveform superimposed.

**Ripple Amplitude and Capacitance:**

- The amplitude of the ripple voltage is affected by three parameters, such as reservoir capacitor value, load current, and capacitor discharge time.
- The discharge time depends upon the frequency of ripple waveform.
- With a constant load current, the ripple amplitude is inversely proportional to the capacitance.
- The reservoir capacitor value can be calculated from load current ripple amplitude and the capacitor discharge time.

![Diagram of capacitor waveform amplitudes and angles](image)

**Capacitor Waveform Amplitudes & Angles**

The waveform parameters are:

- a) \(E_{ave}\) - average dc opv voltage
- b) \(E_{(max)}\) - maximum opv voltage
- c) \(E_{(min)}\) - minimum opv voltage
- d) \(T\) - time period of ac ip waveform
- e) \(V_{r}\) - ripple voltage per p-to-p amplitude
- f) \(t_1\) - capacitor discharge time
- g) \(t_2\) - capacitor charge time
- h) \(\phi_1\) - phase angle of ipf from \(0\) to \(E_{(min)}\)
- i) \(\phi_2\) - phase angle of ipf from \(E_{(min)}\) to \(E_{(max)}\)
RELATIONSHIP BETWEEN $E_0(\text{max})$ and $E_0(\text{min})$:

Since the input wave is sinusoidal,

$$E_0(\text{min}) = E_0(\text{max}) \sin \theta_1$$

which gives $\theta_1 = \sin^{-1} \frac{E_0(\text{min})}{E_0(\text{max})}$

$\theta_2 = 90^\circ - \theta_1$

The period, $T = \frac{1}{f}$ where $f$ = frequency of ac input waveform in degree $\Rightarrow \frac{T}{\text{degree}} = \frac{1}{360^\circ}$

$\theta_2 = \frac{\theta_1 \cdot T}{360^\circ}$

and $\theta_1 = T - \theta_2$

Taking current as constant,

$$C = \frac{I \cdot \theta_1}{V_i}$$

CAPACITOR SELECTION:

→ Large standard value capacitor is always selected in case of a reservoir capacitor.

→ The standard value capacitors are available with ±20% tolerance. If capacitors of more than 10μF, the tolerance is ±10%, ±5%, ±2%.

→ The dc working voltages can be quite small, for large value capacitors. Else capacitor dielectric may breakdown.

CAPACITOR POLARITY:

If the capacitors are incorrectly connected, polarized capacitors explode. This have tragic consequences for the eyes of an experimenter.

The positive terminal is represented by straight bar on the component graphic symbol. This should be connected to the positive point in the circuit.
APPROXIMATE CALCULATION:

APPROXIMATION 1:

1. Assume the load current is constant.
2. Normally, the load current changes by small that it has no significant effect on the calculation.

APPROXIMATION 2:

Discharge time ($t_1$) is approximately equal to the input waveform time period ($t_1 = \dot{t}$).

DIODE SPECIFICATION:

The selected diodes must be able to survive higher levels.

The diode has $-V_p$ at anode, $V_R$ and $+V_p$ at cathode, so diode peak reverse voltage is $V_R = 2V_p$.

The average forward current that a diode pass is equal to the dc output current:

$I_{F,dc} = I_L$.

The diode of a half wave rectifier with a reservoir capacitor does not conduct continuously but repeatedly passes pulses of current to recharge the capacitor each time the diode becomes forward biased. So the current pulse is known as repetitive surge current and is designated as $I_{FRM}$. $I_{FRM}$ over time period $T$ must be equal to $I_L$.

$I_L = \frac{I_{FRM} \times t_2}{(t_1 + t_2)} \Rightarrow I_{FRM} = \frac{I_L (t_1 + t_2)}{t_2}$.

SAGE LIMITING RESISTOR ($R_s$) IN A HWR.
The purpose of a low resistance surge limiting resistor \( (R_s) \) connected in series with the diode \( D_1 \) is to limit the level of any surge current that might pass through the diode.

If switch-on occurs, the ac current is,

\[
I_{f(surge)} = \frac{V_p}{R_s}
\]

\[
R_s = \frac{V_p}{I_{FSM}}
\]

when \( I_{f(surge)} \) is maximum \( (I_{FSM}) \).

**Transformer Selection:**

A power supply transformer is normally defined in terms of rms input, and output voltage and current. The input is usually 115V, 60Hz supply and the transformer peak output voltage is calculated by adding the rectifier voltage drop to the power supply peak output.

The peak voltage is converted into rms to give the secondary value.

\[
V_{s rms} = 0.707 (E_{0(max)} + V_f)
\]

for a HWR with resistive load, \( I_{rms} = 2.2 I_{cal} \) .

for a HWR with capacitive filter, \( I_{cal} = 0.28 I_{rms} \)

\[
I_{rms} = 3.6 I_{cal}
\]

The transformer primary current is

\[
I_{p rms} = \frac{V_{s rms} \times I_{rms}}{V_p \times I_{rms}}
\]

Give a detailed account on half wave rectifier power supply with necessary specifications and selections.
Full Wave Rectifier Power Supply:

Explain in detail about the full wave rectifier power supply with necessary waveforms and diagrams.

- Full wave rectifiers require filter circuits to convert the output waveform to direct voltage.
- It also consists of a reservoir capacitor and a surge limiting resistor which operates exactly similar to half wave rectifier circuit with few important exceptions.

Rectifier with Reservoir Capacitor

\[
\theta_1 = \sin^{-1} \left( \frac{E_{oc,\text{min}}}{E_{oc,\text{max}}} \right)
\]

\[
\theta_2 = 90^\circ - \theta_1
\]

and time \( t_2 = \frac{\theta_2 \times T}{360^\circ} \)

It is seen that the capacitor discharge time for a HWR is equal to the waveform time period, whereas for a FWR, it equals \( t_1 = \frac{T}{2} - t_2 \).
Using the correct value of a reservoir capacitance for a full wave rectifier can be calculated from

\[ C = \frac{I_L t_1}{V_T} \]

Similarly, the repetitive current \( I_{FRM} \) can be determined as

\[ I_{FRM} = \frac{I_L (t_1 + t_2)}{t_2} \]

The diode average current is equal to the half the load current

\[ I_f \text{ (ave)} = \frac{I_L}{2} \]

Another difference between FWR and HWR power supply circuits concerns the reverse voltage applied to the diode. When the instantaneous input voltage is \( V_P \), the reverse biased voltage across \( D_3 \) is \( V_R = V_P - V_F \) or \( V_R = V_P \)

\[ \text{Reverses voltage} \]

![diagram](image)

**Diagram:** DIODE REVERSE VOLTAGE FWR CIRCUIT

**Transformer Selection:**

The transformer specification for a FWR is similar to the HWR. Two diode voltage drops involved in calculating the secondary rms voltage:

\[ V_{c rms} = 0.707 (E_{c max} + 2V_F) \]

For a FWR with capacitive filter, \( I_{L dc} = 0.62I_{c rms} \)

With all transformers, the primary current is

\[ I_P \text{ (rms)} = \frac{V_F \text{ (rms)}}{V_{c \text{ (rms)}}} \]
**Voltage Regulators**

A rectifier with appropriate filters requires a good dc power supply. The main disadvantage is that the dc output voltage changes with change in the input voltage or load current; since the dc output voltage is not constant, this type of power supply is called unregulated power supply.

In order to ensure a constant voltage supply regardless of the variations in input voltage or current, a voltage stabilisation device called voltage regulators are used.

The voltage regulator circuit keeps the output voltage constant inspite of the changes in load current or input voltage.

**Define Voltage Regulator (6H)**

A voltage regulator is a device designed to keep the output voltage of a power supply as nearly as constant as possible.

**Block Schematic Of Regulated Power Supply**

On sketch and explain the block schematic of regulated power supply. (6H)

![Block Schematic of Regulated Power Supply](image)

The input to a voltage regulator is an unregulated dc supply while the output is regulated dc output voltage, which is almost constant.

![Block Schematic of RPS with Waveforms](image)

The transformer steps down the ac voltage input to the level required for the desired dc output.
The rectifier converts this ac voltage into a pulsating dc voltage containing ripples in it.
Then the filter circuit reduces the ripple content and tries to make it smoother.
Still then the filter output contains some ripple, called unregulated dc voltage.
Then the regulator circuit is used to make the output dc voltage constant. The output is called dc voltage to which the load can be connected.

Power Supply Performance Parameters / Characteristics Of Voltage Regulators:

Explain the significance of power supply performance of a dc series regulator.

Load Regulation:
The load regulation can be defined as the change in the regulated output voltage when the load current changes from minimum to maximum.

\[ \text{Load Regulation} = V_{NL} - V_{FL} \]

\[ V_{NL} - \text{No load voltage} \quad \text{and} \quad V_{FL} - \text{Full Load voltage} \]

\[ \% \text{ Load Regulation} = \left( \frac{V_{NL} - V_{FL}}{V_{FL}} \right) \times 100 \]
(ii) **Line Regulation (Source Regulation):**

The line regulation can be defined as the change in regulated load voltage for a specified range of line voltage.

\[
\text{Line Regulation} = \frac{V_{HL} - V_{LL}}{V_{nominal}} 
\]

\[
V_{HL} - \text{High line load voltage} \quad V_{LL} - \text{Low line load voltage}
\]

\[
\gamma = \frac{V_{HL} - V_{LL}}{V_{nominal}} \times 100
\]

\[
= \frac{\Delta V_{out}}{\Delta V_{in}} \times 100\gamma
\]

(iii) **Output Resistance:**

![Figure: Concept of Rout](image)

Practically, Rout is very small in the range of milliohms. The value of Rout is obtained from the slope of load regulation characteristics. (Refer Load Regulation topic graph.)

\[
R_{out} = \frac{\Delta V_{out}}{\Delta I_{L}} \text{Vin and Temperature constant}
\]

(iv) **Voltage Stability Factor (SV):**

SV is the percentage change in the output voltage which occurs per volt change in the input line voltage with load current and temperature as constant. Smaller the SV, better the performance of power supply.

\[
SV = \frac{\Delta V_{out}}{\Delta V_{in}} |_{I_{L} \text{ and Temperature constant}}
\]

(v) **Temperature Stability Factor (ST):**

The temperature stability of a power supply will be determined by temperature coefficients of various semiconductor devices.

\[
ST = \frac{\Delta V_{out}}{\Delta T} |_{V_{in} \text{ and } I_{L} \text{ constant}}
\]

This should be as small as possible.
(vi) Ripple Rejection:

The output of a rectifier consists of ripples, so ripple rejection is a factor which indicates how effectively the regulator circuit rejects the ripples and attenuates it from input to output. If \( V_r \) is the ripple voltage then \( RR \) is given by

\[
RR = \frac{\text{Ripple in output}}{\text{Ripple in input}} = \frac{V_{\text{rout}}}{V_{\text{rlin}}}
\]

In decibels, \( RR' = 20 \log_{10} RR \; \text{dB} \)

As \( V_{\text{rout}} \) is always less than \( V_{\text{rlin}} \), \( RR' \) is RR in dB is always negative when defined as \( V_{\text{rout}}/V_{\text{rlin}} \).

(vii) Total Change in Output Voltage:

If input voltage, load current and temperature are affecting the regulator output voltage, then the total change in output voltage is

\[
\Delta V_o = SV \Delta V_{\text{in}} + R_o \Delta I_L + ST \Delta T
\]

Linear/Basic Voltage Regulator:

The basic voltage regulator consists of:

(i) Voltage reference, \( V_r \)

(ii) Error amplifier

(iii) Feedback network

(iv) Active elements (or shunt control elements).

→ The voltage reference generates a voltage level which is applied to the comparator circuit, which is generally an error amplifier.

→ The second input to the error amplifier is from the feedback network.

→ The error amplifier converts the difference between the output voltage and the reference voltage into the error signal.

→ This error signal then converts the active element of the regulator circuit, in order to compensate the change in output voltage.

→ A resistor is used as an active element, thus the output voltage is maintained constant.
TYPES OF VOLTAGE REGULATORS:

In: Explain with the block diagrams, the basic types of voltage regulator circuits.

There are two types of voltage regulators available, namely:

(i) Series Voltage Regulator
(ii) Shunt Voltage Regulator

(i) SERIES VOLTAGE REGULATOR:

\[ V_{in} \rightarrow \text{control element} \rightarrow V_{L} = V_{o} \]

Unregulated

Feedback signal

Reference voltage

Comparator circuit

Sampling circuit

Fig.: BLOCK DIAGRAM OF SERIES VOLTAGE REGULATOR

→ If in a voltage regulator circuit, the control element is connected in series with the load, the circuit is called series voltage regulator circuit.

→ The unregulated dc voltage is the input to the circuit. The control element controls the amount of input voltage, then gets to the output.

→ The sampling circuit provides the necessary feedback signal.

→ The comparator circuit compares the feedback with the reference voltage to generate the appropriate control signal.

→ If \( V_{o} \) decreases due to increased load, then error detector produces an output that causes the control element to increase \( V_{o} \).

→ Similarly, any tendency of \( V_{o} \) to increase, results in a signal that causes the control element to reduce \( V_{o} \).
TRANSMITTER SERIES REGULATOR (OR) Emitter Follower Series Voltage Regulator

Draw a neat circuit diagram of an emitter follower series voltage regulator circuit:

→ The basic series voltage regulator is called emitter follower series voltage regulator. This is employed to overcome the limitation of shunt regulator (Next topic).

→ The transistor Q\textsubscript{1} is the series control element while the zener diode D is the reference voltage provider.

→ The zener diode is reverse biased, so that it works in the breakdown region. Zener is connected in the base of Q\textsubscript{1} while the emitter of Q\textsubscript{1}. The base emitter junction is always forward biased.

OPERATION:

From the fig, \( V_0 = V_Z - V_{BE} \)

Apply KVL to the input side,

\[ V_{in} = V_{CE} + V_0 \]

\[ V_{CE} = V_{in} - V_0 \]

For transistor Q\textsubscript{1}, \( I_E = I_B + I_C \)

→ \( I_B \) is very small, \( I_E \approx I_C \).

\[ I_E = I_C = I_L \]

Now \( I_B = \frac{I_C}{\beta} = \frac{I_L}{\beta} \)

where \( I_Z \) = zener current & \( I_R \) = current through \( R \).

\[ I_C = I_R - I_B \]

The load current, \( I_L = \frac{V_0}{R_L} \)
**Expression for Voltage Stability Factor ($S_V$):**

The voltage stability factor for emitter follower series regulator is given by

$$S_V = \frac{R_z}{R + R_z}$$

where $R_z = \text{ac resistance or dynamic resistance}$

The value of $R_z$ is very small and by selecting the large value of resistance $R$, $S_V$ can be reduced. Its ideal value is zero (0).

**Expression for Output Resistance:**

The output voltage $V_o$ can be defined as the ratio of applied voltage $V$ to current $I$. For emitter follower SR, $V_o$ is

$$R_o = \frac{V}{I} = \frac{R_z + hfe}{1 + hfe}$$

It can be reduced by selecting a transistor with high value of $hfe$.

**Disadvantages of Emitter Follower Series Voltage Regulator:**

(i) The changes in $V_{fe}$ and $V_z$ due to changes in temperature appear at the output.

(ii) Due to large power dissipation, a heat sink is necessary which makes the circuit bulky.

**Op-Amp Based Voltage Series Regulator:**

![Op-Amp Based Voltage Series Regulator Diagram]

**Regulating Action:**

- The resistive voltage divider formed by $R_2$ and $R_3$ senses any change in the output voltage.
When the output tries to decrease, due to increase in load current, it causes by a decrease in $R_1$, a proportioned voltage decrease is applied to the op-amps, inverting input by the voltage divider.

The small difference voltage (error voltage) is developed across the opamp's input.

This difference voltage is amplified, and the opamp's output voltage $V_B$ decreases.

This causes $V_{out}$ to increase until the voltage to the input again equal to the reference voltage.

The closed loop gain $ACL = \frac{1 + R_2}{R_1}$

### (ii) SHUNT VOLTAGE REGULATOR:

Fig: BLOCK DIAGRAM OF SHUNT REGULATOR

If the control element is connected in parallel with the load, then the regulator circuit is called shunt voltage regulator.

The operation of the circuit is similar to that of series regulator, except that regulation is achieved by controlling the current through parallel transistor $Q_1$. 
A transistor is used as a control element and is being connected in shunt or parallel with the load.

- The output or load voltage is equal to the sum of zero voltage $V_Z$ and the base-emitter voltage $V_{BE}$ of the transistor.

$$V_o = V_Z + V_{BE}$$

**Regulating Action:**

- Assume that the unregulated input voltage increases.
- Due to this, the load voltage $V_L$ also increases.
- As a result, collector current of the transistor $I_C$ also increases.
- This causes the input current $I_I$ to increase, which in turn increases the voltage drop across the series resistance $R$, consequently, load voltage decreases.
- It is valid because of the voltage drop across series resistance $V_R$ and the load voltage is equal to the input voltage, at all times.

$$V_C = V_R + V_L$$

**Flow diagram:**

$$V_i \uparrow \rightarrow V_L \uparrow \rightarrow V_{BE} \uparrow \rightarrow I_B \uparrow \rightarrow I_C \uparrow \rightarrow V_R \uparrow \rightarrow V_L \uparrow$$
Switching Regulation

The operating principle of switching regulation is completely different than that of linear regulators. Switching regulators require an external transistor and a control. The series pass transistors in such a regulator is used as a controlled switch and is operated in the cutoff region (a) saturation region. Hence, the power transmitted across such a transistor is in the form of discrete pulses rather than a steady flow of current.

When the transistor is operated in the cutoff region, there is no current and dissipated. No power, while when it is operated in the saturation region a negligible voltage drop appears across it and hence dissipated very small power, provided max current to load.

Therefore, switching regulators uses the fact that if duty cycle of the pulse waveform is varied, the average value of the voltage also changes proportionally.

\[ \text{Duty Cycle } \delta = \frac{\text{on}}{\text{on} + \text{off}} = \frac{\text{on}}{T} \]

- \text{on} - On time of pulse
- \text{off} - Off time of pulse

The basic switching regulator consists of four major components:

(a) Voltage Source
(b) Switching Transistor
(c) Pulse Generator
(d) Filter.

![Basic Switching Regulation Diagram](image-url)
Switched Mode Power Supply (SMPS)

A power supply is an important element of any type of electronic circuit. It provides the supply for the proper operation of the circuit. The successful operation of the circuit depends on the proper functioning of the power supply. Most electronic circuits require a smooth dc voltage as that of batteries. The power supply in a circuit easy to provide such a constant voltage.

The regulator in a power supply is an important unit which keeps the output dc voltage constant under the variable load and variable input current.

Need of Switched Mode Power Supply:

A linear power supply has following limitations:

a) The required input step down transformer is bulky and expensive.

b) Due to low line frequency, large values of filter capacitors are required.

c) The efficiency is very low.

d) As large is the difference between input and output voltage more is the power dissipation in the series pass transistor.

e) The need for dual supply is not economical and feasible to achieve with the help of linear regulators.

To overcome all these limitations SMPS are needed.
The switch is generally a transistor. The pulse generator output makes it on or off. The pulse generator produces a shaped pulse waveform. The most effective range of pulse waveform frequency is 50 kHz, and the most commonly used filter is RLC.

Switching Voltage Regulator:

The block diagram of basic switching voltage regulator which uses transistor as a switch is shown in the next page.

Working:

The part $R_2/R_1 + R_3$ of the output is fed back to the inverting input of error amplifier. It cont.
with the sequence voltage. The difference is amplified and
given to the comparator inverting terminal.

The oscillator generates a triangular waveform at a
fixed frequency. It is applied to the non-inverting input
of the comparator. The output of the comparator is high
when the triangular voltage waveform is above the level of
the error amplifier output due to this the transistors
Q remain in cutoff state thus the output of the
Comparator is nothing but a sequenced pulse waveform.

Fig. 8 Block diagram of switching regulator.

The period of the pulse waveform is same as that
of oscillator output say T. The duty cycle is denoted as
\( \Delta = \frac{\text{on}}{\text{on}} \). This duty cycle is controlled by difference
between the feedback voltage and sequence voltage.

when \( \Delta \) is on in saturation state, the entire
input voltage \( V_{in} \) appears at point A. Thus current flows through
When $Q$ is off, $L$, still continue to supply current through itself to the load. The diode $D$, provides the return path for the current. The Capacitors $C_1$ act to smooth out the voltage and the voltage at the output is almost dc in nature. The output voltage $V_o$ expressed mathematically as

$$V_o = \frac{\text{ton}}{T} V_{\text{in}} = 8 V_{\text{in}}.$$

The range of operating frequency to get max efficiency is 10 to 50 kHz.

**Types of Switching Regulators:**

The Switch mode regulators use an inductor and there is no input to output isolation. On the other hand, other side converters use transformers and may provide input to output isolation.

There are three basic configurations of switching regulators:

1. **Step down (or) Buck Switching regulator**
2. **Step up (or) Boost Switching regulator**
3. **Inverting type switching regulator**

**Step down Switching regulator:** (Buck)

It consists of inductor $L$ and series transistors $Q$ which act as a switch. The reference for $Q_2$ amplifier is provided by zener voltage $V_z$. The output is fed back to $Q_2$ amplifier through potential divider. The pulse width oscillator controls the operation of $Q$ as...
The transistor \( Q \) is used for switching the input voltage for the required period of time, which is dependent on the load current requirement. The L-C filter averages the switched voltage.

The variable pulse width oscillator controls on/off periods of \( Q \), when on time is more compared to off time, the capacitor charges more, increasing the output voltage. On the other hand, when off time is more compared to on time, the capacitor discharges more, reducing output voltage. Thus, adjusting the duty cycle \( S \) of transistor \( Q \), the output voltage can be regulated.

\[
S = \frac{t_{on}}{t_{on + t_{off}}} = \frac{t_{on}}{T}
\]
a) If output voltage decreases:

The voltage across $R_3$ decreases. The sequence $V_z$ is fixed. Thus, error at input of error amplifier is more. This produces pulse of higher width as the output of the variable pulse width oscillator. As pulse width is high $t_{on}$ is higher for $Q$. This increases the charging of the capacitor $C$ producing more output voltage. Thus decrease output voltage get compensated.

\[ V_c \]

\[ \text{Ton > Toff} \]

\[ \text{Time} \]

b) When output voltage increases:

The voltage across $R_3$ increases. The sequence $V_z$ is fixed. The error at the input of error amplifier decreases. The output of the error amplifier controls the output of variable pulse width oscillator. It produces pulse of smaller width which reduces $t_{on}$ for $Q$. This makes the capacitor $C$ to discharge more to offset any attempt of increase in output voltage.

The output voltage is $V_{out} = 8V_{in}$, where $S = t_{on}$.
Advantages:

1. Higher efficiency
2. Simple to design.
3. Low ripple content
4. Small output ripple
5. Large tolerance of line voltage regulation.

Disadvantages:

1. Single output and no isolation between input and output.
2. Slow transient response compared to linear regulators.
3. Due to finite reverse recovery time of communicating diode, the instantaneous short circuit occurs across the source due to which active switches may fail.
Step up Switching Regulation - (Boost)

The basic elements used in this type are identical to those used in step down type but their arrangement is different.

\[ \text{Working:} \]

Case (1): when Q1 is on, Vce is denoted as Vce(sat) and the voltage across L suddenly become \( V_{\text{in}} - V_{\text{ce(sat)}} \) as shown in Fig. This expands the magnetic yield around the inductor very quickly. This voltage across L can be obtained by applying KVL to V_{\text{in}} during on time \( t \) of \( Q \), the voltage across inductor starts decreasing exponentially from its initial max value \( V_{\text{in}} - V_{\text{ce(sat)}} \).

Case (2): when Q1 is off, the magnetic yield of the inductor L collapses and its polarity gets reversed. This is because an inductor current can not change instantly. Thus voltage \( V_L \) attained after exponential decrease when Q1 is on now gets reversed as shown in the Fig. Due to reversal of polarity...
it gets added to \( V_{in} \).

The diode \( D_1 \) is forward biased due to reversed \( V_L \) and capacitor \( C \) now charge to \( V_{in} + V_L \). The output voltage is voltage across capacitor \( C \), which is \( V_{in} + V_L \), which is more than \( V_{in} \). Thus it act as step up type regulator.

It can be seen that how much \( V_L \) should be added to \( V_{in} \). The shorter the on period of \( Q_1 \), greater voltage will get added to \( V_{in} \) increase the output voltage. The longer the on time of \( Q_1 \), smaller is the inductor voltage \( V_L \) and less voltage will get added to \( V_{in} \), decreasing the output voltage.

When output voltage tapers to decreases due to increase in load current (or) decrease in \( V_{in} \), then on time of \( Q_1 \) get reduced thus \( V_{in} \) increases compensating for the decrease in it.

When output voltage tapers to increase then on time of \( Q_1 \) get increased. This reduces voltage across the inductor. Thus the less voltage gets added to \( V_{in} \), reducing its value. Thus compensates for the attempted increase in output voltage.

Expression for the output voltage:

\[
V_{out} = \frac{V_{in}}{8}
\]
Advantages:

1) The output voltage is higher than input voltage.
2) Efficiency is high greater than 90%.
3) Low input ripple current.

Disadvantages:

1) The duty cycle is limited to 50% to avoid the continuous current mode if the regulator enters the continuous current mode, it stops regulating the output. Thus for a minimum input voltage range, max duty cycle is limited.
2) Due to restricted duty cycle, the peak collector current is very high. This limits its output power rating.
This type of switching regulator produces an output voltage having polarity opposite to that of the input voltage. The elements are again identical to buck and boost type regulator but their connection are different. Any change in output produces error which get amplified by op-amp error amplifier. This controls the on/off period of Q to regulate the output through variable pulse width oscillator.

Case 1: The Q goes into saturation and the voltage across it drops to $V_{CE(sat)}$ which is about 0.3V. Due to this voltage across inductor suddenly rises to $[V_{in} - V_{CE(sat)}]$ and magnetic field around it suddenly expands. Due to connection of diode $D_2$ in this situation it is reverse biased. The inductor voltage starts exponentially decreasing from the initial value $[V_{in} - V_{CE(sat)}]$. 
Case a: Now if $Q_1$ is turned off, the magnetic field across $L$ gets collapsed but inductor current cannot change instantaneously. Thus, voltage across inductor $V_L$ reverse its polarity.

Due to reverse $V_L$, the diode $D_1$ is now forward biased. The capacitor charges through $D_1$ producing output voltage of opposite polarity to that of $V_{in}$. Hence the regulator is called voltage inverter type.

The repetitive on-off action of $Q_1$ produces a repetitive charging and discharging of the capacitor $C$ which is smoothed by the LC filter action. The less period $Q_1$ is on, higher is the output voltage, the greater time $Q_1$ is on, smaller is the output voltage.

Power supply performance and testing:

The power supply is the heart of any electronic equipment. Hence for the high quality and reliable operation, it is necessary to verify the power supply performance by conducting the tests. The test specification must include all the safe operating limits such as temperature, line condition, regulation values, etc. The various test equipment required to test a power supply are:

(i) DC power supply which is capable of supplying voltage and current for the test.

(ii) Electronic load which is capable of handling various system requirements.
Accurate voltmeter, wattmeter, and ammeter
An oscilloscope with bandwidth of 500 MHz or more
You measurement of noise.
Network analyzer (can) frequency response analysis for stability measurement.

Testing Procedure and Specifications:
The various test used to check the performance of a power supply are discussed below.

(i) First switch on
(ii) Inrush current test
(iii) Transient recovery time test
(iv) Static load regulation test
(v) Line regulation test
(vi) Periodic and Random deviation test (PARD)
(vii) Efficiency test
(viii) Power factor
(ix) Start-up time
(x) Short circuit output current
(xi) Over voltage shutdown
(xii) Leakage current
(xiii) Hold up time