SHREE SATHYAM COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ECE

ALL THE 5 UNITS NOTES

FOR II YEAR / III SEMESTER

EC8351-ELECTRONICS CIRCUITS -I
1. Discuss about the DC load line and Q point. (OR) What is D.C. load line, how will you select the operating point, explain it using common emitter amplifier characteristics as an example?[DEC-2006]

DC load line:-

It is the line on the output characteristics of a transistor circuit which gives the values of $I_C$ and $V_{CE}$ corresponding to zero signal (or) DC conditions.

The transistor is biased with a common supply such that the base emitter junction is forward biased and the collector base junction is reversed biased, i.e. Transistor is in the active region.

In the absence of ac signal, the capacitors provide very high impedance, i.e. open circuit. Therefore, the equivalent circuit for common emitter amplifier because, as shown fig.

Applying Kirchhoff’s voltage law to the collector circuit shown in fig.

We get,

$$V_{CC}-I_C (R_C+R_E) - V_{CE} = 0$$

$$V_{CC} - I_C (R_C+R_E) + V_{CE} = 1$$

Where $I_C (R_C+R_E)$ is the voltage drop across $R_C$ and $R_E$, and $V_{CE}$ is the collector emitter voltage. If we arrange the terms in equation 1 as

$$I_C = \left[ -\frac{1}{(R_C + R_E)} \right] V_{CE} + \frac{V_{CC}}{(R_C + R_E)}$$
\[ \frac{1}{R_{dc}} \] \[ V_{cc} + \frac{V_{cc}}{R_{dc}} \] 
\[ \therefore R_{dc} = R_c + R_e \] 

And compare this equation with equation of straight line \( y = mx + c \), where ‘m’ is the slope of the line and ‘c’ is the intercept on y-axis, then we can draw a straight line on the graph of \( I_c, V_{ce} \) which is having slope \( -1/R_{dc} \) & y-intercept \( V_{cc}/R_{dc} \). To determine the two points on the line we assume \( V_{ce} = V_{cc} \) & \( V_{ce} = 0 \).

1. When \( V_{ce} = V_{cc} \); \( I_c = 0 \) and we get a point of cut-off
2. When \( V_{ce} = 0 \); \( I_c = V_{cc}/R_{dc} \) & we get a point saturation region

The term biasing appearing for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point). The intersection of the two points is called operating point.

By definition, quiescent means quiet, still, inactive. The above figure as a general output device characteristic with three operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the active region. Fig shows the horizontal line for the maximum collector current \( I_{c,m} \) and a vertical line at the maximum collector-to-emitter voltage \( V_{cem} \). At the lower end of the scales are the cutoff region, defined by \( IB \leq 0 \mu A \), and the saturation region, defined by \( V_{ce} \leq V_{ces} \). The BJT device...
could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the active region, one can select many different operating areas or points.

Fig. Transistor is driven into active region because the Q point is close to the Active for the driven input signal.

The chosen Q-point often depends on the intended use of the circuit. Biased the BJT at a desired operating point, the effect of temperature must also be taken into account. Temperature causes the device parameters such as the transistor current gain (β) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the
network design must also provide a degree of temperature stability so that temperature changes result in minimum changes in the operating point. This maintenance of the operating point can be specified by a stability factor, S, which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable, and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating region the following must be true:
1. The base–emitter junction must be forward-biased (p-region voltage more positive), with a resulting forward-bias voltage of about 0.6 to 0.7 V.
2. The base–collector junction must be reverse-biased (n-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.

<table>
<thead>
<tr>
<th>Region</th>
<th>Active-region operation</th>
<th>Cutoff-region operation</th>
<th>Saturation-region operation</th>
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<tr>
<td>Base–emitter junction</td>
<td>Forward biased</td>
<td>Reverse biased</td>
<td>Forward biased</td>
</tr>
<tr>
<td>Base–collector junction</td>
<td>Reverse biased</td>
<td>Reverse biased</td>
<td>Forward biased</td>
</tr>
</tbody>
</table>

2. Explain the fixed biasing of BJT with analysis.

**Biasing:** The process of giving proper supply voltages and resistances for obtaining the Q point is called biasing.

The fixed biasing is otherwise called as base bias. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open circuit equivalent. In addition, the dc supply $V_{CC}$ can be separated into two supplies (for analysis purposes only) as shown in Fig to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current $I_B$. The $V_{CC}$ is connected directly to $R_B$ and $R_C$ just as in Fig.
Circuit Diagram:

Base Circuit:

Consider first the base–emitter circuit loop: Writing Kirchhoff’s voltage equation in the clockwise direction for the loop, we obtain

\[ \text{Equation 1} \]

\[ +V_{CC} - I_B R_B - V_{BE} = 0 \]

Note the polarity of the voltage drop across \( R_B \) as established by the indicated direction of \( I_B \). Solving the equation for the current \( I_B \) will result in the following:

\[ \text{Equation 2} \]

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \]

Equation 2 is certainly not a difficult one to remember if one simply keeps in mind that the base current is the current through \( R_B \) and by Ohm’s law that current is the voltage across \( R_B \) divided by the resistance \( R_B \). The voltage across \( R_B \) is the applied voltage \( V_{CC} \) at one end less the drop across the base-to-emitter junction (\( V_{BE} \)). In addition, since the supply voltage \( V_{CC} \) and the base–emitter voltage \( V_{BE} \) are constants, the selection of a base resistor, \( R_B \), sets the level of base current for the operating point.

Collector Circuit:

The collector–emitter section of the network is the indicated direction of current \( I_C \) and the resulting polarity across \( R_C \). The magnitude of the collector current is related directly to \( I_B \) through
\[ I_C = \beta I_B \]

The base current is controlled by the level of \( R_B \) and \( I_C \) is related to \( I_B \) by a constant \( \beta \), the magnitude of \( I_C \) is not a function of the resistance \( R_C \). Change \( R_C \) to any level and it will not affect the level of \( I_B \) or \( I_C \) as long as we remain in the active region of the device. However, as we shall see, the level of \( R_C \) will determine the magnitude of \( V_{CE} \), which is an important parameter. Applying Kirchhoff’s voltage law in the clockwise direction around the indicated closed loop of Fig. will result in the following:

\[ V_{CE} + I_C R_C - V_{CC} = 0 \]

and

\[ V_{CE} = V_{CC} - I_C R_C \]

which states in words that the voltage across the collector–emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across \( R_C \)

\[ V_{CE} = V_C - V_E \]

where \( V_{CE} \) is the voltage from collector to emitter and \( V_C \) and \( V_E \) are the voltages from collector and emitter to ground respectively. But in this case, since \( V_E = 0 \) \( V \), we have

In addition, since

\[ V_{CE} = V_C \]

And \( V_E = 0 \) \( V \)

\[ V_{BE} = V_B - V_E \]

3. Determine the following for the fixed bias configuration of fig.

(a) \( I_{BQ} \) and \( I_{CQ} \)
(b) \( V_{CEQ} \)
(c) \( V_B \) and \( V_C \)
(d) \( V_{BE} \)
3. Explain the collector to base biasing of BJT with analysis.

The fig shows the dc bias with voltage feedback. It is also called the collector to base biasing. It is an improvement over the fixed bias method. In this biasing resistor is connected between the collector and base of the transistor to provide a feedback path. Thus \( I_B \) flows through \( R_B \) and \( (I_C + I_B) \) flows through the \( R_C \).

### Circuit Diagram:

![Circuit Diagram](image)

### Circuit Analysis:

**Base Circuit:**

Let us consider the base circuit, apply the voltage law to the base circuit we get,

\[
\begin{align*}
V_{CC} &= (R_B + R_C)I_B + I_C R_C + V_{BE} \\
&= (R_B + R_C)I_B + \beta I_B R_C + V_{BE} \\
I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} \quad \beta >> 1
\end{align*}
\]

**Collector Circuit:**

Apply KVL to the output circuit

\[
\begin{align*}
V_{CC} &= (I_C + I_B) R_C + V_{CE} \\
V_{CE} &= V_{CC} - (I_C + I_B) R_C
\end{align*}
\]

4. Determine the quiescent levels of \( I_C \) and \( V_{CEQ} \) for the network of Fig.
5. Explain the Voltage divider biasing of BJT with analysis. [NOV/DEC 2007]

In the previous bias configurations the bias current $I_{CQ}$ and voltage $V_{CEQ}$ were a function of the current gain ($\beta$) of the transistor. However, since $\beta$ is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent, or in fact, independent of the transistor beta. If analyzed on an exact basis the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of $I_{CQ}$ and $V_{CEQ}$ can be almost totally independent of beta.

**Circuit Diagram:**

**Base Circuit:**

Let us consider base circuit, Voltage across base $R_2$ is the voltage $V_B$. Apply KVL voltage divider theorem to find the $V_B$, we get,

$$V_B = \frac{R_2(I)}{R_1(I+I_B)+R_2(I)} \times V_{CC}$$

$$V_B = \frac{R_1}{R_1+R_2} \times V_{CC} \quad I >> I_B$$

**Collector Circuit:**

Let us consider collector circuit, voltage across $R_E(V_E)$ can be obtained as,

$$V_E = I_E R_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$
Apply KVL to the collector circuit,
\[ V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0 \]
\[ \therefore V_{CE} = V_{CC} - I_C R_C - I_E R_E \]

**Simplified Circuit of Voltage Divider Bias:**

Her \( R_1 \) and \( R_2 \) are replaced by \( R_B \) and \( V_T \), where \( R_B \) is the Thevenin’s voltage. \( R_B \) can be calculated as,
\[ R_B = \frac{R_1 R_2}{R_1 + R_2} \]

Applying KVL to the base circuit of Fig. we get,
\[ V_T = I_B R_B + V_{BE} + I_E R_E \]
\[ \therefore V_T = V_{BE} + (R_B + R_E) I_B + I_C R_E \]
\[ \therefore I_E = I_C + I_B \]
\[ V_{BE} = V_T - (R_B + R_E) I_B - I_C R_E \]

![Fig. Thevenin’s equivalent circuit for voltage divider bias](image)

6. For the circuit as shown in fig. \( \beta = 100 \) for the si transistor. Calculate \( V_{CE} \) and \( I_C \)

\[ V_B \approx \frac{R_2}{R_1 + R_2} \]
\[ V_{CC} = \frac{5 \times 10^3}{10 \times 10^3 + 5 \times 10^3} \times 10 = 3.33 \text{ V} \]

We know that, \( V_E = V_B - V_{BE} = 3.33 - 0.7 = 2.63 \text{ V} \)
and \( I_R = \frac{V_E}{R_E} = \frac{2.63 \text{ V}}{500} = 5.26 \text{ mA} \)

We know that \( I_B = \frac{I_E}{1 + \beta} = \frac{5.26 \times 10^{-3}}{101} = 52.08 \mu \text{A} \)
and \( I_C = \beta I_B = 100 \times 52.08 \times 10^{-6} = 5.208 \text{ mA} \)
For the circuit shown in fig.\( I_c = 2\text{mA}, \beta = 100 \), calculate \( R_E, V_{EC} \) and stability factor.

\[
I_c = \beta I_B
\]

\[
I_B = \frac{I_c}{\beta} = \frac{2\text{mA}}{100} = 20\text{\mu A}
\]

Applying KVL to voltage divider we get,

\[
V_{CC} - R_1 [I + I_B] - R_2 I = 0
\]

\[
12 - 50 \times 10^3 \times (1 + 20 \times 10^{-6}) - 5 \times 10^3 (I) = 0
\]

\[
12 - 50 \times 10^3 I - 1 - 5 \times 10^3 I = 0
\]

\[
I = 0.2 \text{ mA}
\]

\[
V_B = R_2 \times I = 5 \times 10^3 \times 0.2 \times 10^{-3} = 1 \text{ V}
\]

We know that,

\[
V_B = V_{BE} + I_E R_E = V_{BE} + (I_B + I_C) R_E
\]

\[
1 = 0.7 + (20 \times 10^{-6} + 2 \times 10^{-3}) R_E
\]

\[
R_E = 148.51 \Omega
\]

Applying KVL to collector circuit we get

\[
V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0
\]

\[
V_{CE} = V_{CC} - I_C R_C - (I_B + I_C) R_E
\]

\[
= 12 - 2 \times 10^{-3} \times 2 \times 10^{-3} - (20 \times 10^{-6} + 2 \times 10^{-3}) \times 148.51
\]

Stability factor for voltage divider bias is given as

\[
S = \frac{1 + \beta}{1 + \beta \left( \frac{R_E}{R_E + R_B} \right)}
\]

Before substituting the values in the equation it is necessary to calculate \( R_B \).

We know that \( R_B = R_1 || R_2 \)

\[
= \frac{R_1 R_2}{R_1 + R_2} = \frac{50 \times 10^3 \times 5 \times 10^3}{50 \times 10^3 + 5 \times 10^3} = 4.545 \text{ k\Omega}
\]

Now substituting values of \( R_B, R_E \) and \( \beta \) in the equation of stability factor we get,

\[
S = \frac{100 + 1}{1 + 100 \times \frac{148.51}{148.51 + 4.545 \times 10^3}} = 24.254
\]
8. Stability factor for a fixed bias circuit.

\[ I_B = \frac{V_{CC}}{R_B} \]

When \( I_B \) changes by \( \delta I_B \), \( V_{CC} \) and \( V_{BE} \) are unaffected.

\[ \frac{\partial I_B}{\partial I_C} = 0 \quad \therefore I_C \text{ is not present in the equation.} \]

Substituting this value in equation (10), we get,

\[ S = \frac{1 + \beta}{1 - \beta \left( \frac{\partial I_B}{\partial I_C} \right)} = \frac{1 + \beta}{1 - 0} \]

\[ \therefore S = 1 + \beta \]

**Stability Factor \( S' \)**

\[ S' = \frac{\partial I_C}{\partial V_{BE}} \bigg|_{I_{CO}, \beta \text{constant}} \]

From equation (4) we have,

\[ I_C = \beta I_B + (\beta + 1) I_{CBO} \]

Now representing \( I_B \) in terms of \( V_{BE} \) we get,

\[ I_C = \beta \left( \frac{V_{CC} - V_{BE}}{R_B} \right) + (\beta + 1) I_{CBO} \]

\[ \therefore I_C = \frac{\beta V_{CC} - \beta V_{BE}}{R_B} + (\beta + 1) I_{CBO} \]

\[ \therefore \frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B} + 0 = -\frac{\beta}{R_B} \]

\[ \therefore S' = -\frac{\beta}{R_B} \]

**Stability Factor \( S'' \)**

\[ S'' = \frac{\partial I_C}{\partial \beta} \bigg|_{V_{BE}, I_{CO} \text{ constant}} \]

From equation (10) we have

\[ I_C = \frac{\beta V_{CC} - \beta V_{BE}}{R_B} + (\beta + 1) I_{CBO} \]

\[ \therefore \frac{\partial I_C}{\partial \beta} = \left( \frac{V_{CC} - V_{BE}}{R_B} \right) + I_{CBO} = I_B + I_{CBO} = \frac{I_C}{\beta} \]

\[ \therefore S'' = \frac{\partial I_C}{\partial \beta} \bigg|_{\beta} = 0 = \frac{I_C}{\beta} \quad \text{Since} \ I_B = \frac{I_C}{\beta} \text{ and } I_B \gg I_{CBO} \]
9. Explain about the fixed bias configuration for JFET with analysis.

The simplest of biasing arrangements for the n-channel JFET. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or graphical approach. The configuration of Fig. 6.1 includes the ac levels $V_i$ and $V_o$ and the coupling capacitors ($C_1$ and $C_2$). Recall that the coupling capacitors are “open circuits” for the dc analysis.

**Circuit Diagram:**

![Circuit Diagram](image)

**DC analysis:**

$$I_G = 0 \text{ A}$$

$$V_{RG} = I_G R_G = (0 \text{ A}) R_G = 0 \text{ V}$$

The zero-volt drop across $R_G$ permits replacing $R_G$ by a short-circuit equivalent, as appearing in the network. The fact that the negative terminal of the battery is connected directly to the defined positive potential of $V_{GS}$ clearly reveals that the polarity of $V_{GS}$ is directly opposite to that of $V_{GG}$. Applying Kirchhoff’s voltage law,

$$V_{GS} + V_{GG} = 0$$

$$\therefore V_{GS} = -V_{GG}$$

Since $V_{GG}$ is a fixed dc supply, the voltage $V_{CC}$ is fixed in magnitude, and hence the name fixed. For fixed bias circuit the drain current $I_D$ can be calculated using equation circuit.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

The drain to source voltage of output circuit can be determined by applying KVL.

$$V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D$$
The Q point of the JFET amplifier with fixed bias circuit is given by:

\[ I_{DQ} = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_F} \right]^2 \]

\[ V_{DSQ} = V_{DD} - I_{DQ} R_D \]

Since \( V_{GS} \) is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley’s equation and the resulting level of \( I_D \) calculated.

**Graphical Analysis:** A graphical analysis would require a plot of Shockley’s equation as shown in. Recall that choosing \( V_{GS} = V_F/2 \) will result in a drain current of \( I_{DSS}/4 \) when plotting the equation. For the analysis of this chapter, the three points defined by \( I_{DSS}, V_F \), and the intersection just described will be sufficient for plotting the curve.

The fixed level of \( V_{GS} \) has been superimposed as a vertical line at \( V_{GS} = -V_{GG} \). At any point on the vertical line, the level of \( V_{GS} \) is \(-V_{GG}\) the level of \( I_D \) must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration-commonly referred to as the *quiescent* or *operating point*. The subscript \( Q \) will be applied to drain current and gate-to-source voltage to identify their levels at the \( Q \)-point.

Note in Fig. 2 that the quiescent level of \( I_D \) is determined by drawing a horizontal line from the \( Q \)-point to the vertical \( I_D \) axis as shown in Fig. 2.

The drain-to-source voltage of the output section can be determined by applying Kirchhoff’s voltage law as follows

\[ +V_{DS} + I_D R_D - V_{DD} = 0 \]

\[ V_{DS} = V_{DD} - I_D R_D \]
Determine the following for the network of Fig.
(a) $V_{GSQ}$.
(b) $I_{DO}$.
(c) $V_{DS}$.
(d) $V_D$.
(e) $V_G$.
(f) $V_S$.

Mathematical Approach:
(a) $V_{GSQ} = -V_{GG} = -2 \text{ V}$
(b) $I_{DQ} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 = 10 \text{ mA} \left( 1 - \frac{-2 \text{ V}}{-8 \text{ V}} \right)^2$
   \[= 10 \text{ mA} \left( 1 - 0.25 \right)^2 = 10 \text{ mA} \left( 0.75 \right)^2 = 10 \text{ mA} \left( 0.5625 \right)\]
   \[= 5.625 \text{ mA}\]
(c) $V_{DS} = V_{DD} - I_{DRD} = 16 \text{ V} - (5.625 \text{ mA})(2 \text{ k}\Omega)$
   \[= 16 \text{ V} - 11.25 \text{ V} = 4.75 \text{ V}\]
(d) $V_D = V_{DS} = 4.75 \text{ V}$
(e) $V_G = V_{GS} = -2 \text{ V}$
(f) $V_S = 0 \text{ V}$

Graphical Approach:
The resulting Shockley curve and the vertical line at $V_{GS}=-2 \text{ V}$ are provided in above fig. It is certainly difficult to read beyond the second place without significantly in\r

10. Discuss the various techniques of stabilization of Q-point in a transistor. [NOV/DEC-2009]

   Method of Stabilizing the Q Point (Bias Compensation)
The biasing circuits so far discussed provide stability of operating point in case of variations in the transistor parameters such as $I_{CO}$, $V_{BE}$ and $\beta$. The collector to base bias and the voltage follower bias use the negative feedback to do the stabilization action. This negative feedback reduces the amplification of the signal. If this loss in signal amplification is intolerable and extremely stable biasing conditions are required, then it is necessary to use compensation techniques.

As mentioned earlier, compensation techniques use temperature sensitive devices such as diodes, transistors, thermistors, etc. to maintain operating point constant. In this section we are going to study some compensation techniques.

**Compensation for $V_{BE}$**

a) Diode in Emitter Circuit

![Diode in Emitter Circuit Diagram](image)

**Fig. 1.61 Stabilization by means of voltage divider bias and diode compensation technique**

We know, $V_{BE} = V_T \left[ \frac{R_B + (1+\beta)R_E}{\beta} \right] I_C + \left[ \frac{(R_E + R_B)(1+\beta)}{\beta} \right] I_{CO}$

$\therefore \quad I_C = V_T - V_{BE} + \left[ \frac{(R_E + R_B)(1+\beta)}{\beta} \right] I_{CO}$

$\therefore \quad I_C = \frac{\beta (V_T - V_{BE}) + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E} \quad \ldots (1)$

If we write KVL to the base circuit of the Fig. 1.38, then equation 1 becomes

$I_C = \frac{\beta (V_T - V_{BE} - V_D) + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E} \quad \ldots (2)$

Since $V_D$ tracks $V_{BE}$ with respect to temperature, it is clear from equation (2) that $I_C$
will be insensitive to variations in \( V_{BE} \).

![Diode Compensation in Voltage Divider Bias Circuit](image)

**Fig. 1.62 Diode compensation in voltage divider bias circuit**

Substituting in equation (3), we get,

\[
I_C = \frac{V_{R2} + V_D - V_{BE}}{R_E}
\]

... (4)

If the diode which is used in this circuit is of same material and type as the transistor, the voltage across the diode will have the same temperature coefficient (-2.5 mV/°C) as the base to emitter voltage \( V_{BE} \). So when \( V_{BE} \) changes by \( \partial V_{BE} \) with change in temperature, \( V_D \) changes by \( \partial V_D \) and \( \partial V_D = \partial V_{BE} \), the changes tend to cancel each other and leave the collector current as

\[
I_C = \frac{V_{R2}}{R_E}
\]

Which is unaffected due to change in \( V_{BE} \). From Fig. 1.62 we can see that biasing is provided by \( R_1 \), \( R_2 \) and \( R_E \). The changes in \( V_{BE} \) due to temperature are compensated by changes in the diode voltage which keeps \( I_C \) stable at Q point.

**Compensation for \( I_{CO} \)**

In case of germanium transistors, changes in \( I_{CO} \) with temperature are comparatively larger than silicon transistor. Thus, in germanium transistor changes in \( I_{CO} \) with temperature play the more important role in collector current stability than the changes in the \( V_{BE} \). The Fig. 1.63 shows diode compensation technique commonly used for stabilizing germanium transistors. It offers stabilization against variation in \( I_{CO} \). In this circuit diode is kept in reverse biased condition. In reverse biased condition the current flowing through diode is only the leakage current. If the diode and the transistor are of the same type and material, the leakage current \( I_D \) of the diode will increase with temperature at the same
From Fig. 1.63 we have

\[ I = \frac{V_{CC} - V_{BE}}{R_1} \]

and

\[ I = I_B + I_O \quad \therefore I_B = I - I_O \]

For germanium transistor \( V_{BE} = 0.2 \, V \), which is very small and neglecting change in \( V_{BE} \) with temperature we can write,

\[ I \equiv \frac{V_{CC}}{R_1} \equiv \text{constant} \]

We know,

\[ I_C = \beta I_B + (1 + \beta) I_O \]

Substituting value of \( I_B \) in above equation we get,

\[ I_C = \beta I - \beta I_O + (1 + \beta) I_O \]

If \( \beta \gg 1 \) we get,

\[ I_C = \beta I - \beta I_O + \beta I_O \quad \ldots \quad (5) \]

Now if \( I_O = I_C \) we get,

\[ I_C = \beta I \quad \ldots \quad (6) \]

As \( I \) is constant, \( I_C \) remains fairly constant. In other words, we can say that changes by \( I_C \) with temperature are compensated by diode and thus collector current remains fairly constant.

**Thermistor Compensation**

This method of transistor compensation uses temperature sensitive resistive elements, thermistors rather than diodes or transistors. It has a negative temperature coefficient, its resistance decreases exponentially with increasing temperature as shown in the Fig. 1.64.

The slope of this curve is \( \frac{\partial R_T}{\partial T} \)

\( \frac{\partial R_T}{\partial T} \) is the temperature coefficient for thermistor, and the slope is negative. So we can say that thermistor has negative temperature coefficient of resistance (NTC). Fig. 1.64(a) shows thermistor compensation technique. As shown in Fig. 1.64(a), \( R_2 \) is replaced by thermistor \( R_T \) in self bias circuit. With increase in temperature, \( R_T \) decreases. Hence voltage drop across it also decreases. This voltage drop is nothing but the voltage at the base with respect to ground. Hence, \( V_{BE} \) decreases which reduces \( I_B \). This behavior will tend to offset the increase in collector current with temperature.
We know, \[ I_C = \beta I_B + (1 + \beta)I_{CBO} \]

In this equation, there is increase in \( I_{CBO} \) and decrease in \( I_B \) which keeps \( I_C \) almost constant.

Fig. 1.64 (b) shows another thermistor compensation technique. Here, thermistor is connected between emitter and \( V_{CC} \) to minimize the increase in collector current due to changes in \( I_{CO} \), \( V_{BE} \), or \( \beta \) with temperature.

\( I_C \) increases with temperature and \( R_T \) decreases with increase in temperature. Therefore, current flowing through \( R_E \) increases, which increases the voltage drop across it. E - B junction is forward biased. But due to increase in voltage drop across \( R_E \), emitter (N-type for NPN transistor) is made more positive, which reduces the forward bias voltage \( V_{BE} \). Hence, base current reduces.

\( I_C \) is given by,

\[ I_C = \beta I_B + (\beta + 1)I_{CBO} \]

As \( I_{CBO} \) increases with temperature, \( I_B \) decreases and hence \( I_C \) remains fairly constant.

**Sensistor Compensation Technique**

This method of transistor compensation uses temperature sensitive resistive element, sensistors rather than diodes or transistors. It has a positive temperature coefficient, its resistance increases exponentially with increasing temperature as shown in the Fig. 1.65.

Slope of this curve \( \frac{\partial R_T}{\partial T} \)

\( \frac{\partial R_T}{\partial T} \) is the temperature coefficient for thermistor, and the slope is positive.

So we can say that sensistor has positive temperature coefficient of resistance (PTC).
11. The amplifier shown in Fig. an n-channel FET for which, $I_D=0.8\text{mA}$, $V_P=-20\text{V}$ and $I_{DSS}=1.6\text{mA}$. Assume that $r_d>R_d$. Find (1) $V_{GS}$ (2) $g_m$ (3) $R_s$. [NOV/DEC-2007]

Solution: We have,

i) $V_{DS} = V_P \left( 1 - \sqrt{\frac{I_D}{I_{DSS}}} \right) = -2 \left( 1 - \sqrt{\frac{0.8 \times 10^{-3}}{1.65 \times 10^{-3}}} \right) = -0.6074 \text{ V}$

ii) $g_m = \frac{-2I_{DSS}}{V_P} = \frac{-2 \times 1.65}{-2} = 1.65 \text{ mS}$

$g_m = g_{mo} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 1.65 \left( 1 - \frac{0.6074}{2} \right) \times 10^{-3}$

$= 1.65 \times 10^{-3} \times 0.6963 = 1.15 \text{ mS}$

iii) Applying KVL we have

$0 = V_{GS} + I_D R_s$

$\therefore R_s = - \frac{V_{GS}}{I_D} = - \left( \frac{0.6074}{0.8 \text{ mA}} \right) = 759.25 \Omega$
UNIT II

1. Explain the common emitter amplifier.

To make the transistor work as an amplifier, it is to be biased to operate in the active region, (i.e.) base – emitter junction is to be forward biased, while base – collector junction to be reversed biased.

Let us consider the common emitter amplifier circuit using self bias or voltage divider bias as shown above.

In the absence of input signal, only dc voltages are present in the circuit. This is known as zero-signal or no – signal condition or quiescent condition for the amplifier. The dc collector – emitter voltage $V_{CE}$, the dc collector current $I_C$ and dc base current $I_B$ is the quiescent operating point for the amplifier. On this dc quiescent operating point, we super impose ac signal by application of ac sinusoidal voltage at the input. Due to this base current varies sinusoidally as show in fig.

The output current i.e. the collector current is $\beta$ times larger than the input base current in common emitter configuration. Hence the collector current will also vary sinusoidally about its quiescent value, $I_{CQ}$. The output voltage will also vary sinusoidally as shown below.
The variations in the collector current and the voltage between collector and emitter due to change in the base current are shown below with the help of load line.

The collector current varies above and below its Q point value in-phase with the base current and the collector to emitter voltage varies above and below its Q point value 180° out of phase with the base voltage.

When one cycle of input is completed, one cycle of output will also be completed. This means the frequency of output sinusoidal is the same as the frequency of input sinusoid.
2. Explain the practical common emitter amplifier circuit.

![Practical common emitter amplifier circuit](image)

It consists of different circuit component. The functions of these components are as follows.

**Biasing circuit:**

The resistances $R_1$, $R_2$ and $R_E$ form the voltage divider biasing circuit for the CE amplifier. It sets the proper operating point for the CE amplifier.

**Function of Input capacitor $C_1$ in CE amplifier circuit:**

This capacitor couples the signal to the base of the transistor. It blocks any dc component present in the signal and passes only ac signal for amplification.

**Need for emitter bypass capacitor $C_E$ is used in CE amplifier circuit:**

An emitter bypass capacitor $C_E$ is connected in parallel with the emitter resistance $R_E$ to provide a low reactance path to the amplified ac signal. If it is not inserted, the amplified ac signal passing through $R_E$ will cause a voltage drop across it. This will reduce the output voltage, reducing the gain of the amplifier.

**Need for output coupling capacitor $C_2$:**

The coupling capacitor $C_2$ couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks dc and passes only ac part of the amplified signal.

**Need for $C_1$, $C_2$ and $C_E$:**

We know that the impedance of capacitor is given as,

$$X_c = \frac{1}{\omega C}$$
2 

Thus, at signal frequencies, all the capacitors have extremely small impedance and it can be treated as an ac short circuit. For bias / dc conditions of the transistor all the capacitors act as a dc open circuit.

Consider that the signal source is connected directly to the base of the transistor as shown below.

The source resistance Rs is in parallel with R2 and this will reduce the bias voltage at the transistor base and consequently alter the collector current, which is not desired. By connecting R_L directly, the dc levels of Vcc and V_CE will change. So to avoid this and maintain the stability of bias condition coupling capacitors are connected. By connecting C1, any dc component in the signal is opposed and only ac signal is routed to the transistor amplifier.

The emitter resistance R_E provides bias stabilization. But it also reduces the voltage swing at the output. The emitter bypass capacitor C_E provides a low reactance path to the amplified ac signal increasing the output voltage swing.

For the proper operation of the circuit, polarities of the capacitors must be connected correctly. The –ve terminal must always be connected at a dc voltage level lower than the dc level of +ve terminal.

3. Explain the common collector amplifier circuit in detail.

The dc biasing is provided by R1, R2 and R_E, the load resistance is capacitor coupled to the emitter terminal of the transistor.

When a signal is applied via to the base of the transistor, V_B is increased and decreased as the signal goes positive and negative respectively.

From the figure, we can write that,
\[ V_E = V_B - V_{BE}. \]

Considering \( V_{BE} \) fairly constant, variation in the \( V_B \) appears at emitter and emitter voltage \( V_E \) will vary same as base voltage \( V_B \). Since the emitter is output terminal, the output voltage from a common collector circuit is the same as its input voltage.

4. Obtain the gain, input impedance and output impedance of single stage BJT amplifier using midband analysis. [OR] Derive the expressions for the current gain, input impedance, voltage gain and output admittance of a small signal transistor amplifier in terms of the \( h \)-parameters. [May-2006]

The above shows basic amplifier circuit. To form a transistor amplifier only it is necessary to connect an external load and signal source, along with proper biasing. We can replace transistor circuit with its small signal hybrid model.

Let us analyze hybrid model to find the current gain, the input impedance, the voltage gain, and output impedance.

**Current Gain \((A_i)\):**

For transistor amplifier \( A_i \) is defined as the ratio of output to input currents. It is given by,

\[
A_i = \frac{I_L}{I_1} = -\frac{I_2}{I_1}
\]

Here \( I_L \) and \( I_2 \) are equal in magnitude but opposite in sign. i.e., \( I_L = -I_2 \)
From the circuit equivalent circuit we have,

\[ I_2 = h_f I_1 + h_0 V_2 \]

Substituting \( V_2 = -I_2 R_L \) in the equation we obtain,

\[ I_2 = h_f I_1 + h_0 (-I_2 R_L) \]
\[ I_2 + h_0 I_2 R_L = h_f I_1 \]
\[ I_2(1 + h_0 R_L) = h_f I_1 \]

\[ \frac{I_2}{I_1} = \frac{h_f}{1 + h_0 R_L} \]

\[ A_i = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_0 R_L} \]

\[ A_i = \frac{-h_f}{1 + h_0 R_L} \]

**Current Gain (A_s):**

It is the current gain taking into account the source resistance, \( R_S \) if the model is driven by the current source instead of voltage source. It is given by

\[ A_s = \frac{-I_2}{I_s} = \frac{-I_2 / I_1}{I_s / I_s} \]

\[ A_s = A_i \cdot \frac{I_1}{I_s} \]

Looking at above fig (b) and using current divider equation we get
\[ I_1 = \frac{I_s R_s}{Z_i + R_s} \]
\[ I_1 = \frac{R_s}{I_s} \]
\[ A_{i_s} = \frac{A_i R_s}{Z_i + R_s} \]

**Input impedance (Z\_i):**

R\_i is the input resistance looking into the amplifier input terminals (1, 1'). It is given by,
\[
R_i = \frac{V_i}{I_i}
\]

From the input circuit of equivalent circuit, we have
\[
V_i = h_i I_1 + h_r V_2
\]
\[
Z_i = \frac{V_i}{I_1} = \frac{h_i I_1 + h_r V_2}{I_1}
\]

Substituting \( V_2 = -I_2 R_L = A_i I_1 R_L \)

In the above equation we get,
\[
Z_i = h_i + \frac{h_r A_i I_1 R_L}{I_1} = h_i + h_r A_i R_L
\]

Substituting \( A_i = -\frac{h_f}{1 + h_0 R_L} \)

We..get........... \( Z_i = h_i - \frac{h_r h_f R_L}{1 + h_0 R_L} \)

Dividing numerator and denominator by \( R_L \) we get,
\[
Z_i = h_i - \frac{h_r h_f}{R_L + h_0}
\]
\[
Z_i = h_i - \frac{h_r h_f}{Y_L + h_0} \] Where... \( Y_L = \frac{1}{R_L} \)

\[
Z_i = h_i - \frac{h_r h_f}{Y_L + h_0}
\]

From this equation we can note that input impedance is a function of the load impedance.
Voltage Gain ($A_V$):-

It is the ratio of output voltage $V_2$ to the input voltage $V_1$. It is given by

$$A_V = \frac{V_2}{V_1} \quad \text{Substituting} \quad V_2 = A_i I_L R_i$$

$$A_V = \frac{A_i I_L R_i}{V_1} = \frac{A_i R_i}{Z_i} \quad \text{Since} \quad \frac{I_1}{V_1} = \frac{1}{Z_i}$$

$$A_V = \frac{A_i R_i}{Z_i}$$

Voltage Gain ($A_{VS}$):-

It is voltage gain including the source. It is given by,

$$A_{VS} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_S}$$

$$A_{VS} = A_v \cdot \frac{V_1}{V_S} \quad \text{.............} \quad M$$

Applying potential divider thermo we can write,

$$V_1 = \frac{Z_i}{R_s + Z_i} V_S$$

$$\therefore \quad \frac{V_1}{V_S} = \frac{Z_i}{R_s + Z_i}$$

Substituting value of $\frac{V_1}{V_S}$ in equation ‘$M$’ we get,

$$A_{VS} = A_v \cdot \frac{Z_i}{R_s + Z_i}$$

$$A_{VS} = \frac{A_i R_L}{R_s + R_i} \quad \therefore A_{VS} = \frac{A_i R_L}{Z_i}$$

$$A_{VS} = \frac{A_i R_L}{Z_i}$$

Output Admittance $Y_0$:-

It is the ratio of output current $I_2$ to the output voltage $V_2$. It is given by,

$$Y_0 = \frac{I_2}{V_2} \quad \text{with} \quad V_S = 0$$
We Know, \[ I_2 = h_f I_1 + h_v V_2. \]

Dividing above equation by \( V_2 \) we get,

\[ \frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_v \]

\[ Y_0 = h_f \frac{I_1}{V_2} + h_v, \ldots, N \]

From fig with \( V_S = 0 \) we can write,

\[ R_S I_1 + h_r I_1 + h_v V_2 = 0 \]

\[ \therefore (R_S + h_r)I_1 = -h_v V_2 \]

\[ \therefore \frac{I_1}{V_2} = \frac{-h_v}{R_S + h_r} \]

Substituting value of \( \frac{I_1}{V_2} \) in equation ‘N’ we get,

\[ Y_0 = h_v - \frac{h_r}{R_S + h_r} \]

From this equation we can note that output admittance is a function of the source resistance.

5. Give the comparison between CB, CE and CC amplifiers

<table>
<thead>
<tr>
<th>S.No</th>
<th>Characteristics</th>
<th>Common Base</th>
<th>Common Emitter</th>
<th>Common Collector</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Input Resistance</td>
<td>Very Low (20Ω)</td>
<td>Low (1 KΩ)</td>
<td>High (500 KΩ)</td>
</tr>
<tr>
<td>2</td>
<td>Output Resistance</td>
<td>Very High (1 MΩ)</td>
<td>High (40KΩ)</td>
<td>Low (50 Ω)</td>
</tr>
<tr>
<td>3</td>
<td>Input Current</td>
<td>( I_E )</td>
<td>( I_B )</td>
<td>( I_B )</td>
</tr>
<tr>
<td>4</td>
<td>Output Current</td>
<td>( I_C )</td>
<td>( I_C )</td>
<td>( I_E )</td>
</tr>
<tr>
<td>5</td>
<td>Input Voltage applied between</td>
<td>Emitter and Base</td>
<td>Base and Emitter</td>
<td>Base and Collector</td>
</tr>
<tr>
<td>6</td>
<td>Output Voltage taken from</td>
<td>Collector and Base</td>
<td>Collector and Emitter</td>
<td>Emitter and Collector</td>
</tr>
<tr>
<td>7</td>
<td>Current amplification factor</td>
<td>( \alpha = \frac{I_C}{I_E} )</td>
<td>( \beta = \frac{I_C}{I_B} )</td>
<td>( \gamma = \frac{I_E}{I_B} )</td>
</tr>
<tr>
<td>8</td>
<td>Current Gain</td>
<td>Less than Unity</td>
<td>High(20 to few)</td>
<td>High(20 to few)</td>
</tr>
</tbody>
</table>
6. State and prove the Miller’s theorem. [APR/MAY 2004]

Miller’s Theorem:-

Miller’s thermo states that the current $I_1$ drawn from node 1 through the impedance $Z$ can be obtained by disconnecting node 1 from $Z$ and by bringing impedance $\frac{Z}{(1-K)}$ from node 1 to ground, $\frac{ZK}{(K-1)}$ from node 2 to ground.

![Diagram](image)

If ‘Z’ is the impedance connected between two nodes, node 1 and node 2.

‘Z’ is replaced by two separate impedances $Z_1$ and $Z_2$. Where $Z_1$ is connected between node 1 and ground and $Z_2$ is connected between node 2 and ground.

The $V_i$ and $V_o$ are the voltages at the node 1 and node 2 respectively.

The values of $Z_1$ and $Z_2$ can be derived from the ratio of $V_o$ and $V_i$ denoted as $K$.

The values of impedance $Z_1$ and $Z_2$ are

$$Z_1 = \frac{Z}{(1-K)}; \quad Z_2 = \frac{ZK}{(K-1)}$$

Proof of Miller’s Theorem:-

Miller’s theorem states that the effect of resistance $Z$ on the input circuit is a ratio of input voltage $V_i$ to the current $I$ which flows from the input to the output.

Therefore,
\[ Z_1 = \frac{V_i}{I} \]

Where, \( I = \frac{V_i - V_0}{Z} = \frac{V_i \left[ 1 - \frac{V_0}{V_i} \right]}{Z} = \frac{V_i [1 - A_v]}{Z} \)

\[ \therefore Z_1 = \frac{V_i}{I} = \frac{Z}{1 - A_v} = \frac{Z}{1 - K} \quad \therefore \frac{V_0}{V_i} = A_v = K \]

\[ Z_1 = \frac{Z}{1 - K} \]

Miller’s theorem states that, the effect of resistance \( Z \) on the output circuit is a ratio of output voltage \( V_0 \) to the current \( I \) which flows from the output to the input.

Therefore,

\[ Z_2 = \frac{V_0}{I} \]

Where, \( I = \frac{V_0 - V_i}{Z} = \frac{V_0 \left[ 1 - \frac{V_i}{V_0} \right]}{Z} = \frac{V_0 \left[ 1 - \frac{1}{A_v} \right]}{Z} = \frac{V_0 \left[ A_v - 1 \right]}{A_v} \)

\[ \therefore Z_2 = \frac{V_0}{I} = \frac{Z}{A_v - 1} = \frac{Z A_v}{A_v - 1} = \frac{ZK}{K - 1} \quad \therefore \frac{V_0}{V_i} = A_v = K \]

\[ Z_2 = \frac{ZK}{K - 1} \]
7. Explain the techniques of improving input impedance.

We have seen that out of three configurations (CB, CC and CE), common collector or emitter follower circuit has high input impedance. Typically it is 200 kΩ to 300 kΩ. A single stage emitter follower circuit can give input impedance up to 500 kΩ. However, the input impedance considering biasing resistors is significantly less. Because \( R'_1 = R_1 \parallel R_2 \parallel R_1 \). The input impedance of the circuit can be improved by direct coupling of two stages of emitter follower amplifier. The input impedance can be increased using two techniques:

- Using direct coupling (Darlington connection)
- Using Bootstrap technique

**Darlington Transistors**

Fig. shows the direct coupling of two stages of emitter follower amplifier. This casceded connection of two emitter followers is called the Darlington connection.

**AC Equivalent Circuit:**

Assume that the load resistance \( R_L \) is such that \( R_L \cdot r_e < 0.1 \), therefore we can use approximate analysis method for analysing second stage.

Fig. shows approximate h-parameter (AC) equivalent circuit for common emitter configuration.
The same circuit can be redrawn by making collector common to have approximate h-parameter equivalent circuit for common collector configuration as shown in Fig.

Analysis of second stage:

a) Current Gain ($A_{i2}$):
\[
A_{i2} = \frac{I_o}{I_b} = -\frac{I_e}{I_b} = \frac{I_b + h_{fe} I_o}{I_b} = \frac{I_b(1 + h_{fe})}{I_b} = 1 + h_{fe}
\]

\[A_{i2} = 1 + h_{fe}\] \hspace{1cm} ... (1)

b) Input Resistance ($R_{i2}$):
\[R_{i2} = \frac{V_2}{I_{b2}}\]

Applying KVL to outer loop we get,
\[V_2 - I_{b2} h_{ie} - I_b R_E = 0\]
\[\therefore \quad V_2 = I_{b2} h_{ie} + I_b R_E\]
\[\therefore \quad \frac{V_2}{I_{b2}} = h_{ie} + \frac{I_b}{I_{b2}} R_E\]
\[\therefore \quad R_{i2} = h_{ie} + A_{i2} R_E \quad \text{since} \quad \frac{I_o}{I_{b2}} = A_{i2}\]
\[R_{i2} = h_{ie} + (1 + h_{fe}) R_E\] \hspace{1cm} ... (2)

\[R_{i2} = (1 + h_{fe}) R_E\quad \because \quad h_{ie} \ll (1 + h_{fe}) R_E\] \hspace{1cm} ... (3)

Analysis of first stage:

Looking at Fig. 2.60, we can see that load resistance of the first stage is the input resistance of the second stage i.e. $R_{i2}$. As $R_E$ is high, usually it does not meet the requirement $h_{ie} R_{i2} < 0.1$, and hence we have to use the exact analysis method for analysis of the first stage.

Fig. 2.62 shows the h-parameter equivalent circuit for common emitter configuration.
The same circuit can be redrawn by making collector common to have $h$-parameter equivalent circuit for common collector configuration.

![Diagram](image)

**Fig.**

a) Current Gain ($A_{I1}$):

$$A_{I1} = \frac{I_{e2}}{I_{b1}}$$

$$A_{I1} = \frac{I_{c1}}{I_{b1}}$$

$$I_{e1} = -(I_{b1} + I_{c1}) \quad \ldots (4)$$

and

$$I_{c1} = h_{fe} I_{b1} + h_{ce} V_{ces} = h_{fe} I_{b1} + h_{ce} (I_{e2} R_{L1}) = h_{fe} I_{b1} + h_{ce} I_{c1} R_{L1}$$

Substituting value of $I_{c1}$ equation 4 we get,

$$I_{e1} = -(I_{b1} + h_{fe} I_{b1} + h_{ce} I_{e2} R_{L1}) = -I_{b1} - h_{fe} I_{b1} - h_{ce} I_{c1} R_{L1}$$

$$I_{e1} + h_{ce} R_{L1} I_{c1} = -I_{b1} (1 + h_{fe})$$

$$\frac{I_{c1}}{I_{b1}} = \frac{1 + h_{fe}}{1 + h_{ce} R_{L1}}$$

We know that, $R_{L1} = (1 + h_{ce}) R_E$

$$A_{I1} = \frac{I_{c1}}{I_{b1}} = \frac{1 + h_{fe}}{1 + h_{ce} (1 + h_{fe}) R_E}$$

$$= \frac{1 + h_{fe}}{1 + h_{ce} h_{fe} R_E} \quad \because h_{fe} > > 1$$

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b) Input Resistance ($R_i$):

$$R_i = \frac{V_i}{I_{b1}}$$

Applying KVL to output loop we get,

$$V_i - I_{b1} h_{fe} - h_{re} V_{ce1} + V_{ce1} = 0$$

$$\therefore V_i = I_{b1} h_{fe} + h_{re} V_{ce1} - V_{ce1}$$

The terms $h_{re} V_{ce1}$ is negligible since $h_{re}$ is in the order of $2.5 \times 10^{-4}$

$$= I_{b1} h_{fe} - (I_{b2} R_{l1}) = I_{b1} h_{fe} + I_{b2} R_{l1}$$

$$\therefore R_i = \frac{V_i}{I_{b1}} = h_{fe} + \frac{I_{b2}}{I_{b1}} R_{l1} = h_{fe} + A_{i1} R_{l1}$$

$$\therefore R_i = h_{re} + A_{i1} (1 + h_{fe}) R_E$$  ... (6)

Substituting value of $A_{i1}$ we get,

$$R_i = \frac{V_i}{I_{b1}} = h_{fe} + \frac{(1 + h_{fe}) (1 + h_{fe}) R_E}{1 + h_{re} h_{fe} R_E}$$

$$\therefore R_i = h_{fe} + \frac{(1 + h_{fe})^2 R_E}{1 + h_{re} h_{fe} R_E}$$  ... (7)

$$\therefore h_{re} \ll \frac{(1 + h_{fe})^2 R_E}{1 + h_{re} h_{fe} R_E}$$  ... (8)

Overall Current Gain ($A_i$)

$$A_i = A_{i1} \times A_{i1}$$

$$= \frac{1 + h_{fe}}{1 + h_{re} (1 + h_{fe}) R_E} \times (1 + h_{fe})$$

$$\therefore A_i = \frac{(1 + h_{fe})^2}{1 + h_{re} (1 + h_{fe}) R_E}$$  ... (10)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Single stage</th>
<th>Darlington</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input resistance</td>
<td>$R_i = (1 + h_{fe}) R_E = 168.3 , k\Omega$</td>
<td>$R_i = \frac{(1 + h_{fe})^2 R_E}{1 + h_{re} (1 + h_{fe}) R_E} = 1.65 , M\Omega$</td>
</tr>
<tr>
<td>Current gain</td>
<td>$A_i = 1 + h_{re} = 51$</td>
<td>$A_i = \frac{(1 + h_{re})^2}{1 + h_{re} (1 + h_{re}) R_E} = 500$</td>
</tr>
</tbody>
</table>

Table
Table shows the comparison of input impedance and current gain provided by the single stage amplifier and Darlington connection. It is assumed that $R_k = 3.3\, \text{K}$ and $h$-parameters are as follows:

$$h_{le} = 1100, \quad h_{re} = 2.5 \times 10^{-4}, \quad h_{le} = 50 \quad \text{and} \quad h_{we} = 25 \, \mu\text{A}/\text{V}$$

Look at figure in Table 2.5 we can say that Darlington connection improves input impedance as well as current gain of the circuit.

Overall Voltage Gain:

We know that, $A_v = \frac{A_i R_L}{R_i}$

By subtracting 1 on both sides we get

$$1 - A_v = 1 - \frac{A_i R_L}{R_i}$$

$$\therefore 1 - A_v = \frac{R_i - A_i R_L}{R_i} = \frac{h_{le} + h_{re} A_i R_L}{R_i}$$

$$= \frac{h_{le}}{R_i} \quad \text{since} \quad h_{le} = h_{we} \quad \text{and} \quad h_{le} = 1 - h_{re} = 1$$

$$\therefore A_v = 1 - \frac{h_{le}}{R_i} \quad \ldots \quad (11)$$
We know that the overall voltage gain in multistage amplifier is a product of individual voltage gain.

\[ A_v = A_{v1} A_{v2} = \left(1 - \frac{h_{ie}}{R_{11}}\right) \left(1 - \frac{h_{ie}}{R_{12}}\right) \]

\[ A_v = 1 - \frac{h_{ie}}{R_{12}} - \frac{h_{ic} h_{ie}}{R_{11} R_{12}} + \frac{h_{ie}^2}{R_{11} R_{12}} \]

As we know, input resistance \( R_{in} >> R_{2} \) we can neglect term 3 and term 4 in the above equation.

\[ A_v = 1 - \frac{h_{ie}}{R_{12}} \]

**Output Impedance \((R_{o2})\):**

\[ R_o = \frac{1}{\text{Output admittance}} = \frac{1}{Y_o} \]

From equation, \( Y_o \) of the transistor is given as

\[ Y_o = Y_{o1} = h_{oe} - \frac{h_{fe} h_{ic}}{h_{ic} + R_s} = h_{oe} - \frac{(1 + h_{ie})}{h_{ic} + R_s} \]

Since

\[ h_{oe} = h_{oe} \]

\[ h_{fe} = -(1 + h_{fe}) \]

and

\[ h_{ic} = h_{ie} \]

\[ Y_{o1} = h_{oe} + \frac{(1 + h_{ie})}{h_{ic} + R_s} \]

\[ Y_{o1} = \frac{1 + h_{fe}}{h_{ic} + R_s} \]

\[ \therefore h_{oe} \ll \frac{(1 + h_{fe})}{h_{ic} + R_s} \]

\[ R_{o1} = \frac{1}{Y_{o1}} \]

\[ R_{o1} = \frac{h_{ie} + R_s}{1 + h_{fe}} \]

Looking at Fig. we can see that the \( R_{o1} \) of the first stage is the source resistance for second stage, i.e. \( R_{o2} = R_{o1} \)

\[ R_{o2} = R_{o1} + h_{i2} \frac{h_{i2} + R_s}{1 + h_{fe}} \]

\[ R_{o2} = \frac{h_{ie} + R_s}{1 - h_{fe}} + \frac{h_{i2}}{1 + h_{fe}} \]

\[ R_{o2} = \frac{h_{ie} + R_s}{(1 - h_{fe})^2} + \frac{h_{i2}}{1 + h_{fe}} \]

... (15)
Since the current in $T_2$ is $1 + h_{fe}$ times the current in $T_1$, $h_{re1} = (1 + h_{fe})h_{re2}$ substituting this value of $h_{re1}$ in equation 15 we get,

$$R_{oe} = \frac{(1 + h_{fe})h_{re2} + R_s}{(1 + h_{fe})^2} + \frac{h_{re2}}{1 + h_{fe}} = \frac{h_{re2}}{1 + h_{fe}} + \frac{R_s}{(1 + h_{fe})^2} + \frac{h_{re2}}{1 + h_{fe}}$$

\[\therefore R_{oe} = \frac{R_s}{(1 + h_{fe})^2} + \frac{2h_{re2}}{(1 + h_{fe})}\]

**Bootstrap Emitter Follower**

We have seen that, in emitter follower, the input resistance of the amplifier is reduced because of the shunting effect of the biasing resistors. To overcome this problem the emitter follower circuit is modified, as shown in the Fig.

Here, two additional components are used, resistance $R_s$ and capacitor $C$. The capacitor, is connected between the emitter and the junction of $R_1$, $R_2$ and $R_3$.

For d.c. signal, capacitor $C$ acts as an open circuit and therefore resistance $R_1$, $R_2$ and $R_3$ provides necessary biasing to keep transistor in the active region.

For a.c. signal, the capacitor acts as a short circuit. Its value is chosen such that it provides very low reactance nearly short circuit at lowest operating frequency. Hence, for a.c., the bottom of $R_3$ is effectively connected to the output (the emitter), whereas the top of $R_3$ is at the input (the base). In other words, $R_1$ is connected between input node and output node. For such connection effective input resistance is given by the Miller’s theorem. Refer section The theorem says that the impedance between the two nodes can be resolved into two components, one from each node to ground. The two components are:

$$\frac{Z}{1-K} \quad \text{and} \quad \frac{Z \cdot K}{K-1}$$
In our case $R_3$ is the impedance between output voltage and input voltage and $K$ is the voltage gain $V_o / V_i = A_v$

Fig. shows the bootstrap circuit with two resolved components of $R_3$ using Miller's theorem.

These are

$$R_{M1} = \frac{R_3}{1 - A_v} \quad \text{and} \quad R_{M2} = \frac{R_3 A_v}{A_v - 1}$$

Since, for an emitter follower, $A_v$ approaches unity, then $R_{M2}$ becomes extremely large.

For example, with $A_v = 0.99$ and $R_3 = 200 \, K$, we find $R_{M2} = 20 \, M$.

The $R'_i$ for the circuit shown in Fig. 2.70 can be given as

$$R'_i = R_i \parallel R_M$$
where $R_i = h_{ie} + (1 + h_{re}) R_E$ for emitter follower.

The above effect, when $A_v \to 1$, is called bootstrapping. The name arises from the fact that, if one end of the resistor $R_3$ changes in voltage, the other end of $R_3$ moves through the same potential difference; it is as if $R_3$ is pulling itself up by its bootstraps.

The effective load on the emitter follower can be given as

$$R_{L_{eff}} = R_E \parallel R_1 \parallel R_2 \parallel R_{M2}$$

Because of the capacitor, biasing resistances $R_1$ and $R_2$ come on output side shunting effective load resistance. The resistance $R_{M2}$ is very large and hence it is often neglected.

$$\therefore R_{L_{eff}} = R_E \parallel R_1 \parallel R_2$$

8. Explain with circuit diagram the boot strapped Darlington emitter follower. [Dec – 2002]

**Bootstrap technique:**

If one end of the resistor changes in voltage, other end of the resistor also moves through the same change in voltage. This technique is known as bootstrapping. It is used to increase the input impedance of the Darlington pair circuits.
Bootstrapped Darlington circuit:

- In emitter follower, the input resistance of the amplifier is reduced because of the shunting effect of the biasing resistors.
- But still there is a maximum limit is put by the collector to base resistance of the transistor which appears in parallel with the input resistance.
- It is expressed in admittance form by the parameter $h_{ob}$ of the transistor. Therefore, resistance between base and collector of transistor is given as $1/h_{ob}$, which is of the order of 2MΩ.
- The capacitor $C_0$ is connected between the first collector $C_1$ and the second emitter $E_2$. It acts as a short circuit for a.c signals.
- The collector resistance $R_{C1}$ is connected between $V_{CC}$ and first collector $C_1$. It is essential because, without it, $R_{E2}$ would be shorted to ground.
- Any change in the input causes $E_2$ to change by $A_V V_i$ and as $E_2$ is connected to the collector of the first transistor same changes appear at the collector of the first transistor.
- Hence $1/h_{ob}$ is now effectively increased to $1/(h_{ob}) (1-A_V)$ using Miller’s theorem, and can be ignored for calculation of input resistance.
- Therefore, input resistance of Darlington connection is $R_1 = h_{fe1} h_{fe2} R_{E2}$ and now it is not limited by collector to base resistance of the transistor $T_1$.

AC Equivalent circuit for bootstrapped Darlington Circuit:-

- The analysis of Darlington connection that for second stage we can use approximate analysis, but for first stage we have to use exact analysis.
The figure shows the $h$-parameter equivalent circuits for stage 1 and stage 2 for common emitter configuration.

These circuits are redrawn by making collector to common to get $h$-parameter equivalent circuit for common collector configuration.

Fig. (c) and (d) shows the $h$-parameter equivalent circuits for common collector configuration.

We know that capacitor $C_0$ acts as short circuit for all operating frequencies, therefore it connects collector of first transistor to emitter of second transistor.

First transistor $E_1$ is connected to the $B_2$ of the second transistor.
The complete h-parameter equivalent circuit for bootstrapped Darlington circuit is given below.

![Circuit Diagram]

The equivalent circuit shows that the effective $R_E$ is now the parallel combination of $R_{E2}$ and $R_{C1}$.

$$R_E = R_{E2} \parallel R_{C1}$$

And

$$R_i = h_{fe1} h_{fe2} (R_{E2} \parallel R_{C1}).$$


**Method for Analysis of a Transistor Circuit**

In the previous section we have seen generalized transistor circuit analysis using h-parameters. There are many transistor circuits. Circuits may consist of different biasing techniques, different configurations and so on. The analysis of such transistor circuits for its small signal behaviour can be made by following simple guidelines. These guidelines are:

1. Draw the actual circuit diagram.
2. Replace coupling capacitors and emitter bypass capacitor by short circuit.
3. Replace d.c source by a short circuit. In other words, short $V_{CC}$ and ground lines.
4. Mark the points B(base), C(collector), E(emitter) on the circuit diagram and locate these points as the start of the equivalent circuit.
5. Replace the transistor by its h-parameter model.

Following example explains us how to use guidelines for the analysis of a transistor circuit.

Consider a common emitter amplifier with voltage divider bias circuit as shown in the Fig. (a)
Guideline 5: Replace transistor by its h-parameter model and calculate effective R'_1 (R'_1) and effective R'_0 (R'_0).

For example, in the above circuit R'_1 = R_1 \parallel R_2 \parallel R_l

and R'_0 = R_2 \parallel R_C.

With these guidelines we will analyze CE, CB and CC amplifier circuits in coming sections.

Fig. (a) Circuit with transistor replaced by h-parameter equivalent

Guideline 1: Draw actual circuit diagram

Guideline 2: Short coupling and bypass capacitors

Guideline 3: Short V_{CC} and ground lines.

Guideline 4: Mark points B, C, E and locate these points as the start of the equivalent circuit.

(c) Circuit with V_{CC} and ground short circuit

(d) Circuit with B, C and E points located
10. Draw and explain the JFET low frequency small signal model.

We know that, drain to source current of JFET is controlled by gate to source voltage. The change in the drain current due to change in gate to source voltage can be determined using the transconductance factor $g_m$. It is given as

$$\Delta I_d = g_m \Delta V_{GS} \quad \ldots \quad (1)$$

We know that, in BJT the relation between an output and input quantity is given by amplification factor $\beta$, whereas in JFET this relation is given by transconductance factor $g_m$.

The another important parameter of JFET is drain resistance $r_d$. It is given by

$$r_d = \frac{\Delta V_{DS}}{\Delta I_d} \bigg|_{V_{GS}=\text{constant}} \quad \ldots \quad (2)$$

It determines the output impedance $Z_o$ of the JFET amplifier.

**JFET Low Frequency a.c. Equivalent Circuit**

Fig. shows the small signal low frequency a.c. equivalent circuit for n-channel JFET. The relation of $I_d$ by $V_{gs}$ is included as a current source $g_m V_{gs}$ connected from drain to source. The input impedance is represented by the open circuit at its input terminals, since gate current $I_g$ is zero. The output impedance is represented by $r_d$ from drain to source.

![Fig. JFET low frequency a.c. equivalent circuit for n-channel JFET](image)

**Approximate a.c. Equivalent Circuit**

When the value of external drain resistance $R_D$ is very small as compared to the value of output impedance represented by $r_d$, it is possible to replace $r_d$ by open circuit. This gives us approximate a.c. equivalent circuit of JFET amplifier, as shown in Fig.

![Fig. Approximate ac equivalent circuit for JFET amplifier](image)
11. Draw the small signal analysis of common source amplifier with fixed bias.

Fig. shows common source amplifier with fixed bias. The coupling capacitor $C_1$ and $C_2$ which are used to isolate the d.c. biasing from the applied a.c. signal act as short circuits for the a.c. analysis.

**Fig.** Common source JFET amplifier with fixed bias

Fig shows the low frequency equivalent model for the common source amplifier circuit with fixed bias. It is drawn by replacing:

- All capacitors and d.c. supply voltages with short circuits and
- JFET with its low frequency equivalent circuit.
Fig. A.C. equivalent model for the common source amplifier circuit with fixed bias

Now, we see the input impedance output impedance and voltage gain of the above model.

Input impedance $Z_i$:

Looking into Fig. 3.5 we can say that,

$$Z_i = R_G \quad \text{... (1)}$$

Output Impedance $Z_o$:

The output impedance $Z_o$ is the impedance measured looking from the output side with input voltage ($V_i$) equal to 0. As $V_i = 0$,

$$V_{gs} = 0 \text{ and hence } g_m V_{gs} = 0.$$
The \( g_m V_g = 0 \) allows current source to be replaced by an open circuit, as shown in the Fig. Therefore the output impedance is

\[
Z_o = R_D || r_d \quad \ldots \quad (2)
\]

If the resistance \( r_d \) is sufficiently large compared to \( R_D \), then we say that the output impedance is approximately equal to \( R_D \).

\[
Z_o \approx R_D \quad \therefore r_d \gg R_D \quad \ldots \quad (3)
\]

**Voltage Gain \( A_v \):**

The voltage gain \( A_v = \frac{V_o}{V_i} = \frac{V_o}{V_i} \)

Looking at Fig. 3.5 we can write

\[
V_o = -g_m V_g \ (r_d || R_D) \quad \ldots \quad (4)
\]

As we know \( V_i = V_g \), we can write

\[
V_o = -g_m V_i \ (r_d || R_D) \quad \ldots \quad (5)
\]

\[
A_v = \frac{V_o}{V_i} = -g_m \ (r_d || R_D) \quad \ldots \quad (6)
\]

and if \( r_d \gg R_D \),

\[
A_v = -g_m R_D \quad \ldots \quad (7)
\]

12. Explain the methods of coupling multistage amplifier.

In multistage amplifier, the output signal of preceding stage is to be coupled to the input circuit of succeeding stage. For this interstage coupling, different types of coupling elements can be employed. These are:

1. RC coupling
2. Transformer coupling
3. Direct coupling

**RC Coupling**

Fig. shows RC coupled amplifier using transistors. As shown in the Fig., the output signal of first-stage is coupled to the input of the next stage through coupling capacitor and resistive load at the output terminal of first stage.

The coupling does not affect the quiescent point of the next stage since the coupling capacitor \( C_C \) blocks the dc voltage of the first stage from reaching the base of the second stage. The RC network is broadband in nature. Therefore, it gives a wideband frequency response without peak at any frequency and hence used to cover a complete AF amplifier bands. However its frequency response drops off at very low frequencies due to coupling capacitors and also at high frequencies due to shunt capacitors such as stray capacitance.
Transformer Coupling

Fig. shows transformer coupled amplifier using transistors. As shown in the Fig., the output signal of the first stage is coupled to the input of the next stage through an impedance matching transformer.

Fig. Two stage transformer coupled amplifier using transistors

This type of coupling is used to match the impedance between output and input cascaded stage. Usually, it is used to match the larger output resistance of AF power amplifier to a low impedance load like loudspeaker. As we know, transformer blocks dc, providing dc isolation between the two stages. Therefore, transformer coupling does not affect the quiescent point of the next stage.
These provide high gain at the desired of frequency, i.e. they amplify selective frequencies. For this reason, the transformer-coupled amplifiers are used in radio and TV receivers for amplifying RF signals.

As dc resistance of the transformer winding is very low, almost all dc voltage applied by $V_{CC}$ is available at the collector. Due to the absence of collector resistance it also eliminates unnecessary power loss in the resistor.

**Direct Coupling**

Fig. 2.12 shows direct coupled amplifier using transistors. As shown in the Fig. 2.12 the output signal of first stage is directly connected to the input of the next stage. This direct coupling allows the quiescent dc collector current of first stage to pass through base of the next stage, affecting its biasing conditions.

Due to absence of RC components, its low frequency response is good but at higher frequencies shunting capacitors such as stray capacitances reduce the gain of the amplifier.

The transistor parameters such as $V_{BE}$ and $\beta$ change with temperature causing the collector current and voltage to change. Because of direct coupling these changes appear at the base of the next stage, and hence in the output. Such an unwanted change in the output is called drift and it is serious problem in the direct coupled amplifiers.

Frequency response of transformer coupled amplifier is poor in comparison with that of an RC coupled amplifier. Its leakage inductance and interwinding capacitances does not allow amplifier to amplify the signals of different frequencies equally well. Interwinding capacitance of the transformer coupled may give rise resonance at certain frequency which makes amplifier to give very high gain at that frequency. By putting shunting capacitors across each winding of the transformer, we can get resonance at any desired RF frequency. Such amplifiers are called tuned voltage amplifiers.
13. (i). Draw a cascade amplifier and its equivalent circuit. What are the special features of cascade amplifier?

(ii). Derive the voltage gain, input impedance and output impedance of the above cascade amplifier.

**Cascade amplifier:**
- The cascade amplifier consists of a common emitter amplifier stage in series with a common base amplifier.
- Transistor T₁ and its associated components operate as a common emitter amplifier stage, while the circuit of T₂ functions as a common base output stage.
- The cascade amplifier gives the high input impedance of a common emitter amplifier, as well as the good voltage gain and high frequency performance of a common base circuit.

![Cascade Amplifier Diagram](image)

- For the dc bias conditions of the circuit, it is seen that the emitter current for T₁ is set by $V_{E1}$ and $R_{E1}$.
- Collector current $I_{C1}$ approximately equals $I_{E1}$ and $I_{E2}$ is same as $I_{C1}$. Therefore, $I_{C2}$ approximately equals $I_{E1}$. This current remains constant regardless of the level of $V_{B2}$, as long as $V_{CE1}$ remains enough for current operation of T₁.

The AC equivalent circuit for cascade amplifier is drawn by shorting dc supply and capacitors.
The simplified h-parameter equivalent circuit for cascade amplifier is drawn by replacing transistors with their simplified equivalent circuits.

Analysis of second stage (CB amplifier):

a). Current gain ($A_{i2}$):

$$A_{i2} = \frac{h_{fe}}{1 + h_{fe}}$$

b). Input resistance ($R_{i2}$):

$$R_{i2} = \frac{h_{ie}}{1 + h_{fe}}$$

c). Voltage gain ($A_{v2}$):

$$A_{v2} = \frac{A_{i2} R_{L2}}{R_{i2}}$$

Analysis of first stage (CE amplifier):
a). Current gain ($A_{i1}$):-
\[ A_{i1} = -h_{fe} \]

b). Input resistance ($R_{i1}$):-
\[ R_{i1} = h_{ie} \]

c). Voltage gain ($A_{V1}$):-
\[ A_{V1} = \frac{A_{i1}R_{L1}}{R_{i1}} \]

Overall voltage gain ($A_{V}$):-
\[ A_{V} = A_{V1} \times A_{V2} \]

Overall input resistance ($R_{i}$):-
\[ R_{i} = R_{i1} \parallel R_{B} \]
\[ R_{i} = R_{i1} \parallel R_{3} \parallel R_{4} \]

Overall voltage gain ($A_{V3}$):-
\[ A_{V3} = \frac{V_{0}}{V_{S}} = \frac{V_{0}}{V_{i}} \times \frac{V_{i}}{V_{S}} \]
\[ A_{V3} = A_{V} \times \frac{R_{i}}{R_{i} + R_{S}} \]

Overall current gain ($A_{iS}$):-
\[ A_{iS} = \frac{I_{0}}{I_{S}} = \frac{I_{0} \times I_{C2} \times I_{e2} \times I_{C1} \times I_{b1}}{I_{C2} \times I_{e2} \times I_{C1} \times I_{b1} \times I_{S}} \]
\[ \frac{I_{C2}}{I_{e2}} = -A_{i2} \]
\[ \frac{I_{C1}}{I_{b1}} = -A_{i1} \]
\[ \frac{I_{b1}}{I_{S}} = \frac{R_{B}}{R_{B} + R_{i1}} \]
\[ \therefore A_{iS} = \frac{I_{0}}{I_{C2}} \times (-A_{i2}) \times \frac{I_{C2}}{I_{e2}} \times (-A_{i1}) \times \frac{R_{B}}{R_{B} + R_{i1}} \]

Output resistance ($R_{0}$):-
\[ R_{01} = \alpha \]
\[ R_{02} = \alpha \]
\[ R_{0} = R_{02} \parallel R_{L} \]
14. Draw the circuit diagram for a differential amplifier using BJT’s. Describe common mode and differential modes of working. [APR-2003]

**Differential amplifier:**

The differential amplifier amplifies the difference between two input voltage signals. In an ideal differential amplifier, the output voltage $V_o$ is proportional to the difference between the two input signals.

$$V_o \sim (V_1 - V_2).$$

- Assume that the sine wave on the base of $Q_1$ is positive going while on the base of $Q_2$ is negative going. With a positive going signal on the base of $Q_1$, an amplified negative going signal develops on the collector of $Q_1$.
- Due to positive going signal, current through $R_E$ also increases and hence a positive going wave is developed across $R_E$.
- Due to negative going signal on the base of $Q_2$, an amplified positive going signal develops on the collector of $Q_2$. And a negative going signal develops across $R_E$, because of emitter follower action of $Q_2$.

**Differential Mode Operation:**

![Differential Amplifier Circuit Diagram](image-url)
- So signal voltage across $R_E$, due to the effect of $Q_1$ and $Q_2$ are equal in magnitude and $180^0$ out of phase, due to matched pair of transistors. Hence these two signals cancel each other and there is no signal across the emitter resistance.
- Hence there is no a.c signal current flowing through the emitter resistance. Hence $R_E$ in this case does not introduce negative feedback.
- While $V_0$ is the output taken across collector of $Q_1$ and collector $Q_2$. The two outputs on collector 1 and 2 are equal in magnitude but opposite in polarity.
- The $V_0$ is the difference between these two signals. Hence the difference output $V_0$ is twice as large as the signal voltage from either collector to ground.

**Common Mode Operation:**

- In Common mode, the signals applied to the base of $Q_1$ and $Q_2$ are derived from the same source. So the two signals are equal in magnitude as well as in phase.
- In phase signal voltages at the base of $Q_1$ and $Q_2$ causes in phase signal voltages to appear across $R_E$, which add together. Hence $R_E$ carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier.
- While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of $Q_1$ and $Q_2$.
- Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase. Thus the difference output $V_0$ is almost zero, negligibly small. Ideally it should be zero.
15. Derive the DC analysis of differential amplifier.

**D.C. Analysis**

The d.c. analysis means to obtain the operating point values i.e. $I_C$ and $V_{ESQ}$ for the transistors used. The supply voltages are d.c. while the input signals are a.c., so d.c. equivalent circuit can be obtained simply by reducing the input a.c. signals to zero. The d.c. equivalent circuit thus obtained is shown in the Fig. 2.10. Assuming $R_{S1} = R_{S2}$, the source resistance is simply denoted by $R_S$.

The transistors $Q_1$ and $Q_2$ are matched transistors and hence for such a matched pair we can assume:

i) Both the transistors have the same characteristics.

ii) $R_{E1} = R_{E2}$ hence $R_E = R_{E1} \parallel R_{E2}$.

iii) $R_{C1} = R_{C2}$ hence denoted as $R_C$.

iv) $|V_C| = |V_{EE}|$ and both are measured with respect to ground.

**D.C. equivalent circuit**

![D.C. equivalent circuit diagram]
As the two transistors are matched and circuit is symmetrical, it is enough to find out operating point \( I_Q \) and \( V_{QE} \), for any one of the two transistors. The same is applicable for the other transistor.

Applying KVL to base-emitter loop of the transistor \( Q_1 \),

\[
-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0
\]

But

\[
I_C = \beta I_B \quad \text{and} \quad I_C \equiv I_E
\]

\[
\therefore I_B = \frac{I_E}{\beta}
\]

Substituting in (1), we get

\[
\frac{-I_E}{\beta} R_S - V_{BE} - 2I_E R_E + V_{EE} = 0
\]

\[
\therefore I_E \left[ \frac{-R_S}{\beta} - 2R_E \right] + V_{EE} - V_{BE} = 0
\]

\[
\therefore I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E}
\]

where \( V_{BE} \) = 0.6 to 0.7 V for silicon

\( = 0.2 \) V for germanium transistors.

In practice, generally \( \frac{R_S}{\beta} < 2 R_E \),

\[
\therefore I_E = \frac{V_{EE} - V_{BE}}{2R_E}
\]

From the equation (6), we can observe that

i) \( R_E \) determines the emitter current of \( Q_1 \) and \( Q_2 \) for the known value of \( V_{BE} \).

ii) The emitter current through \( Q_1 \) and \( Q_2 \) is independent of collector resistance \( R_C \).

Now let us determine \( V_{CE} \). As \( I_E \) is known and \( I_E \approx I_C \), we can determine the collector voltage of \( Q_1 \) as

\[
V_C = V_{CC} - I_C R_C
\]

Neglecting the drop across \( R_S \), we can say that the voltage at the emitter of \( Q_1 \) is approximately equal to \(-V_{BE}\). Hence the collector to emitter voltage is

\[
\therefore V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (-V_{BE})
\]

\[
\therefore V_{CE} = V_{CC} + V_{BE} - I_C R_C
\]

Hence \( I_E = I_C \approx I_Q \) while \( V_{CE} = V_{QE} \) for given values of \( V_{CC} \) and \( V_{BE} \).
16. Explain the methods of improving CMRR with constant current source.

**Effect of $R_E$**

To improve the common-mode gain $A_c$, use negative feedback in $A_c$. Thus higher the CMRR, the different

But practically $R_f$

1. Large $R_E$ near transistors.
2. This increases hence practically provide effect of incre
3. Constant current load.
4. Let us discuss the
Without physically increasing the value of $R_E$, the $R_E$ is replaced by a transistor operated at a constant current. Such a constant current source circuit gives the effect of a very high resistance without affecting the Q point values of the differential amplifier. The differential amplifier using constant current bias circuit instead of $R_E$ is shown in the Fig.

The transistor used is $Q_3$ and the values of $R_3$, $R_2$ and $R_1$ are selected so as to give the same operating point values for the two transistors $Q_1$ and $Q_2$.

**Circuit Analysis**

Let current through $R_3$ be $I_{e3}$ while current through $R_1$ is $I$. Neglecting the base current of $Q_3$ which is very small due to large $\beta_{ac}$, we can assume that current through $R_2$ is also $I$.

Applying Kirchhoff's law,

$$-RI_1 - IR_2 + V_{EE} = 0$$

$$\therefore I = \frac{V_{EE}}{R_1 + R_2} \quad \ldots(1)$$

Now

$$V_b = -IR_1$$

Negative sign according to the direction of current.

$$\therefore V_b = -\frac{V_{EE}R_1}{R_1 + R_2} \quad \ldots(2)$$

Now

$$V_e = V_b - V_{BE}$$

and

$$I_{e3} = \frac{V_e - (-V_{EE})}{R_3} \quad \ldots(3)$$

Substituting expressions for $V_b$ and $V_e$,

$$\therefore I_{e3} = \frac{-V_{EE}R_1}{R_1 + R_2} - V_{BE} + V_{EE}$$

$$\therefore I_{e3} = \frac{V_{EE} \left[ \frac{R_2}{R_1 + R_2} \right] - V_{BE}}{R_3} \quad \ldots(4)$$

Neglecting $I_{B}$ we can write

$$I_{C3} = I_{e3}$$

Thus as $V_{EE}$, $R_1$, $R_2$, $R_3$ and $V_{BE}$ are constants, current $I_{C3}$ is almost equal to $I_{e3}$ and also constant. Thus circuit with transistor $Q_3$, acts as a constant current source.

Practically there is substantial increase in CMRR due to constant current bias without increasing biasing voltages and without disturbing Q point values of $Q_1$ and $Q_2$. 

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Temperature Compensation

In practice $V_{BE}$ is not constant but changes with respect to temperature, approximately at the rate of 2.5 mV/°C. This inturn may change $I_{E3}$. Thus there is necessity to provide a thermal compensation.

**Temperature compensated current source**

Such a thermal compensation is provided by replacing $R_2$ with the two diodes $D_1$ and $D_2$ as shown in the Fig.

As the temperature increases, the transistor current i.e. collector current $I_{C3}$ increases. At the same time the diode current also increases. This is because the diode current is given by

$$I_D = I_0 \left[ e^{V_D/\eta V_T} - 1 \right]$$

where $V_D$ is diode bias voltage, $V_T$ is the voltage equivalent of temperature and $\eta$ is constant.

$$V_T = \frac{T}{11600}$$

$\eta = 1$ for germanium $= 2$ for silicon

Due to increased diode current $I_D$, the base current of $Q_3$ decreases. This compensates for the increase in $I_{C3}$.

**Circuit Analysis**

Assume that the voltage drop across the diodes is same as $V_D$,

$$V_D = -V_{BE} + 2V_D$$

Now

$$V_E = V_D - V_{BE}$$

$$\therefore V_E = -V_{BE} + 2V_D - V_{BE}$$

And

$$I_{E3} = \frac{V_E}{R_3} = \frac{-V_{BE} + 2V_D - V_{BE}}{R_3}$$

$$\therefore I_{E3} = \frac{2V_D - V_{BE}}{R_3}$$

If the diode and transistor characteristics are same then $V_D$ is same as $V_{BE}$.

$$\therefore I_{E3} = \frac{V_D}{R_3} = I_{C3}$$

Thus for a given value of $R_3$, the emitter current $I_{E3}$ depends on the voltage drop across diodes. But drop across the diodes is a function of the current $I_D$, which is a part of current $I$, which is determined by the value of $R_1$. Thus the value of $I_{E3}$ can be varied by changing the value of $R_1$ or $R_E$, as per the requirement.

The value of $R_1$ can be obtained as,

$$R_1 = \frac{V_{BE} - 2V_D}{I_{E3}} = \frac{V_{BE} - 1.4(V)}{I_{E3}}$$

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**Current Mirror Circuit**

The circuit in which the output current is forced to equal the input current is called as **current mirror circuit**. In a current mirror circuit, the output current is the mirror image of input current. The basic block diagram is shown in the Fig. (a) while the Fig. (b) shows the circuit diagram.

![Current Mirror Circuit Diagram](image)

(a) Block diagram  
(b) Circuit diagram

**Circuit Analysis**

The circuit consists of two matched transistors $Q_3$ and $Q_4$. Their base-emitter voltage and base currents are same.

$$ \therefore V_{BE3} = V_{BE4} \text{ and } I_{B3} = I_{B4} $$

Similarly, their collector currents are also same.

$$ \therefore I_{C3} = I_{C4} $$

Applying KCL at node a,

$$ I_2 = I_{C4} + I $$

... (1)

Applying KCL at node b,

$$ I = I_{B3} + I_{B4} = 2I_{B4} = 2I_{B3} $$

$$ \therefore I_2 = I_{C4} + 2I_{B4} = I_{C3} + 2I_{B3} $$

... (2)
Now
\[ I_{B3} = \frac{I_c}{\beta} \]
\[ \therefore I_2 = I_c + \frac{2}{\beta} \]

Generally \( \beta \) is very large and hence \( \frac{2}{\beta} \) is negligibly small.
\[ \therefore I_2 \approx I_c \]

Thus the collector current of Q3 is nearly equal to the current I2. Hence once current mirror circuit is set for current I2, it provides constant current bias to the differential amplifier.

Thus I2 can be obtained by writing KVL for the base-emitter loop of transistor Q3.
\[ -I_2R_2 - V_{BE3} + V_{EE} = 0 \]
\[ \therefore I_2 = \frac{V_{EE} - V_{BE3}}{R_2} \]

Selecting R2, the appropriate I2 can be set for the current mirror circuit.

17. What is a transfer characteristic of differential amplifier? Derive it. [MAY -2006]

- The transfer characteristic of the differential amplifier is the graph of differential input \( V_d \) against the currents \( I_{C1} \) and \( I_{C2} \).

- To obtain the transfer characteristics, the following assumptions are made:
  1. The current source circuit used with current \( I_{EE} \) has infinite output resistance.
  2. The source resistances \( R_S \) in the base of transistors Q1 and Q2 are neglected.
  3. The output resistance of each transistor is infinite.

- The assumptions are valid for low frequency, large signals.

For a transistor, we can write the equation for its collector current as
\[ I_C = I_S e^{\frac{V_{BE}}{V_T}} \]

Where,
\( I_S \) = reverse saturation current.
\( V_{BE} \) = base – emitter voltage.
\( V_T \) = voltage equivalent of temperature.

Thus for two transistors we can write the equations for their collector currents as,
\[ I_{C1} = I_s e^{\frac{V_{BE1}}{V_T}} \]
\[ I_{C2} = I_s e^{\frac{V_{BE2}}{V_T}} \]

Where \( I_{S1} = I_{S2} = I_S \) as transistors are matched.

This equation is called as **Ebers-Moll equation** for the transistor.

\[ \therefore \ln \frac{I_{C1}}{I_S} = \frac{V_{BE1}}{V_T} \]
\[ V_{BE1} = V_T \ln \left[ \frac{I_{C1}}{I_S} \right] \]
\[ V_{BE2} = V_T \ln \left[ \frac{I_{C2}}{I_S} \right] \]

Now consider the loop including two inputs and two base emitter junctions, neglecting \( R_S \), as shown in the fig.

Applying KVL to the loop shown,
\[ V_{S1} - V_{BE1} + V_{BE2} - V_{S2} = 0 \]

Substituting \( V_{BE1} \) and \( V_{BE2} \) values in above equation, we get,
\[ V_{s1} - V_T \ln \left[ \frac{I_{c1}}{I_s} \right] + V_T \ln \left[ \frac{I_{c2}}{I_s} \right] - V_{s2} = 0 \]

\[ V_T \left[ \ln \left[ \frac{I_{c2}}{I_s} \right] - \ln \left[ \frac{I_{c1}}{I_s} \right] \right] = V_{s2} - V_{s1} \]

\[ V_T \left[ \ln \left[ \frac{I_{c1}}{I_s} \right] - \ln \left[ \frac{I_{c2}}{I_s} \right] \right] = V_{s1} - V_{s2} \]

\[ V_T \ln \left[ \frac{I_{c1}}{I_{c2}} \right] = V_{s1} - V_{s2} \]

\[ \ln \left[ \frac{I_{c1}}{I_{c2}} \right] = \frac{V_{s1} - V_{s2}}{V_T} \]

\[ \frac{I_{c1}}{I_{c2}} = e^{\frac{V_{s1} - V_{s2}}{V_T}} \]

\[ V_{s1} - V_{s2} = V_d \]

\[ \therefore \frac{I_{c1}}{I_{c2}} = e^{\frac{V_d}{V_T}} \text{ .................A} \]

Now, current through current source \( I_{EE} \) is the addition of the two emitter currents \( I_{E1} \) and \( I_{E2} \).

\[ I_{EE} = I_{E1} + I_{E2} \text{ .................B} \]

But

\[ I_E = \frac{I_c}{\alpha} \therefore I_{ER} = \frac{1}{\alpha} \left[ I_{c1} + I_{c2} \right] \]

Solving equations A and B simultaneously for \( I_{c1} \) and \( I_{c2} \) we get,

\[
I_{c1} = \frac{\alpha I_{EE}}{1 + e^{\frac{-V_d}{V_T}}} \\
I_{c1} = \frac{\alpha I_{EE}}{1 + e^{\frac{-V_d}{V_T}}}
\]
UNIT III
SINGLE STAGE FET, MOSFET AMPLIFIERS

1. Explain class ‘A’ power amplifiers and derive its efficiency. [Dec-2005]

Class ‘A’ Power amplifier:-

The power amplifier is said to be class ‘A’ amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

Class ‘A’ amplifiers are further classified as directly coupled and transformer coupled amplifiers.

Directly Coupled Class ‘A’ amplifier:-

- In direct coupled amplifier, the load is directly connected in the collector circuit.
- A simple fixed- bias circuit can be used as a large signal class ‘A’ amplifier. The transistor used in this circuit is power transistor.
- The value of $R_B$ is selected in such a way that the ‘Q’ point lies at the centre of the d.c load line.
- The overall circuit handles large power, in the range of a few to tens of watts without providing much voltage gain.

Circuit Diagram:

Applying Kirchhoff’s voltage law to the above circuit, we get,

\[ V_{CC} = I_c R_L + V_{CE} \]
\[ I_c R_L = -V_{CE} + V_{CC} \]
\[ I_c = \left[-\frac{1}{R_L}\right] V_{CE} + \frac{V_{CC}}{R_L} \]

Equation of a straight line, $y = mx + c$ .........2

Thus the slope of the load line is $-1/R_L$ while the Y-intercept is $V_{CC}/R_L$.

Graphical Representation:
**DC operation:**

The collector supply voltage $V_{CC}$ and resistance $R_B$ decides the d.c base – bias current $I_{BQ}$.

The expression is obtained applying KVL to the B- E loop and with $V_{BE} = 0.7V$.

\[ \therefore I_{BQ} = \frac{V_{CC} - 0.7V}{R_B} \]

The corresponding collector current is then,

\[ I_{CQ} = \beta I_{BQ} \]

The corresponding collector to emitter voltage is,

\[ V_{CEQ} = V_{CC} - I_{CQ}R_L \]

Hence the Q point can be defined as $Q(V_{CEQ}, I_{CQ})$.

**DC power Input:**

The d.c power input is provided by the supply. With no a.c input signal, the d.c current drawn is the collector bias current $I_{CQ}$. Hence d.c power input is,

\[ P_{DC} = V_{CC} \cdot I_{CQ} \]

It is important to note that even if a.c input signal is applied, the average current drawn from the d.c supply remains same. Hence the above equation represents d.c power input to the class ‘A’ series fed amplifier.

**AC operation:**

- When an input a.c signal is applied, the base current varies sinusoidally.
- Assuming that the nonlinear distortion is absent, the nature of the collector current and collector to emitter voltage also vary sinusoidally.
- The output current i.e. collector current varies around its quiescent value while the output voltage i.e collector to emitter voltage varies around its quiescent value.
- The varying output voltage and output current deliver an a.c power to the load.

**AC power output:**

For an alternating output voltage and output current swings, shown in above graph, we can write,

$V_{min}$ = Minimum instantaneous value of the collector (output) voltage.

$V_{max}$ = Maximum instantaneous value of the collector (output) voltage.

And $V_{PP}$ = Peak to Peak value of a.c output voltage across the load.

\[ \therefore V_{PP} = V_{max} - V_{min} \]
Now \( V_m = \) Amplitude (Peak) of a.c output voltage.

\[
\therefore V_m = \frac{V_{pp}}{2} = \frac{V_{\text{max}} - V_{\text{min}}}{2}
\]

Similarly we can write for the output current as,

\( I_{\text{min}} = \) Minimum instantaneous value of the collector (output) current.

\( I_{\text{max}} = \) Maximum instantaneous value of the collector (output) current.

And \( I_{PP} = \) Peak to Peak value of a.c output (load) current.

\[
\therefore I_{PP} = I_{\text{max}} - I_{\text{min}}
\]

Now \( I_m = \) Amplitude (Peak) of a.c output (load) current.

\[
\therefore I_m = \frac{I_{PP}}{2} = \frac{I_{\text{max}} - I_{\text{min}}}{2}
\]

Hence the r.m.s values of alternating output voltage and current can be obtained as,

\[
V_{rms} = \frac{V_m}{\sqrt{2}} \quad I_{rms} = \frac{I_m}{\sqrt{2}}
\]

Hence we can write,

\[
V_{rms} = I_{rms} \cdot R_L
\]

\[
V_m = I_m \cdot R_L
\]

The a.c power delivered by the amplifier to the load can be expressed by using r.m.s values, maximum i.e. peak values and peak to peak values of output voltage and current.

I). Using r.m.s \( P_{ac} = V_{rms}I_{rms} \) values:-

\( (or)P_{ac} = I_{rms}^2 R_L \)

\( (or)P_{ac} = \frac{V_{rms}^2}{R_L} \)

II) Using peak \( P_{ac} = V_{rms}I_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}} \) values:-

\[
P_{ac} = \frac{V_m I_m}{2} \quad (or)P_{ac} = \frac{I_{m}^2 R_L}{2}
\]

\( (or)P_{ac} = \frac{V_{rms}^2}{2R_L} \)
III). using peak to peak values:

\[ P_{ac} = \frac{V_{m}I_{m}}{2} = \left( \frac{V_{PP}}{2} \right) \left( \frac{I_{PP}}{2} \right) \]

\[ P_{ac} = \frac{V_{PP}I_{PP}}{8} \] .............................(W)

But as \( V_{PP} = V_{max} - V_{min} \) and \( I_{PP} = I_{max} - I_{min} \) : Substitute this in equation (W), then we get,

\[ P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8} \]

**Efficiency:**

The efficiency of an amplifier represents the amount of a.c power delivered (or) transferred to the load, from the d.c source i.e. accepting the d.c power input. The efficiency of an amplifier is,

\[ \% \eta = \frac{P_{ac}}{P_{dc}} \times 100 \]

Now for class ‘A’ operation, we have derived the expressions for \( P_{ac} \) and \( P_{dc} \), hence equations (1) and (2), we can write

\[ \% \eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8V_{CC}I_{cQ}} \times 100 \]

**Maximum Frequency:**

For maximum efficiency calculation, assume maximum swings of both the output voltage and the output current. From the graph we can see that the minimum voltage possible is zero and maximum voltage possible is \( V_{CC} \), for a maximum swing.
Similarly the minimum current is zero and the maximum current possible is 2 $I_{CO}$, for a maximum swing, for maximum swing

$$\begin{align*}
\left\{ \begin{array}{c}
V_{max} = V_{CC} \text{ and } V_{min} = 0 \\
I_{max} = 2I_{CO} \text{ and } I_{min} = 0
\end{array} \right. \\
\end{align*}$$

$$\%\eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8V_{cc}I_{CO}} \times 100$$

$$\%\eta = \frac{(V_{CC} - 0)(2I_{CO} - 0)}{8V_{cc}I_{CO}} \times 100$$

$$\%\eta = \frac{2I_{CO}V_{cc}}{8V_{cc}I_{CO}} \times 100$$

$$\%\eta = 25\%$$

2. Explain transformer – coupled class ‘A’ power amplifiers and derive its efficiency.

(16) [May-2005]

Class ‘A’ Power amplifier:

The power amplifier is said to be class ‘A’ amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

Transformer – Coupled class ‘A’ power amplifiers:

- In transformer coupled type, the load is coupled to the collector circuit.
- The loudspeaker connected to the secondary acts as a load having impedance of $R_L$ ohms.
- The transformer used is a step down transformer with the turns ratio as $n = N_2/N_1$.

Circuit Diagram:
**DC operation:**

- Assumed that the winding resistances are zero ohms. Hence for d.c purposes, the resistance is zero ohms.
- There is no d. c voltage drop across the primary winding of the transformer.
- The slope of the d.c load line is reciprocal of the d.c resistance in the collector circuit, which is zero in this case.
- Hence slope of the d.c load line is ideally infinite. This tells that the d.c load line in the ideal condition is a vertically straight line.
- Applying Kirchoff’s voltage law to the collector circuit we get,
  \[ V_{CC} - V_{CE} = 0 \]
  i.e., \[ V_{CC} = V_{CE} \] .........drop across winding is zero.
- This is the d.c bias voltage \( V_{CEQ} \) for the transistor.

So, \[ V_{CEQ} = V_{CC} \]

- Hence the d.c load line is a vertical straight line passing through a voltage point on the X-axis which is \( V_{CEQ} = V_{CC} \).
- The intersection of d.c load line and the base current set by the circuit is the quiescent operating point of the circuit. The corresponding collector current is \( I_{CQ} \).

**A.C Operation:**

- For the a.c analysis, it is necessary to draw an a.c load line on the output characteristics.
- For a.c purposes, the load on the secondary is the load impedance \( R_L \) ohms. And the reflected load on the primary i.e. \( R'_L \) can be calculated.
- The load line drawn with a slope of \((-1/R_L)\) and passing through the operating point i.e. quiescent point Q is called **a.c load line**.
- The output current i.e. collector current varies around its quiescent value \( I_{CQ} \), when a.c input signal is applied to the amplifier.
- The corresponding output voltage also varies sinusoidally around its quiescent value \( V_{CEQ} \) which is \( V_{CC} \) in this case.
Load line for class A amplifier:

A.C Output Power:

- The a.c power developed is on the primary side of the transformer.
- While calculating this power, the primary values of voltage and current and reflected load \( R'_L \) must be considered.
- The a.c power delivered to the load is on the secondary side of the transformer.
- While calculating load voltage, load current, load power the secondary voltage, current and the load \( R_L \) must be considered.
- Let \( V_{1m} \) = Magnitude or Peak value of primary voltage.
  - \( V_{1\text{rms}} \) = R.M.S value of primary voltage.
  - \( I_{1m} \) = Peak value of primary current.
  - \( I_{1\text{rms}} \) = R.M.S value of primary current.

- Hence the a.c power developed on the primary is given by,
  \[
  P_{ac} = V_{1\text{rms}} I_{1\text{rms}} \\
  P_{ac} = I_{1\text{rms}}^2 R_L \\
  P_{ac} = \frac{V_{1\text{rms}}^2}{R_L} \\
  P_{ac} = \frac{V_{1m} I_{1m}}{\sqrt{2}} = \frac{V_{1m} I_{1m}}{2} \\
  P_{ac} = \frac{I_{1m}^2 R_L}{2} \\
  P_{ac} = \frac{V_{1m}^2}{2 R_L}
  \]
Similarly the a.c power delivered to the load on secondary also can be calculated, using secondary quantities.

Let  

- \( V_{2m} \) = Magnitude or Peak value of secondary or load voltage.
- \( V_{2\text{rms}} \) = R.M.S value of secondary or load voltage.
- \( I_{2m} \) = Peak value of secondary or load current.
- \( I_{2\text{rms}} \) = R.M.S value of secondary or load current.

\[
P_{ac} = V_{2\text{rms}} I_{2\text{rms}} = \frac{V_{2m}^2}{V_{2\text{rms}}} R_L = \frac{V_{2\text{rms}}^2}{R_L}
\]

\[
P_{ac} = \frac{V_{2m} I_{2m}}{2} = \frac{I_{2m}^2}{2} = \frac{V_{2m}^2}{2R_L}
\]

Power delivered on primary is same as power delivered to the load on secondary, assuming ideal transformer.

Primary and secondary values of voltages and currents are related to each other through the turns ratio of the transformer.

The slope of the a.c load line can be expressed in terms of the primary current and the primary voltage. The slope of the a.c load line is,  

\[
\frac{1}{R'} = \frac{I_{1m}}{V_{1m}}
\]

The generalized expression for a.c power output is given by,

\[
P_{ac} = \frac{V_{m} I_{m}}{2} = \frac{\left( V_{pp} \right) \left( I_{pp} \right)}{2} = \frac{V_{pp} I_{pp}}{8} \quad (W)
\]

\[
(or) \quad P_{ac} = \frac{I_{pp}^2 R_{L}}{8} \quad : \quad (or) \quad P_{ac} = \frac{V_{pp}^2}{8R_L}
\]

But as \( V_{pp} = V_{\max} - V_{\min} \) and \( I_{pp} = I_{\max} - I_{\min} \) : Substitute this in equation \( W \), then we get,

\[
P_{ac} = \frac{\left( V_{\max} - V_{\min} \right) \left( I_{\max} - I_{\min} \right)}{8} \quad .... (2)
\]
Efficiency:-

The efficiency of an amplifier represents the amount of a.c power delivered (or) transferred to the load, from the d.c source i.e. accepting the d.c power input. The efficiency of an amplifier is,

\[ \% \eta = \frac{P_{ac}}{P_{dc}} \times 100 \]

Now for class ‘A’ operation, we have derived the expressions for \( P_{ac} \) and \( P_{dc} \), hence equations (1) and (2), we can write

\[ \% \eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8V_{CC}I_{CQ}} \times 100 \]

Maximum Efficiency:

- For maximum efficiency calculation, assume maximum swings of both the output voltage and the output current.

- From the graph we can see that the minimum voltage possible is zero and maximum voltage possible is \( 2V_{CC} \), for a maximum swing.

- Similarly the minimum current is zero and the maximum current possible is \( 2I_{CQ} \), for a maximum swing.

\[
\begin{align*}
V_{max} & = 2V_{CC} and V_{min} = 0 \\
I_{max} & = 2I_{CQ} and I_{min} = 0
\end{align*}
\]

for maximum swing
3. Explain class ‘B’ power amplifiers and derive its efficiency.

Class ‘B’ amplifier: The Power amplifier is said to be class ‘B’ amplifier if the Q-point and the input signal are selected, such that the output signal is obtained only for one half cycle for a full input cycle. Class ‘B’ amplifiers is further classified as Push-Pull and Complementary symmetry amplifiers.

Push-Pull Class ‘B’ amplifier:-
- When both the transistors are of same type i.e. either n-p-n (or) p-n-p then the circuit is called Push-Pull Class B A.F power amplifier circuit.
- The push-pull circuit requires two transformers, one as input transformer called driver transformer and the other to connect the load called output transformer.
- The input signal is applied to the primary of the driver transformer. Both the transformers are centre tapped transformers.
- In the circuit, both Q₁ and Q₂ transistors are of n-p-n type. Both the transistors are in common emitter configuration.
- The driver transformer drives the circuit. The input signal is applied to the primary of the driver transformer.
- The centre tap on the secondary of the driver transformer is grounded. The centre tap on the primary of the output transformer is connected to the supply voltage +V_{CC}

Circuit Diagram:
PUSH-PULL CLASS ‘B’ AMPLIFIER:

- With respect to the centre tap, for a positive half cycle of input signal, the point ‘A’ shown on the secondary of the driver transformer will be positive.
- While the point ‘B’ will be negative. Thus the voltages in the two halves of the secondary of the driver transformer will be equal but with opposite polarity.
- Hence the input signals applied to the base of the transistors $Q_1$ and $Q_2$ will be $180^\circ$ out of phase.
- The transistor $Q_1$ conducts for the positive half cycle of the input producing positive half cycle across the load.
- While the transistor $Q_2$ conducts for the negative half cycle of the input producing negative half cycle across the load.
- Thus across the load, we get a full cycle for a full input cycle.
- When point ‘A’ is positive, the transistor $Q_1$ gets driven into an active region while the transistor $Q_2$ is in cut off region.
- While when point ‘A’ is negative, the point ‘B’ is positive, hence the transistor $Q_2$ gets driven into an active region while the transistor $Q_1$ is in cut off region.

D.C Operation: -

- The d.c biasing point i.e. Q point is adjusted on the X-axis such that $V_{CEQ} = V_{CC}$ and $I_{CEQ}$ is zero.
- Hence the co-ordinates of the Q point are $(V_{CC},0)$. There is no d.c base bias voltage.

D.C. Power input: -

- Each transistor output is in the form of half rectified waveform. Hence if $I_m$ is the peak value of the output current of each transistor, the d.c or average value is $I_m/\pi$, due to half rectified waveform.
- The two currents, drawn by the two transistors, forms the d.c supply are in the same direction.
- Hence the total d.c or average current drawn from the supply is the algebraic sum of the individual average current drawn by each transistor.

\[
\therefore I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi}
\]

- The total d.c power input is given by,
\[
P_{DC} = V_{CC} \times I_{dc}
\]
\[
\therefore P_{DC} = \frac{2}{\pi} V_{CC} I_{m}
\]

A.C Operation:-

- When the a.c signal is applied to the driver transformer, for positive half cycle \(Q_1\) conducts. The path of the current drawn by the \(Q_1\) is shown in fig (a).
- For the negative half cycle \(Q_2\) conducts. The path of the current drawn by the \(Q_2\) is shown in fig (b).
- It can be seen that when \(Q_1\) conducts, lower half of the primary of the output transformer does not carry any current. Hence only \(N_1\) numbers of turns carry the current.
- While when \(Q_2\) conducts, upper half of the primary does not carry any current. Hence again only \(N_1\) number of turns carry the current. Hence the reflected load on the primary can be written as

\[
\therefore R'_L = \frac{R_L}{n_2} \quad \text{(1)}
\]

Where \(n = \frac{N_2}{N_1}\)

\[\text{Diagram of (a) } Q_1 \text{ conduction} \quad \text{Diagram of (b) } Q_2 \text{ conduction}\]

- The step down turns ratio is \(2N_1:N_2\) but while calculating the reflected load, the ratio ‘n’ becomes \(N_2/N_1\). Each transistor shares equal load which is the reflected load \(R'_L\) given by equation (1).
The slope of the a.c load line is \((-1/R'_L)\) while the d.c load line is the vertical line passing through the operating point ‘Q’ on the axis.

**Load Line for push-pull class B amplifier:**

![Load Line Diagram]

- The slope of the a.c load line (magnitude of slope) can be represented in terms of \(V_m\) and \(I_m\) as,

\[
\frac{1}{R'_L} = \frac{I_m}{V_m}
\]

\[
\therefore R'_L = \frac{I_m}{V_m}
\]

Where \(I_m\) = Peak value of the collector current.

**A.C Power Output:**

As \(I_m\) and \(V_m\) are the peak values of the output current and the output voltage respectively, then

\[
V_{rms} = \frac{V_m}{\sqrt{2}} \quad \text{and} \quad I_{rms} = \frac{I_m}{\sqrt{2}}
\]

Hence the a.c power output is expressed as,

While using peak values it can be expressed as,

\[
P_{ac} = \frac{V_m I_m}{2} = \frac{V_m R'_L}{2} = \frac{V_m}{2R'_L}
\]

**Efficiency:**

The efficiency of the class ‘B’ amplifier can be calculated using the basic equation.
Maximum Efficiency:

From the equation (2), it is clear that as the peak value of the collector voltage $V_m$ increases, the efficiency increases. The maximum value of $V_m$ possible is equal to $V_{CC}$.

$$%\eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{2}{2\pi} \times 100$$

$$%\eta = \frac{\pi}{4} \times \frac{V_m}{V_{CC}} \times 100$$

$$%\eta = 78.5\%$$

4. Draw the circuit of a complementary symmetry amplifier and explain its operation. (8) [Dec-2002][May-2005] [JUNE-2006]

Class ‘B’ amplifier:-

The Power amplifier is said to be class ‘B’ amplifier if the Q-point and the input signal are selected, such that the output signal is obtained only for one half cycle for a full input cycle. Class ‘B’ amplifiers is further classified as Push-Pull and Complementary symmetry amplifiers.

Complementary Symmetry Class ‘B’ amplifier:-

When the two transistors form a complementary pair i.e. one n-p-n and other p-n-p then the circuit is called Complementary symmetry Class ‘B’ A.F power amplifier circuit.
The circuit is driven from a dual supply of $\pm V_{CC}$. The transistor $Q_1$ is n-p-n while $Q_2$ is of p-n-p type.

In the positive half cycle of the input signal, the transistor $Q_1$ gets driven into active region and starts conducting.

The same signal gets applied to the base of the $Q_2$ but as it is of complementary type, remains in off condition, during positive half cycle. This result into positive half cycle across the load $R_L$.

**Circuit Diagram of +ve half Cycle:**

- During negative half cycle of the signal, the transistor $Q_2$ being p-n-p gets biased into conduction.
- While the transistor $Q_1$ gets driven into cut off region. Hence only $Q_2$ conducts during negative half cycle of the input, producing negative half cycle across the load $R_L$.
- Thus for a complete cycle of input, a complete cycle of output signal is developed across the load.

**Circuit Diagram of -ve half Cycle:**
Advantages:-
1. As the circuit is transformer less, its weight, size and cost are less.
2. Due to common collector configuration, impedance matching is possible.
3. The frequency response improves due to transformer less class ‘B’ amplifier circuit.

Disadvantages:-
1. The circuit needs separate two separate voltage supplies.
2. The output is distorted to cross-over distortion.

5. For class ‘B’ complementary A.F power amplifier shown below, calculate efficiency and maximum power dissipation per transistor.

Power Dissipation:-
The power dissipation by both the transistors is the difference between a.c power output and d.c power input.

\[ p_d = P_{DC} - P_{ac} = \frac{2}{\pi} V_{CC} I_m - \frac{V_m I_m}{2} \]

\[ p_d = \frac{2}{\pi} V_{CC} \frac{V_m}{R'_L} - \frac{V_m}{2R'_L} \]

\[ p_d = 2 \frac{V_{CC} V_m}{\pi R'_L} - \frac{2V_m}{2R'_L} \]

Let us find out the condition for maximum power dissipation. In case of class ‘A’ amplifier, it is maximum when no signal signal is there. But in class ‘B’ operation, when the input signal is zero, \( V_m = 0 \) hence the power dissipation is zero and not the maximum.

Maximum power dissipation:-
The condition for maximum power dissipation can be obtained by differentiating the equation (N) with respect to \( V_m \) and equating it to zero.

\[ \frac{\partial P_d}{\partial V_m} = \frac{2}{\pi} \frac{V_{CC} V_m}{R'_L} - \frac{2V_m}{2R'_L} = 0 \]

\[ \frac{2}{\pi} \frac{V_{CC}}{R'_L} = \frac{V_m}{R'_L} \]

\[ V_m = \frac{2}{\pi} V_{CC} \]
\[ V_m = \frac{2}{\pi} V_{cc} \] For maximum power dissipation.

This is the condition for maximum power dissipation. Hence the maximum power dissipation is,

\[
(P_d)_{(\text{max})} = \frac{2}{\pi} V_{cc} \times \frac{2}{\pi} \frac{V_{cc}}{R'_L} - \frac{4}{\pi^2} \frac{V^2_{cc}}{2R'_L}
\]

\[
(P_d)_{(\text{max})} = \frac{4}{\pi^2} \frac{V^2_{cc}}{R'_L} - \frac{2}{\pi^2} \frac{V^2_{cc}}{R'_L}
\]

\[
(P_d)_{(\text{max})} = \frac{2}{\pi^2} \frac{V^2_{cc}}{R'_L}
\]

\[
(P_d)_{(\text{max})} = \frac{2}{\pi^2} \frac{V^2_{cc}}{R'_L}
\]

\[
(P_d)_{(\text{max})} = \frac{2}{\pi^2} \frac{V^2_{cc}}{R'_L}
\]

Now \( P_{ac} = \frac{V^2_{m}}{2R'_L} \)

And \( V_m = V_{cc} \) is the maximum condition.

\[
Hence...(P_{ac})_{\text{max}} = \frac{V^2_{cc}}{2R'_L}
\]

\[
Now...(P_d)_{\text{max}} = \frac{2V^2_{cc}}{\pi^2 R'_L} = \frac{4}{\pi^2} \left( \frac{V^2_{cc}}{2R'_L} \right)
\]

\[
\therefore (P_d)_{\text{max}} = \frac{4}{\pi^2} (P_{ac})_{\text{max}}
\]

This much power is dissipated by both the transistors hence the maximum power dissipation per transistor is \((P_d)_{\text{max}}/2\).

\[
\therefore (P_d)_{\text{max}} \text{ per transistor} = \frac{4}{\pi^2} (P_{ac})_{\text{max}}
\]

\[
\therefore (P_d)_{\text{max}} \text{ per transistor} = \frac{2}{\pi^2} (P_{ac})_{\text{max}}
\]

\[
(P_d)_{\text{max}} \text{ per transistor} = \frac{2}{\pi^2} (P_{ac})_{\text{max}}
\]
6. What is meant by cross over distortion and how it is eliminated? [May-2004]

Cross over distortion:-

- In class – B mode, both transistors are biased at cut-off region because the DC bias voltage is zero.
- So input signal should exceed the barrier voltage to make the transistor conduct. Otherwise the transistor doesn’t conduct.
- So there is a time interval between positive and negative alternations of the input signal when neither transistor is conducting. The resulting distortion in the output signal is crossover distortion.

Cross over Distortion:

- To eliminate the cross-over distortion some modifications are necessary.
- The basic reason for the cross over distortion is the cut in voltage of the transistor junction.
- To overcome this cut-in voltage, a small forward biased is applied to the transistors.

Class B with Voltage Divider Bias:
In complementary symmetry circuit, base emitter junctions of both Q₁ and Q₂, are required to provide a fixed bias.

Hence for silicon transistors a fixed bias of 0.7 + 0.7 = 1.4 V is required. This can be achieved by using a potential divider arrangement.

But in this circuit, the fixed bias provided is fixed to say 1.4 V. While the junction cut-in voltage changes with respect to the temperature. Hence there is still possibility of a distortion when there is temperature change.

Class B with two diodes:

Hence instead of R₂, the two diodes can be used to provide the required fixed bias.

As the temperature changes, along with the junction characteristics get changed and maintain the necessary biasing required to overcome the cross-over distortion when there is temperature change.

The arrangement of the circuit with the two diodes is shown in above figure.
7. Explain class ‘C’ power amplifiers and derive its efficiency.

In a class C amplifier, a resonating circuit is used as a load. Thus most of the class C amplifiers are the tuned amplifier.

Class-C amplifiers are biased deep into the cut-off. Figure is a class-C amplifier with a negative supply voltage $V_{BB}$ applied to the base circuit. This negative voltage reverse-biases the base emitter junction of the transistor, so that it will not conduct until the input signal overcomes this reverse bias. This happens for only a small part of positive half of the input waveform (0° or less).

A class C amplifier, as that shown in Fig, is biased to operate for less than 180° of the input signal cycle. The tuned circuit in the output, however, will provide a full cycle of output signal for the fundamental or resonant frequency of the tuned circuit (L and C tank circuit) of the output. This type of operation is therefore limited to use at one fixed frequency, as occurs in a communications circuit, for example. Operation of a class C circuit is not intended primarily for large-signal or power amplifiers.

Circuit Diagram:

Wave form:
The amplified and inverted collector voltage is connected to load resistance \( RL \). As class C amplifier is used with parallel tuned circuit; the output voltage is maximum at the resonant frequency. The resonant frequency is given by

\[
f = \frac{1}{2\pi\sqrt{LC}}
\]

Thus the gain drop on either side of the resonant frequency. Thus the frequency response of the class C amplifier as shown in fig. As gain is maximum at resonant frequency, these amplifiers are used to amplify only narrow band of frequencies.

**Load Lines:**

The fig shows the dc equivalent circuit of the unbiased class C amplifier. The resistance \( R_S \) is the series resistance of an inductor \( L \). The value of \( R_S \) is very small. For DC, the capacitor \( C \) acts an open circuit and does not affect the DC operation. As \( R_S \) is very small, the slope of DC load line is reciprocal of \( R_S \) and is very high tending to infinity. Hence DC load line is almost vertical. The DC load line is not important for class C amplifier.

For AC load line, Q point is designed to be at the lower end of the AC load line. When AC input signal is applied, instantaneously ac operating point moves up theca load line towards the saturation point. The maximum value of the collector current i.e. when \( V_{CE}=0 \) is given by \( (V_{CC}/R_C) \). Both dc and ac load line are shown in figure.

**AC equivalent Circuit:**

The AC equivalent Circuit of class C amplifier as shown in fig.
The inductor has a series resistance $R_S$. The quality factor $Q$ of the inductor is

$$Q = \frac{X_L}{R_S} = \frac{\omega L}{R_S}$$

Where

- $Q_L =$ Quality factor
- $X_L =$ Inductive reactance of coil
- $R_S =$ series coil resistance

The series resonance $R_S$ can be replaced by a parallel resistance $R_P$. This is given by

$$R_p = Q_L \omega L = \omega X_L$$

At resonance, $X_L$ cancels $X_C$ and hence only $R_P$ remains in parallel with $R_L$. Thus the ac resistance seen by the collector at resonance is,

$$r_c = R_p 1 \| R_L$$

The Q factor of the overall circuit is,

$$Q = \frac{r_c}{\omega L} = \frac{r_c}{X_L}$$

**DC clamping of input signal:**

The ac input drives base-emitter junction i.e. the emitter diode. While the amplified current pulse drives the resonant circuit. The input capacitor with emitter diode forms a clamer circuit and hence signal available across the emitter diode is negatively clamped.

The input is almost clamped by $-V_P$. Only positive peaks of current can turn on the emitter diode. Hence the current flows in brief pulse. This shown in fig.

**Filtering the harmonics:**
The current pulse consists of harmonic i.e. the components which are multiply of the fundamental input frequency \( f \). Thus the pulses are equivalent to a group of sine waves having frequencies \( f, 2f, 3f \ldots nf \). These components are called harmonics.

Collector Voltage waveform

At fundamentals frequency, the impedance of the tank circuit is high which produces a large voltage gain. For all other harmonics, due to low impedance of tank circuit, the voltage gain is very less. Hence all the harmonics are filtered and pulse sine wave of fundamental frequency is available across the tank circuit as shown in fig.

**Band width:**

We know that, band width resonant circuit is defined as \( BW = f_2 - f_1 \)

Where, \( f_1 = \text{Lower half power} \)
\( f_2 = \text{Upper half power} \)

The half power frequencies are identical to the frequencies at which the voltage equal 0.707 times maximum gain. The band width of class C amplifier is given by,

\[
BW = \frac{f_c}{Q}
\]

Where, \( Q \) is the quality factor.

**Duty Cycle:** The duty cycle is the ratio of ON period of the transistor to total period of the pulses. The width of current pulse represents on period of transistor.

Thus,

\[
W = \text{Width of pulses} \\
T = \text{Periods of pulses}
\]

Then the duty cycle \( D \) is given by, \( D = \frac{W}{T}=\Phi/360^\circ \).
Output Power:

If the rms value of output voltage across load resistance is measured then the output power is given by,

\[ P_{\text{out}} = \frac{V_{\text{rms}}^2}{R_L} \]

But \[ V_{pp} = 2V_m = 2\sqrt{2}V_{\text{rms}} \]

\[ P_{\text{out}} = \frac{(V_{pp}/2\sqrt{2})^2}{R_L} = \frac{V_{pp}^2}{8R_L} \]

Transistor Dissipation:

The maximum of a class C tuned amplifier is shown in fig (1) While the collector current pulse are shown in fig (2). The peak of the pulses is \( I_{C\text{(sat)}} \) and conduction is \( \Phi \).

As the peak value of the current is \( I_{C\text{(sat)}} \), the transistor peak current rating must be greater than \( I_{C\text{(sat)}} \). The conduction angle \( \Phi \) is much less than 180°.

The power dissipation depends on the conduction angle \( \Phi \). less the conduction angle less the DC power input and less is the transistor dissipation. AS the conduction angle increases upto 180°, the transistor dissipation with \( \Phi=180° \). The variation of transistor dissipation with \( \Phi \) is shown in fig.

The maximum power dissipation at \( \Phi=180° \) is given by,

\[ P_D = \frac{V_{pp\text{(max)}}^2}{40r_c} \]

Where, \( V_{pp\text{(max)}}=2V_{CC} \)

Under normal working condition, as \( \Phi \) much less than 180°,

hence \( P_D \) almost much less than \( P_D\text{(max)} \)

DC Input power:

If the conduction angle is made 180° then the current wave form becomes half wave rectified wave form and, \( I_{dc} = \frac{I_{C\text{(sat)}}}{\pi} = 0318I_{\text{v(sat)}} \)

As \( \Phi \) is always less than 180°, \( I_{dc} \) is also less.

As biasing resistors are absent dc collector drain
in class C amplifier.

The dc input power is given by, \( P_{DC} = V_{CC} I_{DC} \)

**Efficiency:**

The efficiency is given by the ratio of a.c power output to the dc power input.

\[
\%\eta = \frac{P_{out}}{P_{DC}} \times 100 = \frac{P_{out}}{V_{CC} I_{DC}} \times 100
\]

The efficiency depends on the conduction angle \( \Phi \). The fig shows the graph efficiency against the conduction angle \( \Phi \).

In class C amplifier, most of the DC input power converted into a.c load power because the transistor and coil losses are small. When the conduction angle is 180°, the efficiency is 78.5%. The efficiency increases when conduction angle decreases. As indicated, class A amplifier has maximum efficiency of 100%, approached at very small conduction angles.

8. Discuss the class ‘D’ power amplifiers and derive its efficiency.

Class D amplifier or switching amplifier is an electronic amplifier where all power devices (usually MOSFETs) are operated as binary switches. They are either fully on or fully off. Ideally, zero time is spent transitioning between those two state.

The fig. shows the basic concept of class D amplifier. The amplifier consists of two complementary symmetry transistors driving a load \( R_L \). This means one transistor is p-n-p and other is n-p-n.

**Concept of Class D Amplifier:**

![Diagram of Class D Amplifier](image)
The transistors are biased in such a way that they behave as ideal switches. When transistor is ON, it is biased to saturation so that voltage across it is zero while current is high. When transistor is OFF, it is biased to cut-off so that current through it is zero while voltage is high. Thus when input goes positive $Q_1$ conducts heavily acting as closed switch while $Q_2$ is OFF. While when input goes negative, $Q_2$ conducts heavily acting as closed switch while $Q_1$ is OFF. Thus the load voltage $V_o$ across $R_L$ has one of two possible values which are $V_{\text{supply}}$ or 0 V. This is a type of digital output having two levels high and low.

The transistors dissipate almost zero power as in any of the states, either voltage is zero or current is zero for the transistors. Thus entire power input is available to the load. Hence efficiency of class D amplifiers is almost 100%. The figure of merit which is the ratio of the maximum power dissipated in transistor to that delivered to the load, is zero. These facts make the class D amplifier as an ideal amplifier.

Practically class D amplifiers are designed to operate with digital or pulse type of signals. The basic block diagram of unit used along with class D amplifier in the application circuits is shown in the Fig.

**Block Diagram of Class D amplifier:**

The op-amp comparator is used for which one input is sawtooth type while other is sinusoidal. The comparator converts sinusoidal signal to digital pulse type signal with the help of sawtooth waveform. This is called chopping of sinusoidal signal to produce digital signal. This signal drives the class D amplifier. When pulse signal is high the transistors are ON and when it is low, the transistors are OFF. Thus most of the power supplied is delivered to the load by producing high power output signal. The digital signal is converted back to the original sinusoidal signal using low pass filter. Using feedback network, it is fed back to the comparator. Practically instead of power BJL, power MOSFET devices are used as driver devices for class D amplifier.

The class D amplifiers are mainly used in the pulse and digital circuits.
Ideal Performance of class D amplifier:

The transistor Q₁ and Q₂ acts as switches hence when Q₁ is ON, Q₂ is OFF and when Q₂ is ON, Q₁ is OFF. Consider Q₁ is ON and Q₂ OFF. Thus voltage across Q₁ is zero and equivalent circuit is shown in fig. If input is square wave then voltage Vₐ is square wave at the input to the series tuned circuit as shown in the fig.

The square wave signal Vₐ can be expressed in a Fourier series and amplitude of the fundamental component is given by,

\[ V_{1m} = \frac{4}{\pi} V_{cc} \]

Hence the fundamental component can be expressed as,

\[ v_1 = V_{1m} \sin \omega t = \frac{4}{\pi} V_{cc} \sin \omega t \]

The fundamental component of current by

\[ i_1 = \frac{v_1}{R_L} = \frac{1}{R_L} \frac{4}{\pi} V_{cc} \sin \omega t \]

Thus average DC drain current ID is given by,

\[ I_D = \frac{1}{R_L} \left[ \frac{1}{T} \int_0^{T/2} \frac{4}{\pi} V_{cc} \sin \omega t \, (d\omega t) \right] \]

\[ I_D = \frac{4V_{cc}}{\pi R_L} \left[ \frac{1}{T} \left( -\cos \frac{\omega T}{\omega} \right) \right] \]

\[ I_D = \frac{4V_{cc}}{\pi R_L} \left[ -\frac{1}{T \omega} \left( \cos \frac{\omega T}{2} - 1 \right) \right] \]

\[ \omega T = 2\pi \text{ hence } \cos \frac{\omega T}{2} = \cos \pi = -1 \]
\[
I_D = \frac{4V_{cc}}{\pi R_L} \times \frac{1}{2\pi} \times 2 = \frac{4V_{cc}}{\pi^2 R_L}
\]

\[
P_{dc} = V_{cc} \times 2I_D = \frac{8V_{cc}^2}{\pi R_L}
\]

And

\[
P_{ac} = I_{rms}^2 \times R_L = \left( \frac{I_m}{\sqrt{2}} \right)^2 R_L
\]

Where

\[
I_m = \frac{4V_{cc}}{\pi R_L}
\]

\[
P_{ac} = \left( \frac{4V_{cc}}{\pi R_L} \right)^2 \times \frac{R_L}{2} = \frac{1}{2} \times \frac{16V_{cc}^2}{\pi^2 R_L^2}
\]

\[
P_{dc} = P_{ac} = \frac{8V_{cc}^2}{\pi^2 R_L}
\]

The PDC is input while Pac is output power.

\[
\%\text{Eff} = \frac{P_{ac}}{P_{dc}} \times 100 = 100\%
\]

**Non Ideal Performance of class D amplifier:**

Practically BJT when ON has a drop of \( V_{CE} \) (sat) across it while practically FET has a resistance \( R_{on} \) when it is ON. Hence any replaced by ideal short circuit.

The figure shows an equivalent circuit with FET represented by \( R_{on} \) when saturated. If the \( V_{in} \) is square wave, the input to the tuned circuit \( V_a \) is also square wave, but with reduced amplitude. The output voltage assuming a narrow band filter is given by

\[
V_0 = \frac{4}{\pi} V_{cc} \frac{R_I}{R_L + R_{on}} \sin \omega t
\]

The amplitude of the output current is given by
The DC current in each transistor is,

\[ I_D = \frac{4V_{cc}}{\pi} \left[ \frac{1}{R_L + R_{ON}} \right] \]

PDC input power = \( 2V_{CC}ID \)

\[ P_{DC} = \frac{8}{\pi^2} \frac{V_{cc}^2}{R_L + R_{ON}} \]

Pac output power = \( I_{rms}^2 R_L \)

\[ P_{ac} = \frac{8}{\pi^2} \frac{V_{cc}^2}{R_L + R_{ON}} R_L \]

Thus the efficiency of nonideal class D FET amplifier is

\[ \% \eta = \frac{P_{ac}}{P_{DC}} \times 100 \]

\[ \% \eta = \frac{R_L}{R_L + R_{ON}} \times 100 \]

9. Explain the Class S power amplifier:

**Principles of Operation:**

1. The input is pulse width modulated signal.
2. The pulses are amplified by high efficiency pulse amplifier like class D amplifier.
3. The demodulated using low pass filter of the amplifiers signal.

**Block Diagram:**

```
S(t)  ---\( h(t) \)  ---->  Pulse width Modulator
       |                    |                     |
       |                    Vcc    x(t)  ----> Low pass filter  Output
       | Pulse amplifier
```

```
The input signal pulse width modulated which generates constant amplitude pulse. These are amplified by pulse amplifier which is highly efficient switching amplifier like class D amplifier. The modulating frequency, as much higher than the signal frequency is completely removed using the low pass filter at the last stage.

The basic difference between class D and class S amplifiers is that the output stage of the class D uses tuned circuit which is tuned to the fundamental frequency of the input while the output stage of the class S uses the low pass filter which recovers the input signal. If the saturation resistance of the transistor is neglected, the efficiency of the class s amplifier also approaches to 100%.

10. Explain the MOSFET power amplifiers.

Power amplifier designed to switch large currents ON and OFF use MOSFET devices. MOSFET based class-D amplifier is commonly employed. Other applications include line drivers for digital switching circuits, switched mode voltage regulators. The advantage of using MOSFET device for switching is the turn off time is not delayed by minority-carrier storage, as it is in a BJT. Further current in a MOSFET is due to majority carriers only and they are not subjected to thermal runaway. In addition, very large input impedance of MOSFET, makes the designed of drivers circuits less complex.

Complementary Symmetry MOSFET amplifier with Single Power Supply:

During the positive half cycle, current flows through Q1, C1 and R1 causing the left side of C1 to charge positive. During the negative half cycle, Q2 is turned on and C1 discharge through Q2 and load.

Circuit Diagram:

This causes current to flow through the load in the opposite direction. This process is repeatedly. In this type of the circuit the capacitor must be large enough to supply energy to the load during the negative half cycle. These capacitors range is thousands of microfarad.
**MOSFET based class D power amplifier:**

In class D amplifier, transistor is used as switch instead of current sources. When transistor is operated as switch, the power dissipation is ideally zero and hence the efficiency of class D amplifiers approaches 100%.

The figure shows the class D amplifier using MOSFETs. Here MOSFETs are switched ON and OFF, so that they are held in a linear range for essentially zero time during each cycle of the input sine wave. The output voltage for this circuit switches between 0 and $+V_{cc}$. This square wave output is applied to high Q series resonance circuit which will transmit the fundamental frequency along while blocking the harmonics.

**Totem Pole MOSFET switching device:**

A switching circuit called totem pole with MOSFET as switching device is shown in figure. The Totem pole inverts the input that is output is high when the input is low and vice versa. The MOSFET $Q_2$ and $Q_3$ form the Totem Pole output. When the input is high $Q_1$ and $Q_3$ are ON, acting as closed switches and $Q_2$ is OFF acting as open switch. Hence the output is low. When the input is low $Q_1$ and $Q_3$ are OFF, $V_{DD}$ is available at the gate of $Q_2$ is ON. Hence the output is high.
Advantages:

MOSFET are operated in switching mode (either ON or OFF) the power dissipation in MOSFETs is ideally zero and hence the efficiency of the circuit approaches to 100%.

Disadvantages:

1. Needs filters with sharp cut-off frequencies, and design of such filters is complex
2. They produce noise in the form of electromagnetic interference due to high speed switching of large currents.

11. Give the design procedure for heat sinks. (6) [May-2004]

Heat sink:-

The heat sink is used to observe the heat produced in the transistor junctions while its operation. Usually power amplifiers are provided with heat sinks.

The heat dissipation problem is very much analogous to a simple electric circuit and the Ohm’s law. An electric current flow when there exits a potential difference while the heat flows when there exists a temperature difference $(T_2 - T_1)$. Then similar to an electric resistance a thermal resistance can be obtained as,

$$\theta = \frac{T_2 - T_1}{P_d} \text{oC/W(}or\text{)C/mW} \quad \text{...............(1)}$$

Where $P_d$ is the heat dissipated or heat flow, due to the power dissipation.

From the above relation we can write,

$$T_2 - T = \theta P_d \text{ oC}$$

and .... $P_d = \frac{T_2 - T}{\theta} W(\text{or}) mW$

Now to develop the thermal-electric analogy let us define some parameters as,

$T_1 = \text{Junction Temperature}$
\( T_C = \) Case Temperature

\( T_A = \) Ambient Temperature

\( \theta_{JA} = \) Total thermal resistance (junction to ambient)

\( \theta_{JC} = \) Transistor thermal resistance (junction to Case)

\( \theta_{CS} = \) Insulator thermal resistance (Case to heat sink)

\( \theta_{SA} = \) Heat sink thermal resistance (heat sink to ambient)

**Heat flow from power transistor:**

From this heat flow diagram, an electrical analogous circuit can be obtained as,

\[
\begin{align*}
T_J & \quad \text{Junction Temperature} \\
T_C & \quad \text{Case Temperature} \\
T_S & \quad \text{Sink Temperature} \\
T_A & \quad \text{Ambient Temperature}
\end{align*}
\]

Thus from the property of series circuit, the total thermal resistance can be obtained as,

\[
\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \cdot C / W
\]
But
\[ \theta_{JA} = \frac{T_J - T_A}{P_d} \] ……………from definition of \( \theta \) in equation (1).

\[ T_J = P_d \theta_{JA} + T_A \]

Thus the total power handling capacity \( P_d \) of the device can be obtained as,

\[ P_d = \frac{T_J - T_A}{\theta_{JA}} = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} \]

Similarly the temperatures of case and sink can be obtained from,

\[ \theta_{CS} = \frac{T_C - T_S}{P_d} \]
\[ \theta_{SA} = \frac{T_S - T_A}{P_d} \]

\( \text{(or) } \theta_{CS} + \theta_{SA} = \frac{T_C - T_A}{P_d} \)

**Heat Sink Design:**

Manufacturers usually specify the total thermal resistance from the case to air i.e. \( \theta_{CA} \) for heat sinks. From the electrical analogous circuit we can write,

\[ \theta_{CA} = \theta_{CS} + \theta_{SA} = \theta_{JA} - \theta_{JC} \]

\( \text{Where} \ldots \theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \)

For the given circuit, \( V_{CE} \) and \( I_C \) values are known hence power dissipation \( P_d \) can be obtained as,

\[ P_d = V_{CE} I_C \]

\[ \text{But} \ldots \theta_{JA} = \frac{T_J - T_A}{P_d} \]
12 Calculate the input power, output power and the efficiency of class A amplifier shown in the Fig. The input voltage causes a base current 5 mA r.m.s.

![Diagram](image)

Fig. 14.51

**Solution**: Using equation (2) from section 14.7.1, we can determine \( I_{BQ} \):

\[
I_{BQ} = \frac{V_C}{R_B} = \frac{18 - 0.7}{1.2 \times 10^3} = 14.4167\ \text{mA}
\]

Now \( I_{CO} = \beta I_{BQ} = 40 \times 14.4167 = 576.67\ \text{mA} \)

And \( V_{CEQ} = V_C - I_{CO} R_L = 18 - 576.67 \times 10^{-7} \times 16 = 8.7733\ \text{V} \)

So \( P_{dc} = V_C I_{CO} = 18 \times 576.67 = 10.38\ \text{W} \)

This is the input power.

Now input a.c. voltage causes a base current of 5 mA r.m.s.

\[
\therefore (I_b)_{rms} = 5\ \text{mA}
\]

\[
\therefore (I_c)_{rms} = \beta (I_b)_{rms} = 40 \times 5 = 200\ \text{mA}
\]

This is nothing but the output collector current, r.m.s. value \( I_{rms} \).

\[
\therefore I_{rms} = 200\ \text{mA}
\]

Using equation (13) from section 14.8, we can write,

\[
P_{ac} = (I_{rms})^2 R_L = (200 \times 10^{-3})^2 \times 16 = 640\ \text{mW}
\]

This is the power delivered to the load.

Hence the efficiency of the amplifier is,

\[
\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{640 \times 10^{-3}}{10.38} \times 100 = 6.165\ %
\]
13. The operating junction temperature of a transistor is 125 °C. The total dissipation at a 25 °C case temperature is 0.5 W and at a 25 °C of ambient temperature, the total dissipation is 0.2 W. What is the value of thermal resistance $\theta_{CA}$?

Solution: $T_1 = 125 \, ^\circ\text{C}$

- When $T_C = 25 \, ^\circ\text{C}, P_d = 0.5 \, \text{W}$
- and $T_A = 25 \, ^\circ\text{C}, P_d = 0.2 \, \text{W}$

From the equation (7.99) we can write,

$$T_2 - T_1 = \theta_{21} P_d$$

$$\therefore \quad T_2 = T_1 + \theta_{21} P_d$$

$$\therefore \quad T_J = T_C + \theta_{JC} P_d$$

$$\therefore \quad 125 = 25 + \theta_{JC} \times 0.5$$

$$\therefore \quad \theta_{JC} = \frac{125 - 2.5}{0.5} = 200 \, ^\circ\text{C/W}$$

Similarly,

$$T_J = T_A + \theta_{JA} P_d$$

$$\therefore \quad 125 = 25 + \theta_{JA} \times 0.2$$

$$\therefore \quad \theta_{JC} = \frac{125 - 2.5}{0.5} = 500 \, ^\circ\text{C/W}$$

Now

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

We can add the two thermal resistance $\theta_{CS}$ and $\theta_{SA}$, to define the equivalent thermal resistance between case and ambient as $\theta_{CA}$.

$$\therefore \quad \theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

Hence $\theta_{JA} = \theta_{JC} + \theta_{CA}$

$$\therefore \quad 500 = 200 + \theta_{JA}$$

$$\therefore \quad \theta_{CA} = 500 - 200$$

$$\quad = 300 \, ^\circ\text{C/W} \text{ or } 0.3 \, ^\circ\text{C/mW}$$
UNIT IV

FREQUENCY RESPONSE OF AMPLIFIERS

1. Draw the high frequency hybrid π model for a transistor in the CE configuration and explain the significance of each component. (12)

Hybrid - π Common Emitter Transistor Model:

- Common emitter circuit is most important practical configuration and hence we have chosen this circuit for the analysis of transistor using hybrid - π model for a transistor in the CE configuration.
- For this model, all parameters (resistances and capacitances) in the model are assumed to be independent of frequency. But they may vary with the quiescent operating point.

Elements in the Hybrid - π model:

- $C_{b'e}$ and $C_{b'c}$:
  
  We know that, forward biased PN junction exhibits a capacitive effect called the diffusion capacitance. This capacitive effect of normally forward biased base-emitter junction of the transistor is represented by $C_{b'e}$ or $C_e$ connected between B' and E represents the excess minority carrier storage in the base.
The reverse bias PN junction exhibits a capacitive effect called the transition capacitance. This capacitive effect of normally reverse biased collector base junction of the transistor is represented by $C_c$ in the hybrid - $\pi$ model.

- $r_{bb'}$: The internal node $b'$ is physically not accessible bulk node B represents external base terminal. The bulk resistance between external base terminal and internal node $B'$ is represented as $r_{bb'}$, as shown in the fig. this resistance is called as base spreading resistance.

- **Virtual Base:**

- $r_{b'e}$: The resistance $r_{b'e}$ is that portion of the base emitter which may be thought of as being in series with the collector junction. This establishes a virtual base $B'$ for the junction capacitances to be connected to instead of $b$. this is illustrated in fig.

- $r_{b'c}$: We know that, due to early effect, the varying voltages across the collector to emitter junction results in base-width modulation. A change in the effective base width causes the emitter current to change. This feedback effect between output and input is taken into account by connecting $g_{b'c} or r_{b'c}$ between $n'$ and $c$.

- $g_m$: Due to the small changes in voltage $V_{b'e}$ across the emitter junction, there is excess-minority carrier concentration injected into the base which is proportional to the $V_{b'e}$. This effect accounts for the current generator $g_m V_{b'e}$ in fig.

  \[
g_m = \frac{\Delta I_c}{\Delta V_{b'e}} \quad \text{At constant } V_{CE}
\]

- $r_{ce}$: The $r_{ce}$ is the output resistance. It is also the result of the early effect.

2. Derive the expression for CE short circuit current gain and current gain with resistive load, at high frequencies. (16 Marks)

CE Short – circuit gain using hybrid $\pi$ model:
For the analysis of short circuit current gain we have to assume $R_L = 0$.

With $R_L = 0$, i.e. output short circuited $r_{ce}$ becomes zero, $r_{be}$, $C_e$ and $C_{b'e}$ appear in parallel.

When $C_C$ admittance is given as

$$j\omega C_M = \frac{iC_{b'C}}{V_{b'e}} j\alpha C_C (1 + g_m R_L)$$

Hence, the miller capacitance is $C_M = C_{b'C}(1 + g_m R_L)$

Here, $R_L = 0$

$\therefore$ $C_M = C_{b'C} (C_C)$

As $r_{b'e} >> r_{be}, r_{b'C}$ is neglected. With these approximations we get simplified hybrid $-\pi$ model for short circuit CE transistor as shown in above figure.

Parallel combination of $r_{b'e}$ and $(C_e + C_C)$ is given as
Further simplified hybrid-π model:

\[
Z = \frac{r_{b'e}}{1 + j\omega r_{b'e}(C_e + C_C)}
\]

**Fig. Further simplified hybrid - π model**

We can write

\[
V_{b'e} = I_b Z
\]

The current gain for the above circuit can be given as

\[
A_i = \frac{I_L}{I_b} = -g_m V_{b'e} \implies I_L = -g_m V_{b'e}
\]

Substituting value of \( V_{b'e} / I_b \):

\[
A_i = -g_m Z
\]

\[
A_i = \frac{-g_m r_{b'e}}{1 + j\omega r_{b'e}(C_e + C_C)}
\]

We know that \( h_{fe} = g_m r_{b'e} \)

**Current Gain**

\[
A_i = \frac{-h_{fe}}{1 + j\omega r_{b'e}(C_e + C_C)}
\]
In the output circuit $r_{ce}$ is in parallel with $R_L$. For high frequency amplifiers $R_L$ is small as compared to $r_{ce}$ and hence we can neglect $r_{ce}$. Using Miller’s theorem, we can split $r_{b'C}$ and $C_C$ to simplify the analysis.

Simplified Hybrid –$$\pi$$ circuit for a single transistor with a resistive load $R_L$

Further simplification of input circuit:

Amplifier gain $K$ is given as

$$K = \frac{V_o}{V_{b'e}}$$

Where $V_o = -g_m V_{b'e} R_L$

$$K = -g_m R_L$$

Assuming $R_L = 2K$ and $g_m = 50 \text{ mA/V}$

We get $K = -100$

And

$$\frac{r_{b'C}}{1-K} = \frac{4M}{1-(-100)} \approx 40K$$

$\therefore r_{b'C} = 4M\Omega$

The value $r_{b'C}/(1-K) >> r_{b'e}(1K)$ and hence $r_{b'C}/(1-K)$ which is in parallel with $r_{b'e}$ can be neglected.
C_c also resolved by Miller’s theorem.

\[
\frac{1}{j\omega C_c} = \frac{1}{j\omega C_c (1 + g_m R_L)}
\]

\[
\frac{C_c}{1 - K} = C = C_c (1 + g_m R_L) \ldots \ldots \ldots 1
\]

As C_e and C are in parallel, the total equivalent capacitance is given as

\[
C_{eq} = C_e + C_c (1 + g_m R_L) \ldots \ldots 2
\]

From equation (2) we can say that input capacitance Is increased. C_c (1+g_m R_L) is called Miller capacitance.

With these approximations input circuit becomes, as shown in figure (B).

**Further simplification for output circuit:**

- At output circuit value of C_c can be calculated as

\[
\frac{1}{j\omega C_c} \approx \frac{1}{j\omega C_c} \cdot K = -100
\]

\[
C_c \left( \frac{K}{K-1} \right) \approx C_c
\]

- At figure (B) we can see that there are two independent time constants, one associated with the input circuit and one associated with the output circuit.

- As input capacitance [C_e + C_c(1+g_m R_L)] is very high in comparison with output capacitance [C_c].

- As results, output time constant is negligible in comparison with the input time constant and may be ignored.

\[
r_{b'C} \left( \frac{K}{K-1} \right) \approx r_{b'C} \implies K = -100
\]

\[
\approx 4M\Omega
\]
This value of $r_{b'C}$ is very high in comparison with load resistance $R_L$ which is parallel with $r_{b'C}$. Hence $r_{b'C}$ can be ignored.

![Fig. Further simplified hybrid - π model for CE with $R_L$](image)

Parallel combination of $r_{b'C}$ and $C_{eq}$ is given as

$$Z = \frac{r_{b'e}}{r_{b'e} + 1/j\omega C_{eq}} = \frac{r_{b'e}}{1 + j\omega r_{b'e} C_{eq}}$$

This gives equivalent circuit as shown in below.

![Equivalent circuit](image)

From the above figure we can write, $V_{b'e} = I_b Z$  

$$Z = \frac{V_{b'e}}{I_b}$$

The current gain for the circuit can be given as,

$$A_i = \frac{I_L}{I_b} = -\frac{g_m V_{b'e}}{I_b}$$

Substituting value of ‘$Z$’ we get,
\[ A_i = \frac{-g_m V_{be}}{1 + j\omega r_{be} C_{eq}} = \frac{-h_{fe}}{1 + j2\pi f r_{be} C_{eq}} \implies h_{fe} = g_m r_{be} \]

3. What are the effects of coupling, bypass capacitors and internal capacitances on the bandwidth of the amplifier? (8) [Dec-2003]

**Effect of Coupling Capacitors:**
- The reactance of a capacitor is \( X_C = \frac{1}{j2\pi f C} \).
- At medium and high frequencies, the factor \( f \) makes \( X_C \) very small, so that all coupling capacitors behave as short circuits.
- At low frequencies, \( X_C \) increases. This increase in \( X_C \) drops the signal voltage across the capacitor and reduces the circuit gain.
- As signal frequencies decrease, the capacitor reactance increases and circuit gain continues to fall, reducing the output voltage.

**Effect of Bypass Capacitors:**
- At lower frequencies, the bypass capacitor \( C_E \) is not a short. So, the emitter is not at ac ground.
- \( X_C \) in parallel with \( R_E \) (\( R_S \) in case of FET) creates impedance. The signal voltage drops across this impedance reducing the circuit gain.
**Effect of internal Capacitances:-**

- At high frequencies, the coupling capacitors act as short circuit and do not affect the amplifier frequency response.
- However, at high frequencies, the internal capacitances, commonly known as junction capacitances do come into play, reducing the circuit gain.
- In case of the BJT, $C_{be}$ is the base emitter junction capacitance and $C_{bc}$ is the base collector junction capacitance.
- In case of JFET, $C_{gs}$ is the internal capacitance between gate and source and $C_{gd}$ is the internal capacitance between gate and drain.
- At higher frequencies, the reactance of the junction capacitances is low.
- As frequency increases, the reactance of junction capacitances falls. When these reactances become small enough, they provide shunting effect as they are in parallel with junctions. This reduces the circuit gain and hence the output voltage.

1. **Derive expressions for the short circuit current gain of common emitter amplifier at HF. Define alpha cut-off frequency, beta cut-off frequency and transition frequency and derive their values in terms of the circuit parameters.**
   
   (16 Marks) [May-2005]

   **CE Short – circuit gain using hybrid $\pi$ model:**

   ![Fig. The hybrid - $\pi$ circuit for a single transistor with a resistive load $R_L$](image)

   - For the analysis of short circuit current gain we have to assume $R_L = 0$.
   - With $R_L = 0$, i.e. output short circuited $r_{ce}$ becomes zero, $r_{b'e}$, $C_e$ and $C_{b'c}$ appear in parallel.
   - When $C_c$ admittance is given as $j\omega C_m = \frac{ic_{bc}}{V_{b'e}} - j\omega \frac{V_{b'e}}{C_c (1 + g_m R_L)}$
Hence, the miller capacitance is \( C_M = c_{b'C}(1 + g_m R_L) \)

Here, \( R_L = 0 \) \( \therefore C_M = C_{b'C} (C_C) \)

\( \because r_{b'e} \gg r_{b'e}, r_{b'C} \) is neglected. With these approximations we get simplified hybrid – \( \pi \) model for short circuit CE transistor as shown in above figure.

Parallel combination of \( r_{b'e} \) and \( (C_e + C_C) \) is given as

\[
Z = \frac{1}{r_{b'e} + \frac{j \omega (C_e + C_C)}{1 + j \omega r_{b'e} (C_e + C_C)}}
\]

Further simplified hybrid-\( \pi \) model:-

We can write \( V_{b'e} = I_b Z \); \( Z = \frac{V_{b'e}}{I_b} \)

The current gain for the above circuit can be given as
\[ A_i = \frac{I_L}{I_b} = -\frac{g_m V_{b'e}}{I_b} \cdot I_L = -g_m V_{b'e} \]

Substituting value of \( V_{b'e} / I_b \):
\[ A_i = -g_m Z \]
\[ A_i = \frac{-g_m r_{b'e}}{1 + j\omega r_{b'e} (C_e + C_C)} \]

We know that \( h_{fe} = g_m r_{b'e} \)

\[ A_i = \frac{-h_{fe}}{1 + j\omega r_{b'e} (C_e + C_C)} \quad \text{.........(A)} \]

From the equation (A) we can say that current is not constant.

When frequency is small, the term containing \( f \) is very small

Compared to 1 and hence at low frequency, \( A_i = -h_{fe} \).

But as frequency increases \( A_i \) reduces as shown in fig.

Let us put
\[ f_\beta = \frac{1}{2\pi r_{b'e} (C_e + C_C)} \]

Substituting value of \( f_\beta \) in equation (A) we get,
\[ A_i = \frac{-h_{fe}}{1 + j\frac{f}{f_\beta}} \]

\[ |A_i| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}} \quad \text{.........N} \]

\[ Atf = f_\beta \]

\[ |A_i| = \frac{h_{fe}}{\sqrt{2}} \]
$f_\beta$ (Cut-off frequency):-

It is the frequency at which transistor’s short circuit CE current gain drops by 3dB or $1/\sqrt{2}$ times its value at low frequency. It is given as

$$f_\beta = \frac{1}{2\pi r_{b'e}(C_e + C_C)}$$

(or) $$f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_C)}$$

(or) $$f_\beta = \frac{1}{h_{fe}2\pi g_m(C_e + C_C)}$$

$g_{b'e} = \frac{1}{r_{b'e}} = \frac{g_m}{h_{fe}}$

$f_\alpha$ (Cut-off frequency):-

It is the frequency at which transistor’s short circuit CB current gain drops by 3dB or $1/\sqrt{2}$ times its value at low frequency. It is given as

$$A_i = \frac{-h_{fb}}{1 + j\frac{f}{f_\alpha}}$$

where,

$$f_\alpha = \frac{1}{2\pi r_{b'e}(1 + h_{fb})C_e}$$

$$f_\alpha = \frac{1 + h_{fe}}{2\pi r_{b'e}C_e} \approx \frac{h_{fe}}{2\pi r_{b'e}C_e}$$

$$|A_i| = \frac{h_{fb}}{\sqrt{1 + \left(\frac{f}{f_\alpha}\right)^2}}$$

$$Atf = f_\alpha$$

$$|A_i| = \frac{h_{fb}}{\sqrt{2}}$$

The parameter $f_r$:-

It is the frequency at which short circuit CE current gain becomes unity.

At $f = f_r$, equation (N) becomes
The ratio of $f_T/f_\beta$ is quite large compared to 1. Hence equation (X) becomes,

$$1 = \frac{h_{fe}}{f_T} \frac{f_\beta}{f_T}$$

$$f_T = h_{fe}f_\beta$$

Substituting values of $f_\beta$, we get

$$f_T = h_{fe} \times \frac{g_m}{h_{fe} 2\pi(C_e + C_C)}$$

$$f_T = \frac{g_m}{2\pi(C_e + C_C)}$$

Since $C_e >> C_C$ we can write,

$$f_T = \frac{g_m}{2\pi C_e}$$

2. Derive the equation for $g_m$ which gives the relation between $g_m$, $I_C$ temperature. (8 Marks) [May-2003]

Let us consider a p-n-p transistor in the CE configuration with $V_{CC}$ bias in the collector circuit.

The transconductance is nothing but the ratio of change in the collector current due to small changes in the voltage $V_{BE}$ across the emitter junction. It is given as,

$$g_m = \left. \frac{\partial I_C}{\partial V_{BE}} \right|_{V_{CE}}$$

(1)

We know that, the collector current in active region is given as

$$I_C = I_{CO} - \alpha I_E$$

And therefore

$$\partial I_C = \alpha \partial I_E \therefore I_{CO} = \text{constant} t.$$ .

Substituting value of $\partial I_C$ in equation (1) we get,
The emitter diode resistance, $r_e$ is given as
\[ r_e = \frac{\partial V_E}{\partial I_E} \]

Substituting $r_e$ in place of $\partial I_E/\partial V_E$ we get,
\[ g_m = \frac{\alpha}{r_e} \tag{3} \]

The emitter diode is a forward biased diode and its dynamic resistance is given as,
\[ r_e = \frac{V_T}{I_E} \tag{4} \]

Where $V_T$ is the “volt equivalent of temperature”, defined by
\[ V_T = \frac{K T}{q} \]

Where ‘K’ is the Boltzmann constant in joules per degree Kelvin ($1.38 \times 10^{-23}$ J/K) is the electronic charge ($1.6 \times 10^{-19}$ C).

Substituting value of $r_e$ in equation (3) we get,
\[ g_m = \frac{\alpha I_E}{V_T} - I_C = I_{CO} - \alpha I_E \]

For pnp transistor $I_C$ is negative. For an npn transistor $I_C$ is positive, but the foregoing analysis (with $V_E = +V_{BE}$) leads to $g_m = (I_C - I_{CO})/V_T$.

Hence, for either type of transistor, $g_m$ is positive.
\[ g_m = \frac{I_C - I_{CO}}{V_T} \rightarrow I_C >> I_{CO} \tag{5} \]

Substituting value of $V_T$ in equation (5) we get,
\[ g_m = \frac{I_C q}{KT} = \frac{I_C \times 1.6 \times 10^{-19}}{1.38 \times 10^{-23} T} = \frac{11600 I_C}{T} \tag{6} \]

From equation (6) we can say that transconductance $g_m$ is directly proportional to collector current and inversely proportional to temperature.
3. Define the expression for lower 3dB and higher 3dB frequency for cascaded amplifier.

**Lower Cut-off frequency (3dB):-**

Let us consider the lower 3dB frequency of ‘n’ identical cascaded stages as \( f_L(n) \). It is the frequency for which the overall gain falls to \( 1/\sqrt{2} \) (3dB) of its midband value.

\[
\left[ \frac{1}{\sqrt{1 + \left( \frac{f_L}{f_L(n)} \right)^2}} \right]^n = \frac{1}{\sqrt{2}}
\]

\[
\sqrt{2} = \left[ \frac{1}{\sqrt{1 + \left( \frac{f_L}{f_L(n)} \right)^2}} \right]^n
\]

Squaring on both sides we get,

\[
2 = \left[ 1 + \left( \frac{f_L}{f_L(n)} \right)^2 \right]^n
\]

Taking \( n^{th} \) root on both sides we get,

\[
2^\frac{1}{n} = \left[ 1 + \left( \frac{f_L}{f_L(n)} \right)^2 \right]
\]

\[
2^\frac{1}{n} - 1 = \left( \frac{f_L}{f_L(n)} \right)^2
\]

Taking square root on both sides we get

\[
\sqrt{2^\frac{1}{n} - 1} = \frac{f_L}{f_L(n)}
\]

\[
f_L(n) = \frac{f_L}{\sqrt{2^\frac{1}{n} - 1}}
\]

Where, \( f_L(n) \) = Lower 3dB frequency of identical cascaded stages.
\[ f_L = \text{Lower 3dB frequency of single stage.} \]
\[ n = \text{number of stages.} \]

**Higher Cut-off frequency (3dB):**

Let us consider the lower 3dB frequency of ‘n’ identical cascaded stages as \( f_H(n) \). It is the frequency for which the overall gain falls to \( \frac{1}{\sqrt{2}} \) (3dB) of its midband value.

\[
\frac{1}{\sqrt{1 + \left( \frac{f_H(n)}{f_H} \right)^2}^n} = \frac{1}{\sqrt{2}}
\]

\[
\sqrt{2} = \left[ 1 + \left( \frac{f_H(n)}{f_H} \right)^2 \right]^n
\]

Squaring on both sides we get,

\[
2 = \left[ 1 + \left( \frac{f_H(n)}{f_H} \right)^2 \right]^{-n}
\]

Taking \( n^{th} \) root on both sides we get,

\[
\frac{1}{2^n} = \left[ 1 + \left( \frac{f_H(n)}{f_H} \right)^2 \right]^{n}
\]

\[
\frac{1}{2^n} - 1 = \left( \frac{f_H(n)}{f_H} \right)^2
\]

Taking square root on both sides we get

\[
\sqrt{\frac{1}{2^n} - 1} = \frac{f_H(n)}{f_H}
\]

\[
f_H(n) = f_H \sqrt{2^n - 1}
\]

Where, \( f_H(n) = \text{Higher 3dB frequency of identical cascaded stages.} \)
\( f_H = \text{Higher 3dB frequency of single stage.} \)
n = number of stages.

In multistage amplifier \( f_L(n) \) is always greater than \( f_L \) and \( f_H(n) \) is always less than \( f_H \). Therefore, we can say that bandwidth of multistage amplifier is always less than single stage amplifier.

If stages are not identical \( f_H \) can be given as

\[
\frac{1}{f_H} = 1.1 \sqrt{\frac{1}{f_1^2} + \frac{1}{f_2^2} + \ldots + \frac{1}{f_n^2}}
\]

4. **What is rise time?** Derive the relation between rise time and upper Cut-off frequency and bandwidth.

**Rise time:** The rise time is an indication of how fast the amplifier can respond to a discontinuity in the input voltage.

**Rise Time and its relation to Upper Cut-off frequency:**

When a step input is applied, the amplifier’s high frequency RC networks prevent the output from responding immediately to the step input.

The output voltage starts from zero and rises towards the steady state value \( V \), with a time constant \( R_2 C_2 \).

The output voltage is given by

\[
V_0 = V(1 - e^{-t_1/R_2C_2}) \] ........................(1)

The time required for \( V_0 \) to reach one-tenth of its final value is calculated as
\[ 0.1 V = V \left(1 - e^{-t_1 / R_2 C_2}\right) \]
\[ 0.1 = 1 - e^{-t_1 / R_2 C_2} \]
\[ 0.9 = e^{-t_1 / R_2 C_2} \]
\[ \frac{t_1}{R_2 C_2} = 0.1 \]
\[ t_1 = 0.1R_2 C_2 \ldots \ldots (2) \]

Similarly, the time required for \( V_0 \) to reach nine-tenths its final value is calculated as
\[ 0.9 V = V \left(1 - e^{-t_2 / R_2 C_2}\right) \]
\[ 0.1 = 1 - e^{-t_2 / R_2 C_2} \]
\[ 0.9 = e^{-t_2 / R_2 C_2} \]
\[ \frac{t_2}{R_2 C_2} = 0.1 \]
\[ t_2 = 2.3R_2 C_2 \ldots \ldots (3) \]

The difference between these two values (\( t_1 \) & \( t_2 \)) is called the rise time \( t_r \) of the circuit.
The time \( t_r \) is an indication of how fast the amplifier can respond to a discontinuity in the input voltage.
The rise time is given as
\[ t_r = t_2 - t_1 = 2.3R_2 C_2 - 0.1R_2 C_2 \]
\[ t_r = 2.2R_2 C_2 \]

The upper 3dB frequency is given as
\[ f_H = \frac{1}{2\pi R_2 C_2} \]

Therefore, upper 3dB frequency can be represented in terms of rise time as given below:
\[ f_H = \frac{2.2}{2\pi t_r} = \frac{0.35}{t_r} \]

Upper 3dB frequency is inversely proportional to the rise time \( t_r \).

**Relation between Bandwidth and Rise time:-**

The frequency range from \( f_L \) to \( f_H \) is called the bandwidth of the amplifier.
Usually \( f_L << f_H \), therefore we can approximate the equation for bandwidth
The relation of rise time with upper 3dB frequency as

\[ f_H = \frac{2.2}{2\pi t_r} = \frac{0.35}{t_r} \]

Therefore, we can relate bandwidth with rise time

\[ BW \approx f_H = \frac{0.35}{t_r} \]

5. Derive the relation between Sag and Lower Cut-off frequency.

The amplifier’s low frequency RC networks consists of coupling and bypass capacitors make amplifier’s output to decrease with large time constant. As a result, the output voltage has sag or tilt associated with it.

The tilt, or sag, in time \( t_1 \) is given by

\[ \%\text{tilt} = P = \frac{V - V'}{V} \times 100 \]

\[ \%\text{tilt} = \frac{t_1}{R_1 C_1} \times 100\% \]

The lower dB frequency can be determined from the output response by carefully measuring the tilt.

We know that, the lower 3dB frequency is given as
\[ f_L = \frac{1}{2\pi R_1 C_1} \]

Therefore, lower 3dB frequency can be represented in terms of tilt

\[ P = \frac{T}{2 R_1 C_1} \times 100 \]
\[ P = \frac{1}{2 \pi f R_1 C_1} \times 100 \quad \Rightarrow \quad T = \frac{1}{f} \]
\[ P = \frac{\pi}{2 \pi f R_1 C_1} \times 100 \]
\[ P = \frac{\pi f_L}{f} \times 100 \]
\[ f_L = \frac{P f}{100 \pi} \]

6. What is the effect of coupling and bypass capacitor on the input & output circuit of a BJT amplifier at low frequencies. (10 Marks)

Let us consider a common emitter amplifier. The amplifier has three RC networks that affect its gain as the frequency is reduced below midrange. These are
RC network formed by the input coupling capacitor $C_1$ and the input impedance of the amplifier.

1. RC network formed by the output coupling capacitor $C_2$, the resistance looking in at the collector, and the load resistance.
2. RC network formed by the emitter bypass capacitor $C_E$ and the resistance looking in at the emitter.

**Input RC network:**

RC network formed by $C_1$ and $V_{out}$ is the output voltage of the network.

Applying voltage divider theorem we can write,

$$V_{out} = \left( \frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} \right) V_{in}$$

We know that a critical point in the amplifier response is generally accepted to occur when the output voltage is 70.7 % of the input ($V_{out} = 0.707 \times V_{in}$).

Thus we can write, at critical point

$$\frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} = 0.707 = \frac{1}{\sqrt{2}}$$

At the condition $R_{in} = X_{C1}$.

At the condition the overall gain is reduced due to the attenuation provided by the input RC network. The reduction in overall gain is given by

$$A_p = 20 \log \left( \frac{V_{out}}{V_{in}} \right) = 20 \log (0.707) = -3dB$$

The frequency $f_C$ at this condition is called lower critical frequency and is given by

$$f_C = \frac{1}{2\pi R_{in} C_1}$$

Where...

$$R_{in} = R_1 \parallel R_2 + h_{ie}$$

$$\therefore f_C = \frac{1}{2\pi \left( R_1 \parallel R_2 + h_{ie} \right) C_1}$$

If the resistance of input source is taken into account the above equation becomes
\[ f_c = \frac{1}{2\pi(R_S + R_{in})C_1} \]

The phase angle in an input RC circuit is expressed as \( \theta = \tan^{-1}\left(\frac{X_{C1}}{R_{in}}\right) \)

**Output RC Network:-**

Output RC network formed by \( C_2 \), resistance looking in at the collector and the load resistance.

![Output RC Network Diagram](image)

The critical frequency for this RC network is given by,

\[ f_c = \frac{1}{2\pi(R_c + R_L)C_2} \]

The phase angle in the output RC circuit is expressed as \( \theta = \tan^{-1}\left(\frac{X_{C2}}{R_c + R_L}\right) \)

**By pass Network: -**

RC network formed by the emitter bypass capacitor \( C_E \) and the resistance looking in at the emitter.
Here, \( \frac{h_{ie} + R_{TH}}{\beta} \) is the resistance looking in at the emitter. It is derived as follows:

\[
R = \frac{V_e}{I_e} + \frac{h_{ie}}{\beta} \approx \frac{V_b}{\beta I_b} + \frac{h_{ie}}{\beta} \\
R = \frac{I_b R_{TH}}{\beta I_b} + \frac{h_{ie}}{\beta} = \frac{R_{TH} + h_{ie}}{\beta}
\]

Where \( R_{TH} = R_1 || R_2 || R_S \). It is the thevenin’s equivalent resistance looking from the base of the transistor towards the input.

The critical frequency for the bypass network is

\[
f_C = \frac{1}{2\pi RC_E} \\
(or) f_C = \frac{1}{2\pi \left[ \left( \frac{h_{ie} + R_{TH}}{\beta} \right) || R_E \right] RC_E}
\]

We can see that each network has a critical frequency. It is not necessary that all these frequencies should be equal. The network which has higher critical frequency than other two networks is called dominant network. The dominant network determines the frequency at which the overall gains of the amplifier begin to drop.

10. Determine the low frequency response of the amplifier circuit shown in figure.
Given data’s:-

\[ R_S = 680 \, \Omega; \quad R_1 = 68 \, K \, \Omega; \quad R_2 = 22 \, K \, \Omega. \]

\[ h_{ie} = 1.1 \, K \, \Omega; \quad C_1 = C_2 = 0.1 \, \mu F; \quad C_E = 10 \, \mu F. \]

\[ R_C = 2.2 K \, \Omega; \quad R_L = 10 \, K \, \Omega; \quad \beta = 100. \]

**Solution:-**

a). Input RC network:

\[
f_c (\text{input}) = \frac{1}{2\pi [R_S + (R_1 \parallel R_2 \parallel h_{ie})] C_1}
\]

\[
f_c (\text{input}) = \frac{1}{2\pi [680 + (68K \parallel 22K \parallel 1.1K)] \times 0.1 \times 10^{-6}}
\]

\[
f_c (\text{input}) = \frac{1}{2\pi [680 + 1031.7] \times 0.1 \times 10^{-6}}
\]

\[
f_c (\text{input}) = 929.8 \, Hz.
\]

b). Output RC network:

\[
f_c (\text{output}) = \frac{1}{2\pi [R_C + R_L] C_2}
\]

\[
f_c (\text{output}) = \frac{1}{2\pi [2.2K + 10K] \times 0.1 \times 10^{-6}}
\]

\[
f_c (\text{output}) = 130.45 \, Hz.
\]

C) Bypass RC network:-
We have calculated all the three critical frequencies:

a). $f_c (input) = 929.8 \text{Hz}$.  
b). $f_c (output) = 130.45 \text{Hz}$.  
c). $f_c (bypass) = 923.7$

**Low frequency response** of the amplifier:

![Graph showing the low frequency response of the amplifier](image-url)

Fig. Low frequency response of the amplifier
14. What do meant by frequency response of an amplifier? How it is plotted?

**Frequency Response of Amplifiers**

Let us consider an audio frequency amplifier which operates over audio frequency range extending from 20 Hz to 20 kHz. The audio frequency amplifiers are used in everyday life. For example, they are used in radio receivers, to address large public meeting, annual social gathering of college, for various announcements to be made for passengers on railway platforms, etc.

Over the range of frequencies at which it is to be used, an amplifier should ideally provide the same amplification for all frequencies. The degree to which this is done is usually indicated by a curve, known as frequency response curve of the amplifier. This curve is a plot of the voltage gain of an amplifier against the frequency of input signal. A typical frequency response of an RC coupled amplifier is illustrated in Fig.

![Frequency Response Curve](image)

**Fig. A typical frequency response of an amplifier**

To plot this curve, input voltage to the amplifier is kept constant and frequency of input signal is continuously varied. The output voltage at each frequency of input signal is noted; and the gain of the amplifier is calculated. The output voltage or the voltage gain of the amplifier is then plotted against frequency. For an A.F. amplifier, the frequency range of interest is quite large, from 20 Hz to 20 kHz. Hence to show clearly the voltage gain over such a wide frequency range, the frequency of input signal is plotted on x-axis using log scale (instead of usual linear scale). However the output voltage or voltage gain of the amplifier is plotted on y-axis with linear scale.

It is seen from the frequency response curve of an audio frequency amplifier that the gain of the amplifier remains fairly constant in the mid-frequency range, while the gain varies with frequency in low and high frequency regions of the curve. The frequency response is nearly ideal over a wide range of mid-frequency. Only at low and high frequency ends, the gain deviates from ideal characteristics. The decrease in voltage gain with frequency is called roll-off.
15. Explain about the high frequency of FET.

In the high frequency model of FET, the capacitances between nodes have to be added in the low frequency model. The resulting equivalent circuit is shown in Fig.

\( C_{gs} \) represents the barrier capacitance between gate and source. \( C_{gd} \) is the barrier capacitance between gate and drain. \( C_{ds} \) is the drain to source capacitance of the channel. There interval capacitances leads to feedback from output to input and the voltage amplification decreases at higher frequencies.

\[
V_o = \frac{I_Z}{Z}
\]

Where \( I_Z \) = Short-circuit current and

\( Z \) = impedance between the terminals

<table>
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<tr>
<th>Parameter</th>
<th>( g_m )</th>
<th>( r_d )</th>
<th>( c_{ds} )</th>
<th>( C_{gs} ), ( C_{gd} )</th>
<th>( r_{gs} ),</th>
<th>( r_{gd} )</th>
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<td>0.1 – 1</td>
<td>1 – 10 pF</td>
<td>&gt;10^5Ω</td>
<td>&gt;10^6Ω</td>
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<td></td>
<td>MΩ</td>
<td>pF</td>
<td>pF</td>
<td></td>
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</tr>
</tbody>
</table>

The Common Source (CS) Amplifier at High Frequencies.

The circuit of Fig. shows the CS amplifier.

The output voltage \( V_o \) between D and S is given by

\[
V_o = I_Z \frac{1}{Z}
\]
Let us calculate Z. To calculate Z, the independent generator Vi is the short-circuited, so that \( V_i = 0 \), and hence is no current in the dependent generator \( g_m V_i \). Thus, the Z is the parallel combination of the impedance corresponding to \( R_l \), \( C_d \), \( r_d \) and \( C_{gd} \) and it is given by

\[
Z = \frac{1}{Y_L + Y_{ds} + g_d + Y_{gd}} \quad \text{---------------------}(2)
\]

Where \( Y_L = \frac{1}{R_L} \) : Admittance corresponding to \( R_L \)
\( Y_{ds} = j\omega C_{ds} \) : Admittance corresponding to \( C_{ds} \)
\( g_d = \frac{1}{r_d} \) : Conductance corresponding to \( r_d \)
\( Y_{gd} = j\omega C_{gd} \) : Admittance corresponding to \( C_{gd} \)

The current I in the direction from D to S with output terminals shorted is given by,

\[
I = g_m V_i + V_i Y_{gd} = V_i (-g_m + Y_{gd}) \quad \text{---------------------}(3)
\]

**Voltage Gain**

The voltage gain for common source amplifier circuit with the load \( R_L \) is given by,

\[
A_v = V_o \frac{V_i}{V_i} = \frac{IZ}{V_i} = -\frac{I}{V_i Y}
\]

Substituting the values of \( I \) and \( Y \) from equations (2) and (3) we have,

\[
A_v = \frac{-g_m + Y_{gd}}{Y_L + Y_{ds} + g_d + Y_{gd}} \quad \text{---------------------}(4)
\]

At low frequencies, \( Y_{ds} \) and \( Y_{gd} = 0 \) and hence equation (4) reduces to

\[
A_v = \frac{-g_m}{Y_L + g_d} = \frac{-g_m \frac{r_d}{Z_L}}{Y_L + \frac{g_d}{r_d} \frac{Z_d}{Z_L}} = \frac{-g_m r_d Z_d}{r_d + Z_L}
\]

\[
= -g_m \frac{Z_d}{Z_L} \quad \text{where} \quad Z_L = r_d || Z_L \quad \text{---------------------}(5)
\]

**Input Admittance**

At high frequencies, the gate circuit is not isolated from the drain circuit; however, it is connected by \( C_{gd} \). Using Miller's theorem, we can split this admittance : \( Y_{gd} (1 - k) \) between G and S, and \( Y_{gd} \left(1 - \frac{1}{k}\right) \) between D and S, where \( k = A_v \). Hence the input admittance is given by,

\[
Y_i = Y_{gs} + (1 - A_v) Y_{gd}
\]

Equation (6) indicates that, for the FET amplifier, the input admittance is negligible over a wide range of frequencies if the gate-source and gate-drain capacitances are negligible.
Input Capacitance (Miller Effect)

Consider the FET with a drain-circuit resistance $R_d$. For this amplifier the $A_v$ in the audio frequency range is given by,

$$A_v = -g_m R_d$$

where $R'_d = r_d R_d$

Substituting the value of $A_v$ in the equation (6) we have,

$$\frac{Y_i}{j\omega} = C_i = C_{gs} + (1 + g_m R'_d) C_{gd}$$

... (7)

This increase in input capacitance $C_i$ over the capacitance from gate to source is called the Miller effect.

This input capacitance affects the gain at high frequencies in the operation of cascaded amplifiers. In cascaded amplifiers, the output from one stage is used as the input to a second amplifier. Hence the input impedance of the second stage acts as a shunt across the output of the first stage and $R_d$ is shunted by the capacitance $C_i$. Since the reactance of a capacitor decreases with increasing frequencies, the resultant output impedance of the first stage will be correspondingly low for the high frequencies. This will result in a decreasing gain at the higher frequencies.

Output Admittance

For the circuit shown in the Fig. 6.39, the output impedance is obtained by "looking into the drain" with the input voltage set equal to zero. If $V_i = 0$ in Fig. 6.39 (b), we see $r_d$, $C_{ds}$ and $C_{gd}$ in parallel. Hence the output admittance with $R_L$ considered external to the amplifier is given by,

$$Y_o = g_d + Y_{ds} + Y_{gd}$$

... (8)

Common Drain Amplifier at High Frequencies

The Fig. shows the common drain amplifier circuit and the small signal equivalent circuit at high frequencies.
Voltage Gain

The output voltage $V_o$ can be found from the product of the short-circuit and the impedance between terminals $S$ and $N$. Thus voltage gain is given by,

$$\frac{V_o}{V_i} = \frac{g_m + j\omega C_{gs}}{R_s + (g_m + g_d + j\omega C_T)}$$

...(9)

where

$$C_T = C_{gs} + C_{ds} + C_{sn}$$

$C_{sn}$: Capacitance from source to ground

$$A_V = \frac{(g_m + j\omega C_{gs}) R_s}{1 + (g_m + g_d + j\omega C_T) R_s}$$

...(10)

At low frequencies the gain reduces to

$$A_V = \frac{g_m R_s}{1 + (g_m + g_d) R_s}$$

...(11)

Input Admittance

The input admittance $Y_i$ can be obtained by applying Miller's theorem to $C_{gs}$. It is given by,

$$Y_i = j\omega C_{gd} + j\omega C_{gs}(1 - A_V) = j\omega C_{gd}$$

because

$$A_V = 1.$$ 

Output Admittance

The output admittance $Y_o$ with $R_s$ considered external to the amplifier, is given by,

$$Y_o = g_m + g_d + j\omega C_T$$

...(13)

At low frequencies, the output resistance $R_o$ is,

$$R_o = \frac{1}{g_m + g_d} = \frac{1}{g_m}$$

since $g_m >> g_d$.

...(14)

Frequency Response of Common Source Amplifier

Let us consider a typical common source amplifier as shown in Fig. 6.41.

Fig. shows the high frequency equivalent circuit for the given amplifier circuit. It shows that at high frequencies coupling and bypass capacitors act as short circuits and do not affect the amplifier high frequency response. The equivalent circuit shows internal capacitances which affect the high frequency response.
Fig. High frequency equivalent circuit

Using Miller theorem this high frequency equivalent circuit can be further simplified as follows:

The internal capacitance $C_{gd}$ can be split into $C_{\text{in (miller)}}$ and $C_{\text{out (miller)}}$ as shown in the Fig.

Fig. Simplified high frequency equivalent circuit

where

$$C_{\text{in (miller)}} = C_{gd} \left( A_v + 1 \right)$$
$$C_{\text{out (miller)}} = \frac{C_{gd}}{\left( A_v \right)}$$

FET data sheets do not directly provide values for $C_{gs}$ and $C_{gd}$. The data sheet normally provides values for input capacitance, $C_{\text{iss}}$ and the reverse transfer capacitance $C_{\text{rss}}$. From $C_{\text{iss}}$ and $C_{\text{rss}}$ the values for $C_{gs}$ and $C_{gd}$ can be calculated as follows:
Input RC Network

Fig 1 shows input RC network. This network is further reduced as shown in fig 2. Since, $R_S << R_G$

The critical frequency for the reduced input network is given as, $f_c(\text{input}) = \frac{1}{2\pi R_S C_T}$

Or $f_c = \frac{1}{2\pi} R_S \left[ C_{G_S} + C_{in}(\text{miller}) \right]$

The phase shift in high frequency input RC network is $\theta = \tan^{-1}(R_S/X_{CT})$

Output RC Network:

Output network with current source

The critical frequency for the above circuit is given as,

$f_c = \frac{1}{2\pi} \frac{1}{C_{out}(\text{miller})} = \frac{1}{2\pi} (R_{in} || R_L) C_{out}(\text{miller})$

The phase shift in high frequency output RC network is $\theta = \tan^{-1}(\theta_0/X_{Cout}(\text{miller}))$
UNIT V

POWER SUPPLIES AND ELECTRONIC DEVICE TESTING

1) Explain the operation of a half wave rectifier circuit with various parameters that govern its performance?

The circuit of a half wave rectifier is shown in fig. below:

Construction:

The rectifying element conducts only during positive half cycle of input ac supply. The negative half cycles of ac supply are eliminated from the output. This rectifier circuit consists of resistive load, rectifying element is p-n junction diode, and the source of ac voltage, all connected in series. Usually the rectifier circuits are operated from the ac mains supply. To obtain the desired dc voltage across the load, the ac voltage is applied to the rectifier circuit using suitable step up or step down transformer with suitable turns ratio.

The input to the rectifier circuit shown above is a sinusoidal voltage. Let R_f be the forward resistance of the diode and when the diode is reverse biased, the diode almost acts as an open circuit, conducting no current.

Operation:

During the positive half cycle of secondary ac voltage, terminal (A) becomes positive with respect to terminal (B). The diode is forward biased and the current flows in the circuit in the clockwise direction as shown in fig. below. The current will flow for almost full positive half cycle. This current is also flowing through load resistance R_L, hence denoted as load current i_L.
During negative half cycle, when terminal (A) is negative with respect to terminal (B), diode becomes reverse biased. Hence no current flows in the circuit as shown in figure above. Thus the circuit current is in the form of half sinusoidal pulses called pulsating dc. Similarly, the load voltage is also in the form of half sinusoidal pulses. Since the output is pulsating in nature, it is necessary to calculate the average value of load current and average value of output voltage.

The load current can be mathematically expressed as:
\[ i_L = \begin{cases} 
I_m \sin \omega t, & 0 < \omega t < \pi \\
0, & \pi < \omega t < 2\pi 
\end{cases} \]

**Performance parameters of half wave rectifier:**

**Average DC load current:**

The average or dc value of alternating current is obtained by integration. For finding out the average value of an alternating waveform, we have to determine the area under the curve over one complete cycle i.e from 0 to 2\(\pi\) and then dividing it by the base i.e 2\(\pi\).

Mathematically, current waveform can be described as:
\[ i_L = \begin{cases} 
I_m \sin \omega t, & 0 \leq \omega t \leq \pi \\
0, & \pi \leq \omega t \leq 2\pi 
\end{cases} \]

where \(I_m\) = peak value of load current
As current flows during negative half cycle of ac input voltage, i.e., between $\omega t = 2\pi$, we change the limits of integration.

$$I_{DC} = \frac{1}{2\pi} \int_{0}^{2\pi} iLd(\omega t)$$

$$= \frac{1}{2\pi} \int_{0}^{2\pi} \text{Im} \sin \omega t d(\omega t)$$

$$I_{DC} = \frac{1}{2\pi} \int_{0}^{\pi} \text{Im} \sin \omega t d(\omega t)$$

$$= -\frac{\text{Im}}{2\pi} [\cos \pi - \cos 0]$$

$$= -\frac{\text{Im}}{2\pi} [-1 - 1]$$

$$I_{DC} = \frac{\text{Im}}{\Pi} = \text{average value}$$

Applying Kirchhoff's voltage law, we can write,

$$I_m = \frac{E_{sm}}{R_f + R_s + R_L}$$

Where $R_s = \text{resistance of secondary winding of transformer}$. If $R_s$ is not given, it should be neglected while calculating $I_m$.

**Average DC load voltage ($E_{DC}$)**

The average dc load voltage is the product of average dc load current and the load resistance $R_L$.

$$E_{DC} = I_{DC} R_L = \frac{\text{Im} R_L}{\Pi} = \frac{E_{sm}}{(R_f + R_s + R_L)\Pi} R_L$$

The winding resistance $R_s$ and forward diode resistance $R_f$ are practically very small compared to $R_L$.

$$E_{DC} = \frac{E_{sm}}{\Pi\left(1 + \frac{R_f + R_s}{R_L}\right)}$$

But $R_f$ and $R_s$ are small compared to $R_L$. 

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\[ E_{DC} = \frac{E_{sm}}{\Pi} \]

**RMS Load current (I_{rms})**

The R.M.S means squaring, finding mean and then finding square root. Hence R.M.S value of load current can be obtained as,

\[
I_{rms} = \sqrt{\frac{1}{2\Pi} \int_0^\Pi \left[ \text{Im} \sin \omega t \right]^2 d(\omega t)}
\]

\[
= \text{Im} \sqrt{\frac{1}{2\Pi} \int_0^\Pi \left[ \frac{1 - \cos 2\omega t}{2} \right] d(\omega t)}
\]

\[
= \text{Im} \sqrt{\frac{1}{2\Pi} \left\{ \frac{\omega t}{2} - \frac{\sin(2\omega t)}{4} \right\}^\Pi_0}
\]

\[
= \text{Im} \sqrt{\frac{1}{2\Pi} \left( \frac{\Pi}{2} \right)}
\]

\[
I_{rms} = \frac{\text{Im}}{2}
\]

**D.C Power output (P_{dc})**:

The d.c power output can be obtained as,

\[
P_{dc} = E_{dc}I_{dc} = I_{dc}^2R_L
\]

D.C power output \( = I_{dc}^2R_L = \left[ \frac{\text{Im}}{\Pi} \right]^2R_L \)

\[
P_{dc} = \left[ \frac{\text{Im}}{\Pi} \right]^2R_L
\]

Where \( I_m = \frac{E_{sm}}{R_f + R_L + R_s} \)

\[
P_{dc} = \frac{E_{sm}2RL}{\Pi^2[R_f + R_L + R_s]^2}
\]

**A.C power input (P_{ac})**
The power input taken from the secondary of transformer is the power supplied to three resistances namely $R_L$, the diode resistance $R_f$ and winding resistance $R_s$. The a.c power is given by,

$$P_{ac} = I_{rms}^2 [R_L + R_f + R_s]$$

But $I_{rms} = \frac{I_m}{\sqrt{2}}$ for half wave

$$P_{ac} = I_m^2/4 [R_L + R_f + R_s]$$

**Rectifier efficiency ($\eta$)**

The rectifier efficiency is defined as the ratio of output d.c power to input a.c power.

$$\eta = \frac{D.C.\text{output power}}{A.C.\text{input power}} = \frac{P_{dc}}{P_{ac}}$$

$$\eta = \frac{(4/\pi)2RL}{R_f + R_s + RL}$$

$$\eta = \frac{0.406}{1 + \left(\frac{R_f + R_s}{RL}\right)}$$

if $(R_f + R_s) \ll R_L$ as mentioned earlier, we get the maximum theoretical efficiency of half wave rectifier as,

$$\% \eta = 0.406 \times 100 = 40.6 \%$$

Thus in half wave rectifier, maximum 40.6% ac power gets converted to d.c power in the load. If the efficiency of rectifier is 40% then what happens to the remaining 60% power. It is present in terms of ripples in the output which is fluctuating component present in the output. Thus more the rectifier efficiency, less are ripple contents in the output.

**Ripple factor:**

It is seen that the output of half wave rectifier is not pure dc but a pulsating dc. The output contains pulsating components called ripples. Ideally there should not be any ripples in the rectifier output. The measure of such ripples present in the output is with the help of a factor called ripple factor denoted by $\gamma$. It tells how smooth the output is.
Smaller the ripple factor closer is the output to a pure dc. The ripple factor expresses how much successful the circuit is, in obtaining pure dc from ac input.

Mathematically ripple factor is defined as the ratio of R.M.S value of the ac component in the output to the average of dc component present in the output.

Ripple factor \( \gamma = \frac{R.M.S \text{ value of ac component}}{\text{Average of dc component}} \)

RMS Value of ac component = \( I_{ac} = \sqrt{I_{RMS}^2 - I_{DC}^2} \)

\[
\gamma = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}^2}
\]

\[
\gamma = \sqrt{\left( \frac{I_{RMS}^2}{I_{DC}^2} \right) - 1}
\]

Substituting the values of \( I_{RMS} \) and \( I_{DC} \), we get \( \gamma = 1.211 \) for half wave rectifier.

**Peak Inverse Voltage (PIV):**

The peak inverse voltage is the peak voltage across the diode in the reverse direction. For half wave rectifier the value of PIV is \( E_{sm} \).

**Transformer utilization factor (T.U.F)**

The factor which indicates how much is the utilization of the transformer in the circuit is called transformer utilization factor. (T.U.F)

\[
\text{T.U.F} = \frac{\text{DC power to the load}}{\text{AC power rating of secondary}}
\]

\[
= \frac{I_{2dc}R_L}{E_{rms}I_{rms}}
\]

\[
= \frac{(I_m / \pi)^2 R_L}{(E_{sm} I_m / 2\sqrt{2})}
\]

neglecting forward resistance \( R_f \) of diode, \( E_{sm} \approx I_m R_L \)

\[
\text{T. U. F} = \frac{I_m^2 R_L}{\pi^2 I_m^2 R_L} = 0.287
\]

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Voltage regulation:

The secondary voltage should not change with respect to the load current. The voltage regulation is the factor which tells us about the change in the dc output voltage as load changes from no load to full load condition.

If \((V_{dc})_{NL} = \) D.C voltage on no load

\((V_{dc})_{FL} = \) D.C voltage on full load

Then voltage regulation is defined as,

\[
\text{Voltage regulation} = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}}
\]

less the value of voltage regulation , better is the performance of rectifier circuit.

For a full wave circuit,

\[
(V_{dc})_{NL} = E_{sm} \quad \text{and} \quad (V_{dc})_{FL} = I_{dc} R_L
\]

the regulation can be expressed as,

\[
\% R = \frac{R_f + R_s + R_L - R_L}{R_L} \times 100
\]

\[
\% R = \frac{R_f + R_s}{R_L} \times 100
\]

Neglecting winding resistance \(R_s\), the regulation can be expressed as,

\[
\% R = \frac{R_f}{R_L} \times 100
\]

Where \(R_f = \) forward resistance of the diode.
2. Describe the working principle of full wave rectifier and derive its characteristic parameters?

**Full wave rectifier:**

The full wave rectifier conducts during both positive and negative half cycles of input a.c. supply. In order to rectify both the half cycles of a.c. input, two diodes are used in this circuit. The diodes feed a common load $R_L$ with the help of a center tap transformer. The a.c. voltage is applied through a suitable power transformer with proper turns ratio.

The full wave rectifier circuit is shown in fig

![Full wave rectifier circuit diagram](image)

For the proper operation of the circuit, a center-tap on the secondary winding of the transformer is essential.

**Operation of the circuit:**

Consider the positive half cycle of ac input voltage in which terminal (A) is positive and terminal (B) negative. The diode $D_1$ will be forward biased and hence will conduct; while diode $D_2$ will be reverse biased and will act as an open circuit and will not conduct.

The diode $D_1$ supplies the load current, i.e. $i_L = i_{d1}$. This current is flowing through upper half of secondary winding while the lower half of secondary winding of the transformer carries no current since diode $D_2$ is reverse biased and acts as an open circuit.

In the next half cycle of ac voltage, polarity reverses and terminal (A) becomes negative and (B) positive. The diode $D_2$ conducts, being forward biased, while $D_1$ does not, being reverse biased.
The diode $D_2$ supplies the load current, i.e. $i_L = i_{d2}$. Now the lower half of the secondary winding carries the current but the upper half does not.

Hence we get rectified output across the load. The load current is sum of individual diode currents flowing in corresponding half cycles. It is also noted that the two diodes do not conduct simultaneously but in alternate half cycles. The individual diode currents and the load current are shown in the fig.

Thus the full wave rectifier circuit essentially consist of two half-wave rectifier circuits working independently (working in alternate half cycles of ac) of each other but feeding a common load. The output load current is still pulsating d.c and not pure d.c.

**Wave forms:**

![Wave forms diagram](image)

**Maximum load current:**

- $R_f$ = forward resistance of diodes
- $R_s$ = winding resistance of each half of secondary
- $R_L$ = load resistance
- $e_s$ = instantaneous a.c. voltage across each half of secondary

$$e_s = E_{mp}\sin \omega t$$

$$\omega = 2\pi f$$
$E_{sm} =$ maximum value of a.c. input voltage across each half of secondary winding

Hence we can write the expression for the maximum value of the load current, looking at equivalent circuit shown in fig.

**Average dc load current ($I_{DC}$):**

Consider one cycle of load current $i_L$ from 0 to $2\pi$ to obtain the average value which is d.c value of load current.

\[ i_L = I_m \sin \omega t \quad 0 \leq \omega t \leq \pi \]

But for $\pi$ to $2\pi$ the current $i_L$ is again positive while $\sin \omega t$ term is negative during $\pi$ to $2\pi$. Hence in the region $\pi$ to $2\pi$ the positive $i_L$ can be represented as negative of $I_m \sin (\omega t)$

\[ i_L = -I_m \sin \omega t \quad \pi \leq \omega t \leq 2\pi \]

\[ I_{av} = I_{DC} = \frac{1}{2\pi} \int_{0}^{2\pi} iLd(\omega t) \]

\[ = \frac{1}{2\pi} \left[ \int_{0}^{\pi} I_m \sin \omega t d(\omega t) + \int_{\pi}^{2\pi} -I_m \sin \omega t d(\omega t) \right] \]

\[ = \frac{I_m}{2\pi} \left[ -\cos 2\pi + \cos 0 + \cos 2\pi - \cos \pi \right] \]

But $\cos \pi = -1$

\[ = \frac{I_m}{2\pi} \left[ -(-1) + 1 + 1 - (-1) \right] \]

\[ I_{dc} = \frac{2I_m}{\pi} \text{ for full wave rectifier} \]
For half wave it is \( I_m/\pi \) and full wave rectifier is the combination of two half wave circuits acting alternately in two half cycles of input. Hence obviously the d.c value for full wave circuit is \( 2I_m/\pi \).

**Average DC load voltage (E\(_{\text{dc}}\))**

The d.c load voltage is,

\[
E_{\text{dc}} = I_{\text{dc}} R_L = \frac{2I_m RL}{\pi}
\]

Substituting value of \( I_m \)

\[
E_{\text{dc}} = \frac{2E_{\text{sm}} RL}{\pi[R_f + R_s + R_L]} = \frac{2E_{\text{sm}}}{\pi[1 + \frac{R_f + R_s}{R_L}]}
\]

But as \( R_f \) and \( R_s \ll R_L \) hence \( \frac{R_f + R_s}{R_L} \ll 1 \)

\[
E_{\text{dc}} = \frac{2E_{\text{sm}}}{\pi}
\]

**RMS Load current (I\(_{\text{rms}}\))**

The RMS value of current can be obtained as follows:

\[
I_{\text{rms}} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i^2_L d(\omega t)}
\]

Since two half wave rectifier are similar in operation we can write,

\[
I_{\text{rms}} = \sqrt{\frac{2}{2\pi} \int_0^{2\pi} [\text{Im}\sin \omega t]^2 d(\omega t)}
\]

\[
= \text{Im} \sqrt{\int_0^{\pi} \left[ \frac{1 - \cos 2\omega t}{2} \right] d(\omega t)}
\]

\[
I_{\text{rms}} = \text{Im} \sqrt{\frac{1}{2\pi} \left[ \frac{\omega t}{2} - \frac{\sin(2\omega t)}{2} \right]_0^\pi}
\]

\[
= \text{Im} \sqrt{\frac{1}{2\pi} [\pi - 0]}
\]

\[
I_{\text{rms}} = \frac{\text{Im}}{\sqrt{2}}
\]
D.C Power output (P_{dc})

The d.c power output can be obtained as,

\[ P_{DC} = E_{DC} I_{DC} = I_{dc}^2 R_L \]

D.C power output = \( I_{dc}^2 R_L = \left( \frac{2 I_m}{\Pi} \right)^2 R_L \)

\[ P_{dc} = \frac{4 E_{sm}^2}{\Pi^2} \frac{1}{(R_s + R_f + R_L)^2} \times R_L \]

A.C power input (P_{ac})

The a.c power input is given by,

\[ P_{ac} = I_{rms}^2 [R_L + R_f + R_s] \]

\[ P_{ac} = I_m^2 \frac{(R_s + R_f + R_L)}{2} \]

Substituting value of \( I_m \) we get,

\[ P_{ac} = E_{sm}^2 \times \frac{1}{(R_s + R_f + R_L)^2} \times \frac{1}{2} \]

\[ P_{ac} = E_{sm}^2 \times \frac{1}{2(R_f + R_s + R_L)} \]

Rectifier efficiency (\( \eta \))

The rectifier efficiency is defined as the ratio of output d.c power to input a.c power.

\[ \eta = \frac{D.C.outputpower}{A.C.inputpower} = \frac{P_{dc}}{P_{ac}} \]

\[ \eta = \frac{8RL}{\Pi^2(2R_f + R_s + R_L)} \]

but if \( R_f + R_s \ll R_L \), neglecting it from denominator

\[ \eta = \frac{8RL}{\Pi^2(2RL)} = \frac{8}{\Pi 2} \]
\[ \%\eta_{\text{max}} = \frac{8}{\Pi^{2}} \times 100 = 81.2\% \]

This is the maximum theoretical efficiency of full wave rectifier.

**Ripple factor \( (\gamma) \)**

The ripple factor is given by a general expression,

\[ \text{Ripple factor} = \frac{\text{Irms}}{\text{Idc}} \]

For full wave \( I_{\text{rms}} = \frac{I_{m}}{\sqrt{2}} \) and \( I_{\text{dc}} = \frac{2I_{m}}{\Pi} \)

Substituting in the above equation,

\[ \text{Ripple factor} = \sqrt{\frac{\frac{\text{Irms}}{\sqrt{2}}}{\frac{2\text{Irms}}{\Pi}}} - 1 \]

\[ = \sqrt{\frac{\Pi^{2}}{8}} - 1 \]

\[ \text{Ripple factor} = \gamma = 0.48 \]

This indicates that the ripple contents in the output are 48% of the d.c component which is much less than that for the half wave circuit.

**Peak inverse voltage (PIV)**

It can be observed from the circuit diagram that when diode is reversed biased then full transformer secondary voltage gets impressed across it. The drop across conducting diode is assumed zero. Thus the peak value of the inverse voltage to which diode gets subjected is voltage across both the parts of the transformer secondary.

It can be seen that when \( D_2 \) is reverse biased, point A is at \(-E_{\text{sm}}\) with respect to ground while point B is at \(+E_{\text{sm}}\) with respect to ground, neglecting diode drop. Thus total peak voltage across \( D_2 \) is \( 2E_{\text{sm}} \). \( \text{PIV of diode} = 2E_{\text{sm}} \)
where $E_{sm}$ = maximum value of ac voltage across half the secondary of transformer.
If the diode drop is considered to be 0.7 V then the PIV of reverse biased diode is

$$\text{PIV of diode} = 2E_{sm} - 0.7$$

This is because only one diode conducts at a time.

**Transformer utilization factor (T.U.F)**

In full wave rectifier, the secondary current flows through each half separately in every half cycle. While the primary of transformer carries current continuously. Hence T.U.F is calculated for primary and secondary windings separately and then the average T.U.F is determined.

Secondary T.U.F =

$$\frac{\text{DCpower to the load}}{\text{AC power rating of secondary}} = \frac{I_{dc} R_L}{E_{rms} I_{rms}}$$

$$= (\frac{2}{\Pi} I_m)^2 \frac{E_{sm}}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

Neglecting Forward Resistance $R_f$ Of Diode, $E_{sm} \approx I_m R_l$

Secondary T.U.F =

$$\frac{4 \times I_m^2 R_L}{\Pi R_L} = \frac{8}{\Pi 2} = 0.812$$

The primary of the transformer is feeding two half-wave rectifiers separately. These two half-wave rectifiers work independently of each other but feed a common load. We have already derived the T.U.F for half wave circuit to be equal to 0.287. Hence T.U.F for primary winding = 2 x T.U.F of half wave circuit.

$$= 2 \times 0.287 = 0.574$$
Average T.U.F for full Wave rectifier circuit =

\[
\frac{T.U.F_{primary} + T.U.F_{secondary}}{2} = \frac{0.574 + 0.812}{2} = 0.693
\]

Thus in full-wave circuit transformer gets utilized more than the half wave rectifier.

**Voltage regulation:**

The secondary voltage should not change with respect to the load current. The voltage regulation is the factor which tells us about the change in the dc output voltage as load changes from no load to full load condition.

If \( (V_{dc})_{NL} \) = D.C voltage on no load

\( (V_{dc})_{FL} \) = D.C voltage on full load

then voltage regulation is defined as,

\[
\text{voltage regulation} = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}}
\]

less the value of voltage regulation, better is the performance of rectifier circuit.

For a full wave circuit,

\[
(V_{dc})_{NL} = \frac{2E_{sm}}{\Pi} \quad \text{and} \quad (V_{dc})_{FL} = I_{dc} R_L
\]

the regulation can be expressed as,

\[
\%R = \left( \frac{2E_{sm}}{\Pi} - I_{dc} R_L \right) I_{dc} R_L \times 100
\]

Now \( I_m = \frac{E_{sm}}{R_f + R_s + R_L} \)

\( E_{sm} = I_m (R_f + R_s + R_L) \)

And \( I_{dc} = \frac{2I_m}{\Pi} \)

\[
\%R = \frac{R_f + R_s + R_L - R_L}{R_L} \times 100
\]
\[ \%R = \frac{R_f + R_s}{R_L} \times 100 \]

Neglecting winding resistance \( R_s \), the regulation can be expressed as,

\[ \%R = \frac{R_f}{R_L} \times 100 \] where \( R_f \) = forward resistance of the diode.

3) Explain in detail the operation of full wave Bridge rectifier circuit?

The bridge rectifier circuits are mainly used as,
a) a power rectifier circuit for converting ac power to dc power, and
b) a rectifying system in rectifier type ac meters, such as ac voltmeter, in which the ac voltage under measurement is first converted into dc and measured with conventional meter. In this system, the rectifying elements are either copper oxide type or selenium type.

The bridge rectifier circuit is essentially a full-wave rectifier circuit, using four diodes, forming the four arms of an electrical bridge. To one diagonal of the bridge, the ac voltage is applied through a transformer if necessary, and the rectified dc voltage is taken from the other diagonal of the bridge. The main advantage of this circuit is that it does not require a center tap on the secondary winding of the transformer. Hence wherever possible, ac voltage can be directly applied to the bridge.
Operation of the Circuit

Consider the positive half of ac input voltage. The point A of secondary becomes positive. The diodes D₁ and D₂ will be forward biased, while D₃ and D₄ reverse biased. The two diodes D₁ and D₂ conduct in series with the load and the current flows as shown.

In the next half cycle, when the polarity of ac voltage reverses hence point B becomes positive diodes D₃ and D₄ are forward biased, while D₁ and D₂ reverse biased. Now the diodes D₃ and D₄ conduct in series with the load and the current flows as shown in

\[ E_{DC} = I_{DC} R_L = \frac{2E_{sm}}{\pi} \]

\[ P_{DC} = I_{DC}^2 R_L = \frac{4}{\pi^2} I_m^2 R_L \]

\[ P_{AC} = I_{RMS}^2 (R_s + 2R_f + R_L) \]

\[ = \frac{I_m^2 (2R_f + R_s + R_L)}{2} \]

\[ \eta = \frac{8R_L}{\pi^2 (R_s + 2R_f + R_L)} \]

\[ \% \eta_{max} = 81.2\% \]

\[ \gamma = 0.48 \]
Advantages of Bridge Rectifier Circuit

1) The current in both the primary and secondary of the power transformer flows for the entire cycle and hence for a given power output, power transformer of a small size and less cost may be used.

2) No center tap is required in the transformer secondary. Hence, wherever possible, ac voltage can directly be applied to the bridge.

3) The current in the secondary of the transformer is in opposite direction in two half cycles. Hence net d.c. component flowing is zero which reduces the losses and danger of saturation.

4) Due to pure alternating current in secondary of transformer, the transformer gets utilised effectively and hence the circuit is suitable for applications where large powers are required.

5) As two diodes conduct in series in each half cycle, inverse voltage appearing across diodes get shared. Hence the circuit can be used for high voltage applications. Such a peak reverse voltage appearing across diode is called peak inverse voltage rating (PIV) of diode.

Disadvantages of Bridge Rectifier

The only disadvantage of bridge rectifier is the use of four diodes as compared to two diodes in normal full wave rectifier. This causes additional voltage drop as indicated by term $2R_i$ present in expression of $I_m$ instead of $R_i$. This reduces the output voltage.
4. Comparison of rectifiers.

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Parameter</th>
<th>Half Wave</th>
<th>Full Wave</th>
<th>Bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Number of diodes</td>
<td>1</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>2.</td>
<td>Average DC current (I_DC)</td>
<td>(\frac{I_m}{\pi})</td>
<td>(\frac{2I_m}{\pi})</td>
<td>(\frac{2I_m}{\pi})</td>
</tr>
<tr>
<td>3.</td>
<td>Average DC voltage (E_DC)</td>
<td>(\frac{E_{sm}}{\pi})</td>
<td>(\frac{2E_{sm}}{\pi})</td>
<td>(\frac{2E_{sm}}{\pi})</td>
</tr>
<tr>
<td>4.</td>
<td>RMS current (I_RMS)</td>
<td>(\frac{I_m}{\sqrt{2}})</td>
<td>(\frac{I_m}{\sqrt{2}})</td>
<td>(\frac{I_m}{\sqrt{2}})</td>
</tr>
<tr>
<td>5.</td>
<td>DC power output (P_DC)</td>
<td>(\frac{E_{sm}^2 R_L}{\pi^2} + \frac{4}{\pi^2} I_m^2 R_L)</td>
<td>(\frac{4}{\pi^2} I_m^2 R_L)</td>
<td>(\frac{4}{\pi^2} I_m^2 R_L)</td>
</tr>
<tr>
<td>6.</td>
<td>AC power input (P_AC)</td>
<td>(\frac{E_{sm}^2 (R_L + R_f + R_c)}{4})</td>
<td>(\frac{4}{\pi^2} I_m^2 R_L)</td>
<td>(\frac{4}{\pi^2} I_m^2 R_L)</td>
</tr>
<tr>
<td>7.</td>
<td>Maximum rectifier efficiency ((\eta))</td>
<td>40.6 %</td>
<td>81.2 %</td>
<td>81.2 %</td>
</tr>
<tr>
<td>8.</td>
<td>Ripple factor ((\gamma))</td>
<td>1.21</td>
<td>0.482</td>
<td>0.482</td>
</tr>
<tr>
<td>9.</td>
<td>Maximum load current (I_m)</td>
<td>(\frac{E_{sm}}{R_c + R_f + R_L})</td>
<td>(\frac{E_{sm}}{R_f + R_c + R_L})</td>
<td>(\frac{E_{sm}}{R_f - 2R_f + R_L})</td>
</tr>
<tr>
<td>10.</td>
<td>PIV rating of diode</td>
<td>(E_{sm})</td>
<td>2 (E_{sm})</td>
<td>(E_{sm})</td>
</tr>
</tbody>
</table>

5. Explain in detail the operation of capacitive filter on and half and full wave rectifier operation.

**Principle:**

we know \(X_C = \frac{1}{2\pi fC}\), if \(f\) is low, \(X_C\) is high, i.e., capacitor does not permit dc or low frequency components pass through it. If ‘\(f\)’ is high, then capacitor allows all ac high frequency component can pass through ‘\(C\)’ instead of \(R_L\). Thus capacitor filter always resources all high frequency components.

**Half wave rectifier with capacitor filter:**

**Construction:**

The half wave rectifier with a capacitor filter is shown in the fig. In this case the capacitor is connected in parallel with the output of the half wave rectifier, because, capacitor offers high reactance
Operation:

1. During the (first quarter of) positive half cycle of ac input, the diode D is forward biased hence it acts as switch and directly connects secondary across ‘C’. Now the capacitor quickly charges to a voltage $V_m$ because there is no resistance in the charging path except diode forward resistance which, is negligible.

2. When the input voltage falls (second quarter of positive half cycle) below the capacitor or $V_m$, i.e., $V_i < V_c$ the diode becomes reverse biased ($V_D = V_i - V_c$) as result of this the capacitor started to discharge through the load resistor ‘$R_L$‘.

3. During the negative half cycle, the diode D becomes reverse biased and it does not conduct, so the capacitor C continuously discharges through $R_L$.

4. As the discharging time constant ($= CR_L$) is large, usually 100 times more than charging time, hence the capacitor does not have sufficient time to discharge appreciably. Due to this fact the voltage of capacitor C decreases slightly, this process is repeated till the next positive half cycle.
5. During the next positive half cycle, when the input voltage increases above the capacitor voltage (Vin > Vc), the diode becomes forward biased due to this the capacitor is charged towards its maximum value.

6. The instant at which conduction stops is called the ‘cut out’ point and the time at which the conduction starts is known as ‘cut in point’ which is shown in fig. above.

7. During cut-in to cut-off points, the diode current flows and diode voltage in these instants is greater than the capacitor voltage. Thus the diode current is a short duration of pulses i.e. a surging current.

8. Hence the diode acts as a switch which permits charge to flow in capacitor when the input voltage exceeds the capacitor voltage and then disconnects the source when the input voltage falls below that of capacitor voltage.

Circuit Diagram:

[Diagram showing the circuit with diode and capacitor with voltage waveforms.]
Wave form:

Construction

It consists of either center tapped full wave rectifier or bridge type full wave rectifier with capacitor as filter which is connected across load resistor as shown in fig. We know the inductor filter is only suitable for the heavy loads. An inexpensive filter for light loads is found that the capacitor filter which is connected directly across the load.

Operation

1) During first half of positive half cycle the diode $D_1$ is forward biased, $D_2$ is reverse biased then the capacitor charges up to the peak value of the input voltage and tries to maintain this value $V_{in}$

2) When the input voltage falls below $V_m$ or $V_c$ then ($V_c < V_{in}$) both diodes become reverse biased thus the capacitor starts discharging through the load resistor, it will continue until the input voltage exceeds the capacitor voltage.
3) During the negative half cycle of input, diode D1 is reverse biased and diode D2 is forward biased. When input voltage exceeds the capacitor voltage, the capacitor starts charging the same procedure is repeated for all cycle.

4) However, as the load increases, the discharge of capacitor C will be greater resulting in more ripple and lower dc output voltage.

Wave from:
Expression for Ripple Voltage

The ripple voltage present in the output can be obtained from the ripple factor.

\[
\text{Ripple factor} = \frac{V_{r\text{(rms)}}}{E_{DC}}
\]

Thus

\[
V_{r\text{(rms)}} = \text{R.M.S. ripple voltage} = E_{DC} \times \text{ripple factor}
\]

For full wave rectifier,

\[
\frac{1}{4\sqrt{3} fC R_L} = \frac{V_{r\text{(rms)}}}{E_{DC}} = \frac{V_{r\text{(rms)}}}{I_{DC} R_L}
\]

\[
\therefore \quad V_{r\text{(rms)}} = \frac{I_{DC}}{4\sqrt{3} fC} \text{ volts} \quad \text{(For full wave)}
\]

Thus the ripple voltage with capacitor input filter can be obtained by multiplying ripple factor with d.c. output voltage or by using equation if the d.c. load current is known.
6. Explain about inductor or choke filter and derive its ripple factor.

**Construction:**

It consists of center tapped type rectifier or bridge type rectifier, an inductor and load resistance $R_L$.

The figure indicates that FWR with inductor filter simply consists of a choke in series with the load. We know the characteristic of an inductor, it oppose any change in current, thus it will have a smoothing effect. The impedance of the inductor varies with frequency hence the inductor will remove all the high frequency components and leaves dc and low frequency ripple components.
Operation:

1. When an ac voltage is applied to the primary winding of transformer by transformer action, it can be transferred to secondary winding of the transformer.

2. During the positive half cycle of input, the potential at point ‘A’ is more positive than ‘C’ makes diode D1 starts conducting, thus diode acts as short circuit and permits the current to pass through it. The output current contains dc component and ripple components.

3. During the negative half cycle of input the point ‘A’ is more negative than point ‘C’ makes the diode D1 reverse biased, thus it acts as open circuit and does not permit any current to pass through it. Diode D2 becomes forward biased and starts conduct. The above procedure is repeated, thus the inductor continuously supplying the current to the load.

4. The output of the diode is pass through the inductor but the inductor does not permit any variation in current passing through it. This can be explained as follows:
When the output current of the rectifier increases above the average value, the inductor starts storing the magnetic energy. This stored energy tends to decrease the sudden rise in current.

When the output of the rectifier decreases below the average value, the stored energy prevents the current falling down to zero or minimum value. Thus the output current is always maintained at average value.

We know that the Fourier series for the load current for full wave rectifier as,

\[ i_L = I_m \left[ \frac{2}{\pi} \cos 2\omega t - \frac{4}{3\pi} \cos 4\omega t \right] \]

Neglecting higher order harmonics we get,

\[ i_L = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi} \cos 2\omega t \]

Neglecting diode forward resistances and the resistance of choke and transformer secondary, we can write the d.c. component of current as,

\[ I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi R_L} \]

as \[ I_m = \frac{V_m}{R_L} \]

While the second harmonic component represents a.c. component or ripple present and can be written as,

\[ I_m = \frac{V_m}{Z} \text{ for a.c. component} \]

Now \[ Z = R_L + j2X_L = \sqrt{R_L^2 + 4\omega^2 L^2} \angle \phi \]

where \[ \phi = \tan^{-1} \frac{2\omega L}{R_L} \]

\[ I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}} \]
Hence equation (1) modifies as,

$$i_L = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi \sqrt{R_L^2 + 4\omega^2 L^2}} \cos\left(2\omega t - \phi\right)$$

The negative $\phi$ indicates that current lags the voltage due to inductive circuit.

### Expression for the Ripple Factor

Ripple factor is given by,

$$\text{Ripple factor} = \frac{I_{rms}}{I_{DC}}$$

where

$$I_{rms} = \frac{V_m}{\sqrt{2}}$$

$$I_{rms} = \frac{4V_m}{3\sqrt{2} \pi \sqrt{R_L^2 + 4\omega^2 L^2}}$$

while

$$I_{DC} = \frac{2V_m}{\pi R_L}$$

So, Ripple factor

$$\frac{4V_m}{3\sqrt{2} \pi \sqrt{R_L^2 + 4\omega^2 L^2}}$$

$$= \frac{2}{3\sqrt{2}} \frac{1}{\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

Initially on no load condition, $R_L \to \infty$ and hence $\frac{4\omega^2 L^2}{R_L^2} \to 0$.

So, Ripple factor $= \frac{2}{3\sqrt{2}} = 0.472$

This is very close to normal full wave rectifier without filtering.

But as load increases, $R_L$ decreases hence $\frac{4\omega^2 L^2}{R_L^2} \gg 1$. So neglecting 1 we get,

$$\text{Ripple factor} = \frac{2}{3\sqrt{2}} \frac{1}{\sqrt{\frac{4\omega^2 L^2}{R_L^2}}}$$

$$\gamma = \frac{R_L}{3\sqrt{2} \omega L}$$

So as load changes, ripple changes which is inversely proportional to the value of the inductor.
7. Explain about LC filter and derive for ripple factor and bleeder resistance.

This is also called choke input filter as the filter element looking from the rectifier side is an inductance L. The d.c winding resistance of the choke is \( R_x \). The circuit is also called L-type filter or LC filter. The circuit is shown in the Fig.

![Choke input filter circuit diagram](image)

Fig. Choke input filter

The basic requirement of this filter circuit is that the current through the choke must be continuous and not interrupted. An interrupted current through the choke may develop a large back e.m.f. which may be in excess of PIV rating of the diodes and/or maximum voltage rating of the capacitor C. Thus this back e.m.f. is harmful to the diodes and capacitor. To eliminate the back e.m.f. developed across the choke, the current through it must be maintained continuous.

This is assured by connecting a bleeder resistance, \( R_b \), across the output terminals.

We have seen that the lowest ripple frequency for a full wave rectifier circuit is twice the supply frequency of a.c. input voltage to the rectifier. Let \( f \) in Hz, be the supply frequency.

The equation for "\( e_{in} \)" can now be approximately written as,

\[
e_{in} = E_{am} \left[ \frac{2}{\pi} - \frac{4}{3\pi} \cos 2\omega t \right]
\]

The d.c. current in the circuit will be,

\[
I_{DC} = \frac{2}{\pi} \frac{E_{am}}{R_x + R}
\]

\[
R = R_b \parallel R_L
\]

\[
\therefore E_{DC} \text{ across the load} = I_{DC} \times R = \frac{2}{\pi} \frac{E_{am}}{R_x + R} \times R
\]

\[
\therefore E_{DC (out)} = \frac{2}{\pi} \frac{E_{am}}{1 + \frac{R_x}{R}} = \frac{E_{DC (in)}}{1 + \frac{R_x}{R}}
\]

Normally, \( R_x \) is much less than \( R \), i.e. \( R_x \ll R \)

Then,

\[
E_{DC} = \frac{2}{\pi} E_{am} = E_{DC (in)}
\]
Let us calculate the ripple factor for choke input filter, based on the assumptions already made.

The impedance $Z_2$ of the filter circuit for second harmonic component of input, i.e. at $2\omega$, will be,

$$Z_2 = (R_s) + (j \frac{2\omega L}{|R|})$$

But, $\frac{1}{2\omega C} << R$, and $2\omega L >> R_s$, as per assumptions.

Hence,

$$|Z_2| = 2\omega L$$

Second harmonic component of the current in the filter circuit, will be

$$I_{2m} = \frac{4}{3\pi} \frac{E_{2m}}{Z_2} = \frac{4}{3\pi} \frac{E_{sm}}{2\omega L}$$

The second harmonic voltage across the load is

$$E_{2m} = I_{2m} \times \left[ \frac{1}{2\omega C} \parallel \frac{1}{R} \right] = I_{2m} \times \frac{1}{2\omega C}$$

Since , $\frac{1}{2\omega C} << R$

$$E_{2m} = I_{2m} \times \frac{1}{2\omega C} = \frac{4}{3\pi} \frac{E_{sm}}{2\omega L} \times \frac{1}{2\omega C}$$

$$\therefore E_{2m} = \frac{4}{3\pi} \frac{E_{sm}}{4\omega^2 L C} = \frac{E_{sm}}{3\pi \omega^2 L C}$$

$$\therefore E_{2rms} = \frac{E_{2m}}{\sqrt{2}} = \frac{E_{sm}}{3\sqrt{2} \pi \omega^2 L C}$$

Hence the ripple factor is given by,

$$\text{Ripple factor} = \frac{E_{2rms}}{E_{DC}}$$
The Necessity of Bleeder Resistance $R_B$

\[
I_{DC} = \frac{2}{\pi} \frac{E_{sm}}{R_x + R}
\]

\[
\Rightarrow \quad \frac{2}{\pi} \frac{E_{sm}}{R_x + R} = \frac{4}{3\pi} \frac{E_{sm}}{2\omega L}
\]

\[
\Rightarrow \quad \frac{R + R_x}{R_x} = \frac{3\omega L}{R}
\]

Usually $R_x \ll R$, then

\[ R = 3\omega L \]

Considering the worst case that the load resistance $R_L$ is not connected, then $R = R_B$

Since \[ R = R_B || R_L \]

\[
\Rightarrow \quad R_B = 3\omega L = 3(2\pi f) L
\]

\[ f = 50 \text{ Hz} \]

\[
\Rightarrow \quad R_B = 3 \times 2 \times \pi \times 50 \times L = 943 \text{ L}
\]

Practically, $R_B$ is selected to be equal to 900 L. The values of $L$ and $C$ are selected depending on the ripple factor desired.

The regulation characteristic of the choke-input filter is shown in the Fig. (a).

So long as the value of $[R + R_x]$ is less than $3\omega L$, the d.c. load voltage is approximately constant at \[ \frac{2}{\pi} E_{sm} \] since $I_{DC}$ is then greater than $I_{2m}$.

However, as $[R + R_x]$ becomes larger than $3 \omega L$, i.e. for light loads, the d.c. voltage increases and approaches $E_{sm}$ as $R \to \infty$, since $I_{DC}$ is smaller than $I_{2m}$.

In LC filter, most of the a.c. voltage is dropped across $X_L$ as shown in the Fig.
8. Explain in detail the operation of CLC filter (Or) Pi Filter.

CLC Filter or \( \Pi \) Filter:

This is a capacitor input filter followed by a L section filter. The ripple rejection capability of this filter is very much enhanced. The circuit diagram for the CLC filter is shown in fig. below.

It consists of an inductance \( L \) with a dc winding resistance as \( R_x \) and two capacitors \( C_1 \) and \( C_2 \). The filter is fed from full wave rectifier. Generally two capacitors are selected equal. The rectifier output is given to the capacitor \( C_1 \). This capacitor offers very low reactance to the ac component and low reactance to dc. So it blocks ac component and does not allow it to reach to load while it allows dc component to pass through it. The capacitor \( C_2 \) now allows passing remaining ac component and almost pure dc component reaches to the load. The circuit looks like a \( \Pi \) and hence called as a \( \Pi \) filter.
The ripple factor of a full wave rectifier with CLC filter is given by:

$$\gamma = \frac{\sqrt{2}}{8\omega^3 L C_1 C_2 R_L}$$

**Multiple \( \Pi \) Section filter:**

To obtain almost pure dc to the load, more \( \Pi \) sections may be used one after another. Such a filter using more than one \( \Pi \) section is called a multiple \( \Pi \) section filter.

9. **Draw the block diagram schematic of Regulated power supply**

Typical dc power supply consists of various stages. Figure shows the block diagram schematic of a typical dc power supply consisting of various circuits. The nature of voltages at various points is also shown in fig. below:

The ac voltage is connected to the primary of the transformer. The transformer steps down the ac voltage to the level required for the desired dc output. Thus with suitable turns ratio we get desired ac secondary voltage. The rectifier circuit converts this ac voltage into a pulsating dc voltage. A pulsating dc voltage means a unidirectional voltage containing large varying component called ripple. The filter circuit is used after a rectifier circuit which reduces the ripple content in the pulsating dc and tries to make it smoother. Still then the filter output contains some ripple. This voltage is unregulated dc voltage. A circuit which is used after the filter is the regulator circuit which not only makes the dc voltage smooth and almost ripples free but it also keeps the dc output voltage constant though input dc voltage varies under certain conditions. It keeps output voltage constant under variable load conditions as well.
Thus a voltage regulator circuit is the one which is designed to keep the output voltage of a power supply nearly constant, under varying input voltage conditions and varying load conditions.

10. **Explain the factors affecting the load voltage, power supply performance parameters of a voltage regulator circuits.**

The factors affecting the load voltage are:

1) **Load current:** The practical power supply with regulator load voltage must be constant though load changes from no load to full load condition. But with regulator circuit also the load voltage gets affected by the load current in a power supply.

2) **Line Voltage:** The input to the rectifier which ia ac line voltage decides the level of the output voltage. Hence any change in the line voltage, changes the load voltage and affects the performance of the power supply.

3) **Temperature:** In power supply, the rectifier circuit uses p-n junction diodes. The diode characteristics are temperature sensitive. The other semiconductor devices used in power supplies have their characteristics, temperature dependent.

Power supply performance parameters:
The performance of the overall power supply is judged by specifying some parameters based on the factors given below:

1) **Load Regulation:**

   The load regulation is the change in the regulated output voltage when the load current is changed from no load to full load.

   The load regulation is denoted as LR which is given as:

   \[
   LR = V_{NL} - V_{FL}
   \]

   Where \( V_{NL} \) – load voltage with no load current

   \( V_{FL} \) - load voltage with full load current

   \[
   \%LR = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100
   \]

2) **Line Regulation or Source Regulation:**

   \[
   \]
The line regulation is also called as source regulation. The source regulation is defined as the change in the regulated load voltage for a specified range of line voltage, typically $230V \pm 10\%$.

Mathematically it can be expressed as:

$$SR = V_{HL} - V_{LL}$$

Where $V_{HL}$ – load voltage with high line voltage

$V_{LL}$ - load voltage with low line voltage

The percentage source regulation is defined as,

$$\%SR = \frac{V_{HL} - V_{LL}}{V_{nom.}} \times 100$$

Where, $V_{nom.}$ is the nominal value of load voltage.

3) **Output Resistance:**

Ideally for a power supply circuit $R_{out}$ must be zero and $V_{out}$ must be equal to $V_{NL}$ for whatever value of load current.

$$R_{out} = \frac{\Delta V_{out}}{\Delta I_L}$$

Vin. Temp. Constant

4) **Voltage stability factor ($S_v$) :**

It is defined as the percentage change in the output voltage which occurs per volt change in the input line voltage, with load current and the temperature are assumed constant. Mathematically it can be expressed as

$$S_v = \frac{\Delta V_{out}}{\Delta V_{in}}$$

$I_L$ and Temp. are constant.

Smaller the value of this factor better is the performance of power supply.

5) **Temperature Stability factor ($S_T$):**

The temperature stability of power supply will be determined by temperature coefficients of various temperature sensitive semiconductor devices. Mathematically, it can be expressed as

$$S_T = \frac{\Delta V_{out}}{\Delta T}$$

$I_L$ and $V_{in}$ are constant.
6) Ripple Rejection (RR):

The ripple rejection is a factor, which indicates how effectively the regulator circuit rejects the ripples, and attenuates it from input to output. If $V_R$ is the ripple voltage then the ripple rejection factor is defined as,

$$RR = \frac{\text{Ripple content in output}}{\text{Ripple content in input}} = \frac{V_{R(out)}}{V_{R(in)}}$$

Usually, this factor is expressed in decibel units as

$$RR' = 20 \log_{10} RR \text{ dB}$$

11. Explain the components of basic voltage regulator and types of a Voltage regulator circuits?

The components of a basic regulator circuit are:
- Voltage reference element $V$
- Error amplifier
- Feedback network
- Active series or shunt control element

The voltage reference generates a voltage level, which is applied to the comparator circuit, which is generally error amplifier. The second input to the error amplifier is obtained through feedback network. The error amplifier converts the difference between the output sample and the reference voltage into an error signal. This error signal in turn controls the active element of the regulator circuit, in order to compensate the change in the output voltage. Such an active element is generally a transistor. Thus the output voltage of the regulator is maintained constant.

Based on the location of the control element, the voltage regulator circuit is classified into – shunt and series voltage regulator.
Shunt voltage regulator:

In shunt voltage regulator circuit, the control element is located or connected in parallel to the load as shown in figure below:

\[ V_{in} = I_L + I_{sh} \quad \text{(Unregulated)} \quad \text{Control element} \quad \text{Sampling circuit} \quad \text{Comparator circuit} \quad \text{Feedback signal} \quad \text{Load} \quad V_o \]

It can be seen from the block diagram that only part of the load current to be diverted passes through the control element. Thus the control element is low current, high voltage rating component. The efficiency depends on the load current \( I_L \). Hence shunt regulators are not preferred for varying load conditions.

**Series voltage regulator circuit:**

In series voltage regulator circuit, the control element is located or connected in series to the load as shown in figure below:

\[ V_i \quad \text{Unregulated} \quad \text{Control signal} \quad \text{Control element} \quad \text{Sampling circuit} \quad \text{Feedback signal} \quad \text{Load} \quad V_o \]

In series regulators, the entire current passes through the control element and hence control element is high current, low voltage rating component. As input current...
and load current are same, the efficiency depends on output voltage. It provides good regulation than shunt regulators. It can be used for fixed voltage as well as variable voltage requirements. To compensate for the drop across the series control element, input voltage \( V_{\text{in}} \) must be at least 2 to 3V more than the desired output voltage.

12. Give the comparison between the series and shunt voltage regulators.

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Shunt Regulator</th>
<th>Series Regulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>The control element is in parallel with the load</td>
<td>The control element is in series with the load</td>
</tr>
<tr>
<td>2</td>
<td>Only small current passes through the control element, which is required to be diverted to keep output constant</td>
<td>The entire load current ( I_L ) always passes through the control element</td>
</tr>
<tr>
<td>3</td>
<td>Any change in output voltage is compensated by changing the current ( I_{\text{sh}} ) through the control element as per the control signal</td>
<td>Any change in output voltage is compensated by changing the voltage across the control element as per the control signal</td>
</tr>
<tr>
<td>4</td>
<td>The control element is low current, high voltage rating component</td>
<td>The control element is high current, low voltage rating component</td>
</tr>
<tr>
<td>5</td>
<td>The regulation is poor</td>
<td>The regulation is good</td>
</tr>
<tr>
<td>6</td>
<td>Efficiency depends on load current</td>
<td>Efficiency depends on the output voltage</td>
</tr>
<tr>
<td>7</td>
<td>Not suitable for variable load conditions and preferred for fixed load conditions</td>
<td>Preferred for fixed as well as variable load conditions</td>
</tr>
<tr>
<td>8</td>
<td>Simple to design</td>
<td>Complicated to design as compared to shunt regulators</td>
</tr>
<tr>
<td>9</td>
<td>Eg:- Zener shunt regulator, transistorized shunt regulator, etc</td>
<td>Eg:- Series feedback type regulator, series regulator with pre-regulator and fold back limiting, etc.</td>
</tr>
</tbody>
</table>
13. Give the comparison between rectifier and regulator

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Rectifier</th>
<th>Regulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>It converts pure sinusoidal input into pulsating dc output</td>
<td>It converts the pulsating dc input into constant dc output.</td>
</tr>
<tr>
<td>2</td>
<td>The output contains ripples</td>
<td>The output is ripple free</td>
</tr>
<tr>
<td>3</td>
<td>Output voltage changes with respect to load current, input</td>
<td>Output voltage does not change with respect to load current, input voltage and temperature</td>
</tr>
<tr>
<td></td>
<td>voltage and temperature</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Uses the devices which are diodes</td>
<td>Uses the devices such as transistors, operational amplifiers, etc</td>
</tr>
<tr>
<td>5</td>
<td>Not provided with overload protection, short circuit protection, thermal shutdown, etc</td>
<td>Provided with all sorts of protection circuits</td>
</tr>
<tr>
<td>6</td>
<td>Eg. – Half wave and full wave rectifiers</td>
<td>Eg.- Zener regulator, transistorized regulator, etc</td>
</tr>
</tbody>
</table>

14. Explain in detail the operation of transistorized series voltage regulator circuit along with the protection circuits?

The basic series voltage regulator called emitter follower series voltage regulator is shown in fig.

Below:

The transistor Q₁ is the series control element while Zener diode D is the reference voltage provider. The Zener diode is reverse biased so that it works in the breakdown region. Zener is connected in the base of Q₁ while the load is connected in the emitter of Q₁. The base emitter junction is always forward biased.
Operation:

From the fig. Above, we can write $V_o = V_z - V_{BE}$ \hspace{1cm} (1)

Applying KVL to the input side $V_{in} = V_{CE} + V_o$ \hspace{1cm} (2)

$V_{CE} = V_{in} - V_o$ \hspace{1cm} (3)

So the difference between the input and output voltages is equal to the drop across the transistor $Q_1$.

The emitter current is equal to the load current. So transistor $Q_1$ is in series with the load. Thus the transistor passes the load current and hence called series pass transistor.

If the output voltage decreases, as $V_z$ is constant, it can be seen from equation (2) that the base emitter voltage $V_{BE}$ increases. Thus the transistor $Q_1$ conducts more thereby raising the output voltage, maintaining the output constant. Thus the transistor acts as the controlling element.

For the transistor $Q_1$ we can write $I_E = I_C + I_B$ \hspace{1cm} (3)

As $I_B$ is very small, $I_E \sim I_C$. But the emitter current is same as the load current $I_L$.

$I_E = I_C = I_L$ \hspace{1cm} (4)

Now $I_B = \frac{I_C}{\beta} = \frac{I_L}{\beta}$ \hspace{1cm} (5)

If $I_z$ is the Zener current and $I_R$ is the current through resistance $R$ then

$I_z = I_R - I_B$ \hspace{1cm} (6)

The load current may be calculated from $I_L = (V_o/R_L)$

Power Dissipation:

As the collector current is almost equal to the load current and the voltage across the transistor $V_{CE}$, the product of $V_{CE}$ and $I_L$ gives the power dissipation in the transistor.

$P_D = V_{CE}I_L = (V_{in} - V_o)I_L$

The power dissipation will be maximum when the output terminals are shorted. In such case $V_o = 0$ V and $I_L = I_{SC}$ called short circuit current.

Under this condition due to large power dissipation the transistor may get damaged.

Disadvantages of emitter follower series voltage regulator:

i) There is no provision to vary the output voltage. The output is equal to the zener voltage which is constant. If we want the larger output voltage, the zener must be replaced
ii) The changes in $V_{BE}$ and $V_z$ due to changes in temperature appear at the output.

iii) Due to large power dissipation, heat sink is necessary which makes the circuit bulky.

To avoid the above limitations, a modified emitter follower series circuit called transistorized series feedback type regulator is used.

**Transistorised Series feedback type regulator:**

The modified version of emitter follower series voltage regulator circuit is shown in fig. Below:

The transistor $Q_2$ is connected to the base of $Q_1$. In the collector of $Q_2$ we have a resistance $R_3$ while in the emitter there is a zener diode with current limiting resistance $R$. The transistor $Q_2$ and its associated components constitute the error amplifier, which amplifies the change in the output voltage, which in turn controls the series-pass transistor $Q_1$. The emitter of $Q_2$ is always at a constant reference voltage due to the zener diode. The base of the transistor $Q_2$ is supplied with the potential divider consisting of $R_1$ and $R_2$, across the output side. It is compared with the reference voltage provided by the zener diode which is $V_z$. The current through the resistance $R_3$, splits into two currents namely $I_{B1}$, the base current of $Q_1$ and $I_{C2}$ i.e. the collector current of $Q_2$.

For the circuit shown in fig. Above, we can write:

The current through the resistance $R_1$ and $R_2$ is $I$ neglecting the base current $I_{B2}$.

\[ I = \frac{V_0}{R_1 + R_2} \quad \text{-- (1)} \]

Now the voltage of base with respect to ground is $V_{B2} = I R_2$.
\[ \frac{R_2}{R_1 + R_2} \]  

The emitter of \( Q_2 \) is at a constant voltage \( V_z \) due to the zener diode

\[ V_{BE2} = \frac{R_2}{R_1 + R_2} (V_o - V_z) \]  

Expression for output voltage:

From Fig. Above, the output voltage is \( V_o = V_{BE1} + V_{BE2} + V_z \)  

The current \( I \) through the resistance \( R_1 \) and \( R_2 \) neglecting \( I_{E2} \) is given by eqn (1)

\[ I = \frac{V_o}{R_1 + R_2} \]

\[ V_{BE1} = IR_1 \]

\[ = \frac{R_1}{R_1 + R_2} V_o \]  

Substituting in equation (4) we get,

\[ V_o = \frac{R_1}{R_1 + R_2} (V_o + V_{BE1} + V_z) \]

Rearranging we get,

\[ V_o = \left( \frac{1}{R_1 + R_2} \right) \left( V_{BE2} + V_z \right) \]

This is the required expression for the output voltage. An important advantage of the above circuit is that by using a potentiometer instead of fixed resistances \( R_1 \) and \( R_2 \), the ratio \( R_1 / R_2 \) can be varied.

As \( V_z \) is constant, the above equation states that as the load voltage changes, \( V_{BE} \) for \( Q_2 \) also changes.

Protection Circuit:

The series regulator using transistors has no short circuit protection. If the load terminals are shorted accidentally then,

i) Large amount of load current will flow.  
ii) The series pass transistor \( Q_1 \) will get destroyed  
iii) The diodes used in unregulated power supply, supplying the input voltage \( V_{in} \) to regulator circuit may get destroyed.

To avoid from above some sort of current limiting must be provided to the series regulator. The various protection circuits used for the series voltage regulators are:

1) Constant current limiting  
2) Fold back current limiting  
3) Over voltage protection  
4) Thermal Shutdown
1. Constant current limiting:

In power supply special load current limiting circuits are necessary because the ordinary fuse acts too slowly to protect semiconductor devices. A typical current limiter circuit which may precede the voltage regulator circuit and follow the filter circuit as shown in fig.

The value of \( R_{B1} \) is so chosen so that for normal load current the device \( T_2 \) is off because the voltage drop across the resistor is less than the minimum value of \( V_{BE} \approx 0.7 \text{V} \) needed to turn on the device. Only if the load current becomes excessive will the transistor conduct and this can be utilized to limit the output current of the resistor.

With normal load current through \( R_2 \), \( T_2 \) is off because of an insufficient voltage drop across its base emitter junction. If an overload occurs \( T_2 \) conducts and limits base current of \( T_1 \) which in turn limits the output current.

2. Fold back current limiting:
1. The previous current limiting techniques, the current is restricted to a maximum constant value. The feedback current limiting is a method used particularly in high current regulators, thus the output current under overload or short circuit condition drops to a value well below the maximum load current capability to prevent excessive power dissipation.

2. This method uses the variation of output voltage and it varies the load current accordingly. If the load current is small, there is no need for limiting. But if it increases beyond a maximum then it should be limited.

3. If the load resistance decreases, the drop across it also decreases. This drop in the voltage is sensed and is used to further decrease the amount of current flowing to the load.

4. If the load becomes a short circuit, output voltage and current approaches a new value as shown in the fig.

5. In this circuit, the potential R3 and R4 with T2 acts as a current limiting device. If the load varies, it affects the voltage across R3 because the potential divider R3 and R4 is parallel with R1R2, which is connected across output.

6. So if VL increases VR3 also increases, we know VBE = \(VR3C - VR3\) if VBE = 0.7 V. T2 starts conducting as a result of it limits the current flowing through RL. This continues until the load resistance reaches to its nominal value.
3. Over voltage protection:

A practical regulator circuit has to be always protected against short circuit overload such an arrangement with regulator is shown in fig.

1. The protection circuit uses a small sensing resistance \( R_{CC} \) is added in series with the load resistance and two diodes are connected between the bases of the transistor to the output. The diodes normally remain off condition.

2. When output terminals are overloaded or short circuited then the current through the transistor \( Q_1 \) increases. This increase in voltage drop across the sensing resistor \( R \). So now diodes start conducting.

3. The maximum current flow through \( T_1 \) under short circuit condition is 

\[
I = \frac{2V_d-V_{BE}}{R}
\]

As a result of this there is no further increase in current through the resistance ‘\( R \)’ or through the transistor \( T_1 \). So \( T_1 \) is protected from being damaged

4. The protective circuits can be replaced by another transistor \( T_2 \) as shown in fig. above. In this case the voltage across \( R_{CC} \) is used in turning ON transistor \( T_2 \) and direct the excess current to pass through it.

4. Thermal shutdown:
Thermal shutdown protection is very much necessary because due to self-heating it is possible that the series pass element may get damaged permanently. Such a protection prevents the junction temperature to rise above a safe limiting value. This limiting safe value of junction temperature is 175°C or less.

In this protection scheme, the junction temperature of the series pass element is sensed. By sensing this, its power dissipation is reduced till its temperature drops to a safe value. The thermal shutdown protection circuit is shown in Fig. above.

The transistors Q₂ and Q₃ form a Darlington pair which acts as series pass element. The diode D₂ is the zener diode. It is biased into reverse biased breakdown region with the help of current source I₁. The voltage V₂ produces a bias voltage for Q₄ and Q₅. The transistor Q₅ is off during normal thermal conditions. The resistance ratio R₅ and R₆ is such that at normal temperature the base emitter voltage of Q₅ is not large enough to make Q₅ ON. The zener diode has positive temperature coefficient. As temperature increases, V₂ increases. Hence the resistance R₅ and R₆ provides the enough bias to make Q₅ ON. As Q₅ is turned ON, it shunts current away from Q₁’s base, thus reducing Q₁’s power dissipation. This continues till temperature drops below the safe value. For fast and reliable operation, the transistor Q₅ must have excellent thermal coupling with Q₁.

15. What are the limitations of linear mode power supply?

The linear mode power supply has following limitations.

a) The input step-down transformer is bulky and most expensive component because its operating frequency is very low (say 50Hz). Because of this frequency, large value of filter capacitor is required to decrease the ripple.

b) The efficiency is very low because the difference between the input and output is very high, resulting in which the power dissipation will be more across series pass transistor.

c) The linear mode power supply requires additional ±15V dc source to operate the active device such as op-amp, it may not be economically and practically feasible.

d) For a specified range of input-output variation linear regulators maintain constant output voltage by dissipating the excess power as heat due to this reasons, the linear voltage regulators is suited for medium current applications.

The above problems are overcome using Switched mode power supply (SMPS) are used.
16. Explain the block diagram representation of basic switching regulator

In linear mode power supply, the series pass transistor operates in the active region but in a switching regulator, the series pass transistor is switched between cut-off and saturation at a high frequency which produces a pulse width modulated (PWM) square wave output. This output is filtered through a low pass LC filter to produce an average dc output voltage. Thus the output voltage is proportional to the pulse width and frequency. The efficiency of switching regulator is independent of the input-output voltage thus it approaches 95%. The block diagram representation of switching regulator is shown in fig. Below:

![Block diagram of basic switching regulator](image)

"Theory of switching regulators"

A basic switching regulator consists of four components:

1. **Voltage source:**

   It may be any dc supply - a battery or an unregulated or regulated voltage, it must satisfy the following requirements.

   a) It must supply the required output power and losses associated with the switching regulator.
b) It must be large enough to supply sufficient dynamic range for line and load variations.

c) It must be sufficiently high to meet the minimum requirements of the regulators.

d) It may be required to store energy for a specified amount of time during power failures.

2. Switch:

Typically a transistor or Thyristor is connected as a power switch and is operated in the saturated mode. The pulse generator output alternately turns the switch on and off. To improve the efficiency of a regulator, the series pass transistor is used as a switch rather than a variable resistor in the linear mode power supply. A regulator constructed to operate in this manner is known as series switching regulators.

3. Pulse generator:

It produces a symmetrical square wave varying in either frequency or pulse width called frequency or pulse width modulation. The frequency range of pulse generator for optimum efficiency is 20 KHz.

The duty cycle of the pulse waveform determines the relationship between the input and output voltages. The duty cycle is the ratio of the ON time to period ‘T’ of the pulse waveform i.e.,

\[
\text{Duty cycle} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{t_{ON}}{T}
\]

Where \( t_{ON} \) = on time of the pulse waveform.
\( t_{OFF} \) = off time of the pulse waveform.
\( T \) = time period = \( t_{ON} + t_{OFF} \) = \( \frac{1}{f} \)

There are some trades off between the operating frequency and efficiency. High operating frequency reduces the ripple voltage at the expense of decreased efficiency and increase the noise. On the other hand lower operating frequency improve the
efficiency and reduce the noise but ripple are high hence it requires large filter components.

4. Filter:
Filter converts the pulse from the output of the switch into a dc voltage. The RLC filter is most commonly used in the switching regulator.
The output voltage of switching regulator is a function of the duty cycle and the input voltage \( V_{in} \).

\[
\text{Duty cycle} = \frac{t_{ON}}{t_{ON} + t_{OFF}}
\]

In the above equation, if the time period ‘\( T \)’ is constant, \( V_o \) is directly proportional to the ON-time ‘\( t_{ON} \)’ for a given period of \( V_{in} \). This method of changing output voltage by varying \( t_{ON} \) is referred to as “pulse width modulation”.

Similarly if \( t_{ON} \) is held constant, the output voltage is inversely proportional to the period ‘\( T \)’ or directly proportional to frequency ‘\( f \)’ (i.e. \( =1/T \)) of pulse waveform, then it is known as “frequency modulation”.

**Need of Switched Mode Power Supply**
A linear regulator power supply has following limitations:
1. The required input step down transformer is bulky and expensive.
2. Due to low line frequency (50 Hz), large values of filter capacitors are required.
3. The efficiency is very low.
4. Input must be greater than the output voltage.
Pulse width modulation wave form:

17. Explain the types of switching regulators.

There are three basic configurations:

1. Step down switching regulator (Buck)
2. Step up switching regulator (Boost)
3. Inverted switching regulator (Buck – Boost)

1) Step down switching regulator (Buck):

It is shown in figure above that, when a rectangular pulse is applied on the base terminal, it will saturate and cutoff the pass transistor depending on the ON and OFF period of each cycle. This produces the rectangular pulses at the input to LC filter.
This filter blocks the ac component but passes the dc component to the output. Because of the ON-OFF switching the average value is always less than the input voltage. Thus it is known as “Step down switching regulator”.

A diode is connected from emitter to ground, it is necessary because of inductive kickback. An inductor will try to keep the current through it constant. When the transistor is cut-off, the diode continues to provide a path for current through the inductor. Without the diode, the inductive kickback would provide enough reverse voltage to destroy the transistor.

During the OFF time of $T_1$ the diode $D$ is forward biased and allowing the capacitor to charge. The variation in the output voltage due to charging and discharging action are sufficiently smoothed by the filtering action of $L$ and $C$.

Advantages:
- Higher efficiency
- Simple to design
- Low ripple content
- Small output filter
- Low switch stress
Large tolerance of line voltage regulation
Low cost, size and weight

Disadvantages:
- Single output
- No isolation between input and output
- High input ripple content
- The input voltage must be always slightly greater than output
- Slow transient response compared to linear regulator
- Due to finite reverse recovery time of commutating diode, the instantaneous short circuit occurs across the source, due to which active switches may fail.

2) Step up switching regulator (Boost):

Fig. Above shows the step up switching regulator. The transistor is alternately saturated and cut off. When the transistor is saturated, current flows through the inductor and it expands its magnetic field. When the transistor enters to cut-off region, the magnetic field around the coil collapses and induces a large voltage across the coil of opposite polarity. This keeps the current flowing in the same direction, so that its voltage adds to V_{in}, thus producing an output voltage greater than the input thus it is known as “Step up voltage regulator.”
Advantages:

- The output voltage is higher than input voltage
- The efficiency is high, greater than 90%
- Low input ripple content
- Simple to design

Disadvantages:

- It provides single output.
- The duty cycle is limited to 50% to avoid the continuous current mode. If regulator enters the continuous current mode, it stops regulating the output. Thus for a minimum input voltage range, maximum duty cycle is limited.
- Due to restricted duty cycle, the peak collector current is very high. This limits its output rating.
- No isolation between input and output. Any surge or transient in input can reach to output directly.

3) Inverted Switching Regulator:

![Diagram of Inverted Switching Regulator](image)

Figure above shows the inverting regulator. When the transistor is saturated, current flows through the inductor and sets up the magnetic field around the coil. When the transistor is cut-off, the magnetic field collapses and the inductive kickback keeps
current flowing in the same direction, this makes the diode becomes forward biased and permits capacitor charges to a maximum value, the only path is through the capacitor. The output voltage is measured across the capacitor is negative in magnitude thus it is known as “Inverted switching regulator”.

18. Explain the power control of SCR.

The SCR is an unidirectional device and like diode, it allows to flow current in only one direction. But unlike diode, it has a built in feature to switch ON and OFF. The switching of SCR is controlled by the additional input is called gate and biasing conidian.

There are two types of controlling device
- DC power controlling using SCR
- AC power controlling using SCR

- DC power controlling using SCR

The SCRs conduct in one direction hence can be used in the rectifier circuits. And controlling the instant of turning ON the SCR, the average power delivered to the load also can be controlled.

1. Single phase half wave rectifier: The Fig. 9.65 shows circuit for single phase half wave rectifier using SCR. As shown in the Fig. 9.65, triggering circuit consists of a diode and resistor in series with the gate. By changing resistor R it is possible to change gate current at specific point on the sine wave. Recall that the SCR is a current operated device and it is the gate current (injected carriers) that turns on the SCR.

Therefore by changing resistor R, the point on the sine wave at which the SCR fires can be changed, as shown in the Fig. This makes it possible to change the average power delivered to the load.

In the negative half of cycle, SCR is in the reverse blocking state. The diode D1 in the gate circuit blocks the reverse voltage on the gate.

As shown in the Fig. α is a firing angle and ϕ is a conduction angle. With this gate circuit maximum firing angle we can get is 90°.
2. Single phase full wave rectifier.

In full wave rectifier both positive and negative half of ac supply is used and hence the average value of the dc voltage is high and ripple content is less compared to half wave rectifiers. There are two possible circuits arranging for obtaining full wave rectifiers.

- Using center tapped transformer
- Using bridge rectifier

Full wave rectifier with center tapped transformer

The Fig. 9.67 shows the full wave rectifier using center tapped transformer. Here, SCR1 and SCR2 conduct during positive and negative half cycle, respectively. For pure resistive load, average and rms values of the output voltage can be derived as

\[
V_{dc(\text{av})} = \frac{1}{2\pi} \int_{0}^{2\pi} V_o (\omega t) \, dt = 2 \times \frac{1}{2\pi} \int_{0}^{2\pi} V_m \sin (\omega t) \, dt
\]

\[
\therefore V_{dc(\text{av})} = \frac{V_m}{\pi} (1 + \cos \alpha)
\]

And

\[
V_{\text{rms}} = \left[ 2 \times \frac{1}{2\pi} \int_{0}^{\pi} V_m \sin (\omega t)^2 \, dt \right]^{1/2} = \left[ \frac{V_m}{2\pi} \int_{0}^{\pi} (1 - \cos(2\omega t)) \, dt \right]^{1/2}
\]

\[
\therefore V_{\text{rms}} = V_m \left[ \frac{\pi - \alpha}{2\pi} + \frac{\sin 2\alpha}{4\pi} \right]^{1/2}
\]

The average load power is given by,

\[
P_L(\text{av}) = V_{dc(\text{av})} \times I_{dc(\text{av})} = \left[ \frac{V_{dc(\text{av})}}{R_L} \right]^2 = \left[ I_{dc(\text{av})} \right]^2 R_L \, \text{W}
\]
Wave rectifier with a bridge configuration

The Fig. shows the full wave rectifier using bridge configuration. Here, instead of center tapped transformer four SCRs are used. SCR1 and SCR3 conduct during positive half cycle and SCR2 and SCR4 conduct during negative half cycle.

The Fig. shows the output voltage and current waveform of full wave rectifier with resistive load.
AC Power Control Using SCR

The Fig. shows the simplified circuit for ac power control. Here, two SCRs are connected in antiparallel way. SCR$_1$ is forward biased during the positive half cycle and SCR$_2$ is forward biased during negative half cycle. The firing angle, $\alpha$ for both the SCRs is controlled by gate circuit in their respective half cycles.

Waveforms

The output ac power is inversely proportional to the firing angle.
19. Explain about the Zener diode regulator.

**Zener diode as a shunt regulator**

The simplest shunt voltage regulator circuit uses a zener diode, to regulate the load voltage. The Fig. shows the arrangement of zener diode in a regulator circuit.

**V-I characteristics of zener diode**

To understand the working of the circuit, let us revise the V-I characteristics of a zener diode, as shown in the Fig.

The zener diode is used in its reverse biased region. Under reverse biased condition, the current through the diode is very small of the order of few μA, upto certain limit. When the sufficient reverse bias is applied, electrical breakdown of the zener diode occurs. The large current flows through the zener diode. Such a breakdown occurs at a voltage called zener voltage $V_Z$. Under this condition, whatever may be the current, the voltage across the zener is constant equal to $V_Z$. Thus zener diode acts as an ideal voltage source which maintains a constant load voltage, independent of the current.

**Regulation With Varying Input Voltage**

The Fig. shows a zener regulator under varying input voltage condition.

It can be seen that the output is

$$V_o = V_Z \text{ is constant.}$$

$$\therefore \quad I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L} = \text{constant}$$

And $I = I_Z + I_L$

Now if $V_{in}$ increases, then the total current $I$ increases. But $I_L$ is constant as $V_Z$ is constant. Hence the current $I_Z$ increases to keep $I_L$ constant.

But as long as $I_Z$ is between $I_{Z_{min}}$ and $I_{Z_{max}}$, the $V_Z$, i.e. output voltage $V_o$ is constant. Thus the changes in input voltage get compensated and output is maintained constant.

Similarly if $V_{in}$ decreases, then current $I$ decreases. But to keep $I_L$ constant, $I_Z$ decrease. As long as $I_Z$ is between $I_{Z_{max}}$ and $I_{Z_{min}}$, the output voltage remains constant.
Steps to Analyse Zener Regulator with Varying Input

The steps are,

1. Calculate the load current which is constant

\[ I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L} \]

2. To find \( V_{in(min)} \), the current through zener must be \( I_{Z_{min}} \) to keep it reverse biased.

\[ I = I_L + I_{Z_{min}} \]
\[ V_{in(min)} = V_Z + I \times R \]

3. To find \( V_{in(max)} \), the current through zener must be maximum equal to \( I_{Z_{max}} \).

\[ I = I_L + I_{Z_{max}} \]
\[ V_{in(max)} = V_Z + I \times R \]

4. Hence the range of input is \( V_{in(min)} \) to \( V_{in(max)} \) for which output will be constant equal to \( V_Z \).

Using the same steps, for given \( V_{in} \) range the resistance values can be obtained and zener regulator can be designed.

The maximum power dissipation in the zener diode is given by,

\[ P_D = V_Z \times I_{Z_{max}} \]

The zener diode must be selected with power dissipating rating higher than \( P_D \).

Regulation with a Varying Load

The Fig. shows a zener regulator with a variable load resistance. This is also referred to as load regulation.

The zener diode maintains a constant voltage across \( R_L \) as long as the zener current is greater than \( I_{Z_{min}} \) and less than \( I_{Z_{max}} \). When the load current varies, the zener diode current adjusts itself so that its terminal voltage remains constant. For example, if \( I_{Z_{min}} = 5 \) mA, \( I_{Z_{max}} = 50 \) mA, \( V_Z = 10 \) and \( V_{in} = 20 \) V then at no load \( R_L = \infty \) and \( I_i = 0 \).

Therefore to limit maximum current to 50 mA (\( I_{Z_{max}} \))

\[ R_{(min)} = \frac{V_{in} - V_Z}{I_{Z_{max}}} = \frac{20V - 10V}{50mA} \]
\[ = 200 \Omega \]

As you know \( I_{Z \, min} = 5 \) mA, the maximum load current is 45 mA (\( 50 - 5 \)). This shows that the zener diode in this circuit can maintain output voltage constant for load current from 0 mA to 45 mA.