UNIT 4 MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIER

UNIT 5

FEED BACK AMPLIFIERSAND OSCILLATORS

EC8353 Electronic Devices And Circuits
Syllabus

Class/Sem: II EEE /III Sem

Unit I PN JUNCTION DEVICES 9

PN junction diode –structure, operation and V-I characteristics, diffusion and transient capacitance - Rectifiers – Half Wave and Full Wave Rectifier,– Display devices- LED, Laser diodes- Zener diode- characteristics-Zener Reverse characteristics – Zener as regulator

Unit II TRANSISTORS 9

BJT, JFET, MOSFET- structure, operation, characteristics and Biasing UJT, Thyristor and IGBT - Structure and characteristics.

Unit III AMPLIFIERS 9

BJT small signal model – Analysis of CE, CB, CC amplifiers- Gain and frequency response – MOSFET small signal model– Analysis of CS and Source follower – Gain and frequency response- High frequency analysis.

Unit IV MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIER 9

BIMOS cascade amplifier, Differential amplifier – Common mode and Difference mode analysis – FET input stages – Single tuned amplifiers – Gain and frequency response – Neutralization methods, power amplifiers –Types (Qualitative analysis).

Unit V FEEDBACK AMPLIFIERS AND OSCILLATORS 9

Advantages of negative feedback – voltage / current, series , Shunt feedback –positive feedback – Condition for oscillations, phase shift – Wien bridge, Hartley, Colpitts and Crystal oscillators.

Total (L:45+T:15): 60 Periods

Text Books:

1. DAVid A. Bell ,"Electronic Devices and Circuits", Prentice Hall of India, 2004.
2. Sedra and smith, "Microelectronic Circuits " Oxford University Press, 2004.

UNIT I PN JUNCTION DEVICES

1.1 SEMICONDUCTOR

A semiconductor is a material which has electrical conductivity to a degree between that of a metal (such as copper) and that of an insulator (such as glass). Semiconductors are the foundation of modern electronics, including transistors, solar cells, light-emitting diodes (LEDs), quantum dots and digital and analog integrated circuits.

DIODE

Diode – Di + ode

Di means two and ode means electrode. So physical contact of two electrodes is known as diode and its important function is alternative current to direct current.

1.2 REVIEW OF INTRINSIC AND EXTRINSIC SEMICONDUCTORS

1.2.1 INTRINSIC SEMICONDUCTOR

An intrinsic semiconductor is one, which is pure enough that impurities do not appreciably affect its electrical behaviour. In this case, all carriers are created due to thermally or optically excited electrons from the full valence band into the empty conduction band. Thus equal numbers of electrons and holes are present in an intrinsic semiconductor. Electrons and holes flow in opposite directions in an electric field, though they contribute to current in the same direction since they are oppositely charged. Hole current and electron current are not necessarily equal in an intrinsic semiconductor, however, because electrons and holes have different effective masses (crystalline analogues to free inertial masses).

The concentration of carriers is strongly dependent on the temperature. At low temperatures, the valence band is completely full making the material an insulator. Increasing the temperature leads to an increase in the number of carriers and a corresponding increase in conductivity. This characteristic shown by intrinsic semiconductor is different from the behaviour of most metals, which tend to become less conductive at higher temperatures due to increased phonon scattering.

Both silicon and germanium are tetravalent, i.e. each has four electrons (valence electrons) in their outermost shell. Both elements crystallize with a diamond-like structure, i.e. in such a way that each atom in the crystal is inside a tetrahedron formed by the four atoms which are closest to it. Each atom shares its four valence electrons with its four immediate neighbours, so that each atom is involved in four covalent bonds.

1.2.2 EXTRINSIC SEMICONDUCTOR

An extrinsic semiconductor is one that has been doped with impurities to modify the number and type of free charge carriers. An extrinsic semiconductor is a semiconductor that has been *doped*, that is, into which a doping agent has been introduced, giving it different electrical properties than the intrinsic (pure) semiconductor.

Doping involves adding doping atoms to an intrinsic semiconductor, which changes the electron and hole carrier concentrations of the semiconductor at thermal equilibrium. Dominant

carrier concentrations in an extrinsic semiconductor classify it as either an n-type or p-type semiconductor.

A pure or intrinsic conductor has thermally generated holes and electrons. However these are relatively few in number. An enormous increase in the number of charge carriers can by achieved by introducing impurities into the semiconductor in a controlled manner. The result is the formation of an extrinsic semiconductor. This process is referred to as doping. There are basically two types of impurities: donor impurities and acceptor impurities. Donor impurities are made up of atoms (arsenic for example) which have five valence electrons. Acceptor impurities are made up of atoms (gallium for example) which have three valence electrons.

The two types of extrinsic semiconductor are

- **N-TYPE SEMICONDUCTORS**

Extrinsic semiconductors with a larger electron concentration than hole concentration are known as n-type semiconductors. The phrase 'n-type' comes from the negative charge of the electron. In n-type semiconductors, electrons are the majority carriers and holes are the minority carriers. N-type semiconductors are created by doping an intrinsic semiconductor with donor impurities.

In an n-type semiconductor, the Fermi energy level is greater than that of the intrinsic semiconductor and lies closer to the conduction band than the valence band. Arsenic has 5 valence electrons, however, only 4 of them form part of covalent bonds. The 5th electron is then free to take part in conduction. The electrons are said to be the majority carriers and the holes are said to be the minority carriers.

- **P-TYPE SEMICONDUCTORS**

As opposed to n-type semiconductors, p-type semiconductors have a larger hole concentration than electron concentration. The phrase 'p-type' refers to the positive charge of the hole. In p-type semiconductors, holes are the majority carriers and electrons are the minority carriers. P-type semiconductors are created by doping an intrinsic semiconductor with acceptor impurities. P-type semiconductors have Fermi energy levels below the intrinsic Fermi energy level.

The Fermi energy level lies closer to the valence band than the conduction band in a p- type semiconductor. Gallium has 3 valence electrons, however, there are 4 covalent bonds to fill. The 4^{th} bond therefore remains vacant producing a hole. The holes are said to be the majority carriers and the electrons are said to be the minority carriers.

1.3 PN JUNCTION DIODE

When the N and P-type semiconductor materials are first joined together a very large density gradient exists between both sides of the junction so some of the free electrons from the donor impurity atoms begin to migrate across this newly formed junction to fill up the holes in the P-type material producing negative ions.

1.3.1 FORWARD BIAS CONDITION

When positive terminal of the battery is connected to the P-type and negative terminal to N-type of the PN junction diode that is known as forward bias condition.

- **Operation**

The applied potential in external battery acts in opposition to the internal potential barrier which disturbs the equilibrium.

As soon as equilibrium is disturbed by the application of an external voltage, the Fermi level is no longer continuous across the junction.

Under the forward bias condition the applied positive potential repels the holes in P type region so that the holes move towards the junction and the applied positive potential repels the electrons in N type region so that the electrons move towards the junction.

When the applied potential is more than the internal barrier potential the depletion region and internal potential barrier disappear.

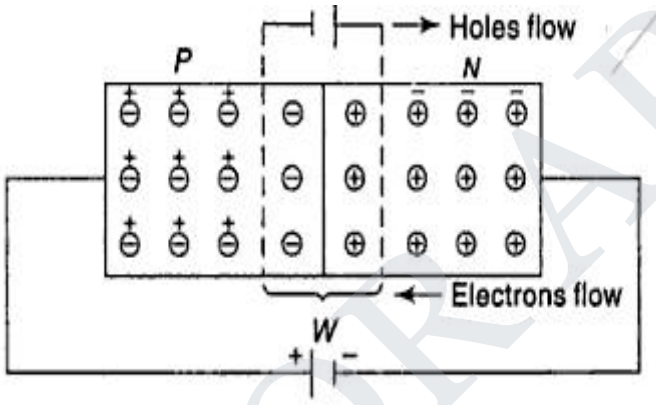
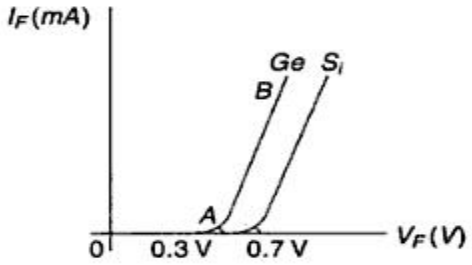


Figure PN junctions under forward bias

- **V-I Characteristics**

As the forward voltage increased for V_F < Vo, the forward current I_F almost zero because the potential barrier prevents the holes from P region and electrons from N region to flow across the depletion region in opposite direction.



V-I characteristics of a diode under forward bias

For V_F > Vo, the potential barrier at the junction completely disappears and hence, the holes cross the junction from P to N type and electrons cross the junction to opposite direction, resulting large current flow in external circuit.

A feature noted here is the cut in voltage or threshold voltage V_F below which the

current is very small. At this voltage the potential barrier is overcome and the current through the junction starts to increase rapidly.

- Cut in voltage is 0.3V for germanium and 0.7 for silicon.

1.3.2 UNDER REVERSE BIAS CONDITION

When the negative terminal of the battery is connected to the P-type and positive terminal to N-type of the PN junction diode that is known as forward bias condition.

- **Operation**

The holes from the majority carriers of the P side move towards the negative terminal of the battery and electrons which from the majority carrier of the N side are attracted towards the positive terminal of the battery.

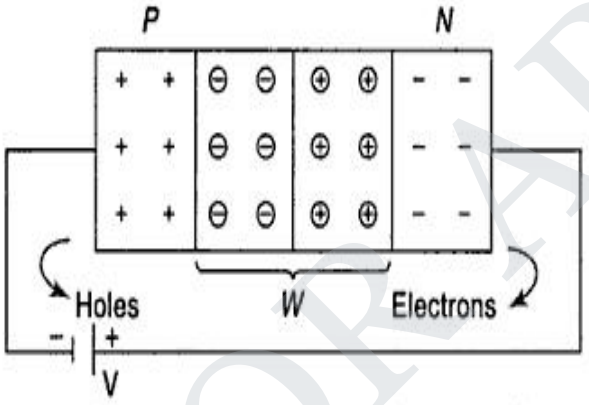


Figure PN junctions under reverse bias

Hence, the width of the depletion region which is depleted of mobile charge carriers increases. Thus, the electric field produced by applied reverse bias, is in the same direction as the electric field of the potential barrier.

Hence the resultant potential barrier is increased which prevents the flow of majority carriers in both directions. The depletion width W is proportional to under reverse bias.

- **V-I characteristics**

Theoretically no current flow in the external circuit. But in practice a very small amount of current of the order of few microamperes flows under reverse bias.

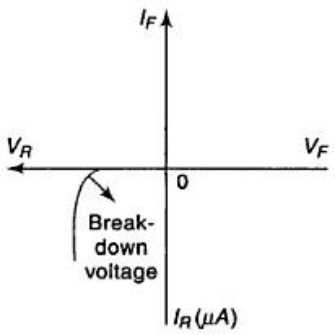


Figure V-I characteristics under reverse bias

Electrons forming covalent bonds of semiconductor atoms in the P and N type regions may absorb sufficient energy from heat and light to cause breaking covalent bonds. So electron hole pairs continuously produced.

Consequently the minority carriers electrons in the P region and holes in the N region, wander over to the junction and flow towards their majority carrier side giving rise a small reverse current. This current is known as reverse saturation current Io.

The magnitude of this current is depends on the temperature because minority carrier is thermally broken covalent bonds.

1.4 Transition capacitances:

1. When P-N junction is reverse biased the depletion region act as an insulator or as a dielectric medium and the p-type an N-type region have low resistance and act as the plates.
2. Thus this P-N junction can be considered as a parallel plate capacitor.
3. This junction capacitance is called as space charge capacitance or transition capacitance and is denoted as CT .
4. Since reverse bias causes the majority charge carriers to move away from the junction , so the thickness of the depletion region denoted as W increases with the increase in reverse bias voltage.
5. This incremental capacitance CT may be defined as
CT = dQ/dV,
Where dQ is the increase in charge and dV is the change or increase in voltage.
6. The depletion region increases with the increase in reverse bias potential the resulting transition capacitance decreases.
7. The formula for transition capacitance is given as CT = Aε/W, where A is the cross sectional area of the region, and W is the width.

1.5 Diffusion capacitance:

1. When the junction is forward biased, a capacitance comes into play , that is known as diffusion capacitance denoted as CD. It is much greater than the transition capacitance.
2. During forward biased the potential barrier is reduced. The charge carriers moves away from the junction and recombine.
3. The density of the charge carriers is high near the junction and reduces or decays as the distance increases.
4. Thus in this case charge is stored on both side of the junction and varies with the applied potential. So as per definition change in charge with respect to applied voltage results in capacitance which here is called as diffusion capacitance.
5. The formula for diffusion capacitance is CD = τID / ηVT , where τ is the mean life time of the charge carrier, ID is the diode current and VT is the applied forward voltage, and η is generation recombination factor.
6. The diffusion capacitance is directly proportional to the diode current.
7. In forward biased CD >> CT . And thus CT can be neglected.

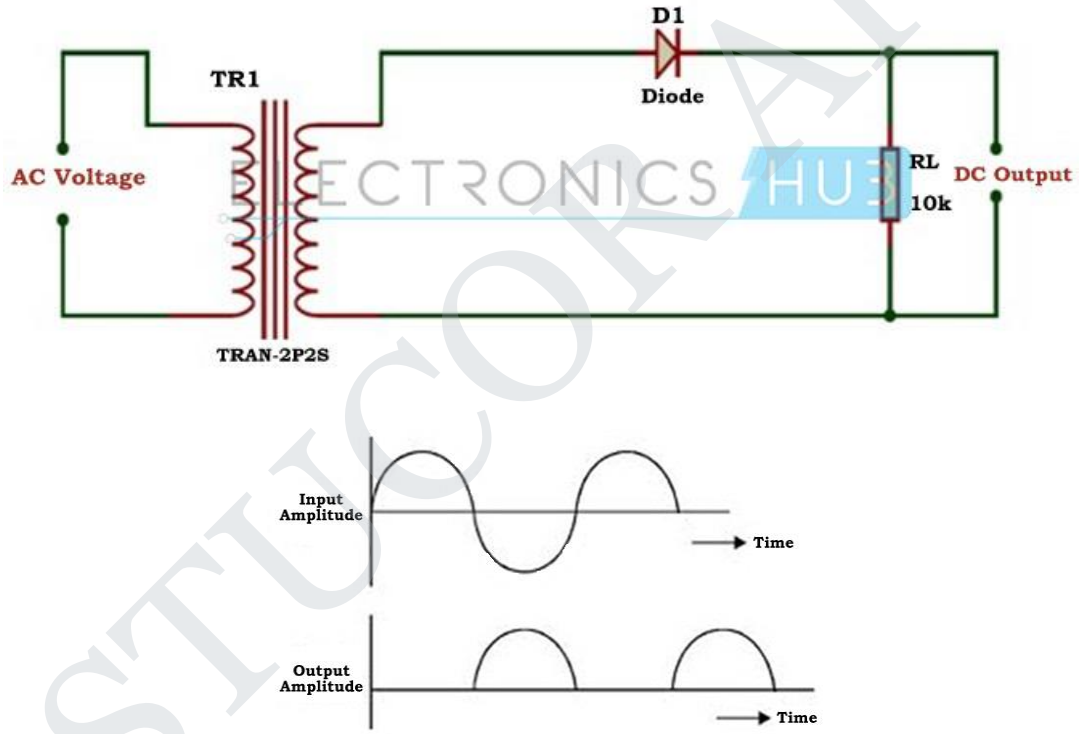
1.6 RECTIFIERS

Rectifiers are classified according to the period of conduction.
They are

- Half Wave Rectifier
- Full Wave Rectifier

1.6.1 Half Wave Rectifier:

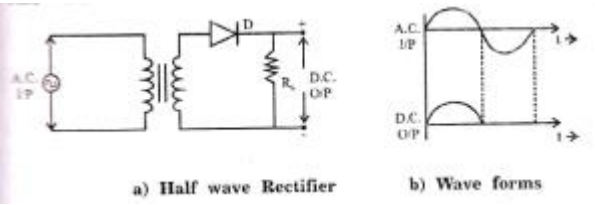
The half wave rectifier is a type of rectifier that rectifies only half cycle of the waveform. This describes the half wave rectifier circuit working. The half rectifier consist a step down transformer, a diode connected to the transformer and a load resistance connected to the cathode end of the diode. The circuit diagram of half wave transformer is shown below:



The main supply voltage is given to the transformer which will increase or decrease the voltage and give to the diode. In most of the cases we will decrease the supply voltage by using the step down transformer here also the output of the step down transformer will be in AC. This decreased AC voltage is given to the diode which is connected serial to the secondary winding of the transformer, diode is electronic component which will allow only the forward bias current and will not allow the reverse bias current. From the diode we will get the pulsating DC and give to the load resistance RL.

1.6.2 Working of Half Wave Rectifier:

The input given to the rectifier will have both positive and negative cycles. The half rectifier will allow only the positive half cycles and omit the negative half cycles. So first we will see how half wave rectifier works in the positive half cycles.



a) Half wave Rectifier b) Wave forms

➢ **Positive Half Cycle:**

- In the positive half cycles when the input AC power is given to the primary winding of the step down transformer, we will get the decreased voltage at the secondary winding which is given to the diode.
- The diode will allow current flowing in clock wise direction from anode to cathode in the forward bias (diode conduction will take place in forward bias) which will generate only the positive half cycle of the AC.
- The diode will eliminate the variations in the supply and give the pulsating DC voltage to the load resistance RL. We can get the pulsating DC at the Load resistance.

➢ **Negative Half Cycle:**

- In the negative half cycle the current will flow in the anti-clockwise direction and the diode will go in to the reverse bias. In the reverse bias the diode will not conduct so, no current in flown from anode to cathode, and we cannot get any power at the load resistance.
- Only small amount of reverse current is flown from the diode but this current is almost negligible. And voltage across the load resistance is also zero.

1.6.3 Characteristics of Half Wave Rectifier:

There are some characteristics to the half wave rectifier they are

➢ **Efficiency:** The efficiency is defined as the ratio of input AC to the output DC.
Efficiency, $\eta = P_{dc} / P_{ac}$

DC power delivered to the load, $P_{dc} = I^2_{dc} R_L = (I_{max/pi})^2 R_L$

AC power input to the transformer, P_{ac} = Power dissipated in junction of diode + Power dissipated in load resistance R_L

$= I^2_{rms} R_F + I^2_{rms} R_L = \{I^2_{MAX}/4\}[R_F + R_L]$

Rectification Efficiency, $\eta = P_{dc} / P_{ac} = \{4/ ^2\}[RL/ (R_F + R_L)] = 0.406/\{1+ R_{F/RL}\}$

If R_F is neglected, the efficiency of half wave rectifier is 40.6%.

- **Ripple factor:** It is defined as the amount of AC content in the output DC. It nothing but amount of AC noise in the output DC. Less the ripple factor, performance of the rectifier is more. The ripple factor of half wave rectifier is about 1.21 (full wave rectifier has about 0.48). It can be calculated as follows:

  The effective value of the load current I is given as sum of the rms values of harmonic currents I1, I2, I3, I4 and DC current Idc.
  $I^2 = I^2_{dc} + I^2_1 + I^2_2 + I^2_4 = I^2_{dc} + I^2_{ac}$

  Ripple factor, is given as $\gamma = I_{ac} / I_{dc} = (I^2 - I^2_{dc}) / I_{dc} = \{(I_{rms} / I_{dc}^2) - 1\} = K_f^2 - 1)$

  Where Kf is the form factor of the input voltage. Form factor is given as

  $K_f = I_{rms} / I_{avg} = (I_{max}/2)/ (I_{max}/pi) = pi/2 = 1.57$

  So, ripple factor, $\gamma = (1.57^2 - 1) = 1.21$

- **Peak Inverse Voltage:** It is defined as the maximum voltage that a diode can with stand in reverse bias. During the reverse bias as the diode do not conduct total voltage drops across the diode. Thus peak inverse voltage is equal to the input voltage Vs.

- **Transformer Utilization Factor (TUF):** The TUF is defined as the ratio of DC power is delivered to the load and the AC rating of the transformer secondary. Half wave rectifier has around 0.287 and full wave rectifier has around 0.693.

Half wave rectifier is mainly used in the low power circuits. It has very low performance when it is compared with the other rectifiers.

1.7 FULL WAVE RECTIFIER

Full wave rectifier rectifies the full cycle in the waveform i.e. it rectifies both the positive and negative cycles in the waveform. We have already seen the **characteristics and working of Half Wave Rectifier**. This Full wave rectifier has an advantage over the half wave i.e. it has average output higher than that of half wave rectifier. The number of AC components in the output is less than that of the input.

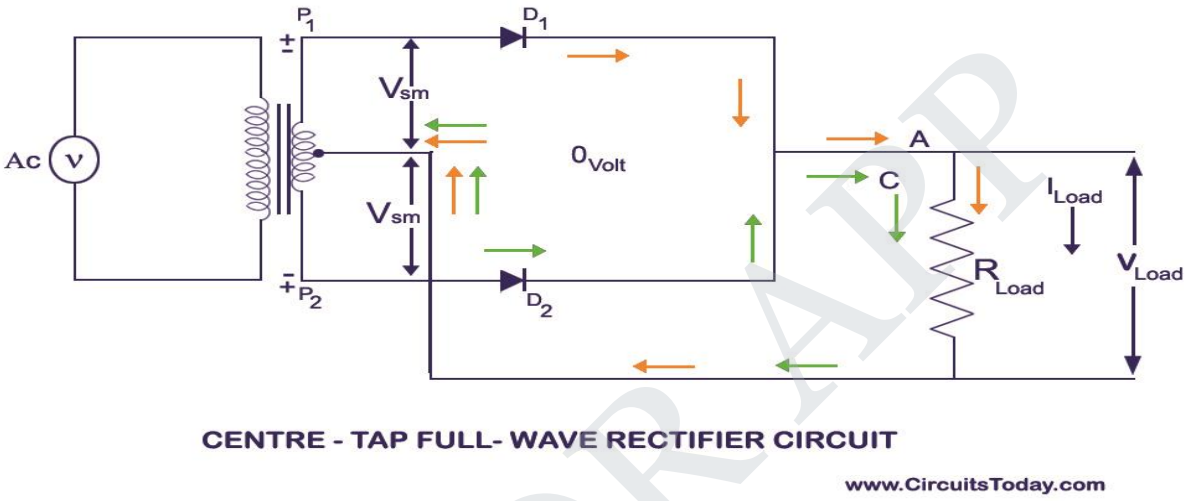
The full wave rectifier can be further divided mainly into following types.

1. Center Tapped Full Wave Rectifier
2. Full Wave Bridge Rectifier

1.7.1 Centre-Tap Full Wave Rectifier

We have already discussed the Full Wave Bridge Rectifier, which uses four diodes, arranged as a bridge, to convert the input alternating current (AC) in both half cycles to direct current (DC).

In the case of centre-tap full wave rectifier, only two diodes are used, and are connected to the opposite ends of a centre-tapped secondary transformer as shown in the figure below. The centre-tap is usually considered as the ground point or the zero voltage reference point.

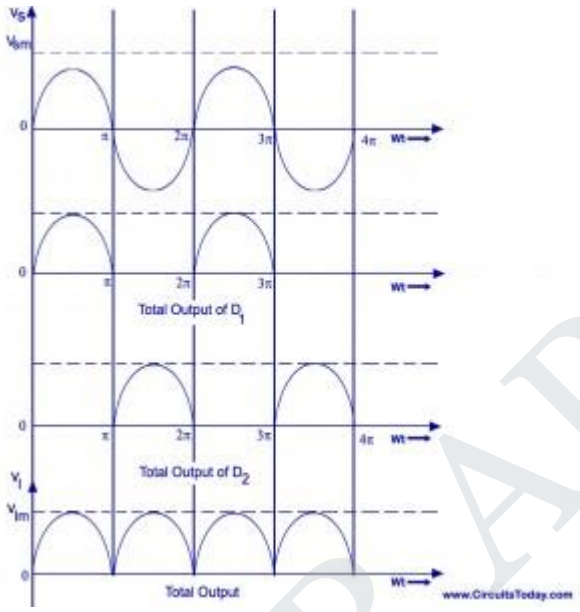


Centre Tap Full Wave Rectifier Circuit

- **Working of Centre-Tap Full Wave Rectifier**

As shown in the figure, an ac input is applied to the primary coils of the transformer. This input makes the secondary ends P1 and P2 become positive and negative alternately. For the positive half of the ac signal, the secondary point D1 is positive, GND point will have zero volt and P2 will be negative. At this instant diode D1 will be forward biased and diode D2 will be reverse biased. As explained in the Theory Behind P-N Junction and Characteristics of P-N Junction Diode, the diode D1 will conduct and D2 will not conduct during during the positive half cycle. Thus the current flow will be in the direction P1-D1-C-A-B-GND. Thus, the positive half cycle appears across the load resistance RLOAD.

During the negative half cycle, the secondary ends P1 becomes negative and P2 becomes positive. At this instant, the diode D1 will be negative and D2 will be positive with the zero reference point being the ground, GND. Thus, the diode D2 will be forward biased and D1 will be reverse biased. The diode D2 will conduct and D1 will not conduct during the negative half cycle. The current flow will be in the direction P2-D2-C-A-B-GND.



Centre-tap Full-wave Rectifier-Waveform

When comparing the current flow in the positive and negative half cycles, we can conclude that the direction of the current flow is the same (through load resistance RLOAD). When compared to the Half-Wave Rectifier, both the half cycles are used to produce the corresponding output. The frequency of the rectified output voltage is twice the input frequency. The output that is rectified, consists of a dc component and a lot of ac components of minute amplitudes.

- **Peak Inverse Voltage (PIV) of Centre-Tap Full Wave Rectifier**

PIV is the maximum possible voltage across a diode during its reverse biased period. Let us analyze the PIV of the centre-tapped rectifier from the circuit diagram. During the first half or the positive half of th input ac supply, the diode D1 is positive and thus conducts and provided no resistance at all. Thus, the whole of voltage Vs developed in the upper-half of the ac supply is provided to the load resistance RLOAD. Similar is the case of diode D2 for the lower half of the transformer secondary.

Therefore, PIV of D2 = Vm + Vm = 2Vm

PIV of D1 = 2Vm

Centre-Tap Rectifier Circuit Analysis

- **Peak Current**

The instantaneous value of the voltage applied to the rectifier can be written as

Vs = Vsm Sinwt

Assuming that the diode has a forward resistance of RFWD ohms and a reverse resistance equal to infinity, the current flowing through the load resistance RLOAD is given as

$$Im = Vsm/(R_F + R_{Load})$$

- **Output Current**

Since the current is the same through the load resistance RL in the two halves of the ac cycle, magnitude od dc current Idc, which is equal to the average value of ac current, can be obtained by integrating the current i1 between 0 and pi or current i2 between pi and 2pi.

$$\mathbf{So\ I_{dc} = 1/\pi \int_0^{\pi} i1\ d(wt) = 1/\pi\ [\int_0^{\pi} I_{max}\ Sin\ wtd(wt) = 2I_m/\pi}$$

Output current of centre Tap rectifier

- **DC Output Voltage**

Average or dc value of voltage across the load is given as

$$\mathbf{So\ I_{dc} = 1/\pi \int_0^{\pi} i1\ d(wt) = 1/\pi\ [\int_0^{\pi} I_{max}\ Sin\ wtd(wt) = 2I_m/\pi}$$

DC Output Voltage of centre Tap Rectifier

- **Root Mean Square (RMS) Value of Current**

RMS or effective value of current flowing through the load resistance R_L is given as

$$\mathbf{I^2_{rms} = 1/\pi \int_0^{\pi} i12 d(wt) = I^2_m/2 \text{ or } I_{rms} = Im/\sqrt{2}}$$

RMS Value of Current of centre Tap Rectifier

- **Root Mean Square (RMS) Value of Output Voltage**

RMS value of voltage across the load is given as

$$\mathbf{V_{LOAD}\ rms = Irms\ R_{LOAD} = [I_M/\sqrt{2}]R_{LOAD}}$$

RMS Value of Output Voltage of Centre Tap Rectifier

- **Rectification Efficiency**

Power delivered to load,

$$P_{dc} = I^2_{dc} R_{LOAD} = (2I_M/\pi)^2 R_{LOAD} = (4/\pi^2) I^2_M R_{LOAD}$$

AC power input to the transformer, P_{ac} = Power dissipated in diode junction + Power dissipated in load resisance R_{LOAD}

$$I^2_{rms} R_F + I^2_{rms} R_{LOAD} = \{I^2_M/2\}[R_F + R_{LOAD}]$$

$$\text{SO, rectification efficiency } \eta = P_{dc}/P_{ac} = \{(4/\pi^2) I^2_M R_{LOAD}\}/\{I^2_M/2\}[R_F + R_{LOAD}]$$

$$= \{0.812/(1 = R_F/R_{LOAD})\}$$

$$\text{In case of bridge rectifier, } \eta = \{0.812/(1+2R_F/R_{LOAD})\}$$

Rectification Efficiency of Centre Tap Rectifier

- **Ripple Factor**

Form factor of the rectified output voltage of a full wave rectifier is given as

$$K_f = I_{rms} / I_{avg} = (I_m/\sqrt{2})/(2I_M/\pi) = \pi \div 2\sqrt{2} = 1.11$$

Ripple Factor of centre Tap Rectifier

- **Regulation**

The dc output voltage is given as

$$V_{dc} = I_{dc} R_{LOAD} = 2/\pi I_M R_{LOAD}$$

$$= 2V_{sm} R_{LOAD}/\pi[R_F + R_{LOAD}]$$

$$= [2V_{sm}/\pi] - Idc\ R_F$$

$$\text{If it is a bridge rectifier, } V+dc+ = [2V_{sm}/\pi] - 2I_{dc} R_F$$

1.7.2 Full wave bridge rectifier.

A Full wave rectifier is a circuit arrangement which makes use of both half cycles of input alternating current (AC) and convert them to direct current (DC). In our tutorial on **Half wave rectifiers**, we have seen that a half wave rectifier makes use of only one half cycle of the input alternating current. Thus a full wave rectifier is much more efficient (double+) than a half wave rectifier. This process of converting both half cycles of the input supply (alternating current) to direct current (DC) is termed full wave rectification.

Full wave rectifier can be constructed in 2 ways. The first method makes use of a center tapped transformer and 2 diodes. This arrangement is known as **Center Tapped Full Wave**

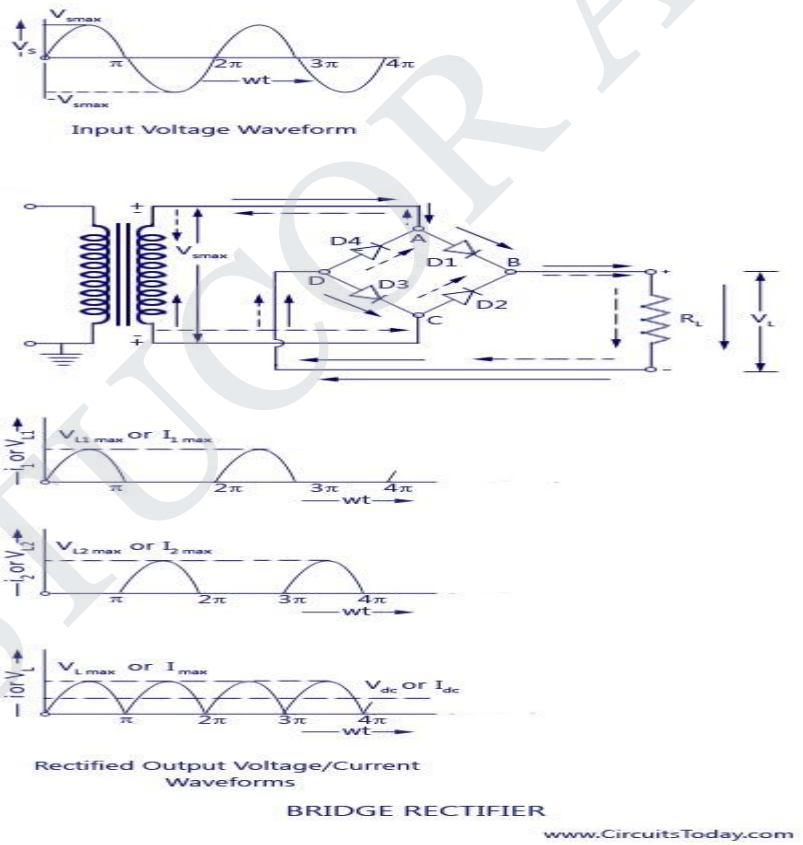
Rectifier. The second method uses a normal transformer with 4 diodes arranged as a bridge. This arrangement is known as a Bridge Rectifier.

Full Wave Rectifier Theory

To understand full wave bridge rectifier theory perfectly, you need to learn half wave rectifier first. In the tutorial of half wave rectifier we have clearly explained the basic working of a rectifier. In addition we have also explained the theory behind a pn junction and the characteristics of a pn junction diode.

Full Wave Rectifier Working & Operation

The working & operation of a full wave bridge rectifier is pretty simple. The circuit diagrams and wave forms we have given below will help you understand the operation of a bridge rectifier perfectly. In the circuit diagram, 4 diodes are arranged in the form of a bridge. The transformer secondary is connected to two diametrically opposite points of the bridge at points A & C. The load resistance R_L is connected to bridge through points B and D.

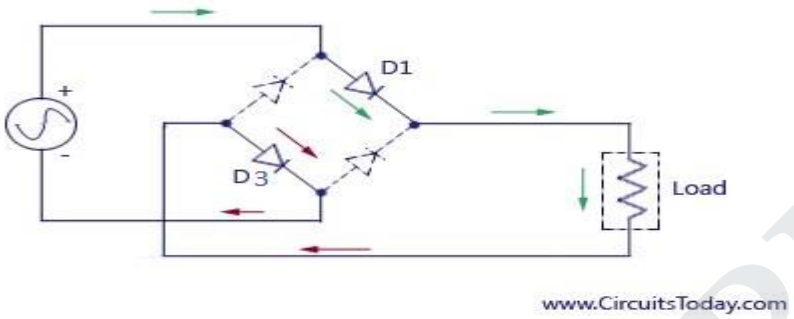


Full Wave Bridge Rectifier – Circuit Diagram with Input and Output Wave Forms

- **During the first half cycle**

During first half cycle of the input voltage, the upper end of the transformer secondary winding is positive with respect to the lower end. Thus during the first half cycle diodes D1 and D_3 are forward biased and current flows through arm AB, enters the load resistance R_L, and returns back flowing

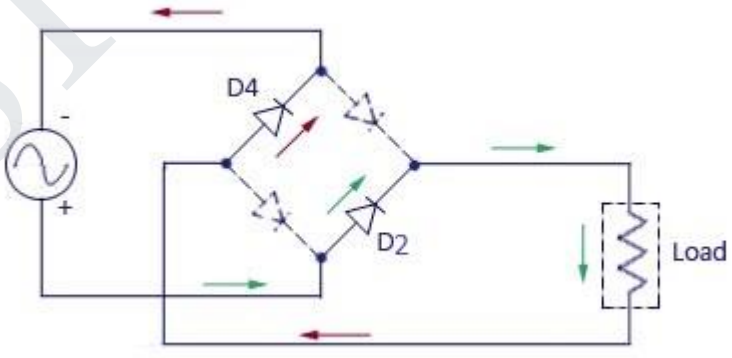
through arm DC. During this half of each input cycle, the diodes D_2 and D_4 are reverse biased and current is not allowed to flow in arms AD and BC. The flow of current is indicated by solid arrows in the figure above. We have developed another diagram below to help you understand the current flow quickly. See the diagram below – the green arrows indicate beginning of current flow from source (transformer secondary) to the load resistance. The red arrows indicate return path of current from load resistance to the source, thus completing the circuit.



Flow of current in Bridge Rectifier

- **During the second half cycle**

During second half cycle of the input voltage, the lower end of the transformer secondary winding is positive with respect to the upper end. Thus diodes D_2 and D_4 become forward biased and current flows through arm CB, enters the load resistance R_L, and returns back to the source flowing through arm DA. Flow of current has been shown by dotted arrows in the figure. Thus the direction of flow of current through the load resistance R_L remains the same during both half cycles of the input supply voltage. See the diagram below – the green arrows indicate beginning of current flow from source (transformer secondary) to the load resistance. The red arrows indicate return path of current from load resistance to the source, thus completing the circuit.



1.8 LIGHT EMITTING DIODE (LED)

A light emitting diode (LED) is known to be one of the best optoelectronic devices out of the lot. The device is capable of emitting a fairly narrow bandwidth of visible or invisible light when its internal diode junction attains a forward electric current or voltage.

The visible lights that an LED emits are usually orange, red, yellow, or green. The invisible light includes the infrared light. The biggest advantage of this device is its high power to light conversion efficiency. That is, the efficiency is almost 50 times greater than a simple tungsten lamp.

The response time of the LED is also known to be very fast in the range of 0.1 microseconds when compared with 100 milliseconds for a tungsten lamp. Due to these advantages, the device wide applications as visual indicators and as dancing light displays.

We know that a P-N junction can connect the absorbed light energy into its proportional electric current. The same process is reversed here. That is, the P-N junction emits light when energy is applied on it. This phenomenon is generally called electro luminance, which can be defined as the emission of light from a semi-conductor under the influence of an electric field.

The charge carriers recombine in a forward P-N junction as the electrons cross from the N-region and recombine with the holes existing in the P-region. Free electrons are in the conduction band of energy levels, while holes are in the valence energy band.

Thus the energy level of the holes will be lesser than the energy levels of the electrons. Some part of the energy must be dissipated in order to recombine the electrons and the holes. This energy is emitted in the form of heat and light.

The electrons dissipate energy in the form of heat for silicon and germanium diodes. But in Galium- Arsenide-phosphorous (GaAsP) and Galium-phosphorous (GaP) semiconductors, the electrons dissipate energy by emitting photons. If the semiconductor is translucent, the junction becomes the source of light as it is emitted, thus becoming a light emitting diode (LED). But when the junction is reverse biased no light will be produced by the LED, and, on the contrary the device may also get damaged.

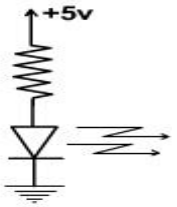
All the semiconductors listed above can be used. An N-type epitaxial layer is grown upon a substrate, and the P-region is produced by diffusion. The P-region that includes the recombination of charge carriers is shown is the top. Thus the P-region becomes the device surface. In order to allow more surface area for the light to be emitted the metal anode connections are made at the outer edges of the P-layer.

For the light to be reflected as much as possible towards the surface of the device, a gold film is applied to the surface bottom. This setting also enables to provide a cathode connection. The re-absorption problem is fixed by including domed lenses for the device. All the wires in the electronic circuits of the device is protected by encasing the device.

The light emitted by the device depends on the type of semiconductor material used. Infrared light is produced by using Gallium Arsenide (GaAs) as semiconductor. Red or yellowlight is produced by using Gallium -Arsenide-Phosphorus (GaAsP) as semiconductor.

- **LED Circuit Symbol**

The circuit symbol of LED consists of two arrow marks which indicate the radiation emitted by the diode.



Symbol of LED

1.8.1 LED Characteristics

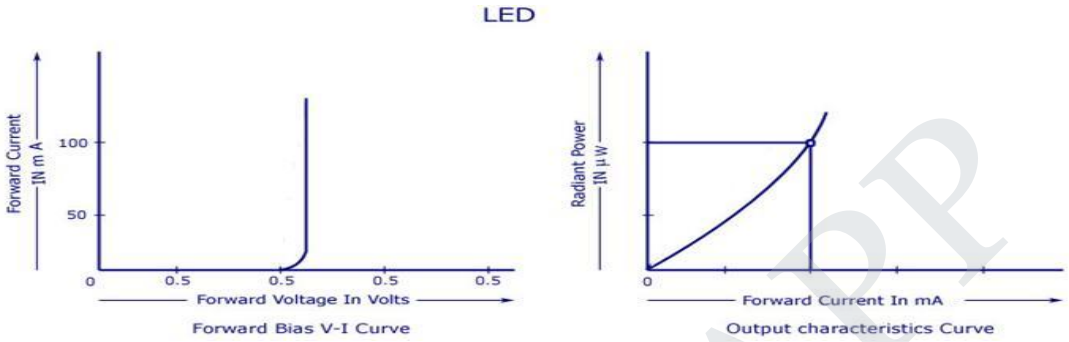


Figure 5.3 LED characteristics curve

The forward bias Voltage-Current (V-I) curve and the output characteristics curve is shown in the figure above. The V-I curve is practically applicable in burglar alarms. Forward bias of approximately 1 volt is needed to give significant forward current. The second figure is used to represent a radiant power-forward current curve. The output power produced is very small and thus the efficiency in electrical-to-radiant energy conversion is very less.

The commercially used LED's have a typical voltage drop between 1.5 Volt to 2.5 Volt or current between 10 to 50 milliamperes. The exact voltage drop depends on the LED current, colour, tolerance, and so on.

1.8.2 LED as an Indicator

The circuit shown below is one of the main applications of LED. The circuit is designed by wiring it in inverse parallel with a normal diode, to prevent the device from being reverse biased. The value of the series resistance should be half, relative to that o f a DC circuit.

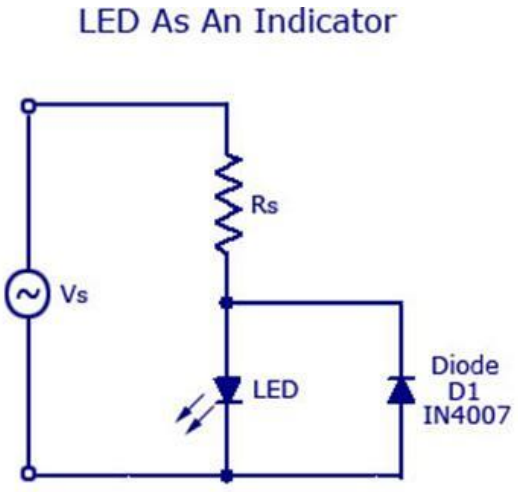


Figure 5.35 LED as an indicator

LEDS displays are made to display numbers from segments. One such design is the seven-segment display as shown below. Any desired numerals from 0-9 can be displayed by passing current through the correct segments. To connect such segment a common anode or common cathode cathode configuration can be used. Both the connections are shown below. The LED's are switched ON and OFF by using transistors.

- **Advantages of LED's**

  - Very low voltage and current are enough to drive the LED.
  - Voltage range – 1 to 2 volts.
  - Current – 5 to 20 mill amperes.
  - Total power output will be less than 150 mill watts.
  - The response time is very less – only about 10 nanoseconds.
  - The device does not need any heating and warm up time.
  - Miniature in size and hence light weight.
  - Have a rugged construction and hence can withstand shock and vibrations.
  - An LED has a life span of more than 20 years.

- **Disadvantages of LED**
  - A slight excess in voltage or current can damage the device.
  - The device is known to have a much wider bandwidth compared to the laser.
  - The temperature depends on the radiant output power and wavelength.

1.9 Laser diode

A laser diode, or LD, is an electrically pumped semiconductor laser in which the active laser medium is formed by a p-n junction of a semiconductor diode similar to that found in a light-emitting diode.

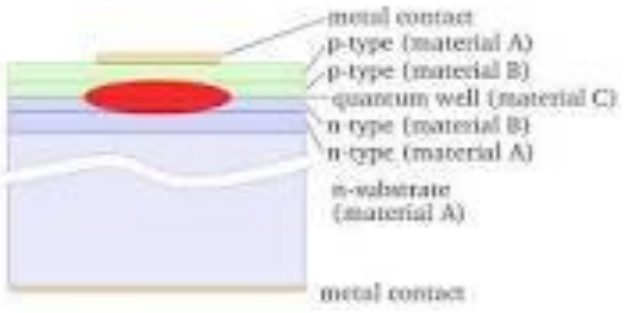
The laser diode is the most common type of laser produced with a wide range of uses that include, but are not limited to, fiber optic communications, barcode readers, laser pointers, CD/DVD/Blu-ray Disc reading and recording, laser printing, laser scanning and increasingly directional lighting sources.

A laser diode is electrically a P-i-n diode. The active region of the laser diode is in the intrinsic (I) region, and the carriers, electrons and holes, are pumped into it from the N and P regions respectively.

While initial diode laser research was conducted on simple P-N diodes, all modern lasers use the double-hetero structure implementation, where the carriers and the photons are confined in order to maximize their chances for recombination and light generation.

Unlike a regular diode used in electronics, the goal for a laser diode is that all carriers recombine in the I region, and produce light. Thus, laser diodes are fabricated using direct bandgap semiconductors. The laser diode epitaxial structure is grown using one of the crystal growth techniques, usually starting from an N doped substrate, and growing the I doped active layer,

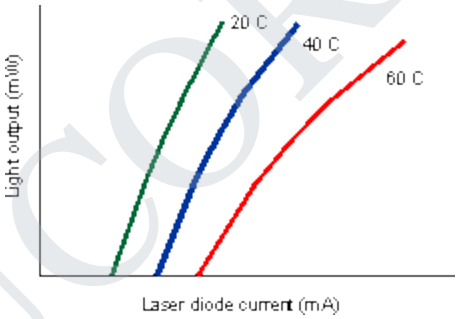
followed by the P doped cladding, and a contact layer. The active layer most often consists of quantum wells,



1.9.1Laser diode L/I characteristic

One of the most commonly used and important laser diode specifications or characteristics is the L/I curve. It plots the drive current supplied against the light output.

This laser diode specification is used to determine the current required to obtain a particular level of light output at a given current. It can also be seen that the light output is also very dependent upon the temperature.



Laser diode L/I Characteristic

From this characteristic, it can be seen that there is a threshold current below which the laser action does not take place. The laser diode should be operated clear of this point to ensure reliable operation over the full operating temperature range as the threshold current rises with increasing temperature. It is typically found that the laser threshold current rises exponentially with temperature.

- Laser Diode Specifications & Characteristics

a summary or overview of laser diode specifications, parameters and characteristics used in defining laser diode performance for datasheets.

In this section

- Laser diode technology
- Laser diode types

- Structure & materials
- Theory & operation
- Specs & characteristics
- Lifetime, failure & reliability
- Other diodes

When using a laser diode it is essential to know its performance characteristics. Accordingly laser diode specifications are required when designing equipment using laser diodes or for maintenance using near equivalents.

Like any electronics components, many of the specifications are relatively generic, but other parameters will tend to be more focussed on the particular component. This is true for laser diode specifications and characteristics.

There are a number of laser diode specifications, or laser diode characteristics that are key to the overall performance and these are outlined.

1.10 A ZENER DIODE

A Zener diode is a type of diode that permits current not only in the forward directionlike a normal diode, but also in the reverse direction if the voltage is larger than the breakdownvoltage known as "Zener knee voltage" or "Zener voltage". The device was named after ClarenceZener, who discovered this electrical property.

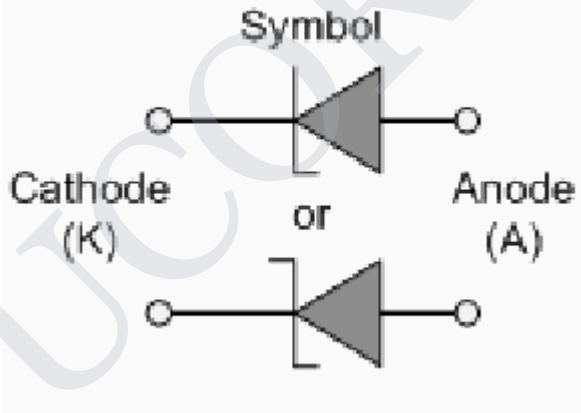


Figure 4.6 Diode symbol

- ✓ However, the Zener Diode or "Breakdown Diode" as they are sometimes called, arebasically the same as the standard PN junction diode but are specially designed to have a lowpre-determined Reverse Breakdown Voltage that takes advantage of this high reverse voltage.

- ✓ The point at which a zener diode breaks down or conducts is called the "Zener Voltage" (Vz).The Zener diode is like a general-purpose signal diode consisting of a silicon PNjunction.
- ✓ When biased in the forward direction it behaves just like a normal signal diode passingthe rated current, but when a reverse voltage is applied to it the reverse saturation currentremains fairly constant over a wide range of voltages.
- ✓ The reverse voltage increases until thediodes breakdown voltage VB is reached at which point a process called Avalanche Breakdown occurs in the depletion layer and the current flowing through the zener diode increasesdramatically to the maximum circuit value (which is usually limited by a series resistor).

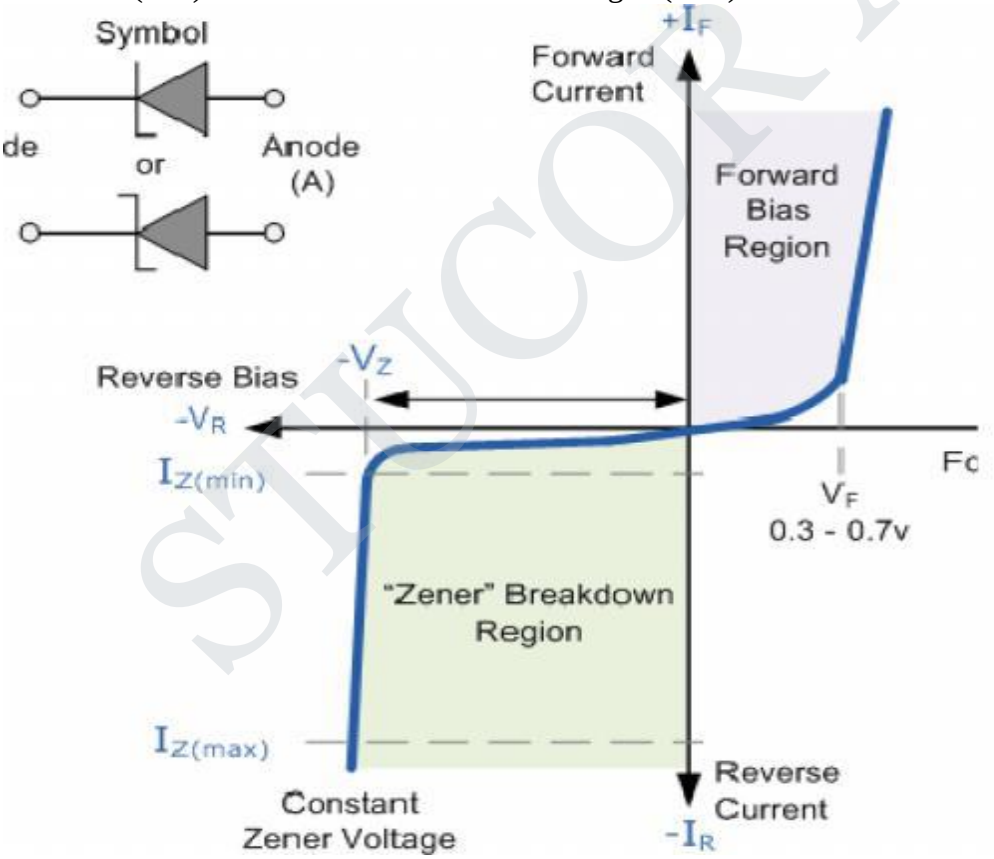
- ✓ Thisbreakdown voltage point is called the "zener voltage" for zener diodes.

- ✓ **Avalanche Breakdown*:*** There is a limit for the reverse voltage. Reverse voltage can increase until the diode breakdown voltage reaches. This point is called Avalanche Break down region. At this stage maximum current will flow through the zener diode. This breakdown point is referred as “Zener voltage”.

The point at which current flows can be very accurately controlled (to less than 1%tolerance) in the doping stage of the diodes construction giving the diode a specific zenerbreakdown voltage, (Vz) ranging from a few volts up to a few hundred volts. This zenerbreakdown voltage on the I-V curve is almost a vertical straight line.

1.10.1 Zener diode characteristics

The Zener Diode is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply. From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current IZ(min) and the maximum current rating IZ(max).



1.10.2 Zener Regulator:

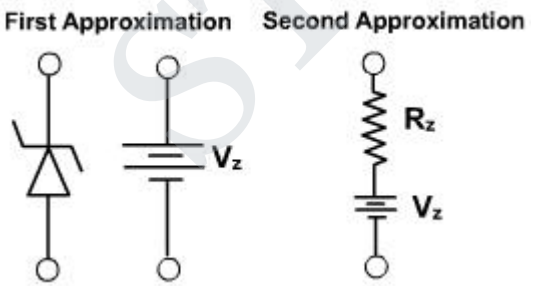
When zener diode is forward biased it works as a diode and drop across it is 0.7 V. When it works

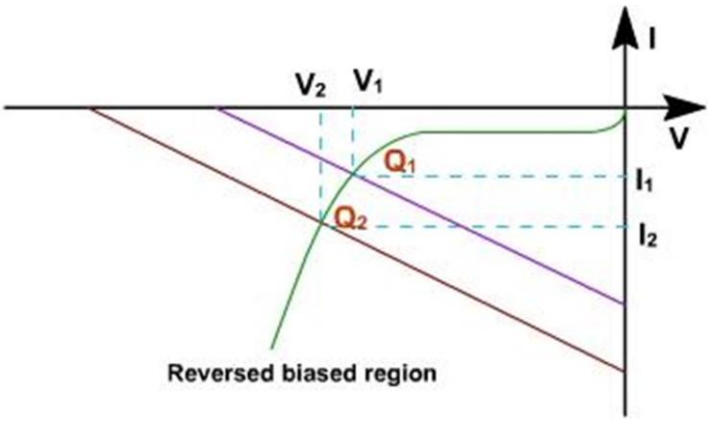
in breakdown region the voltage across it is constant (V_Z) and the current through diode is decided by the external resistance. Thus, zener diode can be used as
a voltage regulator in the configuration shown in figure 2 for regulating the dc voltage. It maintains the output voltage constant even through the current through it changes.

Figure 2 **Figure 3**

The load line of the circuit is given by $V_S = I_S R_S + V_Z$. The load line is plotted along with zener characteristic in figure The intersection point of the load line and the zener characteristic gives the output voltage and zener current.

To operate the zener in breakdown region V_S should always be greater then V_Z. R_S is used to limit the current. If the V_S voltage changes, operating point also changes simultaneously but voltage across zener is almost constant. The first approximation of zener diode is a voltage source of V_Z magnitude and second approximation includes the resistance also. The two approximate equivalent circuits are shown in below figure





If second approximation of zener diode is considered, the output voltage varies slightly as shown in figure The zener ON state resistance produces more I * R drop as the current increases. As the voltage varies form V_1 to V_2 the operating point shifts from Q_1 to Q_2.

The voltage at Q_1 is

$V_1 = I_1 R_Z + V_Z$

and at Q_2

$V_2 = I_2 R_Z + V_Z$

Thus, change in voltage is $V_2 - V_1 = (I_2 - I_1) R_Z$

Review Questions

PART-B

1. With a neat diagram explain the working of a PN junction diode in forward bias and reverse bias and show the effect of temperature on its V-I characteristics. (16)
2. Explain V-I characteristics of Zener diode. (8)
3. Draw the circuit diagram and explain the working of full wave bridge rectifier and derive the expression for average output current and rectification efficiency. (8)
4. Explain the operation of FWR with centre tap transformer. Also derive the following for this transformer.dc output voltage (4) dc output current (2) (iv) RMS output voltage. (4)
5. Explain the following regulator circuits : (i) Transistorized shunt regulator. (8) (ii) Zener diode shunt regulator. (8)
6. Draw the circuit diagram and explain the operation of full wave rectifier using center tap transformer and using bridge rectifier without center tap transformer. Obtain the expression for peak inverse voltage. (16)
7. With neat diagram explain the construction and working of LED. (8)

UNIT 2 TRANSISTORS

2.1 INTRODUCTION

The transistor is the main building block "element" of electronics. It is a semiconductor device and it comes in two general types: the Bipolar Junction Transistor (BJT) and the Field Effect Transistor (FET).

It is named as transistor which is an acronym of two terms: "transfer-of-resistor." It means that the internal resistance of transistor transfers from one value to another values depending on the biasing voltage applied to the transistor. Thus it is called Transfer resistor: i.e. TRANSISTOR.

A bipolar transistor (BJT) is a three terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and hence the name bipolar.

The voltage between two terminals controls the current through the third terminal. So it is called current controlled device. This is the basic principle of the BJT

It can be used as amplifier and logic switches. BJT consists of three terminals:

- Collector : C
- Base : B
- Emitter : E

➢ **TYPES**

There are two types of bipolar transistors

- NPN transistor and
- PNP transistor.

2.1.1 TRANSISTOR CONSTRUCTION

PNP Transistor: In PNP transistor a thin layer of N-type silicon is sandwiched between two layers of P-type silicon.

NPN Transistor: In NPN transistor a thin layer of P-type silicon is sandwiched between two layers of N-type silicon. The two types of BJT are represented in figure 2.1

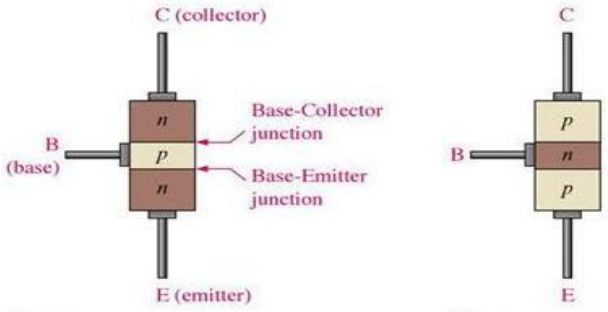


Figure 2.1 Transistors: NPN, PNP

The symbolic representation of the two types of the BJT is shown in figure 2.2

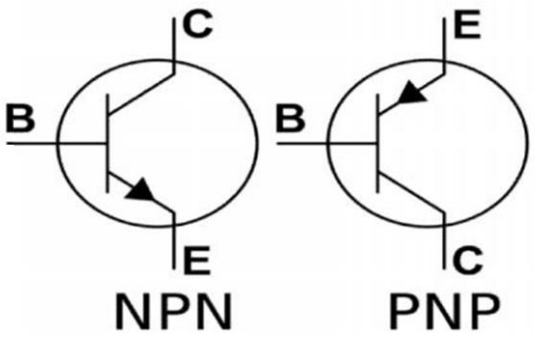


Figure 2.2 circuit symbol: NPN transistor ,PNP transistor

Area:[C>E>B]

- The area of collector layer is largest. So it can dissipate heat quickly.
- Area of base layer is smallest and it is very thin layer.
- Area of emitter layer is medium.

Doping level:[E>C>B]

- Collector layer is moderately doped. So it has medium number of charges.
- Base layer is lightly doped. So it has a very few number of charges.
- Emitter layer is heavily doped. So it has largest number of charges.

Junctions:

- There are two junctions in this transistor – junction J-1 and junction J-2.
- The junction between collector layer and base layer is called as collector-base junction or C-B junction.
- The junction between base layer and emitter layer is called as base-emitter junction or B-E junction. The two junctions have almost same potential barrier voltage of 0.6V to 0.7V, just like in a diode.

Equivalent diode representation:

The transistor formed by back to back connection of two diodes

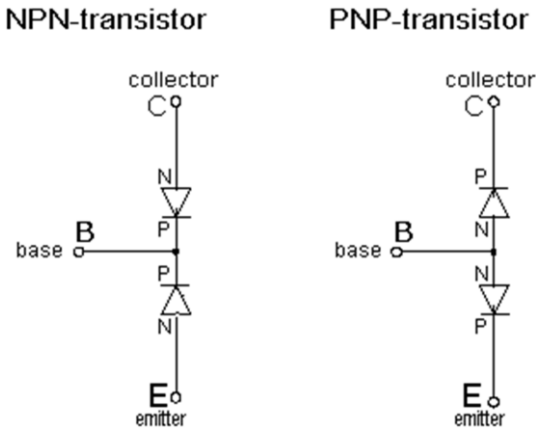


Figure 2.3 The equivalent diode representation for the NPN and PNP transistors

The states of the two pn junctions can be altered by the external circuitry connected to the transistor. This is called biasing the transistor.

Usually the emitter- base junction is forward biased and collector –base junction is reverse biased. Due to forward bias on the emitter- base junction an emitter current flows through the base into the collector. Though, the collector –base junction is reverse biased, almost the entire emitter current flows through the collector circuit.

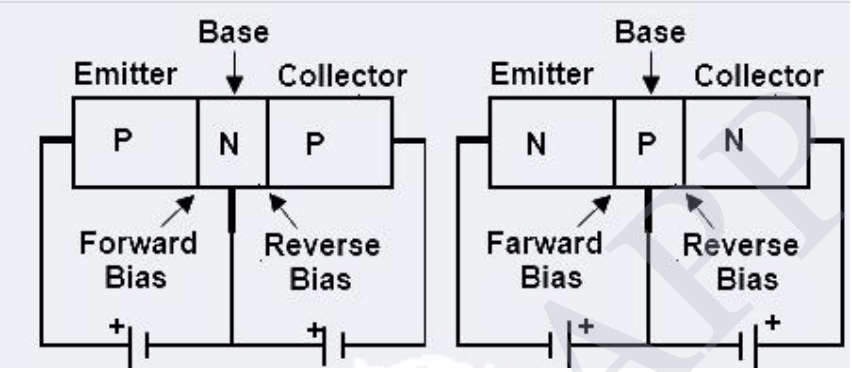


Figure 2.4 Transistor biasing: PNP transistor, NPN transistor

A single pn junction has two different types of bias:

- Forward bias
- Reverse bias

There are two junctions in bipolar junction transistor. Each junction can be forward or reverse biased independently. Thus there are four modes of operations:

Table 2.1 Modes of operation of transistor

Modes	Emitter-Base junction	Collector- Base junction
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward
Reverse active	Reverse	Forward

Forward Active

In this mode of operation, emitter-base junction is forward biased and collector base junction is reverse biased. Transistor behaves as a source. With controlled source characteristics the BJT can be used as an amplifier and in analog circuits.

Cut off

When both junctions are reverse biased it is called cut off mode. In this situation there is nearly zero current and transistor behaves as an open switch.

Saturation

In saturation mode both junctions are forward biased large collector current flows with a small voltage across collector base junction. Transistor behaves as an closed switch.

Reverse Active

It is opposite to forward active mode because in this emitter base junction is reverse biased and collector base junction is forward biased. It is called inverted mode. It is no suitable for amplification.However the reverse active mode has application in digital circuits and certain analog switching circuits.

2.1.2 TRANSISTOR CURRENTS

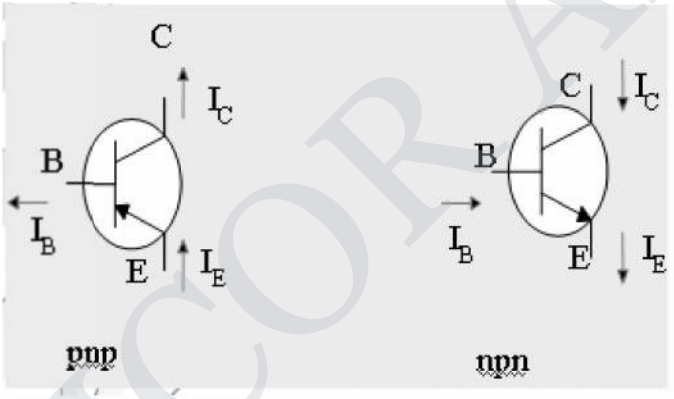


Figure 2.5 Transistor current flow directions

- The arrow is always drawn on the emitter The arrow always point toward the n-type

- The arrow indicates the direction of the emitter current:

  pnp:E-> B

  npn: B-> E

I_C = the collector current, I_B = the base current, I_E = the emitter current

2.2 OPERATION OF AN NPN TRANSISTOR

Emitter base junction is forward biased and collector base junction is reverse biased. Due to emitter base junction is forward biased lot of electrons from emitter entering the base region.

Base is lightly doped with P-type impurity. So the number of holes in the base region is very small.

Due to this, electron- hole recombination is less (i.e,) few electrons(<5%) combine with holes to constitute base current(I_B)

The remaining electrons (>95%) crossover into collector region, to constitute collector current(I_C).

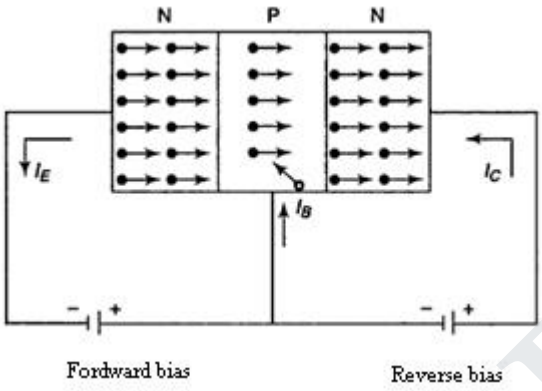


Figure 2.6 Current in NPN transistor

2.2.1 OPERATION OF A PNP TRANSISTOR

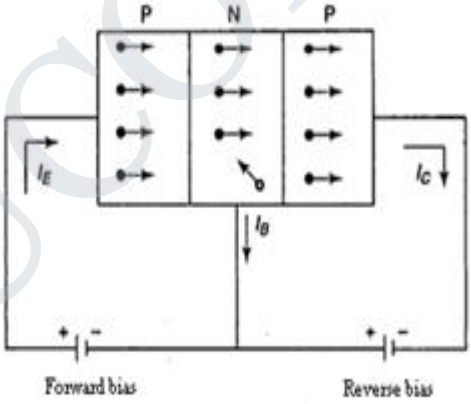


Figure 2.7 Current in PNP transistor

Emitter base junction is forward biased and collector base junction is reverse biased. Due to emitter base junction is forward biased lot of holes from emitter entering the base region and electrons from base to emitter region.

Base is lightly doped with N-type impurity. So the number of electrons in the base region is very small.

Due to this, electron- hole recombination is less (i.e,) few holes (<5%) combine with electrons to constitute base current(I_B)

2.3 CONFIGURATION OF TRANSISTOR CIRCUIT

A transistor is a three terminal device. But require '4' terminals for connecting it in a circuits.
(i.e.) 2 terminals for input, 2 terminals for output.

Hence one of the terminal is made common to the input and output circuits. Common terminal is grounded.

➢ TYPES OF CONFIGURATIONS

Three types of configuration is available

1) Common base(CB) configuration
2) Common emitter (CE) configuration
3) Common collector (CC) configuration

2.3.1 COMMON BASE(CB) CONFIGURATION

In common base configuration circuit is shown in figure. Here base is grounded and it is used as the common terminal for both input and output.

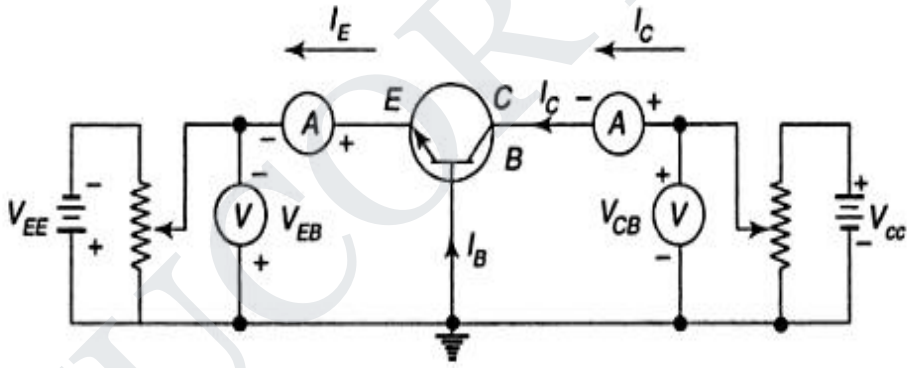


Figure 2.10 Circuit to determine CB static characteristics

It is also called as grounded base configuration. Emitter is used as a input terminal where as collector is the output terminal.

Input characteristics:

It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant.

To determine input characteristics, the collector base voltage V_{CB} is kept constant at zero and emitter current I_E is increased from zero by increasing V_{EB}.This is repeated for higher fixed values of V_{CB}.

A curve is drawn between emitter current and emitter base voltage at constant collector base

voltage is shown in figure 2.11.When V_{CB} is zero EB junctions is forward biased. So it behaves as a diode so that emitter current increases rapidly.

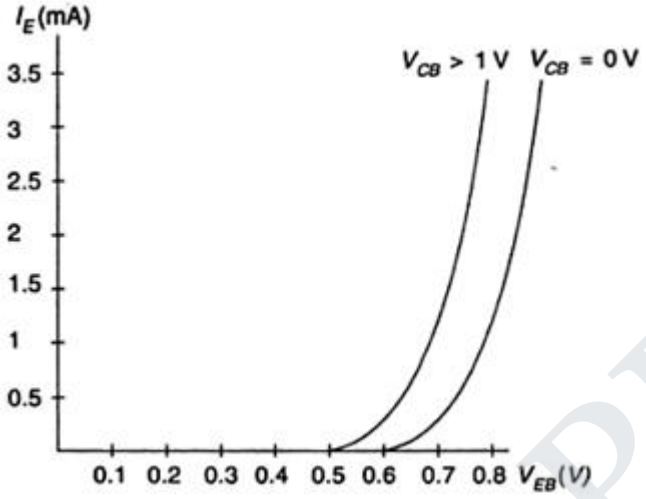


Figure 2.11 CB input characteristics

- **Output Characteristics**

It is defined as the characteristic curve drawn between output voltage to output current whereas input current is constant.To determine output characteristics, the emitter current I_E is kept constant at zero and collector current Ic is increased from zero by increasing V_{CB}.This is repeated for higher fixed values of I_E.

From the characteristic it is seen that for a constant value of I_E, Ic is independent of V_{CB} and the curves are parallel to the axis of V_{CB}.As the emitter base junction is forward biased the majority carriers that is electrons from the emitter region are injected into the base region.

In CB configuration a variation of the base-collector voltage results in a variation of the quasi- neutral width in the base. The gradient of the minority-carrier density in the base therefore changes, yielding an increased collector current as the collector-base current is increased. This effect is referred to as the Early effect.

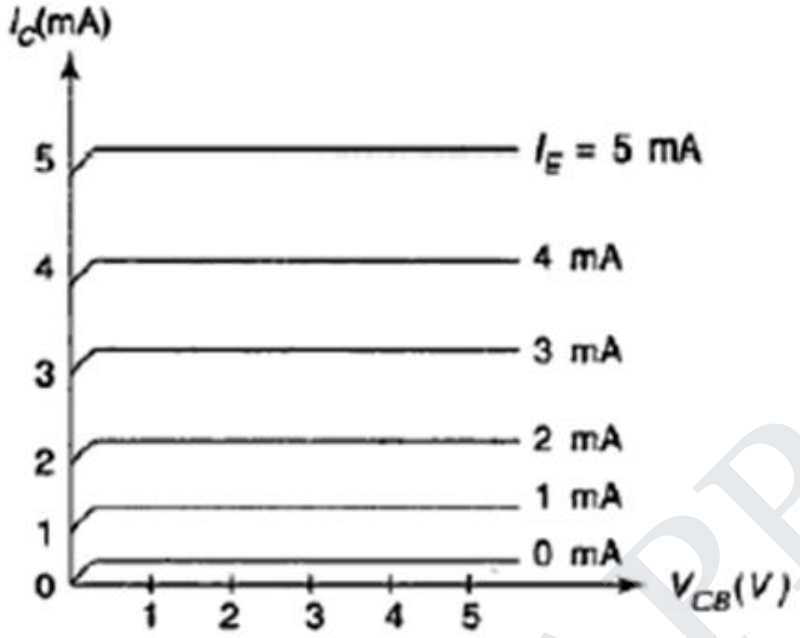


Figure 2.12 CB output characteristics

2.3.2 CE CONFIGURATION

In common emitter configuration circuit is shown in figure. Here emitter is grounded and it is used as the common terminal for both input and output. It is also called as grounded emitter configuration. Base is used as a input terminal whereas collector is the output terminal.

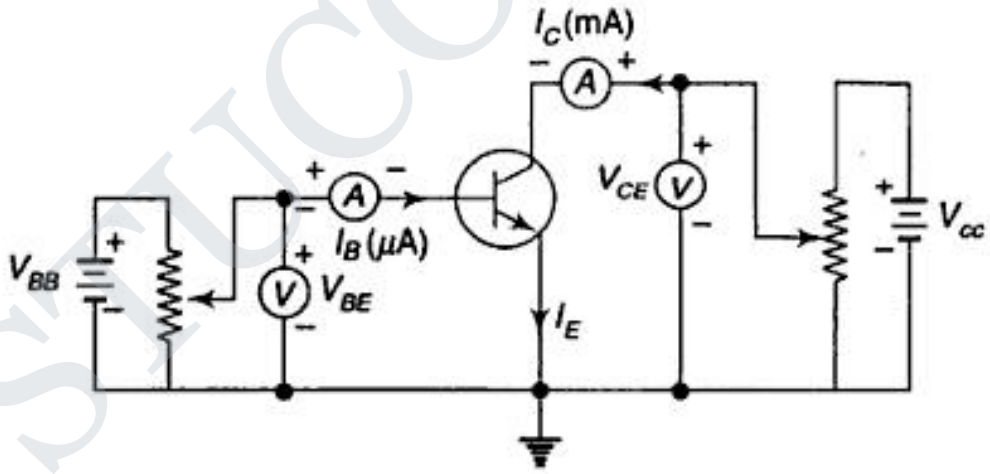


Figure 2.13 Circuit to determine CE static characteristics

- **Input Characteristics**

It is defined as the characteristic curve drawn between input voltages to input current whereas output voltage is constant.

To determine input characteristics, the collector base voltage V_{CB} is kept constant at zero and base current I_B is increased from zero by increasing V_{BE}.This is repeated for higher fixed values of V_{CE}.

A curve is drawn between base current and base emitter voltage at constant collector base voltage is shown in figure2.14. Here the base width decreases. So curve moves right as V_{CE} increases.

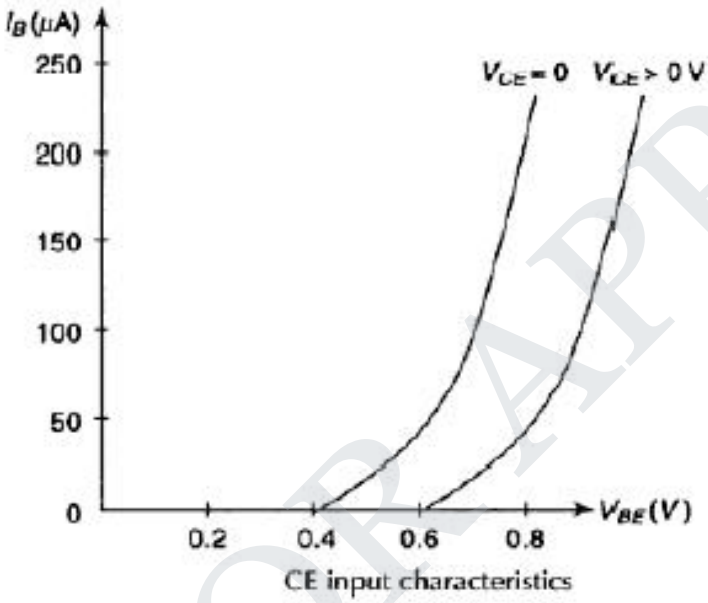


Figure 2.14 CE input characteristics

- **Output Characteristics**

It is defined as the characteristic curve drawn between output voltage to output current whereas input current is constant.

To determine output characteristics, the base current I_B is kept constant at zero and collector current Ic is increased from zero by increasing V_{CE}.This is repeated for higher fixed values of I_B.

From the characteristic it is seen that for a constant value of I_B, Ic is independent of V_{CB} and the curves are parallel to the axis of V_{CE}.

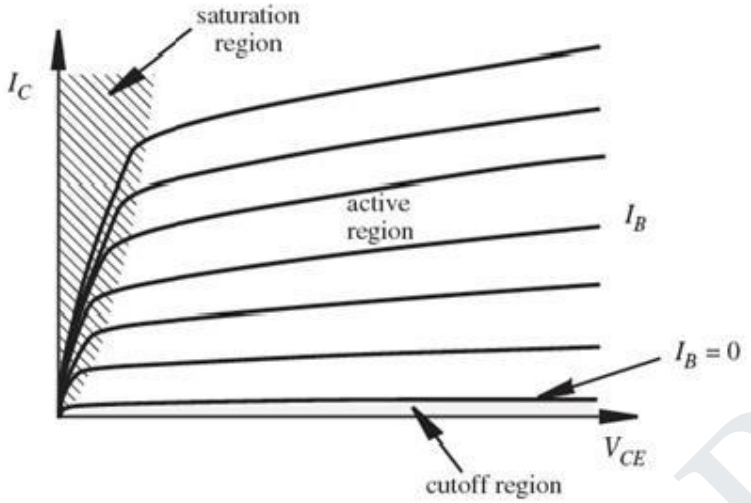


Figure 2.15 CE output Characteristics

The output characteristic has 3 basic regions:

- Active region –defined by the biasing arrangements.

- Cutoff region – region where the collector current is 0A

- Saturation region- region of the characteristics to the left of VCB = 0V.

Active region	Saturation region	Cut-off region
□ I_E increased, I_C increased. □ BE junction forward bias and CB junction reverse bias. □ Refer to the graph, $I_C \approx I_E$ □ I_C not depends on V_{CB} □ Suitable region for the transistor working as amplifier.	□ BE and CB junction is forward bias □ Small changes in V_{CB} will cause big different to I_C □ The allocation for this region is to the left of V_{CB}=0V.	□ Region below the line of I_E=0 A □ BE and CB is reverse biase □ No current flow at collector, only leakage current.

2.3.3 CC CONFIGURATION

In common collector configuration circuit is shown in figure. Here collector is grounded and it is used as the common terminal for both input and output. It is also called as grounded collector configuration. Base is used as a input terminal whereas emitter is the output terminal.

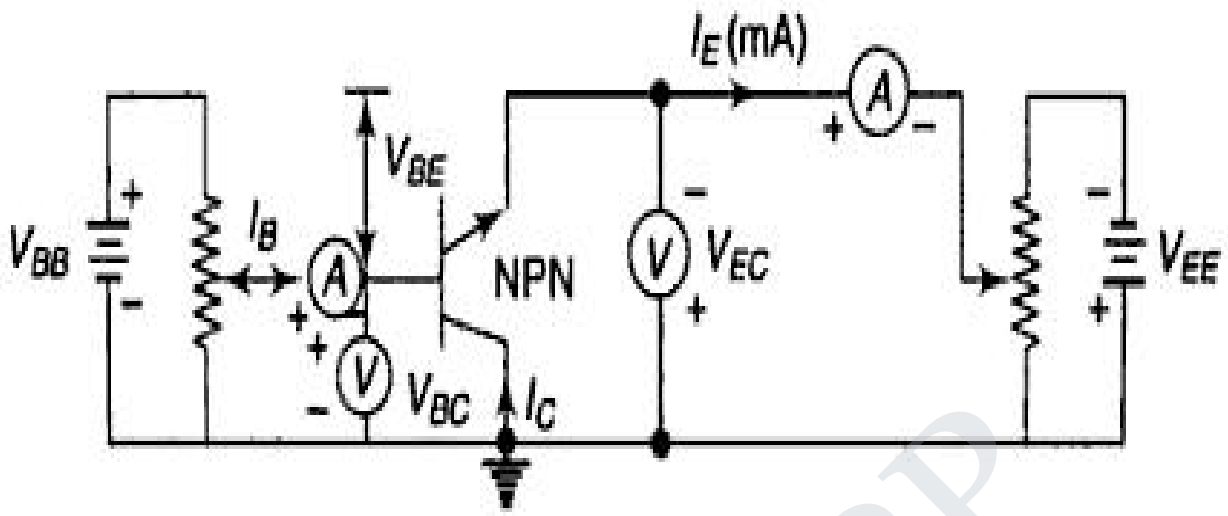


Figure 2.16 Circuits to determine CC static characteristics

- **Input Characteristics**

It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant.

To determine input characteristics, the emitter base voltage V_{EB} is kept constant at zero and base current I_B is increased from zero by increasing V_{BC}.This is repeated for higher fixed values of V_{CE}.A curve is drawn between base current and base emitter voltage at constant collector base voltage is shown in figure2.17.

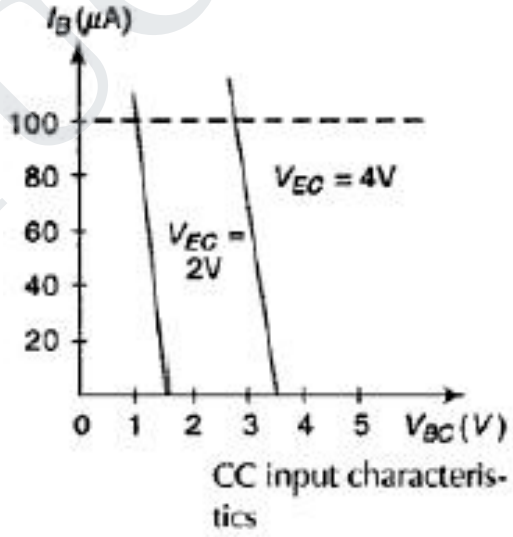


Figure 2.17 CC input characteristics

- **Output Characteristics**

It is defined as the characteristic curve drawn between output voltage to output current

whereas input current is constant.

To determine output characteristics, the base current I_B is kept constant at zero and emitter current I_E is increased from zero by increasing V_{EC}. This is repeated for higher fixed values of I_B.

From the characteristic it is seen that for a constant value of I_B, I_E is independent of V_{EB} and the curves are parallel to the axis of V_{EC}.

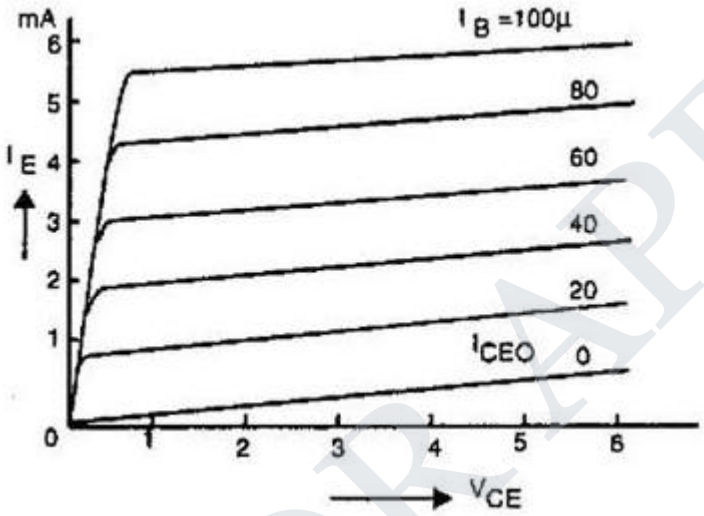


Figure 2.18 CC output characteristics

A comparison of CB, CE and CC Configurations

Property	*CB*	*CE*	*CC*
Input resistance	Low (about 100 Ω)	Moderate (about 750 Ω)	High (about 750 kΩ)
Output resistance	High (about 450 kΩ)	Moderate (about 45 kΩ)	Low (about 25 Ω)
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift between input & output voltages	0 or 360°	180°	0 or 360°
Applications	for high frequency circuits	for audio frequency circuits	for impedance matching

2.4 Field Effect Transistor:

The field effect transistor is a semiconductor device, which depends for its operation on the control of current by an electric field. There are two of field effect transistors:

1. JFET (Junction Field Effect Transistor)
2. MOSFET (Metal Oxide Semiconductor Field Effect Transistor) The FET has

several advantages over conventional transistor.

1. In a conventional transistor, the operation depends upon the flow of majority and minority carriers. That is why it is called bipolar transistor. In FET the operation depends upon the flow of majority carriers only. It is called unipolar device.
2. The input to conventional transistor amplifier involves a forward biased PN junction with its inherently low dynamic impedance. The input to FET involves a reverse biased PN junction hence the high input impedance of the order of M-ohm.
3. It is less noisy than a bipolar transistor.
4. It exhibits no offset voltage at zero drain current.
5. It has thermal stability.
6. It is relatively immune to radiation.

The main disadvantage is its relatively small gain bandwidth product in comparison with conventional transistor.

2.4.1 Operation of FET:

Consider a sample bar of N-type semiconductor. This is called N-channel and it is electrically equivalent to a resistance as shown in **fig. 1**.

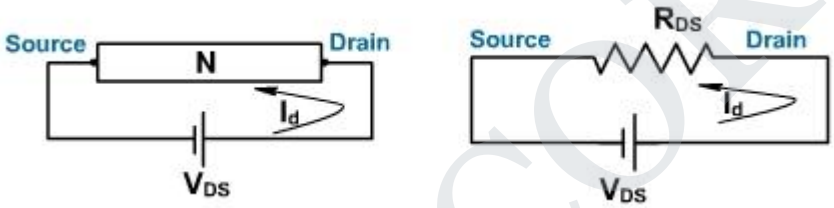


Fig. 1

Ohmic contacts are then added on each side of the channel to bring the external connection. Thus if a voltage is applied across the bar, the current flows through the channel.

The terminal from where the majority carriers (electrons) enter the channel is called source designated by S. The terminal through which majority carriers leaves the channel is called drain and designated by D. For an N-channel device, electrons are the majority carriers. Hence the circuit behaves like a dc voltage V_{DS} applied across a resistance R_{DS}. The resulting current is the drain current I_D. If V_{DS} increases, I_D increases proportionally.

Now on both sides of the n-type bar heavily doped regions of p-type impurity have been formed by any method for creating pn junction. These impurity regions are called gates (gate1 and gate2) as shown in **fig. 2**.

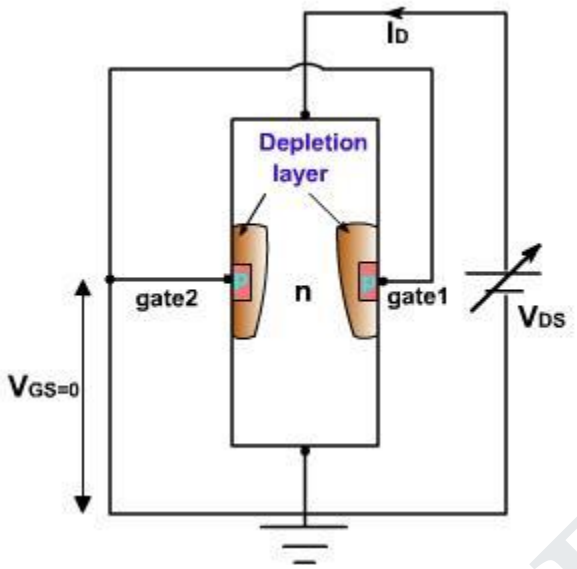


fig. 2.

Both the gates are internally connected and they are grounded yielding zero gate source voltage (V_{GS} =0). The word gate is used because the potential applied between gate and source controls the channel width and hence the current.

As with all PN junctions, a depletion region is formed on the two sides of the reverse biased PN junction. The current carriers have diffused across the junction, leaving only uncovered positive ions on the n side and negative ions on the p side. The depletion region width increases with the magnitude of reverse bias. The conductivity of this channel is normally zero because of the unavailability of current carriers.

The potential at any point along the channel depends on the distance of that point from the drain, points close to the drain are at a higher positive potential, relative to ground, then points close to the source. Both depletion regions are therefore subject to greater reverse voltage near the drain. Therefore the depletion region width increases as we move towards drain. The flow of electrons from source to drain is now restricted to the narrow channel between the no conducting depletion regions. The width of this channel determines the resistance between drain and source.

Consider now the behavior of drain current I_D vs drain source voltage V_{DS}. The gate source voltage is zero therefore V_{GS}= 0. Suppose that V_{DS} is gradually linearly increased linearly from 0V. I_D also increases.

Since the channel behaves as a semiconductor resistance, therefore it follows ohm's law. The region is called ohmic region, with increasing current, the ohmic voltage drop between the source and the channel region reverse biased the junction, the conducting portion of the channel begins to constrict and I_D begins to level off until a specific value of V_{DS} is reached, called the **pinch of voltage V_P**.

At this point further increase in V_{DS} do not produce corresponding increase in I_D. Instead, as V_{DS} increases, both depletion regions extend further into the channel, resulting in a no more cross section, and hence a higher channel resistance. Thus even though, there is more voltage, the resistance is also greater and the current remains relatively constant. This is
called pinch off or saturation region. The current in this region is maximum current that FET can produce and designated by I_{DSS}. (Drain to
source current with gate shorted)

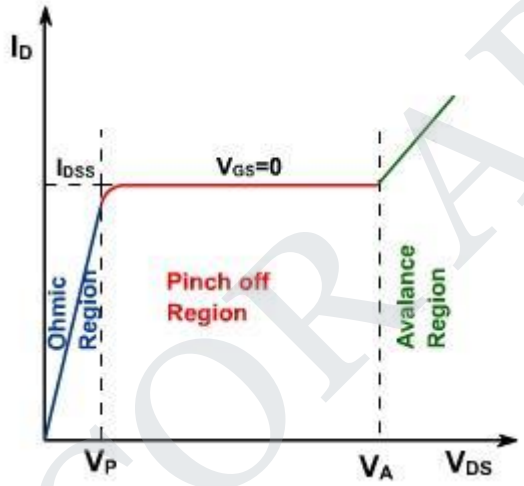


Fig. 3

As with all pn junctions, when the reverse voltage exceeds a certain level, avalanche breakdown of pn junction occurs and I_D rises very rapidly as shown in **fig. 3**.

Consider now an N-channel JFET with a reverse gate source voltage as shown in **fig. 4**.

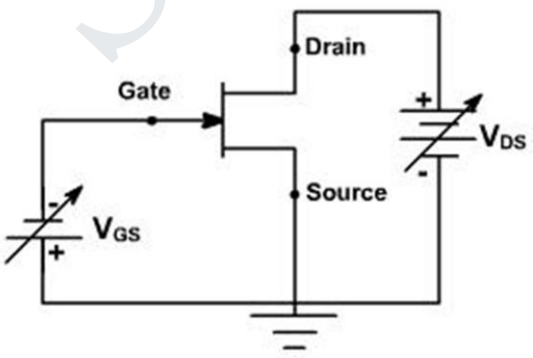


Fig. 4

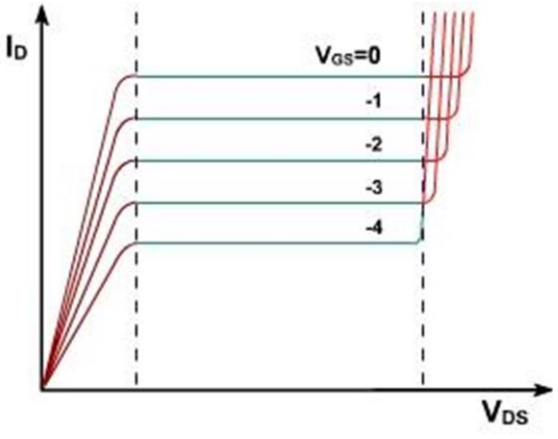


Fig. 5

The additional reverse bias, pinch off will occur for smaller values of | V_{DS} |, and the maximum drain current will be smaller. A family of curves for different values of V_{GS}(negative) is shown in **fig. 5**.

Suppose that V_{GS}= 0 and that due of V_{DS} at a specific point along the channel is +5V with respect toground. Therefore reverse voltage across either p-n junction is now 5V. If V_{GS} is decreased from 0 to –1V the net reverse bias near the point is 5 - (-1) = 6V. Thus for any fixed value of V_{DS}, the channel width decreases as V_{GS} is made more negative.

Thus I_D value changes correspondingly. When the gate voltage is negative enough, the depletion layers touch each other and the conducting channel pinches off (disappears). In this case the drain current is cut off. The gate voltage that produces cut off is symbolized V_{GS}(off) . It is same as pinch off voltage.

Since the gate source junction is a reverse biased silicon diode, only a very small reverse current flows through it. Ideally gate current is zero. As a result, all the free electrons from the source go to the draini.e. I_D = I_S. Because the gate draws almost negligible reverse current the input resistance is very high 10's or 100's of M ohm. Therefore where high input impedance is required, JFET is preferred over BJT. The disadvantage is less control over output current i.e. FET takes larger changes in input voltage to produce changes in output current. For this reason, JFET has less voltage gain than a bipolar amplifier.

Transductance Curves:

The transductance curve of a JFET is a graph of output current (I_D) vs input voltage (V_{GS}) as shown in **fig. 1**.

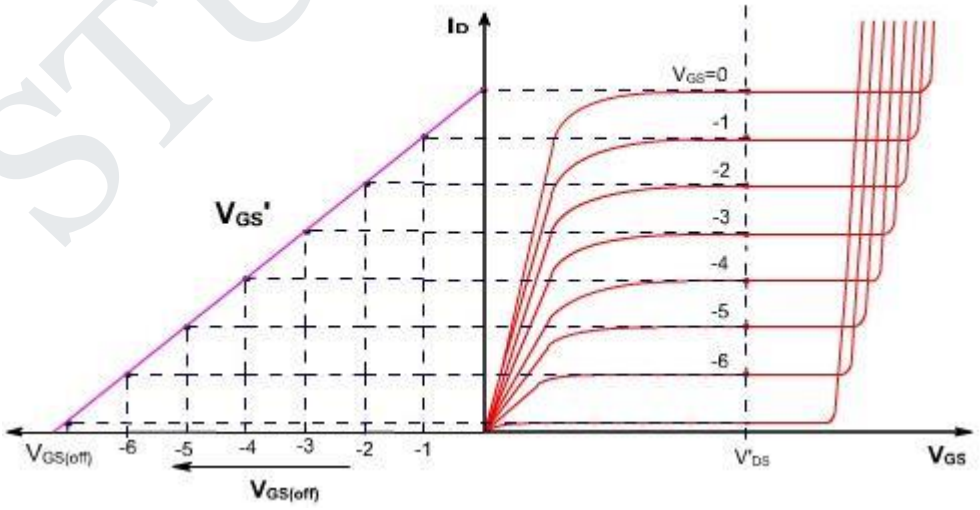


Fig. 1

By reading the value of I_D and V_{GS} for a particular value of V_{DS}, the transductance curve can be

plotted. The transductance curve is a part of parabola. It has an equation of

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(Off)}}\right)^2$$

Data sheet provides only I_{DSS} and V_{GS}(off) value. Using these values the transductance curve can be plotted.

2.5 MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

- Like JFET, it has a source, Drain and Gate.
- It is also called IGFET (Insulated Gate FET) because gate terminal is insulated from channel. Therefore it has extremely high input resistance.

➢ **Types of MOSFET**

It has two types

- Depletion mode MOSFET
  - N-channel
  - P-channel
- Enhancement mode MOSFET
  - N-channel
  - P-channel

The enhancement-type MOSFET is usually referred to as an E-MOSFET, and the depletion type, a D-MOSFET. The drain current in a MOSFET is controlled by the gate-source voltage VGS.

2.5.1 Depletion mode-MOSFET [D-MOSFET]

In depletion mode of operation the bias voltage on the gate reduce the number of charge carriers in the channel and therefore reduce the drain current I_D. It operates in both depletion
mode and enhancement mode.

➢ **Symbol**

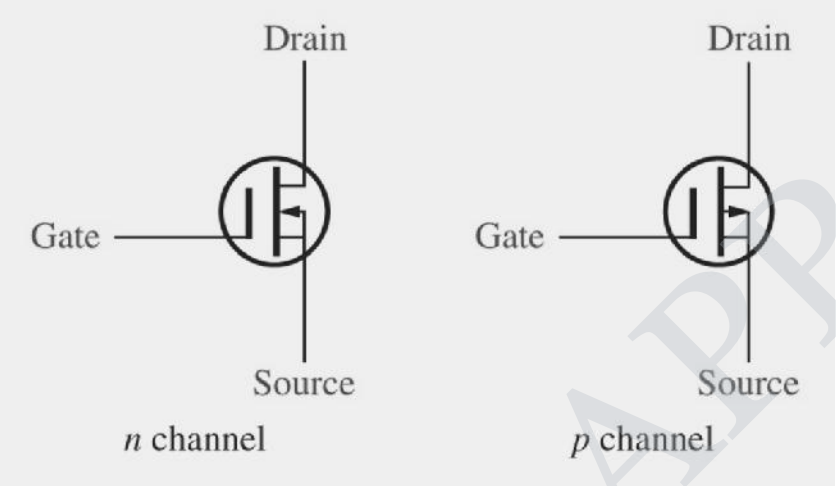


Figure 3.5 D-MOSFET symbol for n-channel and p-channel

2.5.2 Construction

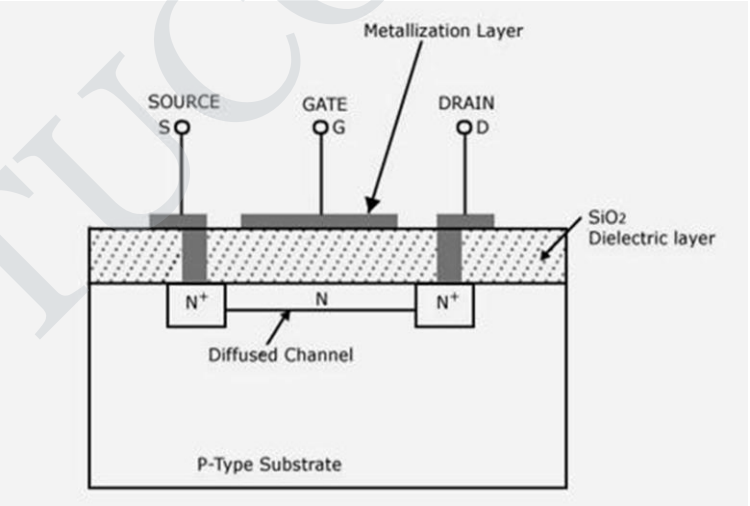


Figure 3.6 structure of n-channel D-MOSFET

- It consists of lightly doped p-type substrate in which two highly doped n-regions are diffused.
- The source and drain terminals are connected through metallic contacts to n-doped

regions linked by an n-channel. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing (as revealed by the prefix di-) electric fields within the dielectric when exposed to an externally applied field.

- Then the thin layer of metal aluminium is formed over the Sio_2 layer. This metal overs the entire channel region and it forms the gate(G).

2.5.3 Operation of N-channel D-MOSFET

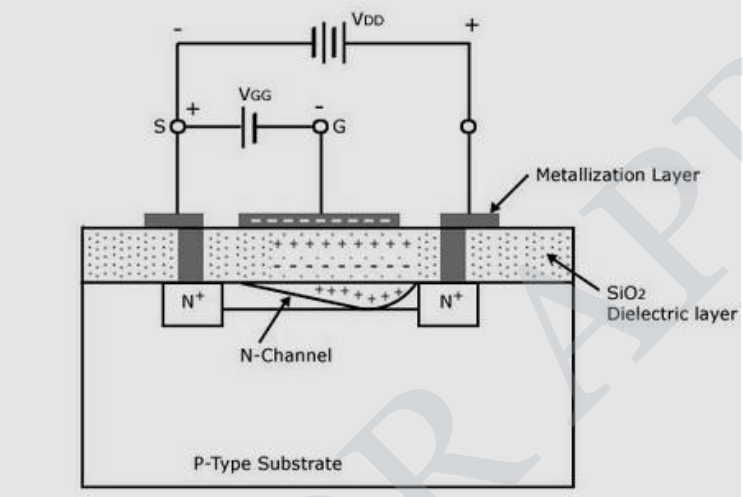


Figure 3.7 n-channel D-MOSFET under applied bias

Case (i) "when and is increased from zero"

- Here N-base (Drain) is connected to positive supply. It act as a reverse bias. Due to this, depletion region gets increases.
- Free electron from n-channel are attracted towards positive potential of drain terminal. This establishes current through channel flows from drain to source and denoted as I_{DSS}.

Pinch of voltage

The pinch off voltage is the voltage at which the junction is depleted of charge carriers.

Case (ii) "whenand is increased from zero"

- The negative charge on gate repels conduction electrons from the channel and attract holes from the p-type substrate.
- Due to this electron-hole recombination occurs and reduce the number of free electrons in the channel available for conduction, reducing Drain current (I_D).
- When negative voltage of is incresed the pinch of voltage decreased. When is further increased the channel is fully depleted and no current flows through it.

- The negative voltage depletion MOSFET.

➢ **Characteristics curve**

Two types

- Drain characteristics [ ]
- Transfer characteristics [ ]

D-MOSFET's are biased to operate in two modes :depletion or enhancement mode.

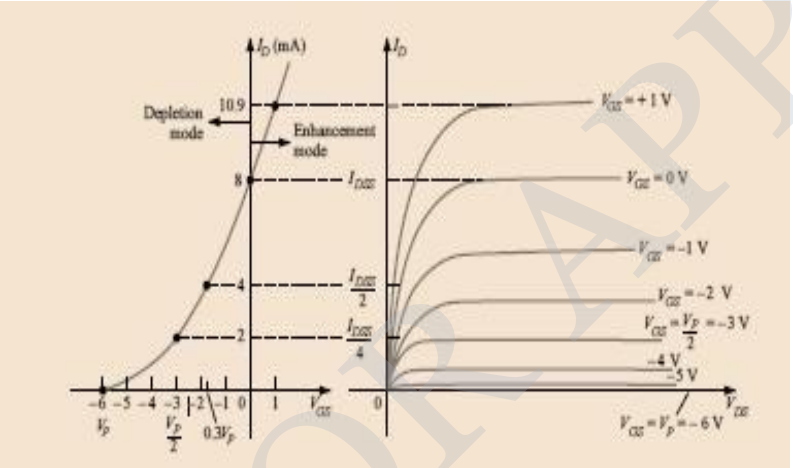


Figure 3.8 Drain and transfer characteristics

2.5.4 ENHANCEMENT- MODE MOSFET [E-MOSFET]

- In this mode bias on the gate increases the number of charge carriers in the channel and increases the drain current (I_D).
- It operates only in the enhancement mode and has no depletion mode of operation.It has no physical channel.

- **Symbol of E-MOSFET**

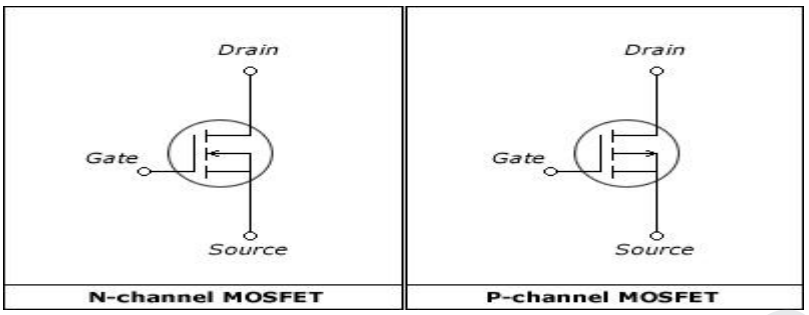


Figure 3.9 symbol of n-channel and p0channel E-MOSFET

- **Basic Construction**

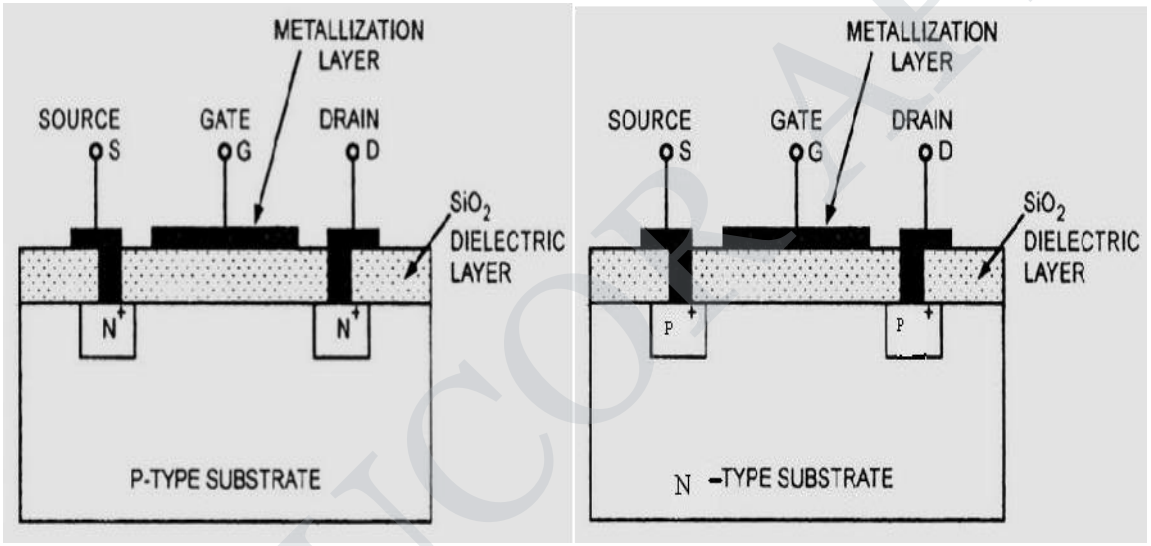


Figure 3.10 Construction of n-channel and p-channel E-MOSFET

In the basic construction of the n-channel enhancement-type MOSFET, a slab of p-type material is formed from a silicon base and is again referred to as thesubstrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level.

The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-typ material.

In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

➢ **Operation**

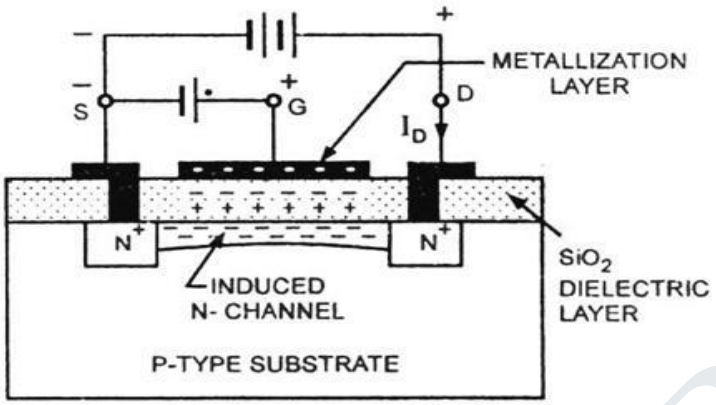
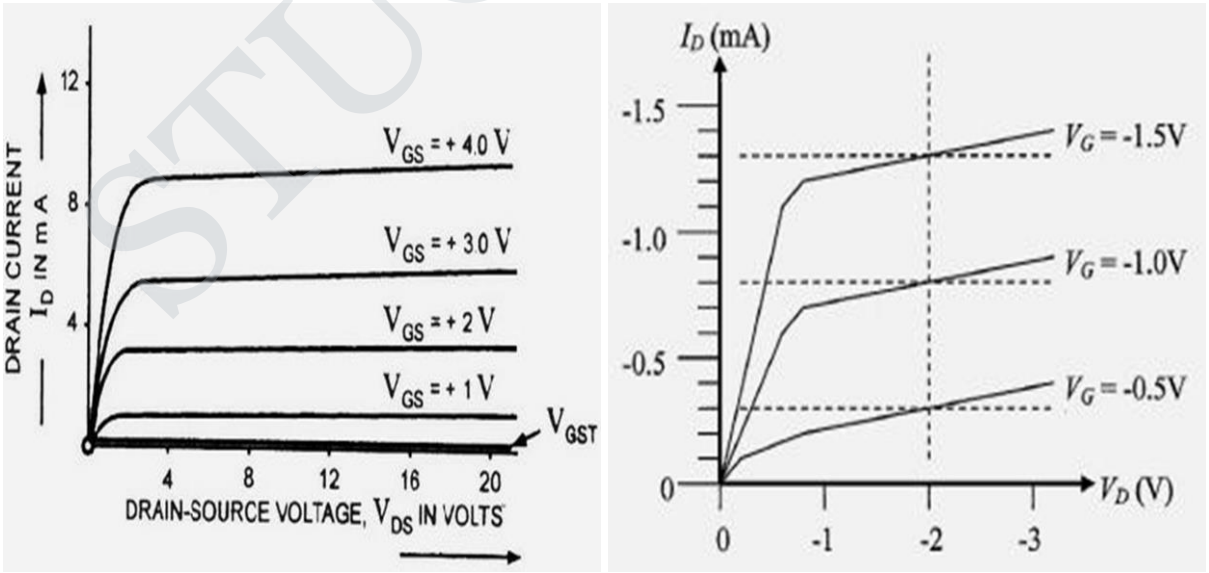


Figure 3.11 N-channel E-MOSFET under applied bias

- If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device, the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion- type MOSFET and JFET where I_D - I_{DSS}.
- It is not sufficient to saturation level as occurred for the JFET and depletion-type MOSFET.
- The conductivity of the channel is enhanced by the positive bias voltage on the gate, the device is known as enhancement MOSFET. E-MOSFET's are normally called as "OFF – MOSFET"

➢ **Characteristics of E-MOSFET**

Drain characteristics curve



a) N-channe b) P-channel

Figure 3.12 Drain characteristics curve a) n-channel b) p-channel

2.6 BIASING

2.6.1 Fixed Bias or Base Bias:

In order for a transistor to amplify, it has to be properly biased. This means forward biasing the base emitter junction and reverse biasing collector base junction. For linear amplification, the transistor should operate in active region (If I_E increases, I_C increases, V_{CE} decreases proportionally).

The source V_{BB}, through a current limit resistor R_B forward biases the emitter diode and V_{CC} through resistor R_C (load resistance) reverse biases the

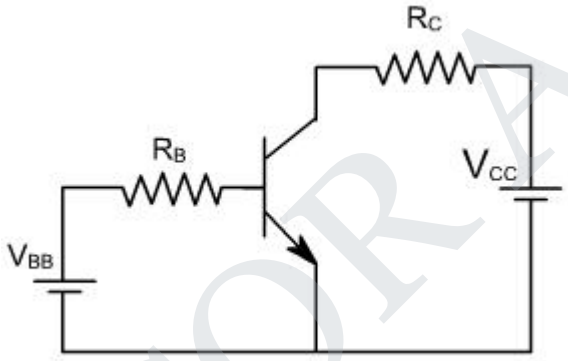


Fig. 1

The dc base current through R_B is given by

$I_B = (V_{BB} - V_{BE}) / R_B$

or $V_{BE} = V_{BB} - I_B R_B$

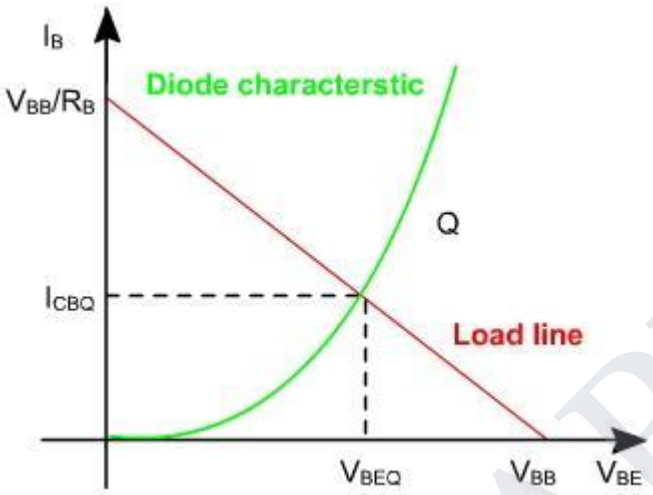
Normally V_{BE} is taken 0.7V or 0.3V. If exact voltage is required, then the input characteristic (I_B vs V_{BE}) of the transistor should be used to solve the above equation. The load line for the input circuit is drawn on input characteristic. The two points of the load line can be obtained as given below

For $I_B = 0$, $V_{BE} = V_{BB}$.

and For $V_{BE} = 0$, $I_B = V_{BB}/ R_B$.

The intersection of this line with input characteristic gives the operating point Q as shown in **fig. 2**. If an ac signal is connected to the base of the transistor, then variation in V_{BE} is about Q -

point. This gives variation in I_B and hence I_C.



In the output circuit, the load equation can be written as

$V_{CE} = V_{CC} - I_C R_C$

This equation involves two unknown V_{CE} and I_C and therefore can not be solved. To solve this equation output characteristic (I_C vs V_{CE}) is used.

The load equation is the equation of a straight line and given by two points: $I_C = 0$,

$V_{CE} = V_{CC}$

& $V_{CE} = 0$, $I_C = V_{CC} / R_C$

The intersection of this line which is also called dc load line and the characteristic gives the operating point Q as shown in **fig. 3**.

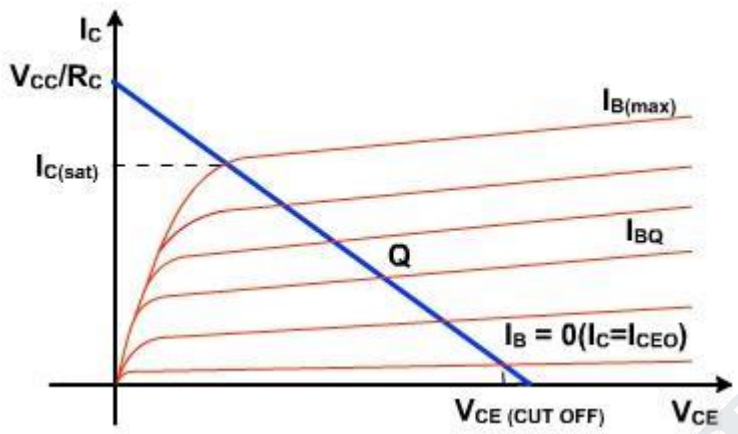


Fig. 3

The point at which the load line intersects with $I_B = 0$ characteristic is known as cut off point. At this point base current is zero and collector current is almost negligibly small. At cut off the emitter diode comes out of forward bias and normal transistor action is lost. To a close approximation.

V_{CE} (cut off)V_{CC} (approximately).

The intersection of the load line and $I_B = I_{B(max)}$ characteristic is known as saturation point . At this point $I_B = I_{B(max)}$, $I_C = I_{C(sat)}$. At this point collector diodes comes out of reverse bias and again transistor action is lost. To a close approximation,

$I_{C(sat)}$ V_{CC} / R_C(approximately).

The $I_{B(sat)}$ is the minimum current required to operate the transistor in saturation region. If the I_B is less than I_B (sat), the transistor will operate in active region. If $I_B > I_B$ (sat) it always operates in saturation region.

If the transistor operates at saturation or cut off points and no where else then it is operating as a switch is shown in **fig. 4**.

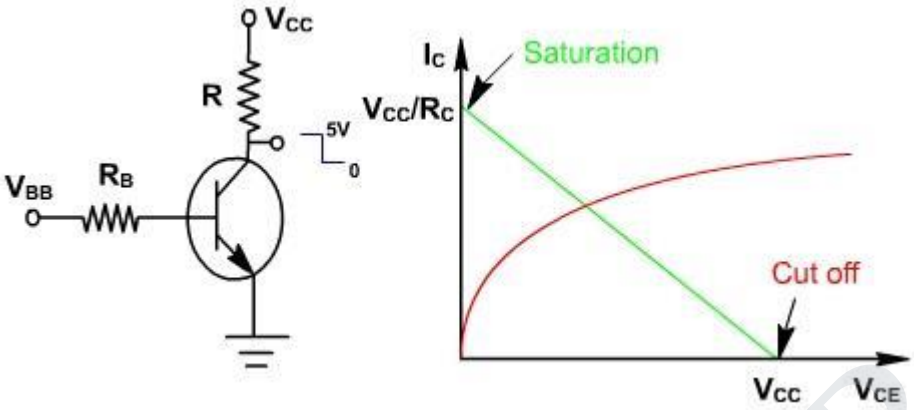


Fig. 4

$V_{BB} = I_B R_B + V_{BE}$

$I_B = (V_{BB} - V_{BE}) / R_B$

If $I_B > I_{B(sat)}$, then it operates at saturation, If $I_B = 0$, then it operates at cut off.

If a transistor is operating as an amplifier then Q point must be selected carefully. Although we can select the operating point any where in the active region by choosing different values of R_B & R_C but the various transistor ratings such as maximum collector dissipation $P_{C(max)}$ maximum collector voltage $V_{C(max)}$ and $I_{C(max)}$ & $V_{BE(max)}$ limit the operating range.

Once the Q point is established an ac input is connected. Due to this the ac source the base current varies. As a result of this collector current and collector voltage also varies and the amplified output is obtained.

If the Q-point is not selected properly then the output waveform will not be exactly the input waveform. i.e. It may be clipped from one side or both sides or it may be distorted one.

- **Stability of Operating Point**

Let us consider three operating points of transistor operating in common emitter amplifier.

1. Near cut off
2. Near saturation
3. In the middle of active region

If the operating point is selected near the cutoff region, the output is clipped in negative half cycle as shown in **fig. 1**.

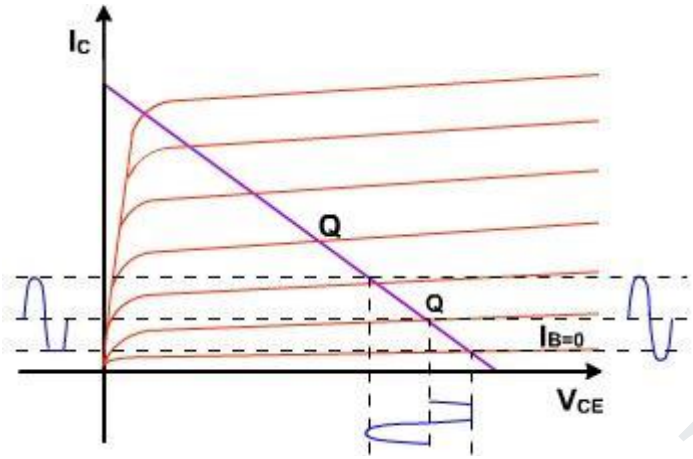


Fig. 1

If the operating point is selected near saturation region, then the output is clipped in positive cycle as shown in **fig. 2**.

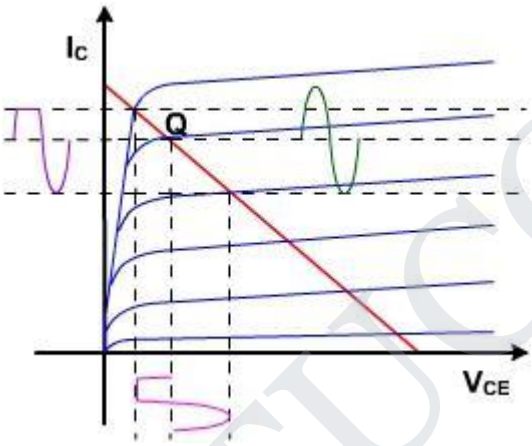


Fig. 2

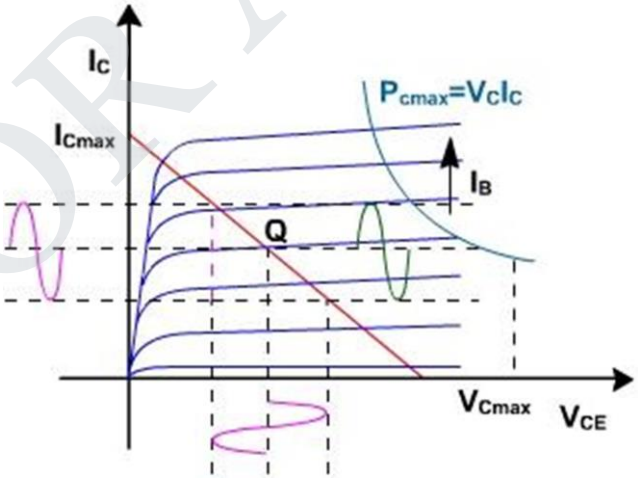


Fig. 3

If the operating point is selected in the middle of active region, then there is no clipping and the output follows input faithfully as shown in **fig. 3**. If input is large then clipping at both sides will take place. The first circuit for biasing the transistor is CE configuration is fixed bias.

In biasing circuit shown in **fig. 4(a)**, two different power supplies are required. To avoid

the use of two supplies the base resistance R_B is connected to V_{CC} as shown in **fig. 4(b)**.

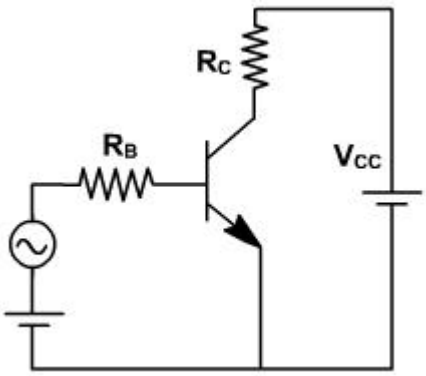


Fig. 4(a)

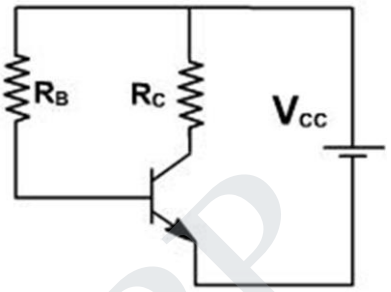


Fig. 4(b)

Now V_{CC} is still forward biasing emitter diode. In this circuit Q point is very unstable. The base resistance R_B is selected by noting the required base current I_B for operating point Q.

$I_B = (V_{CC} - V_{BE}) / R_B$

Voltage across base emitter junction is approximately 0.7 V. Since V_{CC} is usually very high

i.e. $I_B = V_{CC} / R_B$

Since I_B is constant therefore it is called fixed bias circuit.

2.7 UNI JUNCTION TRANSISTOR (UJT)

Unijunction transistor (abbreviated as UJT), also called the double-base diode is a 2-layer, 3-terminal solid-state (silicon) switching device. The device has-a unique characteristic that when it is triggered, its emitter current increases re generatively (due to negative resistance characteristic) until it is restricted by emitter power supply. Since the device has one pn junction and three leads it is commonly called UJT.

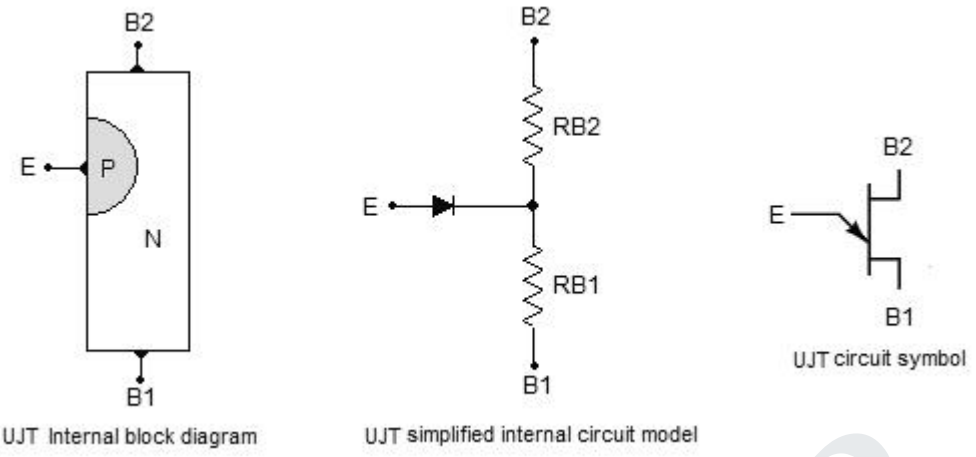


Figure 5.1 UJT structure, Equivalent circuit and Symbol

2.7.1 Construction of a UJT

The basic structure of a unijunction transistor is shown in figure. It essentially consists of a lightly-doped N-type silicon bar with a small piece of heavily doped P-type material alloyed to its one side to produce single P-N junction. The single P-N junction accounts for the terminology unijunction. The silicon bar, at its ends, has two ohmic contacts designated as base-1 (B_1) and base-2 (B_2), as shown and the P-type region is termed the emitter (E). The emitter junction is usually located closer to base-2 (B_2) than base-1 (B_1) so that the device is not symmetrical, because symmetrical unit does not provide optimum electrical characteristics for most of the applications.

The symbol for unijunction transistor is shown in figure. The emitter leg is drawn at an angle to the vertical line representing the N-type material slab and the arrowhead points in the direction of conventional current when the device is forward-biased, active or in the conducting state. The basic arrangement for the UJT is shown in figure.

A complementary UJT is formed by diffusing an N-type emitter terminal on a P-type base. Except for the polarities of voltage and current, the characteristics of a complementary UJT are exactly the same as those of a conventional UJT.

- The device has only one junction, so it is called the unijunction device.
- The device, because of one P-N junction, is quite similar to a diode but it differs from an ordinary diode as it has three terminals.
- The structure of a UJT is quite similar to that of an N-channel JFET. The main difference is that P-type (gate) material surrounds the N-type (channel) material in case of JFET and the gate surface of the JFET is much larger than emitter junction of UJT.

- In a unijunction transistor the emitter is heavily doped while the N-region is lightly doped, so the resistance between the base terminals is relatively high, typically 4 to 10 kilo Ohm when the emitter is open.
- The N-type silicon bar has a high resistance and the resistance between emitter and base-1 is larger than that between emitter and base-2. It is because emitter is closer to base-2 than base-1.
- UJT is operated with emitter junction forward- biased while the JFET is normally operated with the gate junction reverse-biased.
- UJT does not have ability to amplify but it has the ability to control a large ac power with a small signal. It exhibits a negative resistance characteristic and so it can be employed as an oscillator.

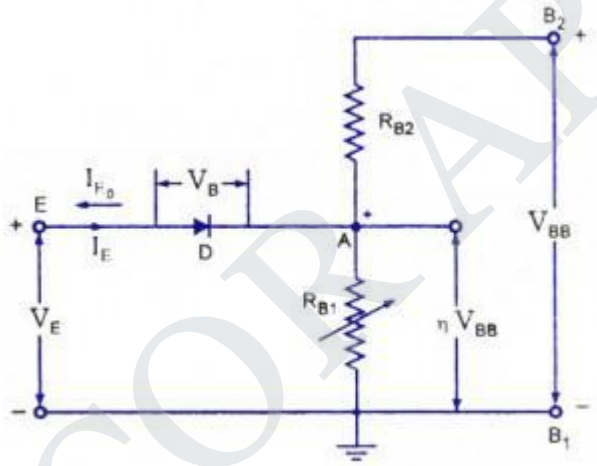


Figure 5.2 Equivalent circuit of UJT

2.7.2 UJT parameters

R_{BBO} : It is the resistance between the terminals B1 and B2. In simple words, it is the resistance of the N-Type bar when measured lengthwise. If RB1 is resistance of the bar from E to B1 and RB2 is the resistance of the bar from E to B2, then R_{BBO} can be expressed as R_{BBO}= RB1
+RB2. The typical range of R_{BBO} is from 4KΩ to 10KΩ.

Intrinsic standoff ratio (η) : It is the ratio of RB1 to the sum of RB1 and RB2. It can be expressed as η = RB1/(RB1+RB2) or η = RB1/R_{BBO}. The typical range of intrinsic standoff ratio is from 0.4 to 0.8

- **Operation of a UJT**

Imagine that the emitter supply voltage is turned down to zero. Then the intrinsic stand-off voltage reverse-biases the emitter diode, as mentioned above. If V_B is the barrier voltage of the emitter diode, then the total reverse bias voltage is $V_A + V_B = \eta V_{BB} + V_B$. For silicon V_B = 0.7 V.

Now let the emitter supply voltage V_E be slowly increased. When V_E becomes equal to ηV_{BB}, I_{Eo} will be reduced to zero. With equal voltage levels on each side of the diode,

neither reverse nor forward current will flow.

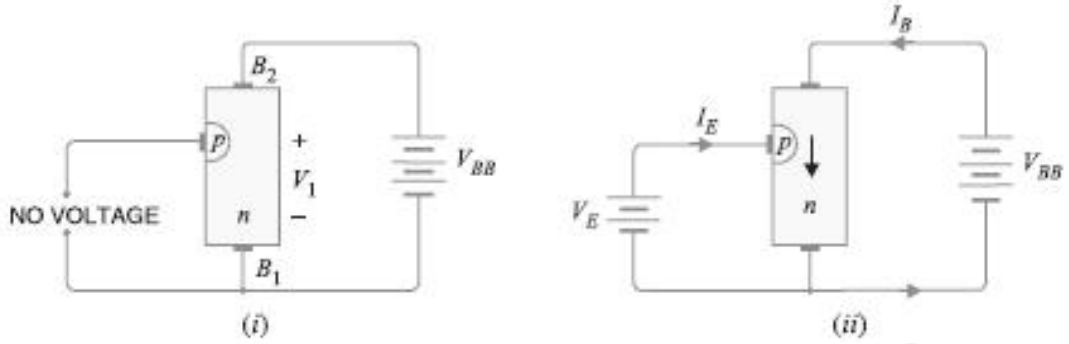


Figure 5.3 operation UJT under (i) V_E=0 (ii) applied V_E

When emitter supply voltage is further increased, the diode becomes forward-biased as soon as it exceeds the total reverse bias voltage (ηV_{BB} + V_B). This value of emitter voltage V_E is called the peak-point voltage and is denoted by V_P. When V_E = V_P, emitter current I_E starts to flow through R_{B1} to ground, that is B_1. This is the minimum current that is required to trigger the UJT. This is called the peak-point emitter current and denoted by I_P. Ip is inversely proportional to the interbase voltage, V_{BB}.

Now when the emitter diode starts conducting, charge carriers are injected into the RB region of the bar. Since the resistance of a semiconductor material depends upon doping, the resistance of region RB decreases rapidly due to additional charge carriers (holes). With this decrease in resistance, the voltage drop across RB also decrease, cause the emitter diode to be more heavily forward biased. This, in turn, results in larger forward current, and consequently more charge carriers are injected causing still further reduction in the resistance of the RB region. Thus the emitter current goes on increasing until it is limited by the emitter power supply. Since VA decreases with the increase in emitter current, the UJT is said to have negative resistance characteristic. It is seen that the base-2 (B2) is used only for applying external voltage VBB across it. Terminals E and B1 are the active terminals. UJT is usually triggered into conduction by applying a suitable positive pulse to the emitter. It can be turned off by applying a negative trigger pulse.

- **UJT Characteristics**

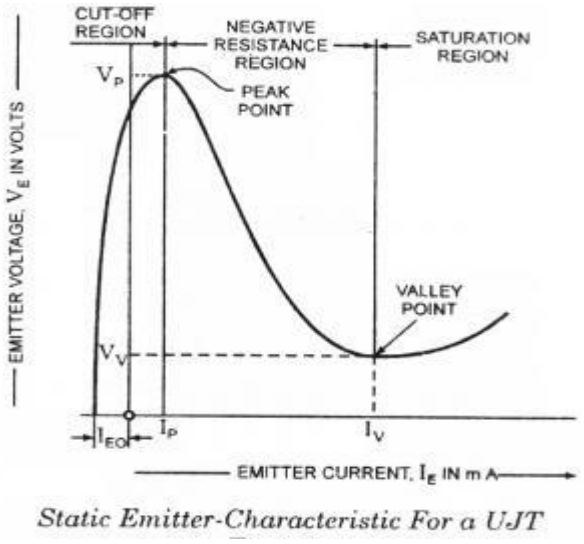


Figure 5.4 static Emitter Characteristics for a UJT

The static emitter characteristic (a curve showing the relation between emitter voltage V_E and emitter current I_E) of a UJT at a given inter base voltage V_{BB} is shown in figure. From figure it is noted that for emitter potentials to the left of peak point, emitter current I_E never exceeds I_{Eo} . The current I_{Eo} corresponds very closely to the reverse leakage current I_{Co} of the conventional BJT. This region, as shown in the figure, is called the cut-off region. Once conduction is established at $V_E = V_P$ the emitter potential V_E starts decreasing with the increase in emitter current I_E. This Corresponds exactly with the decrease in resistance R_B for increasing current I_E. This device, therefore, has a negative resistance region which is stable enough to be used with a great deal of reliability in the areas of applications listed earlier. Eventually, the valley point reaches, and any further increase in emitter current I_E places the device in the saturation region, as shown in the figure5.4.

Three other important parameters for the UJT are I_P, V_V and I_V and are defined below:

Peak-Point Emitter Current I_p : It is the emitter current at the peak point. It represents the rnimrnum current that is required to trigger the device (UJT). It is inversely proportional to the interbase voltage V_{BB}.

Valley Point Voltage V_V: The valley point voltage is the emitter voltage at the valley point. The valley voltage increases with the increase in interbase voltage V_{BB}.

Valley Point Current I_V: The valley point current is the emitter current at the valley point. It increases with the increase in inter-base voltage V_{BB}.

➢ **Special Features of UJT.**

The special features of a UJT are :

1. A stable triggering voltage (V_P)— a fixed fraction of applied inter base voltage V_{BB}.
2. A very low value of triggering current.
3. A high pulse current capability.
4. A negative resistance characteristic.
5. Low cost.

2.7.3 Applications of UJT.

- ✓ Relaxation oscillators.
- ✓ Switching Thyristors like SCR, TRIAC etc.
- ✓ Magnetic flux sensors.
- ✓ Voltage or current limiting circuit.
- ✓ Bistable oscillators.
- ✓ Voltage or current regulators.
- ✓ Phase control circuits.

- **UJT relaxation oscillator.**

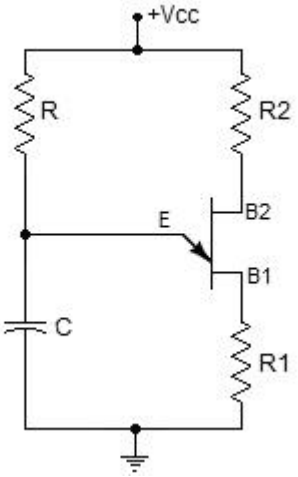


Figure 5.5 UJT relaxation oscillator

The circuit diagram of a UJT relaxation oscillator is given shown above. R1 and R2 are current limiting resistors. Resistor R and capacitor C determines the frequency of the oscillator.

The frequency of the UJT relaxation oscillator can be expressed by the equation

Where η is the intrinsic standoff ratio and *ln* stand for natural logarithm.

When power supply is switched ON the capacitor C starts charging through resistor R. The capacitor keeps on charging until the voltage across it becomes equal to 0.7V plus ηVbb. This voltage is the peak voltage point "Vp" denoted in the characteristics curve (Fig:2). After this point the emitter to RB1 resistance drops drastically and the capacitor starts discharging through this path. When the capacitor is discharged to the valley point voltage "Vv" (refer Fig : 1) the emitter to RB1 resistance climbs again and the capacitor starts charging. This cycle is repeated and results in a sort of sawtooth waveform across the capacitor. The saw tooth waveform across the capacitor of a typical UJT relaxation oscillator is shown in the figure below.

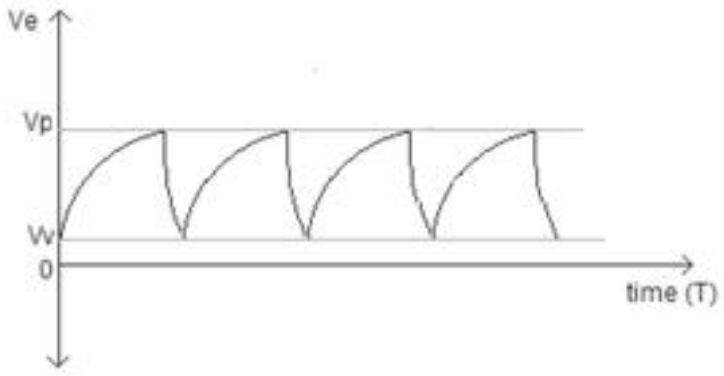


Figure 5.6 wave across the capacitor in a UJT relaxation oscillator

2.8 SILICON CONTROLLED RECTIFIER (SCR)

2.8.1 Introduction

The SCR stand for Silicon Control Rectifier, it is used in industries because it can handle high values of current and voltage.

Three terminals

- Anode - P-layer
- Cathode - N-layer (opposite end)
- Gate - P-layer near the cathode

Three junctions - four layers

Connect power such that the anode is positive with respect to the cathode - no current will flow

A silicon controlled rectifier is a semiconductor device that acts as a true electronic switch. It can change alternating current and at the same time can control the amount of power fed to the load. SCR combines the features of a rectifier and a transistor.

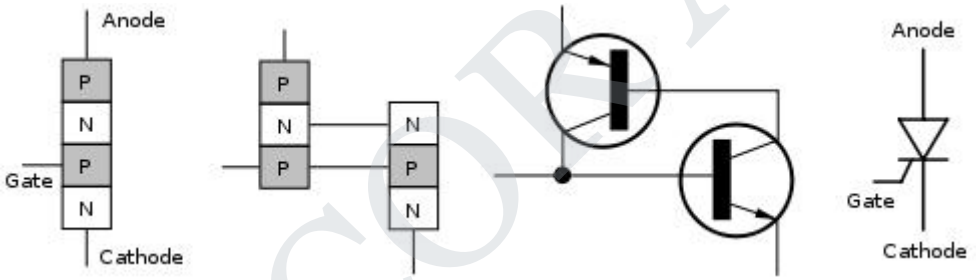


Figure 5.7 Basic Structure, equivalent transistor model and symbol of SCR

- **Construction**

When a pn junction is added to a junction transistor the resulting three pn junction device is called a SCR. ordinary rectifier (pn) and a junction transistor (npn) combined in one unit to form pnpn device.

Three terminals are taken : one from the outer p- type material called anode a second from the outer n- type material called cathode K and the third from the base of transistor called Gate. GSCR is a solid state equivalent of thyratron. The gate anode and cathode of SCR correspond to the grid plate and cathode of thyratron SCR is called thyristor.

- **Working Principle**

Load is connected in series with anode the anode is always kept at positive potential w.r.t cathode.

- **SCR Operation / Working**

The Silicon Control Rectifier SCR start conduction when it is forward biased. For this purpose the cathode is kept at negative and anode at positive. When positive clock pulse is applied at the gate the SCR turns ON.

When forward bias voltage is applied to the Silicon Control Rectifier SCR, the junction J1 and J3 become forward bias while the junction J2 become reverse bias.

When we apply a clock pulse at the gate terminal, the junction J2 become forward bias and the Silicon Control Rectifier SCR start conduction.The Silicon Control Rectifier SCR turn ON and OFF very quickly, At the OFF state the Silicon Control Rectifier SCR provide infinity resistance and in ON state, it offers very low resistance, which is in the range of 0.01Ω to 1Ω.

- **SCR Firing & Triggering**

The Silicon Control Rectifier SCR is normally operated below the forward break over voltage (VBO). To turn ON the Silicon Control Rectifier SCR we apply clock pulse at the gate terminal which called triggering of Silicon Control Rectifier, but when the Silicon Control Rectifier SCR turned ON, now if we remove the triggering voltage, the Silicon Control Rectifier SCR will remain in ON state. This voltage is called Firing voltage.

- **When Gate is Open**

No voltage applied to the gate, j2 is reverse biased while j1 and j3 are FB . J1 and J3 is just in npn transistor with base open .no current flows through the load RL and SCR is cut off. If the applied voltage is gradually increased a stage is reached when RB junction J2 breakdown .the SCR now conducts heavily and is said to be ON state. the applied voltage at which SCR conducts heavily without gate voltage is called Break over Voltage.

- **When Gate is Positive w.r.to Cathode:-**

The SCR can be made to conduct heavily at smaller applied voltage by applying small positive potential to the gate.J3 is FB and J2 is RB the electron from n type material start moving across J3 towards left holes from p type toward right. Electrons from j3 are attracted across junction J2 and gate current starts flowing. as soon as gate current flows anode current increases. the increased anode current in turn makes more electrons available at J2 breakdown and SCR starts conducting heavily. the gate loses all control if the gate voltage is removed anode current does not decrease at all. The only way to stop conduction is to reduce the applied voltage to zero.

- **Break over Voltage**

It is the minimum forward voltage gate being open at which SCR starts conducting heavily i.e turned on.

- **Peak Reverse Voltage (PRV)**

It is the maximum reverse voltage applied to an SCR without conducting in the reverse direction.

- **Holding Current**

It is the maximum anode current gate being open at which SCR is turned off from on conditions.

2.8.2 V-I Characteristics of SCR

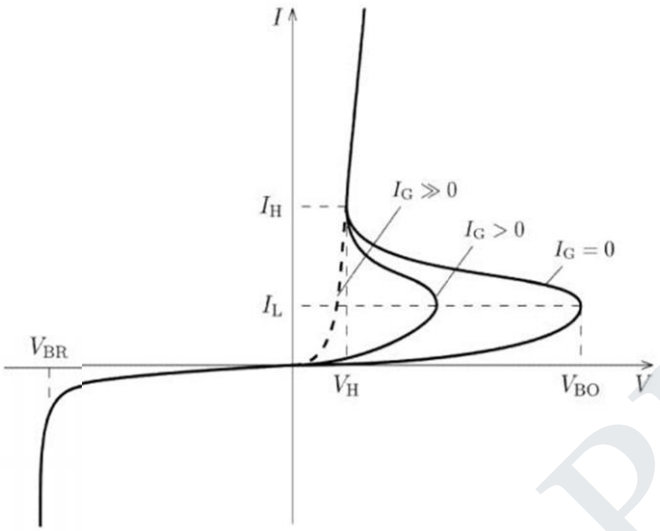


Figure 5.9 V-I Characteristics of SCR

- **Forward Characteristics** When anode is +vew.r.t cathode the curve between V &I is called Forward

characteristics. OABC is theforward characteristics of the SCR at Ig =0. if the suppliedvoltage is increased from zero point A is reached .SCR starts conducting voltage across SCR
suddenly drops (dotted curve AB) most of supply voltage appears across RL

- **Reverse Characteristics**

When anode is –ve w.r.t cathode the curve b/w V&I is known as reverse characteristics reverse voltage come across SCR when it is operated with ac supply reverse voltage is increased anode current remains small avalanche breakdown occurs and SCR starts conducting heavily is known as reverse breakdown voltage.

- **Application**

  - ✓ SCR as a switch
  - ✓ SCR Half and Full wave rectifier
  - ✓ SCR as a static contactor
  - ✓ SCR for power control
  - ✓ SCR for speed control of d.c.shunt motor
  - ✓ Over light detector

2.8.3 DIAC (DIODE A.C. SWITCH)

The DIAC is a full-wave or bi-directional semiconductor switch that can be turned on in both forward and reverse polarities.The DIAC gains its name from the contraction of the words DIode Alternating Current.

The DIAC is widely used to assist even triggering of a TRIAC when used in AC switches.

DIACs are mainly used in dimmer applications and also in starter circuits for florescent lamps.

A Diac is two terminal , three layer bi directional device which can be switched from its off state for either polarity of applied voltage.

- **Circuit symbol**

The DIAC circuit symbol is generated from the two triangles held between two lines as shown below. In some way this demonstrates the structure of the device which can be considered also as two junctions

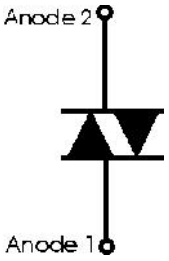


Figure 5.10 symbol of DIAC

The two terminals of the device are normally designated either Anode 1 and Anode 2 or Main Terminals 1 and 2, i.e. MT1 and MT2.

- **Construction**

The DIAC can be constructed in either npn or pnp form. The two leads are connected to p regions of silicon separated by an n- region. The structure of DIAC is similar to that of a transistor differences are

- ✓ There is no terminal attached to the base layer
- ✓ The three regions are nearly identical in size. The doping concentrations are identical to give the device symmetrical properties.

The DIAC can e fabricated as either a two layer or a five layer structure. In the three layer structure the switching occurs when the junction that is reverse biased experiences reverse breakdown. The three layer version of the device is the more common and can have a break-over voltage of around 30 V. Operation is almost symmetrical owing to the symmetry of the device.

A five layer DIAC structure is also available. This does not act in quite the same manner, although it produces an I-V curve that is very similar to the three layer version. It can be considered as two break-over diodes connected back to back.

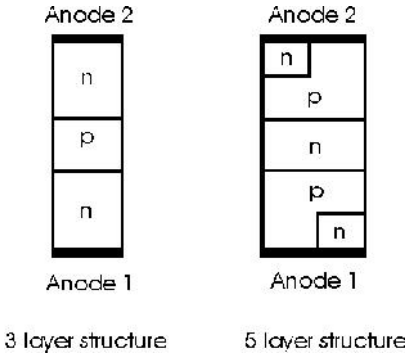


Figure 5.11 The structure of a DIAC

For most applications a three layer version of the DIAC is used. It provides sufficient improvement in switching characteristics. For some applications the five layer device may be used.

- **Operation**

When a positive or negative voltage is applied across the terminals of Diac only a small leakage current Ibo will flow through the device as the applied voltage is increased , the leakage current will continue to flow until the voltage reaches breakover voltage Vbo at this point avalanche breakdown of the reverse biased junction occurs and the device exhibits negative resistance i.e current through the device increases with the decreasing values of applied voltage the voltage across the device then drops to break back voltage Vw.

- **V- I characteristics of a DIAC**

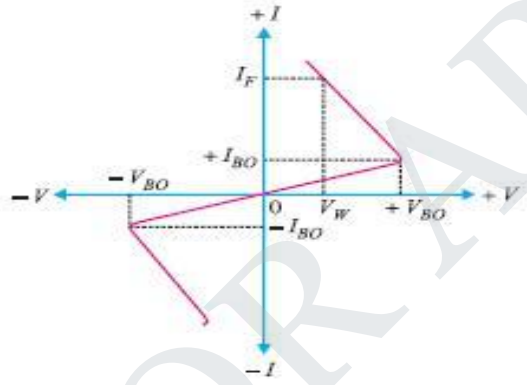


Figure 5.11 V- I characteristics of a DIAC

For applied positive voltage less than + Vbo and Negative voltage less than -Vbo , a small leakage current flows thrugh the device. Under such conditions the diac blocks flow of current and behaves as an open circuit. the voltage +Vbo and -Vbo are the breakdown voltages and usually have range of 30 to 50 volts.

When the positive or negative applied voltage is equal to or greater than tha breakdown voltage Diac begins to conduct and voltage drop across it beco mes a few volts conduction then continues until the device current drops below its holding current breakover voltage and holding current values are identical for the forward and reverse regions of operation.

- **Applications**

Diacs are used for triggering of triacs in adjustable phase control of a c mains power. Applications are light dimming heat control universal motor speed control.Typically the DIAC is placed in series with the gate of a TRIAC. DIACs are often used in conjunction with TRIACs because these devices do not fire symmetrically as a result of slight differences between the two halves of the device. This results in harmonics being generated, and the less symmetrical the device fires, the greater the level of harmonics produced. It is generally undesirable to have high levels of harmonics in a power system.

Anode 2

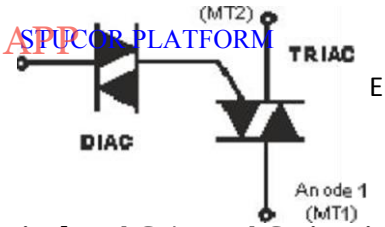


Figure 5.12 Typical DIAC / TRIAC circuit configuration

To help in overcoming this problem, a DIAC is often placed in series with the gate. This device helps make the switching more even for both halves of the cycle. This results from the fact that its switching characteristic is far more even than that of the TRIAC. Since the DIAC prevents any gate current flowing until the trigger voltage has reached a certain voltage in either direction, this makes the firing point of the TRIAC more even in both directions.

2.8.4 TRIAC

The TRIAC is a three terminal semiconductor device for controlling current. It gains its name from the term TRIode for Alternating Current.

It is effectively a development of the SCR or thyristor, but unlike the thyristor which is only able to conduct in one direction, the TRIAC is a bidirectional device.

- **TRIAC symbol**

The circuit symbol recognises the way in which the TRIAC operates. Seen from the outside it may be viewed as two back to back thyristors and this is what the circuit symbol indicates.

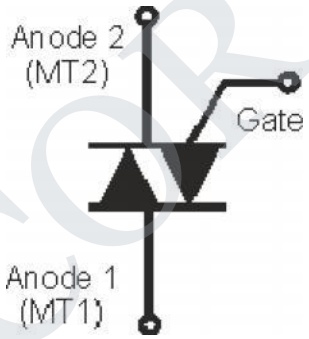


Figure 5.13 TRIAC symbol for circuit diagrams

On the TRIAC symbol there are three terminals. These are the Gate and two other terminals are often referred to as an "Anode" or "Main Terminal". As the TRIAC has two of these they are labelled either Anode 1 and Anode 2 or Main Terminal, MT1 and MT2.

- **TRIAC basics**

The TRIAC is a component that is effectively based on the thyristor. It provides AC switching for electrical systems. Like the thyristor, the TRIACs are used in many electrical switching applications. They find particular use for circuits in light dimmers, etc., where they enable both halves of the AC cycle to be used.

This makes them more efficient in terms of the usage of the power available. While it is possible to use two thyristors back to back, this is not always cost effective for low cost and relatively low power applications.

It is possible to view the operation of a TRIAC in terms of two thyristors placed back to back.

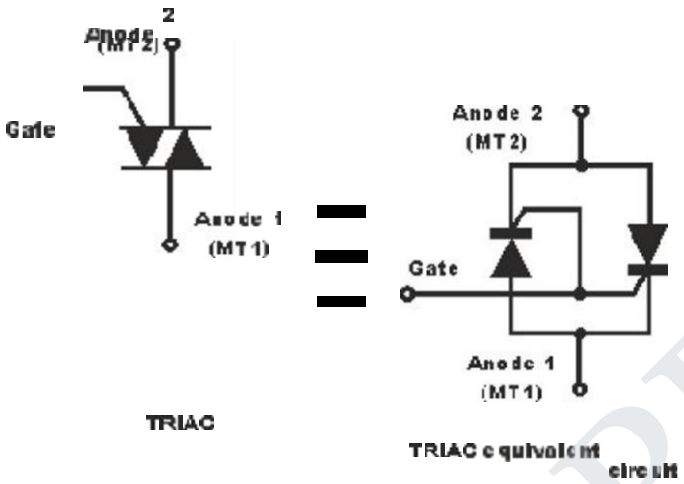


Figure 5.14 TRIAC symbol, equivalent as two thyristors

One of the drawbacks of the TRIAC is that it does not switch symmetrically. It will often have an offset, switching at different gate voltages for each half of the cycle. This creates additional harmonics which is not good for EMC performance and also provides an imbalance in the system

In order to improve the switching of the current waveform and ensure it is more symmetrical is to use a device external to the TRIAC to time the triggering pulse. A DIAC placed in series with the gate is the normal method of achieving this.

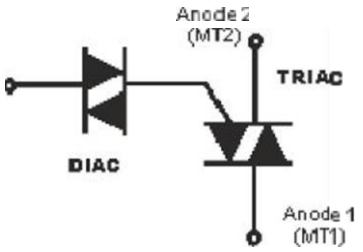


Figure 5.15 DIAC and TRIAC connected together

- **Operation**

With switch S open, there will be no gate current and the triac is cut off. Even with no current the triac can be turned on provided the supply voltage becomes equal to the breakover voltage.

When switch S is closed, the gate current starts flowing in the gate circuit. Breakover voltage of triac can be varied by making proper currnt flow. Triac starts to conduct wheather MT2 is positive or negative w.r.t MT1.

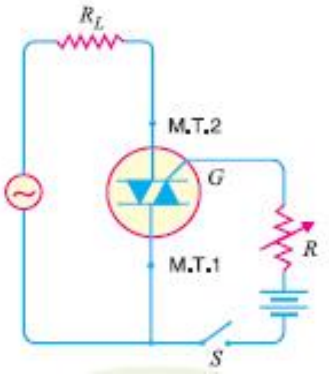


Figure 5.16 TRIAC operation under biasing

If terminal MT2 is positive w.r.t MT1 the TRIAC is on and the conventional current will flow from MT2 to MT1. If terminal MT2 is negative w.r.t MT1 the TRIAC is again turned on and the conventional current will flow from MT1 to MT2.

- **Characteristics**

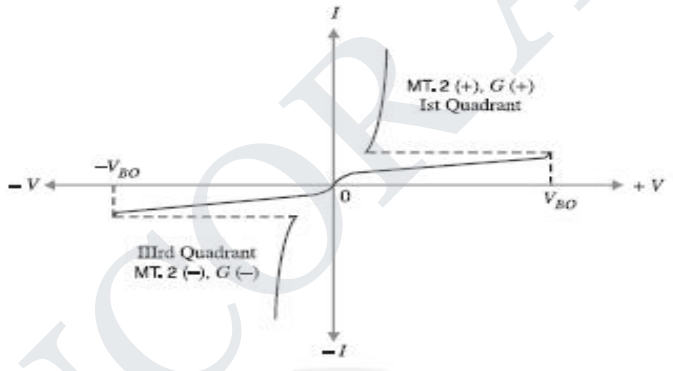


Figure 5.16 The V-I Characteristics curve for TRIAC

The V-I curve for triac in the Ist and IIIrd quadrants are essentially identical to SCR in the Ist quadrant.The triac can be operated with either positive or negative gate control voltage but in normal operation usually the gate voltage is positive in quadrant I and negative in quadrant III. The supply voltage at which the triac is ON depends upon gate current. The greater gate current and smaller supply voltage at which triac is turned on. This permits to use triac to control a,c. power in a load from zero to full power in a smooth and continuous manner with no loss in the controlling device.

- **Advantages and disadvantages**

When requiring to switch both halves of an AC waveform there are two options that are normally considered. One is to use a TRIAC, and the other is to use two thyristors connected back to back - one thyristor is used to switch one half of the cycle and the second connected in the reverse direction operates on the other half cycle.As there are two options the advantages and disadvantages of using a TRIAC must be weighed up.

- **Advantages**

- Can switch both halves of an AC waveform
- Single component can be used for full AC switching

➢ **Disadvantages**

- A TRIAC does not fire symmetrically on both sides of the waveform
- Switching gives rise to high level of harmonics due to non-symmetrical switching
- More susceptible to EMI problems as a result of the non-symmetrical switching
- Care must be taken to ensure the TRIAC turns off fully when used with inductive loads.

➢ **Applications**

TRIACs are used in a number of applications. However they tend not to be used in high power switching applications - one of the reasons for this is the non-symmetrical switching characteristics. For high power applications this creates a number of difficulties, especially with electromagnetic interference.

However TRIACs are still used for many electrical switching applications:

- ✓ Domestic light dimmers
- ✓ Electric fan speed controls
- ✓ Small motor controls
- ✓ Control of small AC powered domestic appliances

2.8.5 INSULATED GATE BIPOLAR TRANSISTOR

The Insulated Gate Bipolar Transistor also called an IGBT for short, is something of a cross between a conventional Bipolar Junction Transistor, (BJT) and a Field Effect Transistor, (MOSFET) making it ideal as a semiconductor switching device.

The IGBT transistor takes the best parts of these two types of transistors, the high input impedance and high switching speeds of a MOSFET with the low saturation voltage of a bipolar transistor, and combines them together to produce another type of transistor switching device that is capable of handling large collector-emitter currents with virtually zero gate current drive.

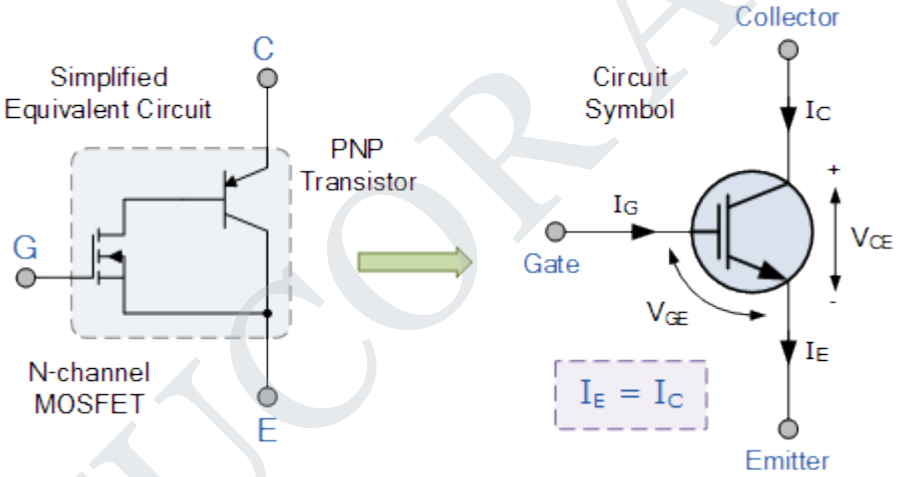
➢ **Typical IGBT**

The Insulated Gate Bipolar Transistor, (IGBT) uses the insulated gate (hence the first part of its name) technology of the MOSFET with the output performance characteristics of a conventional bipolar transistor, (hence the second part of its name). The result of this hybrid combination is that the "IGBT Transistor" has the output switching and conduction characteristics of a bipolar transistor but is voltage-controlled like a MOSFET.

IGBTs are mainly used in power electronics applications, such as inverters, converters and power supplies, were the demands of the solid state switching device are not fully met by power bipolars and power MOSFETs. High-current and high-voltage bipolars are available, but their switching speeds are slow, while power MOSFETs may have high switching speeds, but high-voltage and high-current devices are expensive and hard to achieve.

The advantage gained by the insulated gate bipolar transistor device over a BJT or MOSFET is that it offers greater power gain than the bipolar type together with the higher voltage operation and lower input losses of the MOSFET. In effect it is an FET integrated with a bipolar transistor in a form of Darlington configuration as shown.

- **Insulated Gate Bipolar Transistor**



We can see that the insulated gate bipolar transistor is a three terminal, transconductance device that combines an insulated gate N-channel MOSFET input with a PNP bipolar transistor output connected in a type of Darlington configuration. As a result the terminals are labelled as: Collector, Emitter and Gate. Two of its terminals (C-E) are associated with a conductance path and the third terminal (G) associated with its control.

The amount of amplification achieved by the insulated gate bipolar transistor is a ratio between its output signal and its input signal. For a conventional bipolar junction transistor, (BJT) the amount of gain is approximately equal to the ratio of the output current to the input current, called Beta.

For a metal oxide semiconductor field effect transistor or MOSFET, there is no input current as the gate is isolated from the main current carrying channel. Therefore, an FET's gain is equal to the ratio of output current change to input voltage change, making it a transconductance device and this is also true of the IGBT. Then we can treat the IGBT as a power BJT whose base current is provided by a MOSFET.

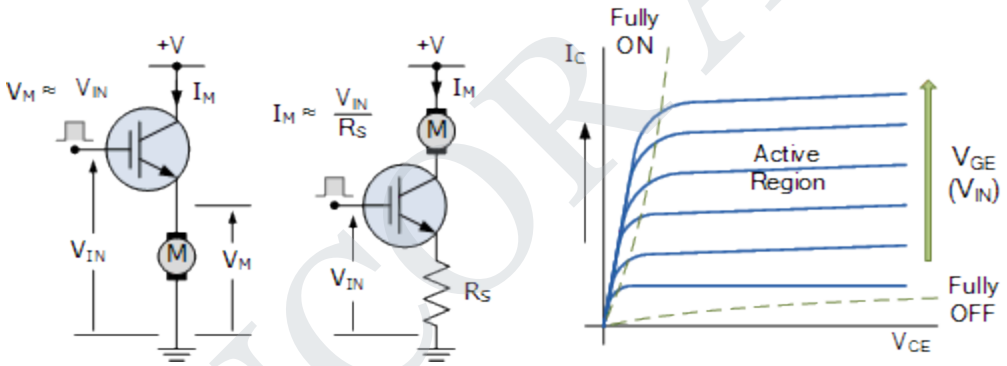
The Insulated Gate Bipolar Transistor can be used in small signal amplifier circuits in much the same way as the BJT or MOSFET type transistors. But as the IGBT combines the low conduction loss of a BJT with the high switching speed of a power MOSFET an optimal solid state switch exists which is ideal for use in power electronics applications.

Also, the IGBT has a much lower "on-state" resistance, R_{ON} than an equivalent MOSFET. This means that the I^2R drop across the bipolar output structure for a given switching current is much lower. The forward blocking operation of the IGBT transistor is identical to a power MOSFET.

When used as static controlled switch, the insulated gate bipolar transistor has voltage and current ratings similar to that of the bipolar transistor. However, the presence of an isolated gate in an IGBT makes it a lot simpler to drive than the BJT as much less drive power is needed.

An insulated gate bipolar transistor is simply turned "ON" or "OFF" by activating and deactivating its Gate terminal. A constant positive voltage input signal across the Gate and the Emitter will keep the device in its "ON" state, while removal of the input signal will cause it to turn "OFF" in much the same way as a bipolar transistor or MOSFET.

- **IGBT Characteristics**



Because the IGBT is a voltage-controlled device, it only requires a small voltage on the Gate to maintain conduction through the device unlike BJT's which require that the Base current is continuously supplied in a sufficient enough quantity to maintain saturation.

Also the IGBT is a unidirectional device, meaning it can only switch current in the "forward direction", that is from Collector to Emitter unlike MOSFET's which have bi-directional current switching capabilities (controlled in the forward direction and uncontrolled in the reverse direction).

The principal of operation and Gate drive circuits for the insulated gate bipolar transistor are very similar to that of the N-channel power MOSFET. The basic difference is that the resistance offered by the main conducting channel when current flows through the device in its "ON" state is very much smaller in the IGBT. Because of this, the current ratings are much higher when compared with an equivalent power MOSFET.

The main advantages of using the Insulated Gate Bipolar Transistor over other types of transistor devices are its high voltage capability, low ON-resistance, ease of drive, relatively fast switching speeds and combined with zero gate drive current makes it a good choice for moderate speed, high voltage applications such as in pulse-width modulated (PWM), variable speed control,

switch-mode power supplies or solar powered DC-AC inverter and frequency converter applications operating in the hundreds of kilohertz range.

A general comparison between BJT's, MOSFET's and IGBT's is given in the following table.

IGBT Comparison Table

Device Characteristic	Power Bipolar	Power MOSFET	IGBT
Voltage Rating	High <1kV	High <1kV	Very High >1kV
Current Rating	High <500A	Low <200A	High >500A
Input Drive	Current 20-200 h_{FE}	Voltage V_{GS} 3-10V	Voltage V_{GE} 4-8V
Input Impedance	Low	High	High
Output Impedance	Low	Medium	Low
Switching Speed	Slow (uS)	Fast (nS)	Medium
Cost	Low	Medium	High

We have seen that the Insulated Gate Bipolar Transistor is semiconductor switching device that has the output characteristics of a bipolar junction transistor, BJT, but is controlled like a metal oxide field effect transistor, MOSFET.

One of the main advantages of the IGBT transistor is the simplicity by which it can be driven ON or OFF or in its linear active region as a power amplifier. With its lower on-state conduction losses and its ability to switch high voltages without damage makes this transistor ideal for driving inductive loads such as coil windings, electromagnets and DC motors.

Review questions:

1. Compare the following DMOSFET& EMOSFET (8)
2. N-channel MOSFET & P-channel MOSFET. (8)
3. Explain the biasing technique for JFET. (16)
4. Explain the construction and characteristics of JFET. (16)
5. Explain the construction and characteristics of EMOSFET. (16)
6. Explain the construction and characteristics of DMOSFET. (16)
7. Explain the biasing characteristics of MOSFET. (16)
8. Explain the working and principle of operation of UJT and mention its applications.(16)
9. Explain the working and characteristics of SCR and its applications. (16)
10. Briefly explain the operation of DIAC (8)
11. Briefly explain the operation of TRIAC (8)

UNIT 3 AMPLIFIERS

3.1BJT SMALL SIGNAL MODEL

3.1.1 CE, CB and CC Amplifiers:

An amplifier is used to increase the signal level. It is used to get a larger signal output from a small signal input. Assume a sinusoidal signal at the input of the amplifier. At the output, signal must remain sinusoidal in waveform with frequency same as that of input. To make the transistor work as an amplifier, it is to be biased to operate in active region. It means base-emitter junction is forward biased and base-collector junction is reverse biased.

Let us consider the common emitter amplifier circuit using voltage divider bias.

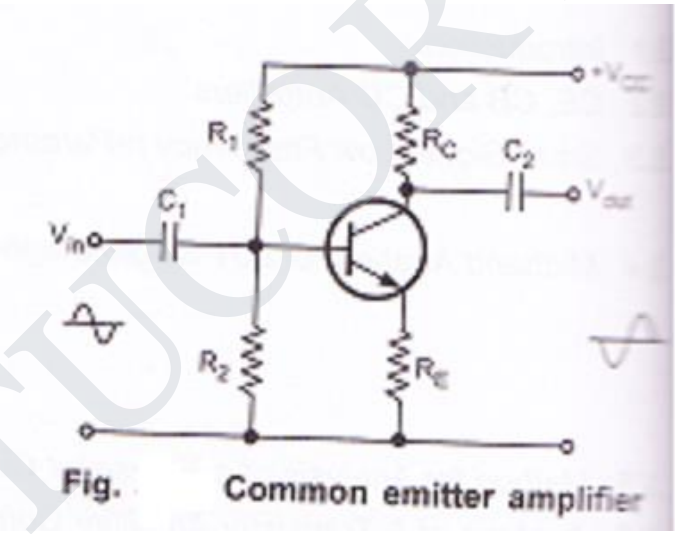


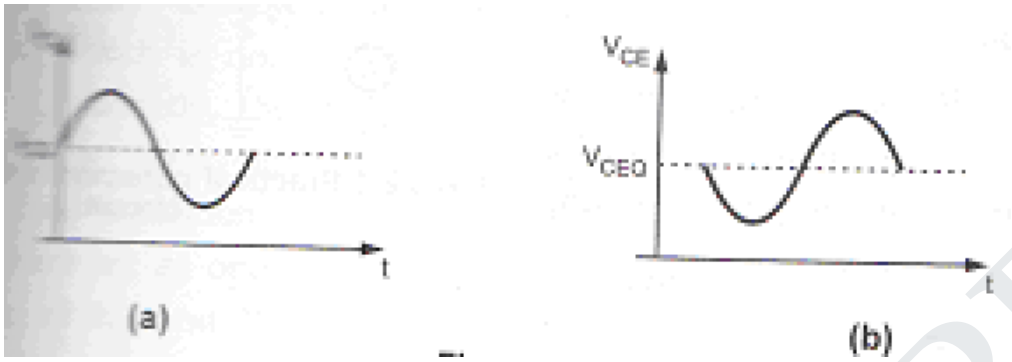
Fig. Common emitter amplifier

In the absence of input signal, only D.C. voltage is present in the circuit. It is known as zero signal or no signal condition or quiescent condition. D.C. collector-emitter voltage V_{CE}, D.C. collector current I_C and base current I_B is the quiescent operating point for the amplifier. Due to this base current varies sinusoidaly as shown in the below figure.

Fig. I_{BQ} is quiescent DC base current

If the transistor is biased to operate in active region, output is linearly proportional to the input. The collector current is β times larger than the input base current in CE configuration. The

collector current will also vary sinusoidally about its quiescent value I_{CQ}. The output voltage will also vary sinusoidally as shown in the below figure.



Variations in the collector current and voltage between collector and emitter due to change in base current are shown graphically with the help of load line in the above figure.

3.1.2 Common Emitter Amplifier Circuit:

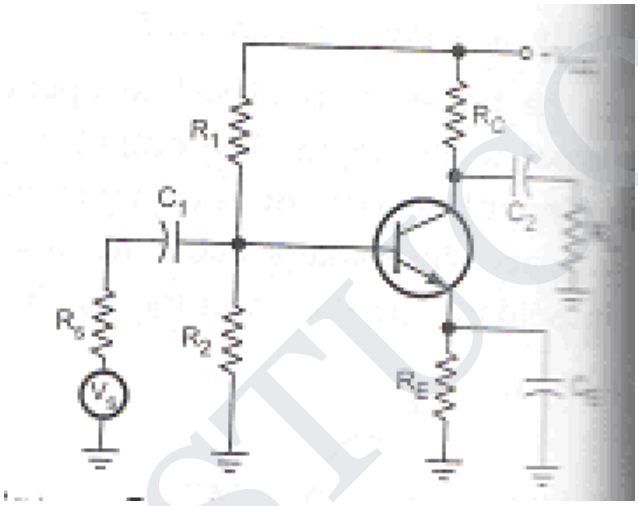


Fig. Practical common-emitter amplifier circuit

From above circuit, it consists of different circuit components. The functions of these components are as follows:

1. **Biasing Circuit:**
   Resistors R_1, R_2 and R_E forms the voltage divider biasing circuit for CE amplifier and it sets the proper operating point for CE amplifier.

2. **Input Capacitor C_1:**

C_1 couples the signal to base of the transistor. It blocks any D.C. component present in the signal and passes only A.C. signal for amplification.

3. Emitter Bypass Capacitor C_E:

C_E is connected in parallel with emitter resistance R_E to provide a low reactance path to the amplified A.C. This will reduce the output voltage and reducing the gain value.

4. Output Coupling Capacitor C_2:

C_2 couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks D.C. and passes only A.C. part of the amplified signal.

Need for C_1, C_2, and C_E:

The impedance of the capacitor is given by,

$$X_C = 1/ (2\prod f_c)$$

Phase reversal:

The phase relationship between the input and output voltages can be determined by considering the effect of positive and negative half cycle separately. The collector current is β times the base current, so the collector current will also increases. This increases the voltage drop across R_C.

$$V_C = V_{CC} - I_C R_C$$

Increase in I_C results in a drop in collector voltage V_C, as V_{CC} is constant. V_i increases in a positive direction, V_o goes in negative direction and negative half cycle of output voltage can be obtained for positive half cycle at the input.

In negative half cycle of input, A.C. and D.C. voltage will oppose each other. This will reduce the base current. Accordingly collector current and drop across R_C both will reduce and it increases the output voltage. So positive half cycle at the output for negative half cycle at the input can be obtained. So there is a phase shift of 180º between input and output voltages for a common emitter amplifier.

3.1.3Common Collector Amplifier Circuit:

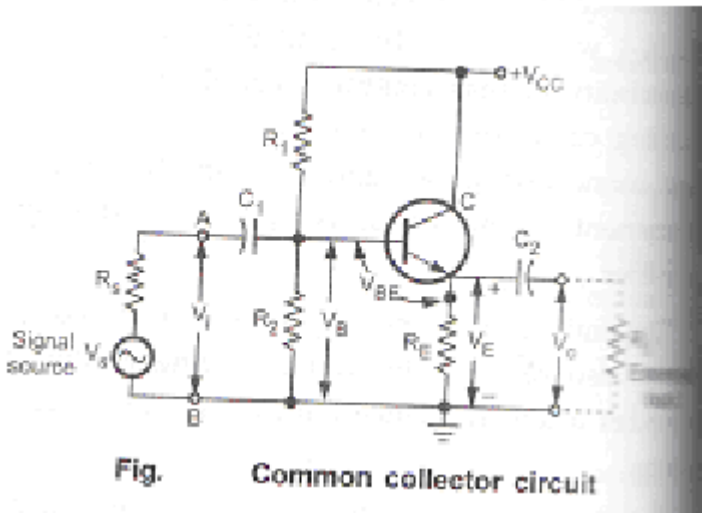


Fig. Common collector circuit

From above circuit, D.C. biasing is provided by R_1, R_2 and R_E. The load resistance is capacitor coupled to the emitter terminal of the transistor. When a signal is applied to base of the transistor, V_B is increased and decreased as the signal goes positive and negative respectively.

From figure, $VE = VB - V_{BE}$

Consider V_{BE} is constant, so the variation in V_B appears at emitter and emitter voltage V_E will vary same as base voltage V_B. In common collector circuit, emitter terminal follows the signal voltage applied to the base. It is also known as emitter follower.

3.1.4 Common Base Amplifier Circuit:

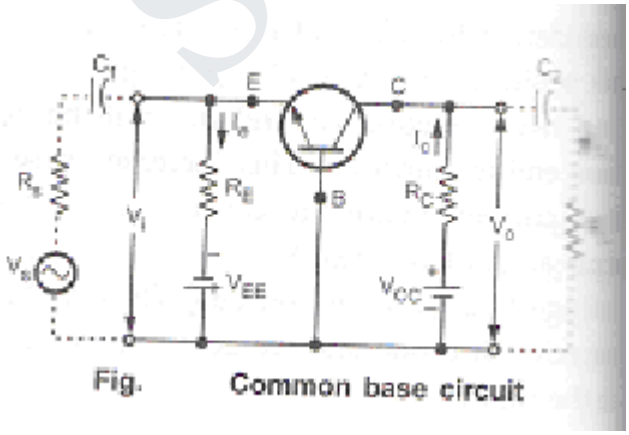


Fig. Common base circuit

From above circuit, the signal source is coupled to the emitter of the transistor through C_1. The load resistance R_L is coupled to the collector of the transistor through C_2. The positive going pulse of input source increases the emitter voltage. As base voltage is constant, forward bias of emitter-base junction reduces. This reduces I_b, I_c and drop across R_c.

$$V_o = V_{CC} - I_C R_C$$

Reduction in I_C results in an increase in V_o. Positive going input produces positive going output and vice versa. So there is no phase shift between input and output in common base amplifier.

3.2 Small Signal Low Frequency h-parameter Model:

Let us consider the transistor amplifier as a block box.

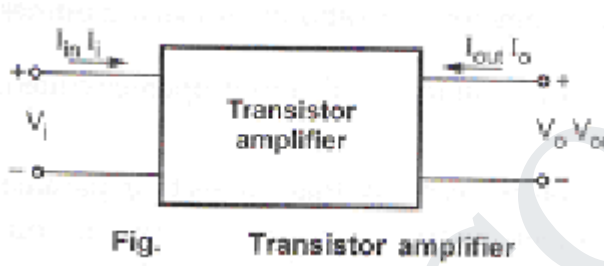


Fig. Transistor amplifier

Where, I_i – input current to the amplifier

V_i - input voltage to the amplifier

I_o – output current of the amplifier

V_o – output voltage of the amplifier

Input current is an independent variable. Input voltage and output current are dependent variables. Input current and output voltage are independent variables.

$$V_i = f_1(I_i, V_o)$$
$$I_o = f_2(I_i, V_o)$$

This can be written in the equation form as,

$$V_i = h_{11} I_i + h_{12} V_o$$
$$I_o = h_{21} I_i + h_{22} V_o$$

The above equation can also be written using alphabetic notations,

$$V_i = h_i \cdot I_i + h_r \cdot V_o$$
$$I_o = h_f \cdot I_i + h_o \cdot V_o$$

- **Definitions of h-parameter:**

The parameters in the above equations are defined as follows:

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0}$$
$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0}$$
$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0}$$
$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0}$$

h_{11} – input resistance with output short-circuited in ohms

h_{12} – fraction of output voltage at input with input open circuited, it is unitless

h_{21} – forward current transfer ratio or current gain with output short circuited, it is unitless

h_{22} – output admittance with input open circuited in mhos

- **Benefits of h-parameters:**

1. Real numbers at audio frequencies
2. Easy to measure
3. Can be obtained from the transistor static characteristic curve
4. Convenient to use in circuit analysis and design
5. Most of the transistor manufacturers specify the h-parameters

3.2.1 h-Parameters for all three configurations:

Transistor can be represented as two port network by making anyone terminal common between input and output. There are three possible configurations in which a transistor can be used, there is a change in terminal voltage and current for different transistor configurations. To designate the type of configuration another subscript is added to h-parameters.

$h_{ie} = h_{11e}$– input resistance in CE configuration

$h_{fb} = h_{21b}$ – short circuit current gain in CB configuration

Table: Summarizes h-parameters for all three configurations

Parameter	CB	CE	CC
Input resistance	h_{ib}	h_{ie}	h_{ic}
Reverse voltage gain	h_{rb}	h_{re}	h_{rc}
Forward transfer current gain	h_{fb}	h_{fe}	h_{fc}
Output admittance	h_{ob}	h_{oe}	h_{oc}

The basic circuit of hybrid model is same for all three configurations, only parameters are different.

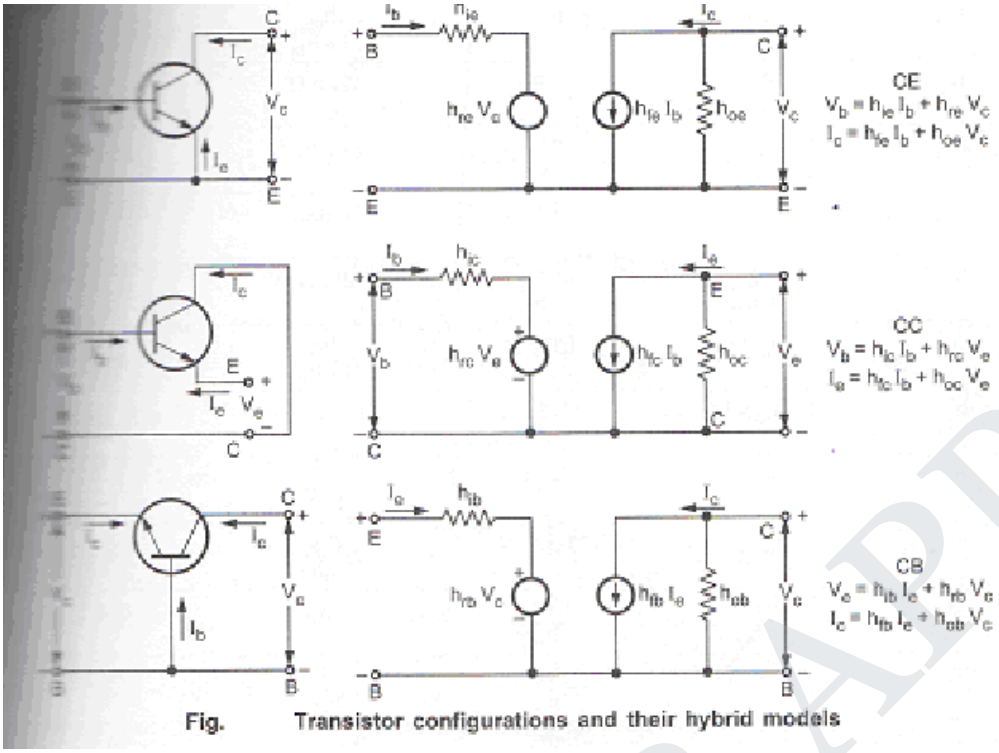


Fig. Transistor configurations and their hybrid models

The circuit and equations are valid for either NPN or PNP transistor and are independent of the type of load or method of biasing.

- ✓ **Determination of h-parameters from characteristics:**

Consider CE configuration, its functional relationship can be defined from the following equations:

$$V_{be} = f_1 (I_b , V_{ce})$$
$$I_c = f_2 (I_b , V_{ce})$$

The input characteristic curve gives the relationship between input voltage V_{BE} and input current I_B for different values of output voltage V_{CE}. The following figure shows the typical input characteristic curve for CE configuration.

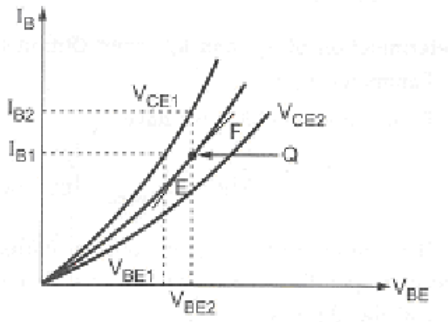


Fig. Typical input characteristic curves for the common emitter transistor configuration

✓ **Determination of h_{ie} and h_{re} from characteristic curve:**

Parameter h_{ie}:

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\text{ constant}} = \frac{V_{BE2} - V_{BE1}}{I_{B2} - I_{B1}}$$

Parameter h_{re}:

$$h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right|_{I_B\text{constant}} = \frac{V_{BE2} - V_{BE1}}{V_{CE2} - V_{CE1}}$$

The output characteristic curve gives the relationship between output current I_C and output voltage V_{CE} for different values of input current I_B.

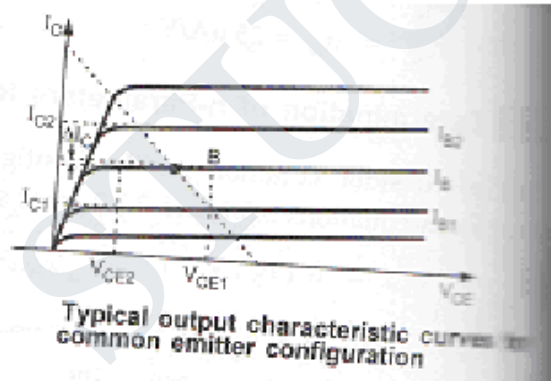


Fig. Typical output characteristic curves in common emitter configuration

✓ **Determination of h_{fe} and h_{oe} from output characteristic curve:**

Parameter h_{fe}:

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\text{constant}} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}$$

Parameter h_{oe}:

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_C}\right|_{I_B \text{ constant}} = \frac{I_{C2} - I_{C1}}{V_{CE2} - V_{CE1}}$$

3.2.2 Method for analysis of a transistor circuit:

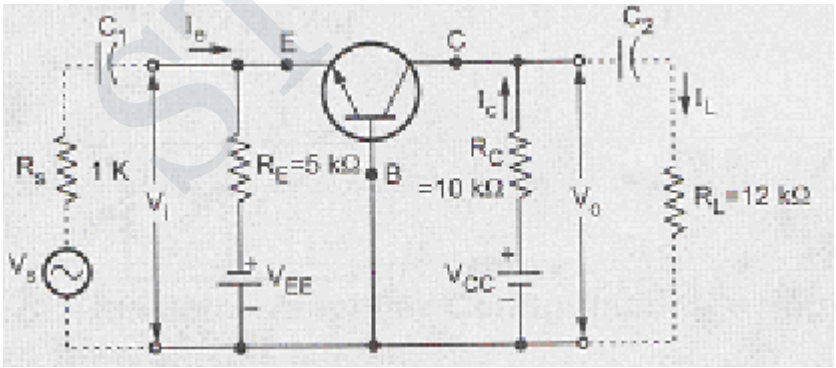
The analysis of transistor circuits for small signal behaviour can be made by following simple guidelines. These guidelines are,

1. Draw the actual circuit diagram
2. Replace coupling capacitors and emitter bypass capacitor by short circuit
3. Replace D.C. source by a short circuit
4. Mark the points B, E, C on the circuit diagram and locate these points as the start of the equivalent circuit
5. Replace the transistor by its h-parameter model

Problem 1:

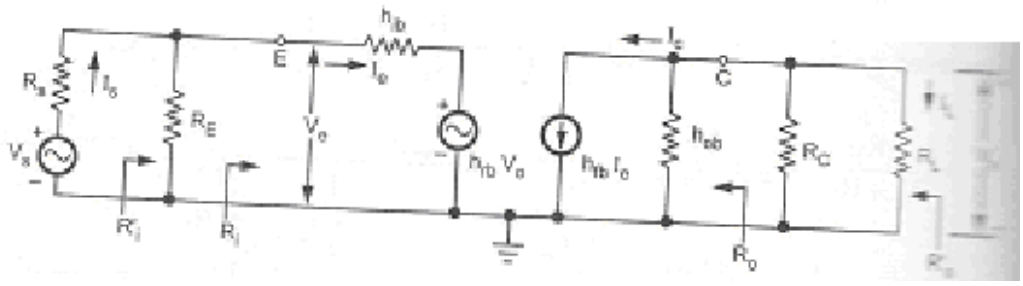
For the common base circuit shown in figure, transistor parameters are $h_{ib} = 22\Omega$,

$h_{fb} = -0.98$, $h_{ob} = 0.49\mu A/V$, $h_{rb} = 2.9*10^{-4}$. Calculate the values of input resistance, output resistance, current gain and voltage gain for the given circuit.



Solution:

Change the given figure into h-parameter equivalent model.



a) Current gain

$$(A_i) = -\frac{h_{fb}}{1+h_{ob}R'_L}$$

$$= \frac{-(-0.98)}{1+0.49\times10^{-6}\times5.45\,K} = 0.977$$

b) Input Resistance

$$(R_i) = h_{ib} + h_{rb}\,A_i\,R'_L$$

$$= 22\,\Omega + 2.9\times10^{-4}\times(0.977)\,(5.45\,K) = 23.54\,\Omega$$

$$R'_i = R_i \parallel R_E = 23.54 \parallel 5\,K = 23.43\,\Omega$$

c) Voltage gain

$$(A_v) = \frac{A_i R'_L}{R_i} = \frac{(0.977)\times(5.45\,K)}{23.54} = 226$$

d) Overall voltage gain

$$A_{VS} = \frac{V_o}{V_s} = \frac{V_o}{V_e}\times\frac{V_e}{V_s} \quad \text{where } \frac{V_o}{V_e} = A_v \quad \frac{V_e}{V_s} = \frac{R'_i}{R'_i+R_s}$$

$$A_{vs} = A_v\frac{R'_i}{R'_i+R_s} = 226\times\frac{23.43}{20.36+1\,K} = 5.174$$

e) Overall current gain

$$A_i = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_e} \times \frac{I_e}{I_s}$$

$$\frac{I_L}{I_c} = -\frac{R_C}{R_C + R_L} = -\frac{10\,K}{10\,K + 12\,K} = -0.454$$

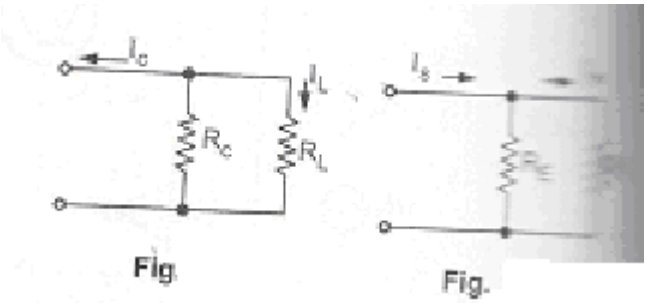


Fig Fig.

$$\frac{I_c}{I_e} = -A_i = -0.977$$

$$\frac{I_e}{I_s} = \frac{R_E}{R_E + R_i} = \frac{5\,K}{5\,K + 23.54} = 0.995$$

$$\therefore A_{i(\text{for circuit})} = (-0.454) \times (-0.977) \times 0.996 = 0.441$$

f) Output Resistance

$$(R_o) = \frac{1}{h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R'_s}}$$

$$= \frac{1}{0.49 \times 10^{-6} - \left(\frac{-0.98 \times 2.9 \times 10^{-4}}{22 + 833.33}\right)} = 1.21\ M\Omega$$

$R_o' = R_o \parallel R_L' = 1.21M \parallel 5.45K = 5.425K\Omega$

Comparison of Transistor Configurations:

3.3 General shape of frequency response of amplifiers:

An audio frequency amplifier which operates over audio frequency range extending from 20 Hz to 20 kHz. Audio frequency amplifiers are used in radio receivers, large public meeting and various announcements to be made for the passengers on railway platforms. Over the range of frequencies at which it is to be used an amplifier should ideally provide the same amplification for all frequencies. The degree to which this is done is usually indicated by the curve known as frequency response curve of the amplifier.

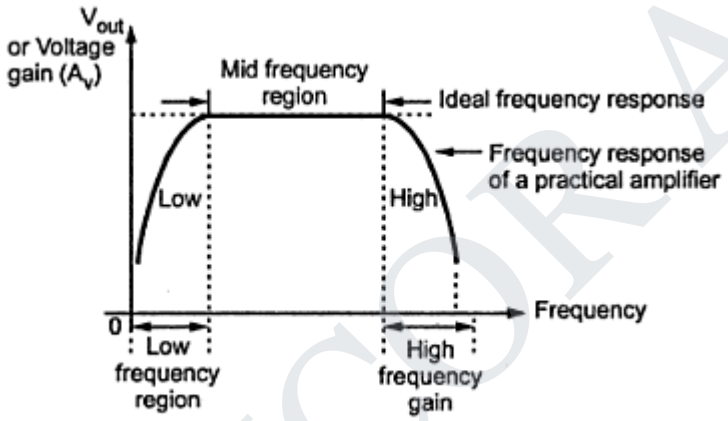


Fig. A typical frequency response of an amplifier

To plot this curve, input voltage to the amplifier is kept constant and frequency of input signal is continuously varied. The output voltage at each frequency of input signal is noted and the gain of the amplifier is calculated. For an audio frequency amplifier, the frequency range is quite large from 20 Hz to 20 kHz. In this frequency response, the gain of the amplifier remains constant in mid-frequency while the gain varies with frequency in low and high frequency regions of the curve. Only at low and high frequency ends, gain deviates from ideal characteristics. The decrease in voltage gain with frequency is called roll-off.

3.3.1 Definition of cut-off frequencies and bandwidth:

The range of frequencies can be specified over which the gain does not deviate more than 70.7% of the maximum gain at some reference mid-frequency.

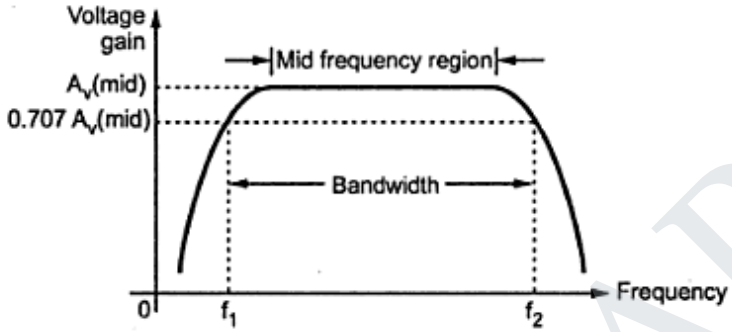


Fig. Frequency response, half power frequencies and bandwidth of an RC coupled amplifier

From above figure, the frequencies f_1 & f_2 are called lower cut-off and upper cut-off frequencies.

Bandwidth of the amplifier is defined as the difference between f_2 & f_1.

Bandwidth of the amplifier = f_2 - f_1

The frequency f_2 lies in high frequency region while frequency f_1 lies in low frequency region. These two frequencies are also called as half-power frequencies since gain or output voltage drops to 70.7% of maximum value and this represents a power level of one half the power at the reference frequency in mid-frequency region.

3.4 Low frequency analysis of amplifier to obtain lower cut-off frequency:

- **Decibel Unit:**

The decibel is a logarithmic measurement of the ratio of one power to another or one voltage to another. Voltage gain of the amplifier is represented in decibels (dBs). It is given by,

Voltage gain in dB = 20 log A_v

Power gain in decibels is given by,

Power gain in dB = 10 log A_p

Where A_v is greater than one, gain is positive and when A_v is less than one, gain is negative. The positive and negative gain indicates that the amplification and attenuation respectively. Usually the maximum gain is called mid frequency range gain is assigned a 0 db value. Any value of gain below mid frequency range can be referred as 0 db and expressed as a negative db value.

Example:

Assume that mid frequency gain of a certain amplifier is 100. Then,

Voltage gain = 20 log 100 = 40 db

At f_1 and f_2 $A_v = 100/\sqrt{2} = 70.7$

Voltage gain at f_1 = Voltage gain at f_2 = 20 log 70.7 = 37 db

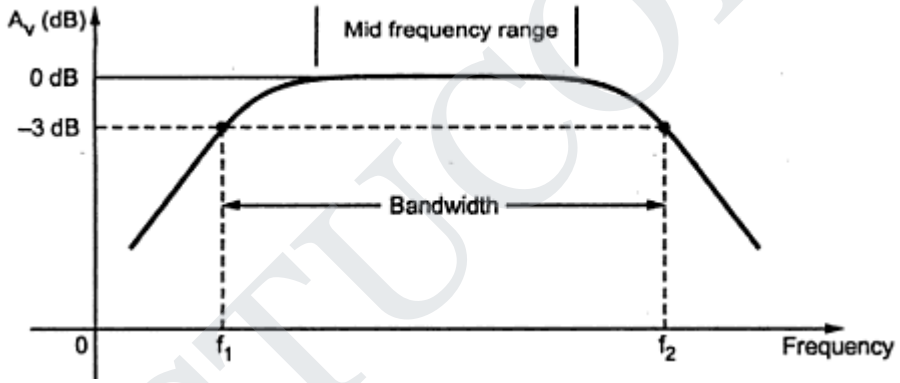


Fig. Normalized voltage gain vs frequency

From above figure, it shows that the voltage gain at f_1 and f_2 is less than 3db of the maximum voltage gain. Due to this the frequencies f_1 and f_2 are also called as 3 db frequencies. At f_1 & f_2 power gain drops by 3 db. For all frequencies within the bandwidth, amplifier power gain is at least half of the maximum power gain. This bandwidth is also referred to as 3 db bandwidth.

- **Significance of octaves and decades:**

The octaves and decades are the measures of change in frequency. A ten times change in frequency is called a decade. Otherwise, an octave corresponds to a doubling or halving of the frequency.

Example:

An increase in frequency from 100 Hz to 200 Hz is an octave.

A decrease in frequency from 100 kHz to 50 kHz is also an octave.

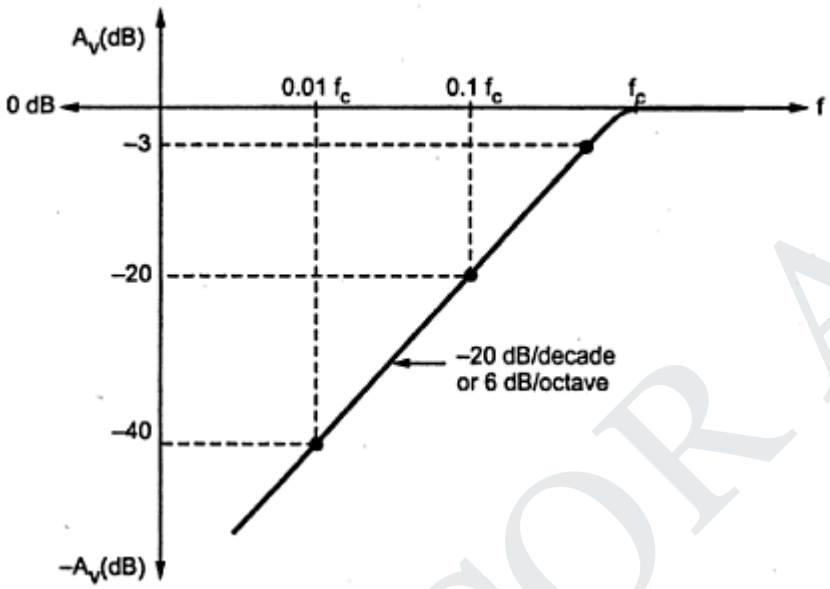


Fig. Frequency response showing significance of decade and octave

At lower and higher frequencies the decrease in the gain of amplifiers is often indicated in terms of db/decades or db/octaves. If the attenuation in gain is 20 db for each decade, then it is indicated by line having slope of 20 db/decade. A rate of -20 db/decade is approximately equivalent to -6db/octave. A rate of -40 db/decade is approximately equivalent to -12db/octave.

- **Midband gain:**

It is defined as the band of frequencies between 10 f_1 and 0.1 f_2. It is denoted as midband gain or A_{mid}.

The voltage gain of the amplifier outside the midband is approximately given as,

$$A = \frac{A_{mid}}{\sqrt{1+(f_1/f)^2}\sqrt{1+(f/f_2)^2}}$$

In midband,

$$f_1/f \approx 0 \text{ and } f/f_2 \approx 0.$$

Midband:

$$A = A_{mid}$$

Below the midband,

$$f/f_2 \approx 0$$

As a result, the equation becomes,

Below midband:

$$A = \frac{A_{mid}}{\sqrt{1+(f_1/f)^2}}$$

Above midband,

$$f_1/f \approx 0.$$

As a result, the equation becomes,

Above midband:

$$A = \frac{A_{mid}}{\sqrt{1+(f/f_2)^2}}$$

- **Problem:**

For an amplifier, midband gain = 100 and lower cutoff frequency is 1 kHz. Find the gain of an amplifier at frequency 20 Hz.

Solution:

Below midband:

$$A = \frac{A_{mid}}{\sqrt{1+(f_1/f)^2}}$$

$$A = \frac{100}{\sqrt{1+\left(\frac{1000}{20}\right)^2}} = 2$$

3.4.1 Effect of various capacitors on frequency response:

- ✓ **Effect of coupling capacitors:**

The reactance of the capacitor is $X_c = 1/2\prod f_c$

At medium and high frequencies, the factor f makes X_c very small, so that all coupling capacitors behave as short circuits. At low frequencies, X_c increases. This increase in X_c drops the signal voltage across the capacitor and reduces the circuit gain. As signal frequencies decrease, capacitor reactance increase and gain continues to fall, reducing the output voltage.

- ✓ **Effect of Bypass capacitors:**

At lower frequencies, bypass capacitor C_E is not a short. So emitter is not at ac ground. X_c in parallel with R_E creates an impedance. The signal voltage drops across this impedance reducing the circuit gain.

- ✓ **Effect of internal transistor capacitances:**

At high frequencies, coupling and bypass capacitors act as short circuit and do not affect the amplifier frequency response. At high frequencies, internal capacitances, commonly known as junction capacitances. The following figure shows the junction capacitances for both BJT and FET. Incase of BJT, C_{be} is the base emitter junction capacitance and C_{bc} is the base collector junction capacitance. Incase of FET, C_{gs} is the internal capacitance between gate and source and C_{gd} is the internal capacitance between gate and drain.

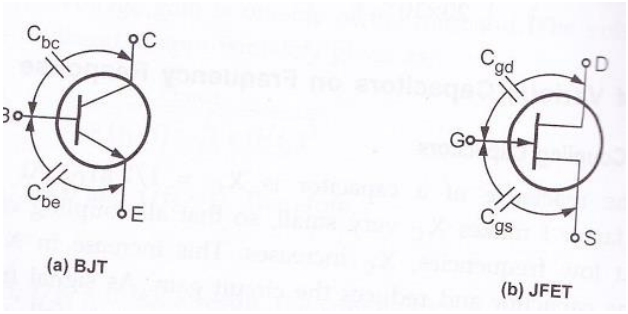


Fig. Internal transistor capacitances

3.5 MOSFET small signal model Amplifiers

It provides an excellent voltage gain with high input impedance. Due to these characteristics, it is often preferred over BJT.

Three basic FET configurations

Common source, common drain and common gate

3.5.1 MOSFET low frequency a.c Equivalent circuit

Figure shows the small signal low frequency a.c Equivalent circuit for n-channel JFET.

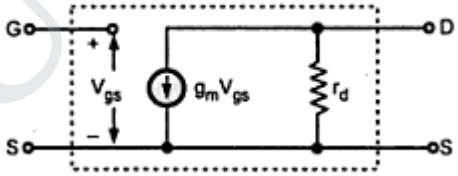


Fig3.1 small signal model of JFET

- ✓ **Common Source Amplifier With Fixed Bias**

Figure shows Common Source Amplifier With Fixed Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis.

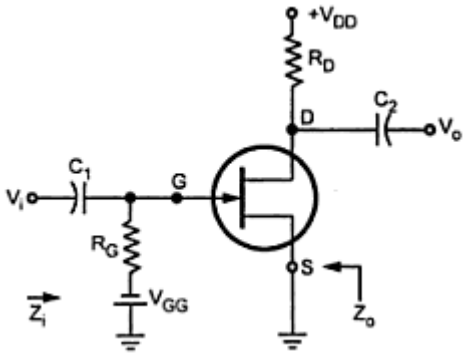


Fig3.2 Common source circuit of JFET

The following figure shows the low frequency equivalent model for Common Source Amplifier With Fixed Bias. It is drawn by replacing

- All capacitors and d.c supply voltages with short circuit
- JFET with its low frequency a.c Equivalent circuit

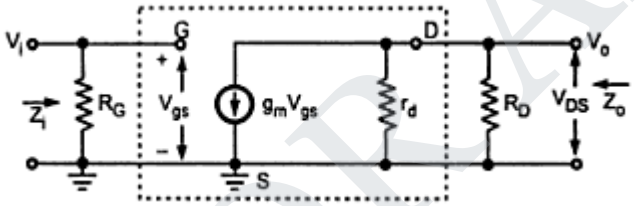


Fig3.3 small signal model of CS **MOSFET** amplifier

- ✓ **Input Impedance Zi**
  - Zi = R_G
- ✓ **Output Impedance Zo**

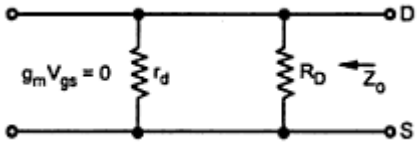


Fig3.4 Equivalent circuit model of **MOSFET** for output

It is the impedance measured looking from the output side with input voltage Vi equal to Zero.

As Vi=0,Vgs =0 and hence g_mVgs =0 . And it allows current source to be replaced by an open circuit.

So,

$$Z_o = R_D \| r_d$$

If the resistance rd is sufficiently large compared to R_D, then

$$Z_o \approx R_D \qquad \because r_d >> R_D$$

Voltage Gain A_v :

The voltage gain $A_v = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

Looking at Fig. we can write

$$V_o = -g_m V_{gs} (r_d \| R_D)$$

As we know $V_i = V_{gs}$ we can write

$$V_o = -g_m V_i (r_d \| R_D)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D)$$

and if $r_d >> R_D$,

$$A_v \approx -g_m R_D$$

Table summarizes performance of common source amplifier with fixed bias.

Parameter	Exact	With $r_d >> R_D$
Z_i	R_G	R_G
Z_o	$R_D \| r_d$	R_D
A_v	$-g_m (R_D \| r_d)$	$-g_m R_D$

3.5.2Common source amplifier with self bias(Bypassed Rs)

Figure shows Common Source Amplifier With self Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short circuits for low frequency analysis.

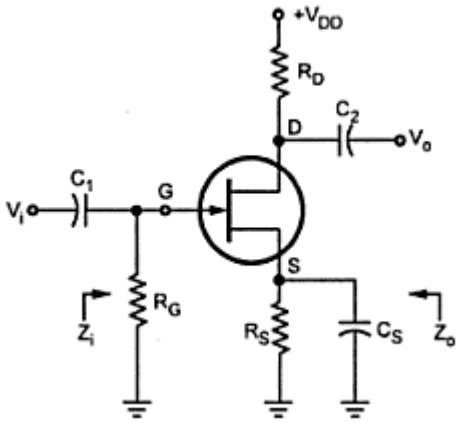


Fig3.5 **Common source amplifier** model of **MOSFET**

The following figure shows the low frequency equivalent model for Common Source Amplifier With self Bias.

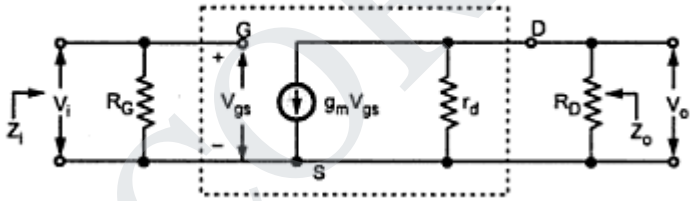


Fig3.6 **Small signal model for Common source amplifier** model of **MOSFET**

i) Input impedance Z_i : $Z_i = R_G$

ii) Output impedance Z_o : $Z_o = r_d \,||\, R_D$

if $r_d >> R_D$ $Z_o \approx R_D$

iii) Voltage gain A_v : $A_v = -g_m (r_d \,||\, R_D)$

If $r_d >> R_D$ $A_v = -g_m R_D$

The negative sign in the voltage gain indicates there is a 180^o phase shift between input and output voltages.

✓ **Common source amplifier with self bias (unbypassed Rs)**

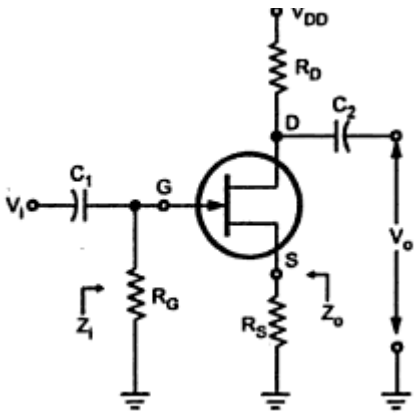


Fig3.7 **Common source amplifier** model of **MOSFET**

Now Rs will be the part of low frequency equivalent model as shown in figure.

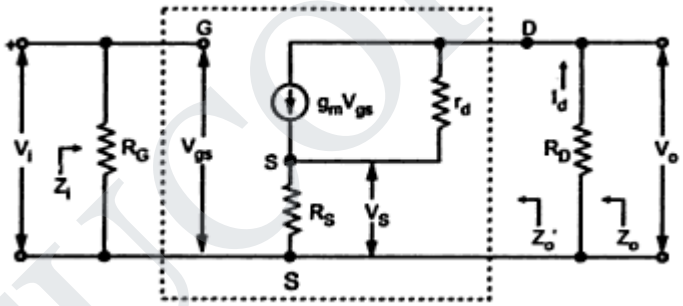


Fig3.8 **Small signal model for Common source amplifier** model of **MOSFET**

✓ **Input Impedance Zi**

- $Zi = R_G$

✓ **Output Impedance Zo**

It is given by

$$Z_o = Z_o' \| R_D$$

where $$Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i = 0}$$

$$Z_o = [\, r_d + R_s\,(\mu + 1)\,] \,||\, R_D$$

$$Z_o = [\, r_d + R_s\,(g_m\, r_d + 1)\,] \,||\, R_D$$

- ✓ **Voltage gain (Av)**
  It is given by

$$A_v = \frac{V_o}{V_i}$$

We know that,

$$V_o = -I_d\, R_D$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m\, r_d\, R_D}{r_d + R_s + R_D + g_m\, R_s\, r_d}$$

Dividing numerator and denominator by r_d we get,

$$\therefore \quad A_v = \frac{V_o}{V_i} = \frac{-g_m\, R_D}{1 + g_m\, R_s + \dfrac{R_s + R_D}{r_d}}$$

If $r_d >> R_s + R_D$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m\, R_D}{1 + g_m\, R_s}$$

Table summarizes performance of common source amplifier with self bias.

Parameter	Bypassed R_S		Unbypassed R_S	
	Exact	$r_d >> R_D$	Exact	$r_d >> R_D$
Z_i	R_G	R_G	R_G	R_G
Z_o	$R_D \parallel r_d$	R_D	$[r_d + R_S(g_m r_d + 1)] \parallel R_D$ or $[r_d + R_S(\mu + 1)] \parallel R_D$	$[r_d + R_S(g_m r_d + 1)] \parallel R_D$ or $[r_d + R_S(\mu + 1)] \parallel R_D$
A_v	$-g_m(R_D \parallel r_d)$	$-g_m R_D$	$\dfrac{-g_m R_D}{1 + g_m R_S + \dfrac{R_S + R_D}{r_d}}$	$\dfrac{-g_m R_D}{1 + g_m R_S}$

✓ **Common source amplifier with Voltage divider bias(Bypassed Rs)**

Figure shows Common Source Amplifier With voltage divider Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short circuits for low frequency analysis.

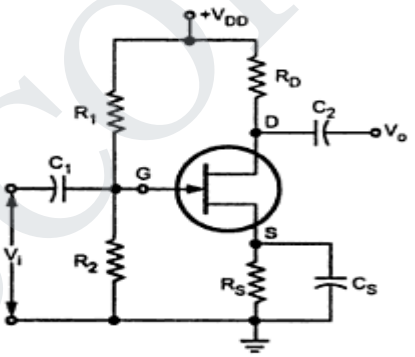


Fig3.9 **Common source amplifier with Voltage divider bias(Bypassed Rs)**

The following figure shows the low frequency equivalent model for Common Source Amplifier With voltage divider Bias

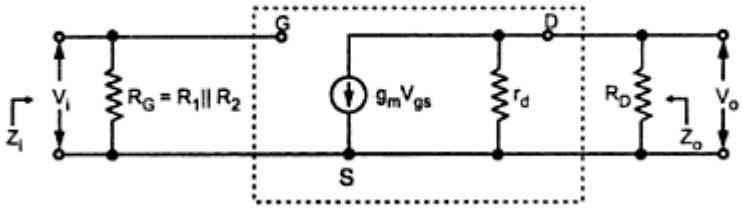


Fig3.10 **small model of Common source amplifier with Voltage divider bias(Bypassed Rs)**

The parameters are given by

$$R_G = R_1 \| R_2$$

$$Z_i = R_G$$

$$= R_1 \| R_2$$

$$Z_o = r_d \| R_D$$

if $r_d >> R_D$ $\quad Z_o \approx R_D$

$$A_v = -g_m (r_d \| R_D)$$

If $r_d >> R_D$ $\quad A_v = -g_m R_D$

The negative sign in the voltage gain indicates there is a 180^o phase shift between input and output voltages.

✓ **Common Drain Amplifier**

In this circuit, input is applied between gate and source and output is taken between source and drain.

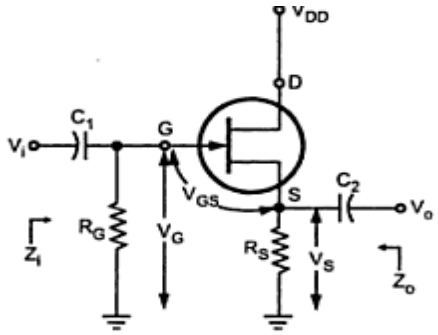


Fig3.12 **Circuit of Common Drain amplifier**

In this circuit, the source voltage is

$$Vs = V_G + V_{GS}$$

When a signal is applied to the **MOSFET** gate via C1 ,VG varies with the signal. As VGS is fairly constant and $Vs = V_G + V_{GS}$, Vs varies with Vi.

The following figure shows the low frequency equivalent model for common drain circuit.

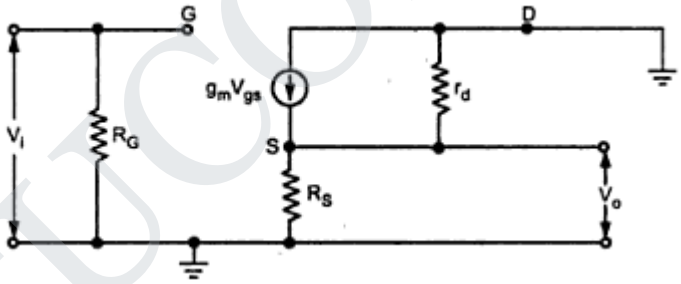


Fig3.13 **small model of Common Drain amplifier**

Input Impedance Zi

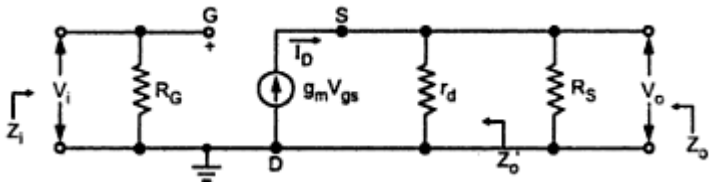


Fig3.13 Simplified small model of Common Drain amplifier

$Zi = R_G$

Output Impedance Zo

It is given by

$$Z_o = Z_o' || R_s$$

where $$Z_o' = \frac{V_o}{I_d}\Big|_{V_i = 0}$$

Applying KVL to the outer loop we can have,

$$V_i + V_{gs} - V_o = 0$$

As $$V_i = 0,$$

$$V_{gs} = V_o$$

Looking at Fig. we can write that,

$$g_m V_{gs} = I_d$$

But Vgs = Vo, so

$$g_m V_o = I_d$$

$$Z_o' = \frac{V_o}{I_d} = \frac{1}{g_m}$$

$$\therefore \quad Z_o = \frac{1}{g_m} || R_s$$

Voltage gain (Av)

It is given by

$$A_v = \frac{V_o}{V_i}$$

Looking at Fig. we can write that,

$$V_o = -I_d (r_d || R_s)$$

and $$I_d = g_m V_{gs}$$

$$\therefore \quad V_o = -g_m V_{gs} (r_d || R_s)$$

But

$$V_i = -V_{gs} + V_o$$
$$= -V_{gs} + [-g_m V_{gs} (r_d \,||\, R_s)]$$

Substitute the value Vo and Vi. Then

$$A_v = \frac{-g_m V_{gs} (r_d \,||\, R_s)}{-V_{gs} (1 + g_m (r_d \,||\, R_s))}$$
$$= \frac{g_m (r_d \,||\, R_s)}{1 + g_m (r_d \,||\, R_s)}$$

if $r_d >> R_s$

$$A_v = \frac{g_m R_s}{1 + g_m R_s}$$

if $g_m R_s >> 1$

$A_v \approx 1$, but it is always less than one.

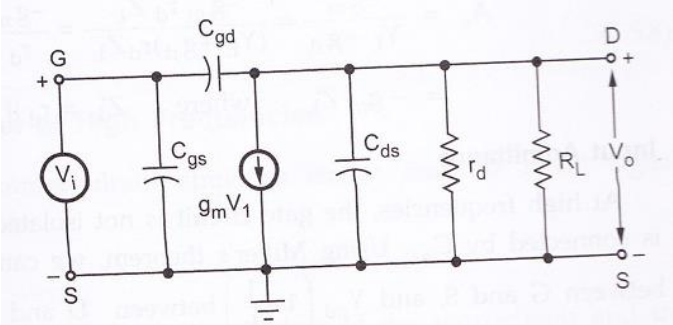
Common drain circuit does not provide voltage gain.& there is no phase shift between input and output voltages.

Table summarizes the performance of common drain amplifier

	Exact	$r_d >> R_D$
Z_i	R_G	R_G
Z_o	$\frac{1}{g_m} \,||\, R_s$	$\frac{1}{g_m} \,||\, R_s$
A_v	$\frac{g_m (r_d \,||\, R_s)}{1 + g_m (r_d \,||\, R_s)}$	$\frac{g_m R_s}{1 + g_m R_s}$

3.6 High frequency analysis of MOSFET:

3.6.1 Common source amplifier at high frequencies:



Small signal equivalent circuit at high frequencies

$$Y = \frac{1}{Z} = Y_L + Y_{ds} + g_d + Y_{gd}$$

where

$Y_L = \frac{1}{R_L}$: admittance corresponding to R_L

$Y_{ds} = j\omega C_{ds}$: admittance corresponding to C_{ds}

$g_d = \frac{1}{r_d}$: conductance corresponding to r_d

$Y_{gd} = j\omega C_{gd}$: admittance corresponding to C_{gd}

$$I = -g_m V_i + V_i Y_{gd} = V_i (-g_m + Y_{gd})$$

Voltage gain:

The voltage gain for common source amplifier circuit with the load R_L is given by,

$$A_v = \frac{V_o}{V_i} = \frac{IZ}{V_i} = \frac{I}{V_i Y}$$

Substituting the values of I and Y from equations (2) and (3) we have,

$$A_v = \frac{-g_m + Y_{gd}}{Y_L + Y_{ds} + g_d + Y_{gd}}$$

At low frequencies, Y_{ds} and $Y_{gd} = 0$ and hence equation (4) reduces to

$$A_v = \frac{-g_m}{Y_L + g_d} = \frac{-g_m r_d Z_L}{(Y_L + g_d) r_d Z_L} = \frac{-g_m r_d Z_L}{r_d + Z_L}$$

$$= -g_m Z_L' \qquad \text{where} \quad Z_L' = r_d \,||\, Z_L$$

Input Admittance:

$$Y_i = Y_{gs} + (1 - A_v) Y_{gd}$$

Input capacitance (Miller Effect):

$$A_v = -g_m R'_d \qquad \text{where} \qquad R'_d = r_d R_d$$

Substituting the value of A_v

$$\frac{Y_i}{j\omega} \equiv C_i = C_{gs} + (1 + g_m R'_d) C_{gd}$$

This increase in input capacitance C_i over the capacitance from gate to source is called Miller effect.

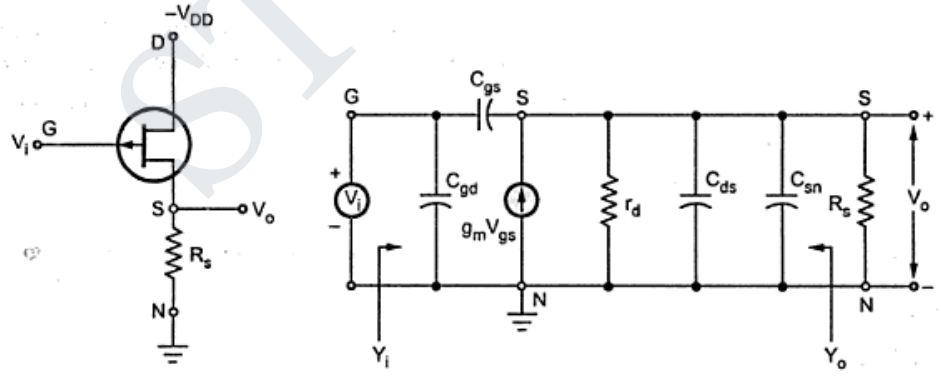
This input capacitance affects the gain at high frequencies in the operation of cascaded amplifiers. In cascaded amplifiers, the output from one stage is used as the input to a second amplifier. The input impedance of a second stage acts as a shunt across output of the first stage and R_d is shunted by the capacitance C_i.

Output Admittance:

From above figure, the output impedance is obtained by looking into the drain with the input voltage set equal to zero. If $V_i = 0$ in figure, r_d , C_{ds} and C_{gd} in parallel. Hence the output admittance with R_L considered external to the amplifier is given by,

$$Y_o = g_d + Y_{ds} + Y_{gd}$$

3.6.2 Common Drain Amplifier at High Frequencies:



a) Source follower

b) Small signal high frequency equivalent circuit

Fig. Common Drain Amplifier Circuit & Small signal equivalent circuit at high

frequencies

Voltage gain:

The output voltage V_o can be found from the product of the short circuit and the impedance between terminals S and N. Voltage gain is given by,

$$\frac{V_o}{V_i} = \frac{g_m + j\omega C_{gs}}{R_s + (g_m + g_d + j\omega C_T)}$$

where $C_T \equiv C_{gs} + C_{ds} + C_{sn}$

$$A_v = \frac{(g_m + j\omega C_{gs})R_s}{1 + (g_m + g_d + j\omega C_T)R_s}$$

At low frequencies the gain reduces to

$$A_v = \frac{g_m R_s}{1 + (g_m + g_d)R_s}$$

✓ **Input Admittance:**

Input Admittance Y_i can be obtained by applying Miller's theorem to C_{gs}. It is given by,

$$Y_i = j\omega C_{gd} + j\omega C_{gs}(1 - A_v) \approx j\omega C_{gd}$$

because $A_v \approx 1$.

✓ **Output Admittance:**

Output Admittance Y_o with R_s considered external to the amplifier, it is given by,

$$Y_o = g_m + g_d + j\omega C_T$$

At low frequencies, output resistance R_o is given by,

$$R_o = \frac{1}{g_m + g_d} \approx \frac{1}{g_m} \quad \text{since } g_m >> g_d$$

3.7 Frequency Response of Common Source Amplifier:

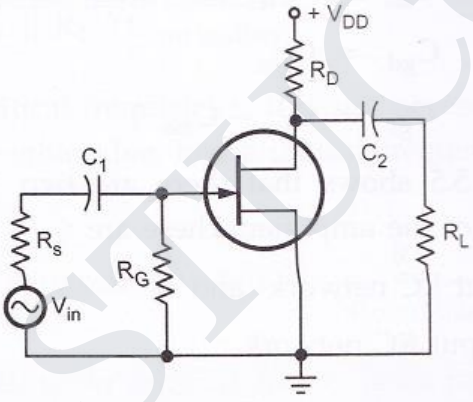


Fig. Typical RC coupled common source amplifier

Let us consider a typical common source amplifier as shown in the above figure.

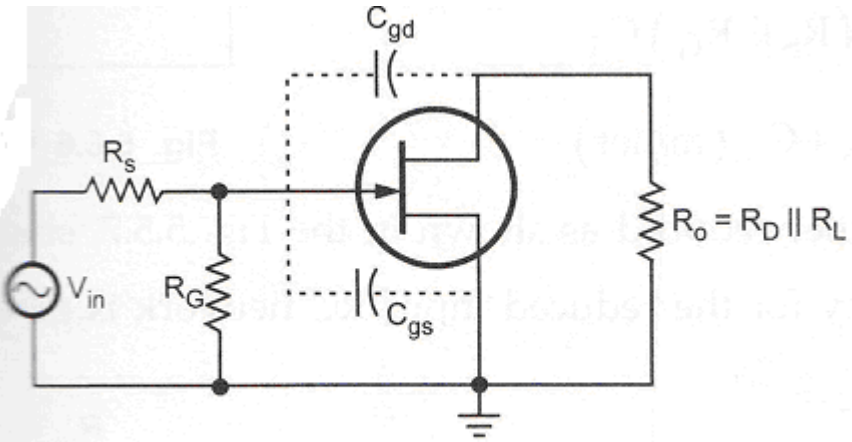


Fig. High frequency equivalent circuit

From above figure, it shows the high frequency equivalent circuit for the given amplifier circuit. It shows that at high frequencies coupling and bypass capacitors act as short circuits and do not affect the amplifier high frequency response. The equivalent circuit shows internal capacitances which affect the high frequency response.

Using Miller theorem, this high frequency equivalent circuit can be further simplified as follows:

The internal capacitance C_{gd} can be splitted into $C_{in(miller)}$ and $C_{out(miller)}$ as shown in the following figure.

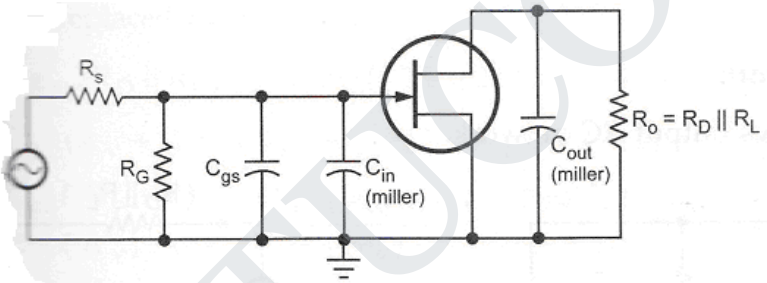


Fig. Simplified high frequency equivalent circuit

$$C_{in\,(miller)} = C_{gd}\,(A_v + 1)$$

$$C_{out\,(miller)} = C_{gd}\,\frac{(A_v + 1)}{(A_v)}$$

Where

$$C_{gd} = C_{rss}$$

$$C_{gs} = C_{iss} - C_{rss}$$

From simplified high frequency equivalent circuit, it has two RC networks which affect the high frequency response of the amplifier. These are,

1. Input RC network
2. Output RC network

Input RC network:

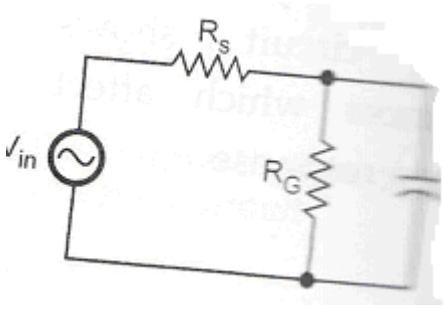


Fig. Input RC network

From above figure,

$$f_{c(input)} = \frac{1}{2\pi(R_S \parallel R_G)C_T}$$

where $C_T = C_{gs} + C_{in}(miller)$

This network is further reduced as follows since $R_s << R_G$

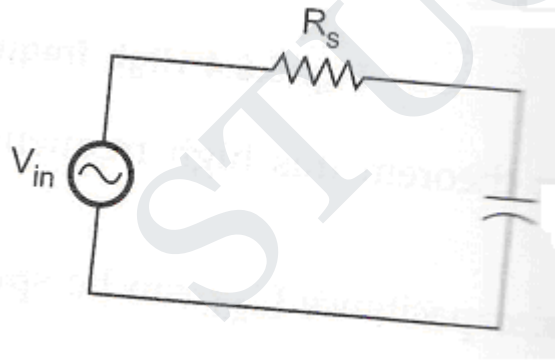


Fig. Reduced input RC network

The critical frequency for the reduced input RC network is,

$$f_{c\,(input)} = \frac{1}{2\pi R_s C_T}$$

or $$f_c = \frac{1}{2\pi R_s [C_{gs} + C_{in\,(miller)}]}$$

The phase shift in high frequency RC network is $\theta = \tan^{-1}\left(\frac{R_s}{X_{C_T}}\right)$

Output RC network:

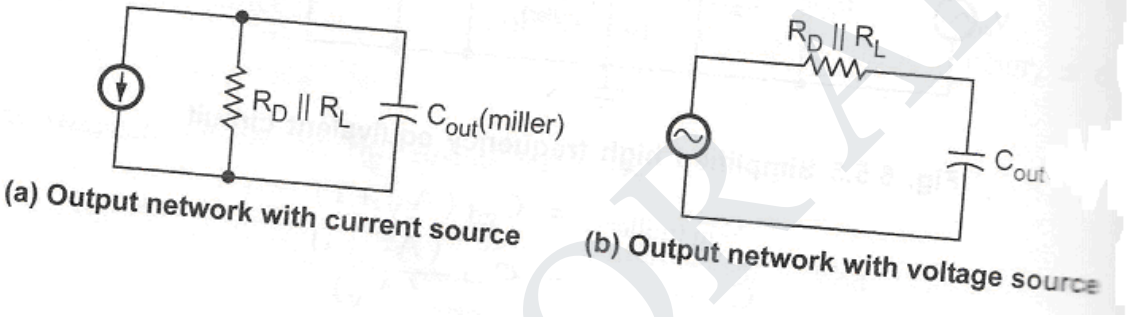


Fig. Output RC network

The critical frequency for the above circuit is,

$$f_c = \frac{1}{2\pi R_o C_{out\,(miller)}} = \frac{1}{2\pi (R_D \parallel R_L) C_{out\,(miller)}}$$

It is not necessary that these frequencies should be equal. The network which has lower critical frequency than other network is called dominant network.

The phase shift in high frequency is

$$\theta = \tan^{-1}\left(\frac{R_o}{X_{C\,out\,(Miller)}}\right)$$

Review questions.

PART-B

1. Describe the methods of determination of h-parameters from its static Input and output characteristics. (8)
2. Draw and explain the h-parameter equivalent circuit of a transistor in CC configuration. derive the expressions for input impedance ,output impedance, voltage gain and current gain (16)
3. Explain the switching characteristics of a transistor with neat sketch. (10)
4. Describe the static input and output characteristics of CB configuration of a transistor with neat circuit diagram. (16)
5. Derive the expression for current gain, input impedance and voltage gain of a CE Transistor Amplifier. (16)
6. Draw the circuit for determining the transistor common base characteristics and explain how the characteristics are measured and draw the graphs. (16)
7. For a common emitter circuit draw the h-parameter equivalent circuit and write the expressions for input impedance, output impedance and voltage gain. (16)
8. Explain the midband analysis of single stage CE, CB and CC amplifiers. (16)
9. Explain the analysis of low frequency response of RC coupled amplifiers. (16)
10. Compare the characteristics of the different configurations of BJT amplifiers.(8)
11. Draw and explain the hybrid π model of a CE configuration of a transistor and derive the necessary expressions.(16)
12. Draw and explain the h-parameter equivalent circuit of a transistor in CE configuration. derive the expressions for input impedance ,output impedance, voltage gain and current gain (16)

UNIT 4 MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIER

4.1 Multistage Amplifiers

In practice, we need amplifier which can amplify a signal from a very weak source such as a microphone, to a level which is suitable for the operation of another transducer

such as loudspeaker . This is achieved by cascading number of amplifier stages, known as multistage amplifier

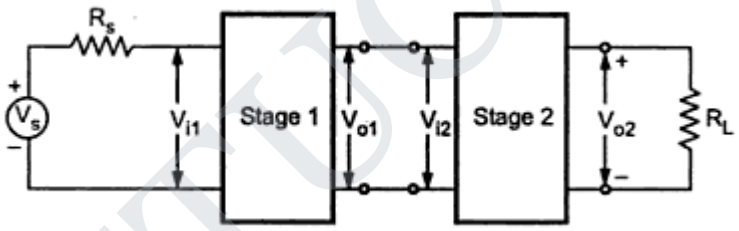
4.1.1 Need for Cascading

For faithful amplification amplifier should have desired voltage gain, current gain and it should match its input impedance with the source and output impedance with the load. Many times these primary requirements of the amplifier can not be achieved with single stage amplifier, because of the limitation of the transistor/FET parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification.

We can say that,

- When the amplification of a single stage amplifier is not sufficient, or,
- When the input or output impedance is not of the correct magnitude, for a particular application two or more amplifier stages are connected, in cascade. Such amplifier,with two or more stages is also known as multistage amplifier.
-

Two Stage Cascaded Amplifier



Vi1 is the input of the first stage and Vo2 is the output of second stage.

So,Vo2/Vi1 is the overall voltage gain of two stage amplifier.

$$A_V = \frac{V_{o2}}{V_{i1}}$$

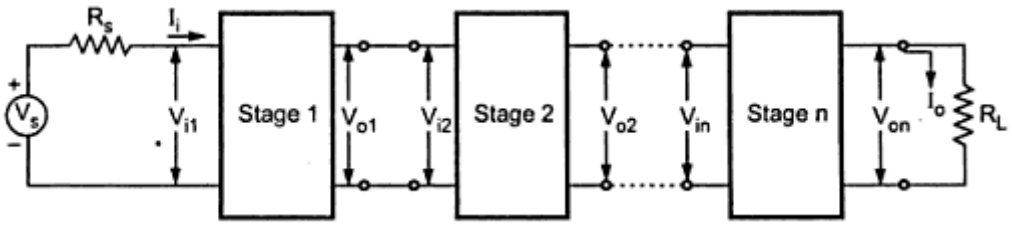
$$= \frac{V_{o2}}{V_{i2}} \frac{V_{i2}}{V_{i1}}$$

$$V_{o1} = V_{i2}$$

$$\therefore A_V = \frac{V_{o2}}{V_{i2}} \frac{V_{o1}}{V_{i1}}$$

$$= A_{V2} A_{V1}$$

n-Stage Cascaded Amplifier



Voltage gain :

The resultant voltage gain of the multistage amplifier is the product of voltage gains of the various stages.

Av = Avl Av2 ... Avn

Gain in Decibels

In many situations it is found very convenient to compare two powers on logarithmic scale rather than on a linear scale. The unit of this logarithmic scale is called decibel (abbreviated dB). The number N decibels by which a power P2 exceeds the power P1 is defined by

$$N = 10 \log \frac{P_2}{P_1}$$

Decibel, dB denotes power ratio. Negative values of number of dB means that the power P2 is less than the reference power P1 and positive value of number of dB means the power P2 is greater than the reference power P1.

For an amplifier, P1 may represent input power, and P2 may represent output power.

Both can be given as

$$P_1 = \frac{V_i^2}{R_i} \text{ and } P_2 = \frac{V_o^2}{R_o}$$

Where Ri and Ro are the input and output impedances of the amplifier respectively.Then,

$$N = 10 \log_{10} \frac{V_o^2 / R_o}{V_i^2 / R_i}$$

If the input and output impedances of the amplifier are equal i.e. Ri = Ro= R, then

$$N = 10 \log_{10} \frac{V_o^2}{V_i^2} = 10 \log_{10} \left(\frac{V_o^2}{V_i^2} \right) = 10 \times 2 \log_{10} \frac{V_o}{V_i} = 20 \log_{10} \frac{V_o}{V_i}$$

Gain of Multistage Amplifier in dB

The gain of a multistage amplifier can be easily calculated if the gain of the individual stages are known in dB, as shown below

$$20 \log_{10} Av = 20 \log_{10} Avl + 20 \log_{10} Av2 + \ldots + 20 \log_{10} Avn$$

Thus, the overall voltage gain in dB of a multistage amplifier is the decibel voltage gains of the individual stages. It can be given as

$$AvdB = AvldB + Av2dB + ... + AvndB$$

4.1.2 Advantages of Representation of Gain in Decibels

Logarithmic scale is preferred over linear scale to represent voltage and power gains because of the following reasons :

- In multistage amplifiers, it permits to add individual gains of the stages to calculate overall gain.
- It allows us to denote, both very small as well as very large quantities of linear, scale by considerably small figures.

For example, voltage gain of 0.0000001 can be represented as -140 dB and voltage gain of 1,00,000 can be represented as 100 dB.

- Many times output of the amplifier is fed to loudspeakers to produce sound which is received by the human ear. It is important to note that the ear responds to the sound intensities on a proportional or logarithmic scale rather than linear scale. Thus use of dB unit is more appropriate for representation of amplifier gains.

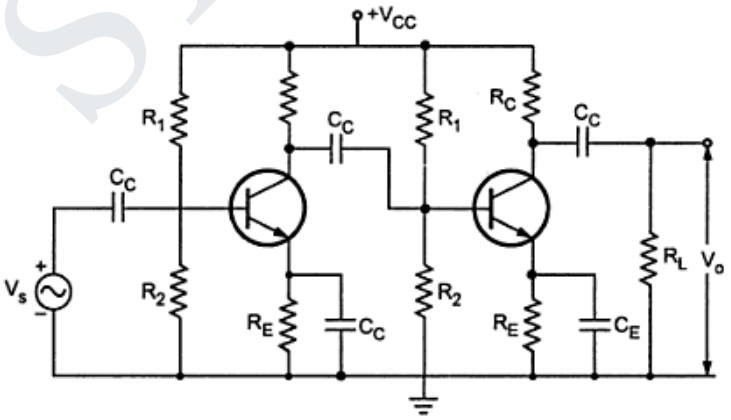
Methods of coupling Multistage Amplifiers

In multistage amplifier, the output signal of preceding stage is to be coupled to the input circuit of succeeding stage. For this interstage coupling, different types of coupling elements can be employed. These are :

1. RC coupling 2. Transformer coupling 3. Direct coupling

- **RC coupling**

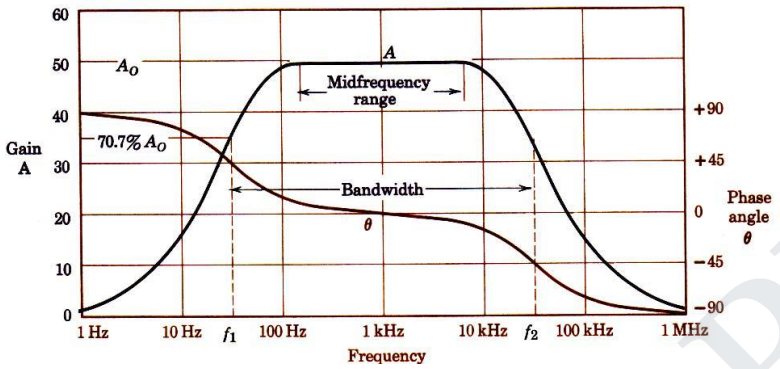
Figure shows RC coupled amplifier using transistors. The output signal of first stage is coupled to the input of the next stage through coupling capacitor and resistive load at the output terminal of first stage



The coupling does not affect the quiescent point of the next stage since the coupling capacitor Cc blocks the d.c. voltage of the first stage from reaching the base of the

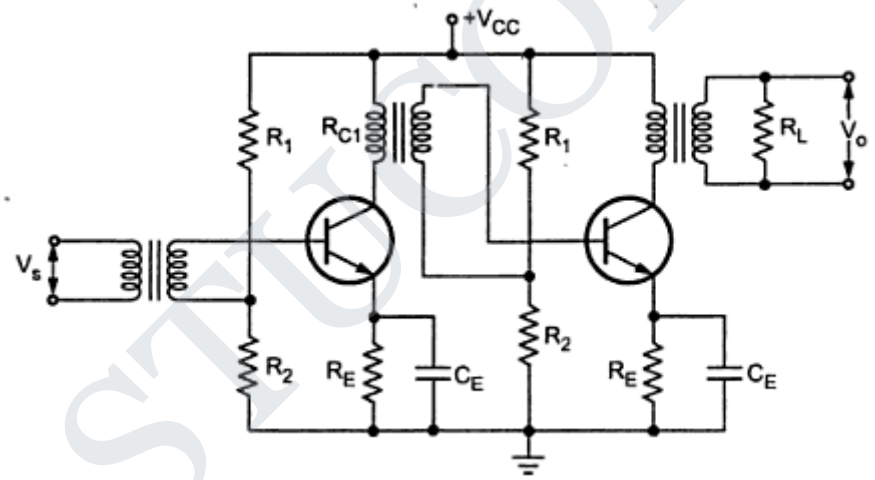
second stage. The RC network is broadband in nature. Therefore, it gives a wideband

frequency response without peak at any frequency and hence used to cover a complete A.F amplifier bands. However its frequency response drops off at very low frequencies due to coupling capacitors and also at high frequencies due to shunt capacitors such as stray capacitance.



✓ Transformer Coupling

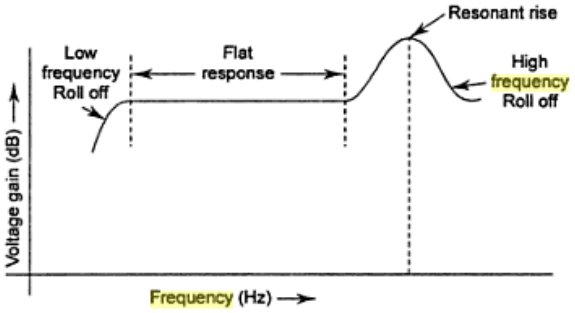
Figure shows transformer coupled amplifier using transistors. The output signal of first stage is coupled to the input of the next stage through an impedance matching transformer



This type of coupling is used to match the impedance between output an input cascaded stage. Usually, it is used to match the larger output resistance of AF power amplifier to a low impedance load like loudspeaker. As we know, transformer blocks d.c, providing d.c. isolation between the two stages. Therefore, transformer coupling does not affect the quiescent point of the next stage.

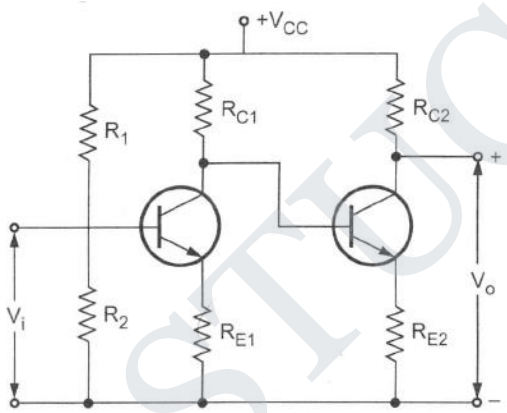
Frequency response of transformer coupled amplifier is poor in comparison with that an RC coupled amplifier. Its leakage inductance and inter winding capacitances does not allow amplifier to amplify the signals of different frequencies equally well. Inter winding capacitance of the transformer coupled may give rise resonance at certain frequency which makes amplifier to give very high gain at that frequency. By putting shunting capacitors across each winding of the transformer, we can get resonance at any desired RF frequency. Such amplifiers are called tuned voltage amplifiers. These provide high gain at the desired of frequency, i.e. they amplify selective frequencies. For

this reason, the transformer-coupled amplifiers are used in radio and TV receivers for amplifying RF signals. As d.c. resistance of the transformer winding is very low, almost all d.c. voltage applied by Vcc is available at the collector. Due to the absence of collector resistance it eliminates unnecessary power loss in the resistor.



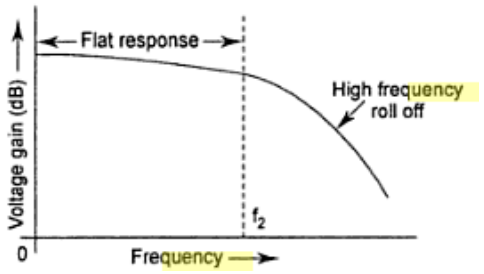
- **Direct Coupling**

Figure shows direct coupled amplifier using transistors. The output signal of first stage is directly connected to the input of the next stage. This direct coupling allows the quiescent d.c. collector current of first stage to pass through base of the next stage, affecting its biasing conditions.



Due to absence of RC components, frequency response is good but at higher frequencies shunting capacitors such as stray capacitances reduce gain of the amplifier.

The transistor parameters such as V_{BE} and β change with temperature causing the collector current and voltage to change. Because of direct coupling these changes appear at the base of next stage, and hence in the output. Such an unwanted change in the output is called drift and it is serious problem in the direct coupled amplifiers.



4.2 Introduction of Differential Amplifier

A device which accepts an input signal and produces an output signal proportional to the input, is called an amplifier. An amplifier which amplifies the difference between The two input signals is called differential amplifier. The differential amplifier configuration is used in variety of analog circuits. The. differential amplifier is an essential and basic building block in modern IC amplifier .The Integrated Circuit (IC) technology is well known now a days, due to which the design of complex circuits become very simple. The IC version of operational amplifier is inexpensive, takes up less space and consumes less power. The. differential amplifier is the basic building block of such IC operational amplifier.

4.2.1 Basics of Differential Amplifier

The Differential Amplifier amplifies the difference between two input voltage signal. Hence it is also called as difference amplifier.
Consider an ideal differential amplifier shown in the Fig. A

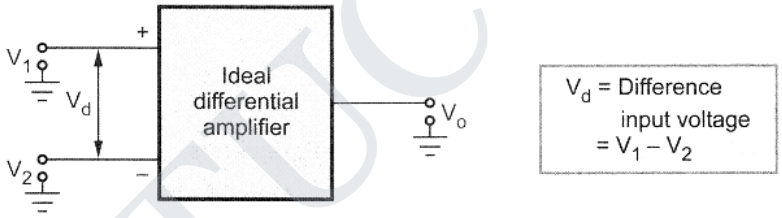


Fig. Ideal differential amplifier

V_1 and V_2 are the two input signals while Vo is the output. Each signal is measured with respect to the ground.
In an ideal differential amplifier, the output voltage Vo is proportional to the difference between the two input signals. Hence we can write,

$$V_o \propto (V_1 - V_2) \quad \ldots(1)$$

Differential Gain A_d

From Equation 1 we can write,

$$\therefore \quad V_o = A_d (V_1 - V_2) \quad \ldots(2)$$

where A_D is the constant of proportionality. The A_D is the gain with which differential amplifier amplifies the difference between two input signals. Thus it is called differential gain of the differential amplifier.
Thus, Ad = Differential gain
The difference between the two inputs (V_1 - V_2) is generally called difference voltage

and denoted as Vd.

$$V_o = A_d V_d \quad ...(3)$$

Hence the differential gain can be expressed as,

$$A_d = \frac{V_o}{V_d} \quad ...(4)$$

Generally the differential gain is expressed in its decibel (dB) value as,

$$A_d = 20 \text{ Log}_{10} (A_d) \text{ in dB} \quad ...(5)$$

➢ Common Mode Gain Ac

If we apply two input voltages which are equal in all the respects to the differential amplifier i.e. V1 = Vz then ideally the output voltage Vo = (V_1 - V_2) A_d, must be zero.But the output voltage of the practical differential amplifier not only depends on thedifference voltage but also depends on the average common level of the two inputs. Such an average level of the two input signals is called common mode signal denoted as V_C

$$V_c = \frac{V_1 + V_2}{2} \quad ...(6)$$

Practically, the differential amplifier produces the output voltage proportional to such common mode signal, also.

The gain with wich it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier A_C.

$$V_o = A_c V_c \quad ..(7)$$

Thus there exists some finite output for V1 = V2 due to such common mode gain A_C, in case of practical differential amplifiers.

So the total output of any differential amplifier can be expressed as,

$$V_o = A_d V_d + A_c V_c \quad ..(8)$$

For an ideal differential amplifier, the differential gain A_d, must be infinite while the common mode gain must be zero.

But due to mismatch in the internal circuitry, there is some output available for V_1 = V2 and gain A_C is not practically zero. The value of such common mode gain A_C very small while the value of the differential gain A_d is always very large.

➢ Common Mode Rejection Ratio (CMRR)

When the same voltage is applied to both the inputs, the differential amplifier is said to be operated in a common mode configuration. Many disturbance signals, noise signal appear as a common input signal to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier.

The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common mode rejection ratio denoted as CMRR.

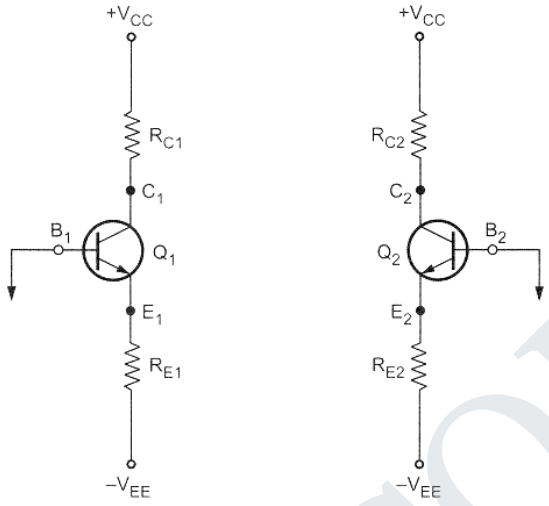
It is defined as the ratio of the differential voltage gain A_d to common mode voltage gain A_C

$$\text{CMRR} = \rho = \left|\frac{A_d}{A_c}\right| \quad ....(9)$$

$$\text{CMRR in dB} = 20 \log \left| \frac{A_d}{A_c} \right| \text{dB} \quad \text{.....(10)}$$

4.2.2 Transistorised Differential Amplifier

The transistorised differential amplifier basically uses the emitter biased circuits which are identical in characteristics. Such two identical emitter biased circuits are



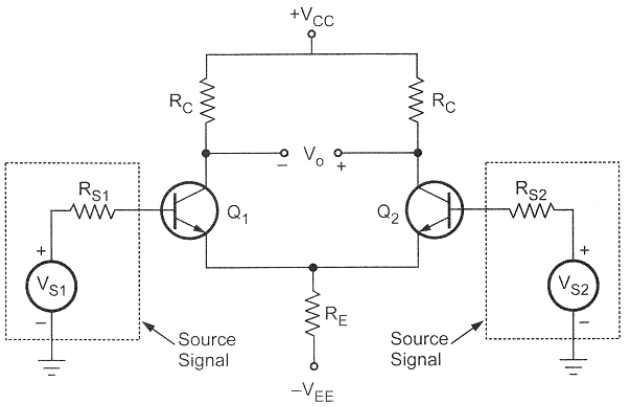
Emitter biased circuits

The two transistors Q1 and Q2 have exactly matched characteristics. The two collector Resistors R_{C1} and R_{C2} are equal while the two emitter resistances R_{E1} and R_{E2} are equal.

$R_{C1} = R_{C2}$ and $R_{E1} = R_{E2}$

The magnitudes of + Vcc and – V_{EE} are also same. The differential amplifier can be obtained by using such two emitter biased circuits. This is achieved by connectinemitter E1 of Q1 to the emitter E2 of Q2. Due to this, R_{E1} appears in parallel with $R_{E2}$and the combination can be replaced by a single resistance denoted as R_E. The base $B_1$of Q1 is connected to the input 1 which is V_{S1} while the base B_2 of Q_2 is connected tothe input 2 which is Vs2. The supply voltages are measured with respect to ground. Thebalanced output is taken between the collector C1 of Q1 and the collector C2 of Q_2. Suchan amplifier is called emitter coupled differential amplifier. The two collectorresistances are same hence can be denoted as R_C.

The output can be taken between two collectors or in between one of the twocollectors and the ground. When the output is taken between the two collectors, none of them is grounded then it is called balanced output, double ended output or floatingoutput. When the output is taken between any of the collectors and the ground, it is calledunbalanced output or single ended output. The complete circuit diagram of such a basicdual input, balanced output differential amplifier is shown in the Fig.



Dual input, balanced output differential amplifier

As the output is taken between two output terminals, none of them is grounded, it is called balanced output differential amplifier.
Let us study the circuit operation in the two modes namely
i) Differential mode operation
ii)Common mode operation

4.2.3 Differential Mode Operation

In the differential mode, the two input signals are different from each other. Consider the two input signals which are same in magnitude but 180" out of phase. These signals, with opposite phase can be obtained from the center tap transformer. The circuit used in differential mode operation is shown in the Fig..

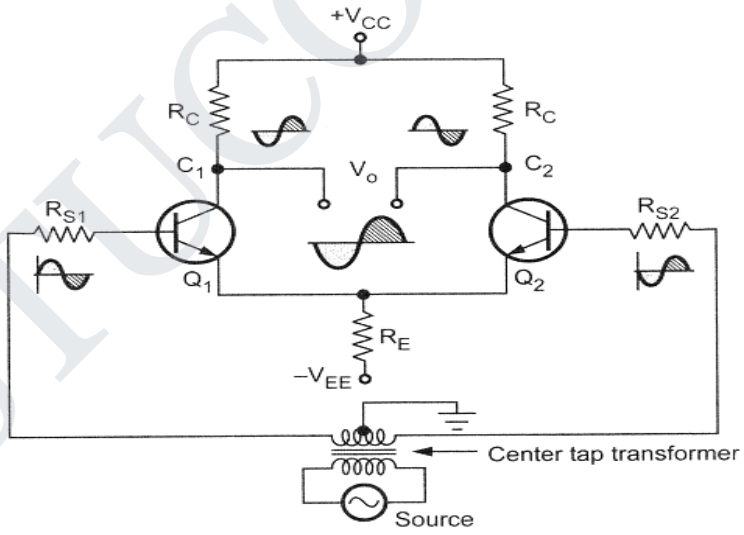


Fig Differential mode operation

Assume that the sine wave on the base of Q_1 is positive going while on the base of Q_2 is negative going. With a positive going signal on the base of Q_1, m amplified negative going signal develops on the collector of Q1. Due to positive going signal, current through R_E also increases and hence a positive going wave is developed across R_E. Due to negative going signal on the base of Q2, an amplified positive going signal develops on the collector of Q_2. And a negative going signal develops across R_E, because of emitter follower action of Q_2. So signal voltages across R_E, due to the effect of Q1 and Q2 are equal in magnitude and 180o out of phase, due to matched pair of transistors. Hence these two signals cancel each other and there is no signal across the emitter resistance. Hence there is no a.c. signal current flowing through the emitter resistance.

Hence R_E in this case does not introduce negative feedback. While Vo is the output taken across collector of Q1 and collector of Q_2. The two outputs on collector L and 2 are equal in magnitude but opposite in polarity. And Vo is the difference between these two signals, e.g. +10 - (-10) = + 20.

Hence the difference output Vo is twice as large as the signal voltage from either collector to ground

4.2.4 common Mode operation

In this mode, the signals applied to the base of Q1 and Q2 are derived from the same source. So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in the Fig.

In phase signal voltages at the bases of Q1 and Q2 causes in phase signal voltages to appear across R_E, which add together. Hence R_E carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier.

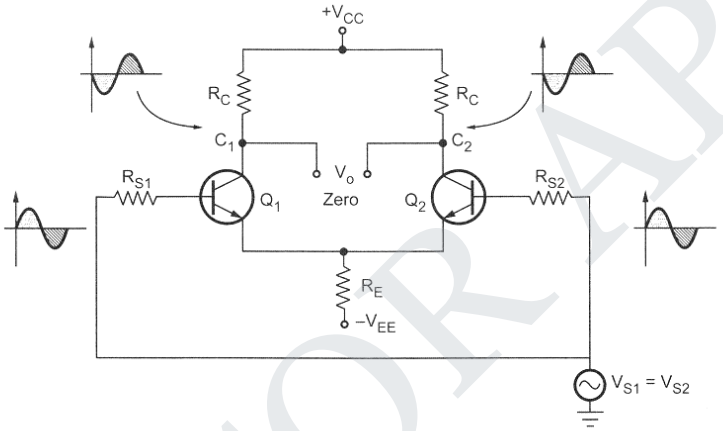


Fig. Common mode operation

While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q_1 and Q2. Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase,

Eg. (20) - (20) = 0. Thus the difference output Vo is almost zero, negligibly small. ideally it should be zero.

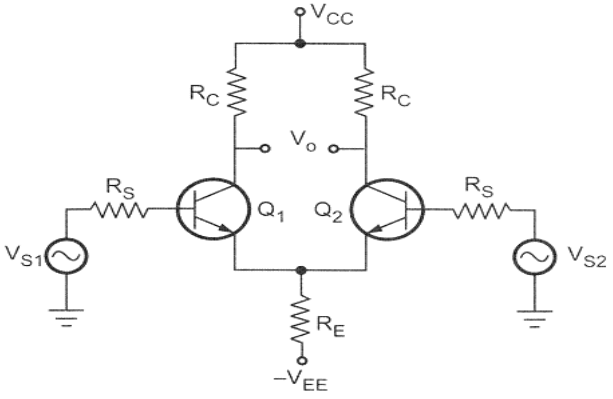
- **Configurations of Differential Amplifier**

The differential amplifier, in the difference amplifier stage in the op-amp, can be used in four configurations :

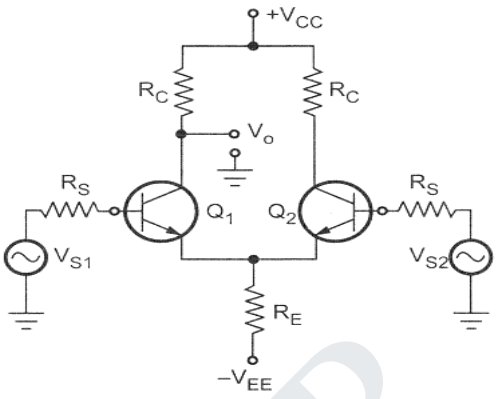
i) Dual input balanced output differential amplifier.
ii) Dual input, unbalanced output differential amplifier.
iii) Single input, balanced output differential amplifier.
iv) Single input, unbalanced output differential amplifier.

The differential amplifier uses two transistors in common emitter configuration. If output is taken between the two collectors it is called balanced output or double ended output. While if the output is taken between one collector with respect to ground it iscalled unbalanced output or single ended output. If the signal is given to both the input terminals it is called dual input, while if the signal is given to only one input terminal and other terminal is grounded it is called single input or single ended input Out of these four configurations the dual input, balanced output is the basic differential amplifier configuration. This is shown in the Fig. (a). The dual input,unbalanced output differential amplifier is shown in the Fig.(b). The single input,balanced output

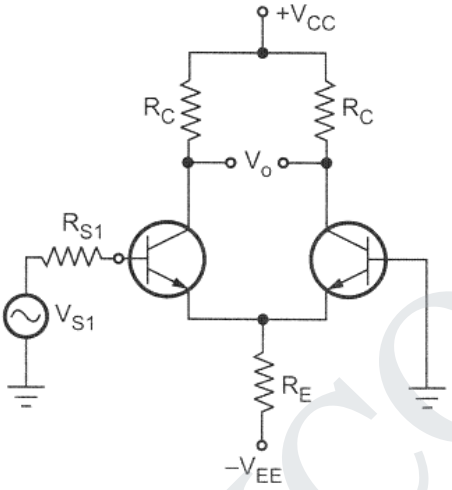
differential amplifier is shown in the Fig (c) and the single input,unbalanced output differential amplifier is shown in the Fig. (d).



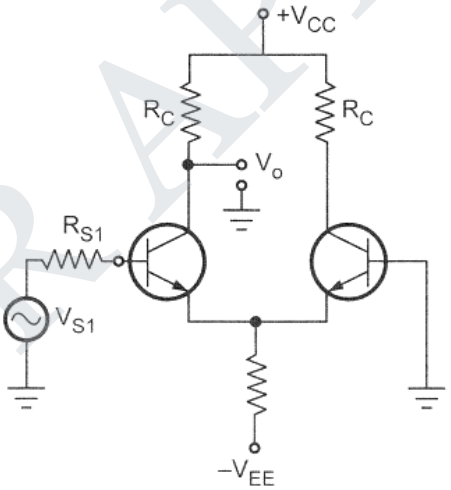
(a) Dual input balanced output



(b) Dual input unbalanced output



(c) Single input balanced output



(d) Single input unbalanced output

4.2.5 D.C. Analysis of Differential Amplifier

The d.c. analysis means to obtain the operating point values i.e. I_{CQ} and V_{CEQ} for the transistors used. The supply voltages are d.c. while the input signals are a.c., so d.c. equivalent circuit can be obtained simply by reducing the input a.c. signals to zero. The d.c. equivalent circuit thus obtained is shown in the Fig.. Assuming $Rs_1 = R_{S2}$, the source resistance is simply denoted by Rs ,

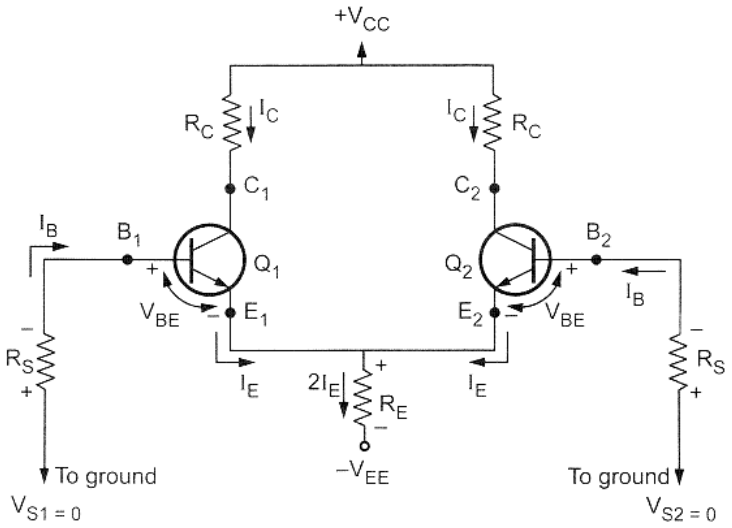


Fig. D.C. equivalent circuit

.

The transistors Q1 and Q_2 are matched transistors and hence for such a matched pair we can assume :

i) Both the transistors have the same characteristics.

ii) $R_{E1} = R_{E2}$ hence $R_E = R_{E1} \text{ ll } R_{E2}$.

iii) $R_{C1} = R_{C2}$ hence denoted as R_C.

iv) $|V_{CC}| = |V_{EE}|$ and both are measured with respect to ground.

As the two transistors are matched and circuit is symmetrical, it is enough to find out operating point I_{CQ} and V_{CEQ}, for any one of the two transistors. The same is applicable for the other transistor.

Apply-g KVL to base-emitter loop of the transistor Q1,

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \ldots(1)$$

$$I_C = \beta I_B \text{ and } I_C \cong I_E$$

$$I_B = \frac{I_E}{\beta} \quad \ldots(2)$$

Substituting in equation (1), we get

$$\frac{-I_E R_S}{\beta} - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \ldots(3)$$

$$I_E \left[\frac{-R_S}{\beta} - 2R_E\right] + V_{EE} - V_{BE} = 0 \quad \ldots(4)$$

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E} \quad \ldots(5)$$

V_{BE} = 0.6 to 0.7 V for silicon

= 0.2 V for germanium transistors.

In practice, generally $\frac{R_S}{\beta} << 2 R_E$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad \ldots(6)$$

Now let us determine V_{CE}. As I_E is known and $I_E \cong I_C$, we can determine the collector voltage of Q_1 as

$$V_C = V_{CC} - I_C R_C \quad \ldots(7)$$

Neglecting the drop across R_S, we can say that the voltage at the emitter of Q_1 is approximately equal to $-V_{BE}$. Hence the collector to emitter voltage is

$$\therefore \quad V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (-V_{BE})$$

$$\therefore \quad V_{CE} = V_{CC} + V_{BE} - I_C R_C \quad \ldots(8)$$

Hence $I_E = I_C = I_{CQ}$ while $V_{CE} = V_{CEQ}$ for given values of V_{CC} and V_{EE}.

Thus for both the transistors, we can determine operating point values, using equations (6) and (8) With the same biasing arrangement, the d.c. analysis remains same for all the four possible configurations of differential amplifier.

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E} \approx \frac{V_{EE} - V_{BE}}{2R_E} \approx I_{CQ}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$

4.3 Tuned amplifier

✓ Communication circuit widely uses tuned amplifier and they are used in MW & SW radio frequency 550 KHz – 16 MHz, 54 – 88 MHz, FM 88 – 108 MHz, cell phones 470 - 990 MHz

✓ Band width is 3 dB frequency interval of pass band and –30 dB frequency interval

✓ Tune amplifiers are also classified as A, B, C similar to power amplifiers based on conduction angle of devices.

Series resonant circuit

Series resonant features minimum impedance (RS) at resonant.

✓ f r = ½√LC; q = L/Rs at resonance L=1/c, BW=fr/Q

✓ It behaves as purely resistance at resonance, capacitive below and inductive above resonance

Paralel resonant circuit

✓ Paralel resonance features maximum impedance at resonance = L/RsC

✓ At resonance Fr=1/2√1/(LC-Rs2/L2); if Rs=0, fr=1/2√(LC)

✓ At resonance it exhibits pure resistance and below fr parallel circuit exhibits inductive and above

capacitive impedance

4.3.1 Need for tuned circuits:

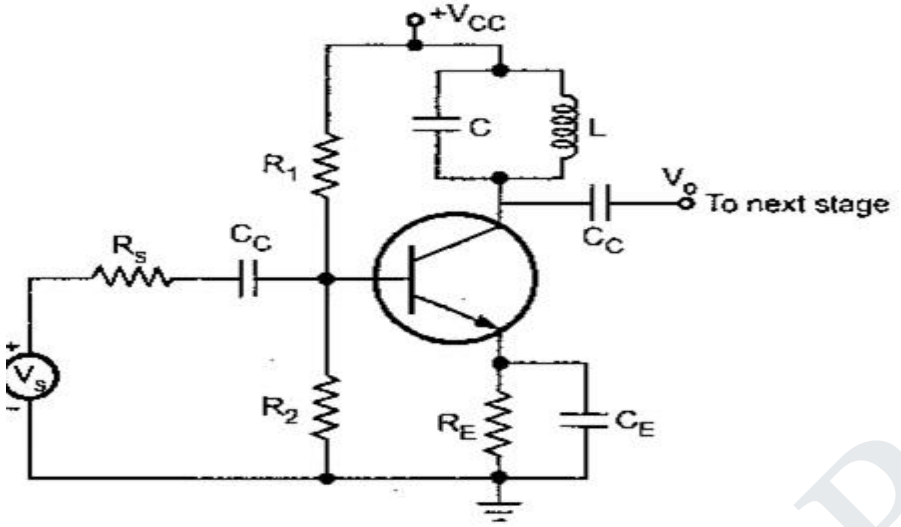
To understand tuned circuits, we first have to understand the phenomenon of self-induction. And to understand this, we need to know about induction. The first discovery about the interaction between electric current and magnetism was the realization that an electric current created a magnetic field around the conductor. It was then discovered that this effect could be enhanced greatly by winding the conductor into a coil. The effect proved to be two-way: If a conductor, maybe in the form of a coil was placed in a changing magnetic field, a current could be made to flow in it; this is called induction.

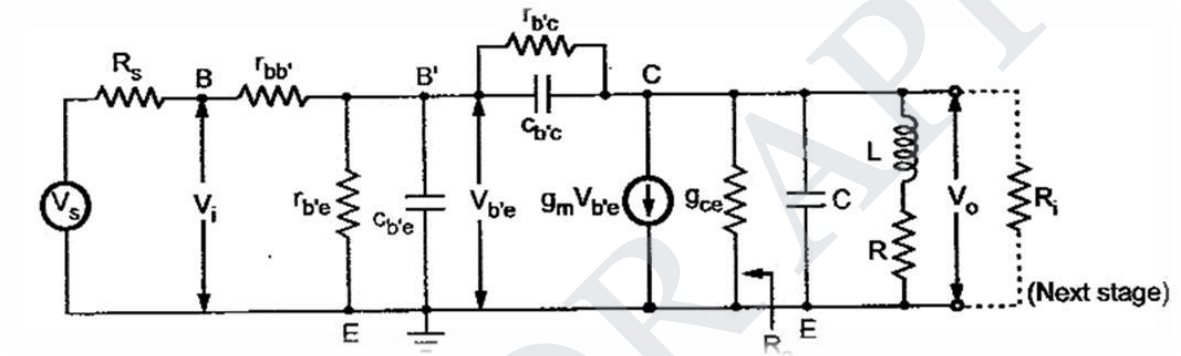
So imagine a coil, and imagine that we apply a voltage to it. As current starts to flow, a magnetic field is created. But this means that our coil is in a changing magnetic field, and this induces a current in the coil. The induced current runs contrary to the applied current, effectively diminishing it. We have discovered self-induction. What happens is that the self-induction delays the build-up of current in the coil, but eventually the current will reach its maximum and stabilize at a value only determined by the ohmic resistance in the coil and the voltage applied. We now have a steady current and a steady magnetic field. During the buildup of the field, energy was supplied to the coil, where did that energy go? It went into the magnetic field, and as long as the magnetic field exists, it will be stored there.

Now imagine that we remove the current source. Without a steady current to uphold it, the magnetic field starts to disappear, but this means our coil is again in a variable field which induces a current into it. This time the current is in the direction of the applied current, delaying the decay of the current and the magnetic field till the stored energy is spent. This can give a funny effect: Since the coil **must** get rid of the stored energy, the voltage over it rises indefinitely until a current can run somewhere! This means you can get a surprising amount of sparks and arching when coils are involved. If the coil is large enough, you can actually get an electric shock from a low-voltage source like an ohmmeter.

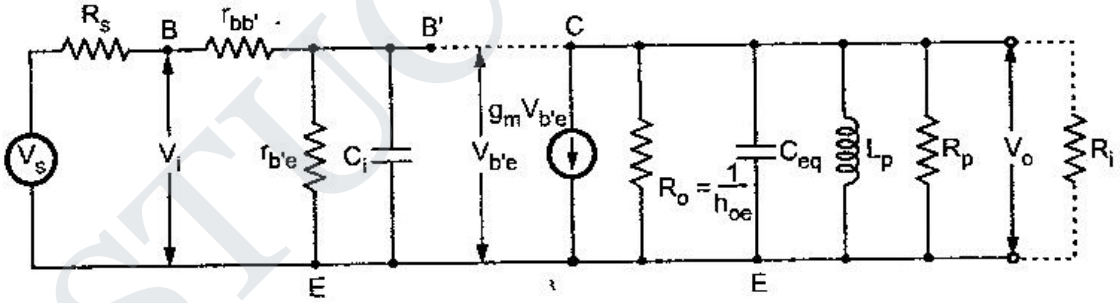
4.3.2 Single tuned amplifier.

Single Tuned Amplifiers consist of only one Tank Circuit and the amplifying frequency range isdetermined by it. By giving signal to its input terminal of various Frequency Ranges. The Tank Circuit onits collector delivers High Impedance on resonant Frequency, Thus the amplified signal is CompletelyAvailable on the output Terminal. And for input signals other than Resonant Frequency, the tank circuit provides lower impedance, hence most of the signals get attenuated at collector Terminal.





Ri- input resistance of the next stage
R**0**-output resistance of the generator gmVb'e
Cc & CE are negligible small
The equivalent circuit is simplified by



Simplified equivalent circuit

$$C_i = C_{b'e} + C_{b'c}(1 - A)$$

$$C_{eq} = C_{b'c}\left(\frac{A-1}{A}\right) + C$$

Where,
A-Voltage gain of the amplifier
C-tuned circuit capacitance

$$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_m h_{re} \approx h_{oe} = \frac{1}{R_o}$$

4.4 General shape of frequency response of amplifiers:

An audio frequency amplifier which operates over audio frequency range extending from 20 Hz to 20 kHz. Audio frequency amplifiers are used in radio receivers, large public meeting and various announcements to be made for the passengers on railway platforms. Over the range of frequencies at which it is to be used an amplifier should ideally provide the same amplification for all frequencies. The degree to which this is done is usually indicated by the curve known as frequency response curve of the amplifier.

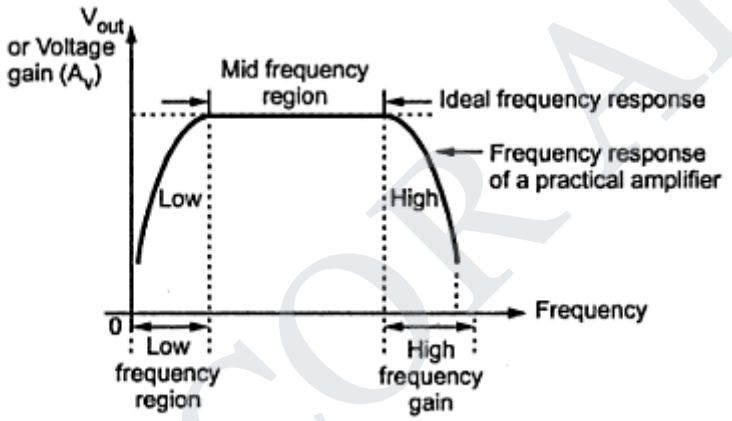


Fig. A typical frequency response of an amplifier

To plot this curve, input voltage to the amplifier is kept constant and frequency of input signal is continuously varied. The output voltage at each frequency of input signal is noted and the gain of the amplifier is calculated. For an audio frequency amplifier, the frequency range is quite large from 20 Hz to 20 kHz. In this frequency response, the gain of the amplifier remains constant in mid-frequency while the gain varies with frequency in low and high frequency regions of the curve. Only at low and high frequency ends, gain deviates from ideal characteristics. The decrease in voltage gain with frequency is called roll-off.

4.4.1 Definition of cut-off frequencies and bandwidth:

The range of frequencies can be specified over which the gain does not deviate more than 70.7% of the maximum gain at some reference mid-frequency.

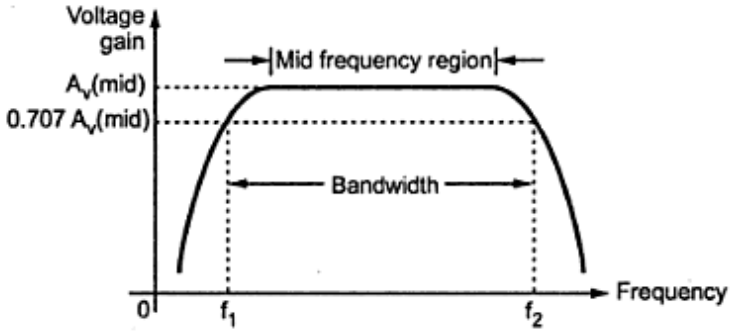


Fig. Frequency response, half power frequencies and bandwidth of an RC coupled amplifier

From above figure, the frequencies f_1 & f_2 are called lower cut-off and upper cut-off frequencies.

Bandwidth of the amplifier is defined as the difference between f_2 & f_1.

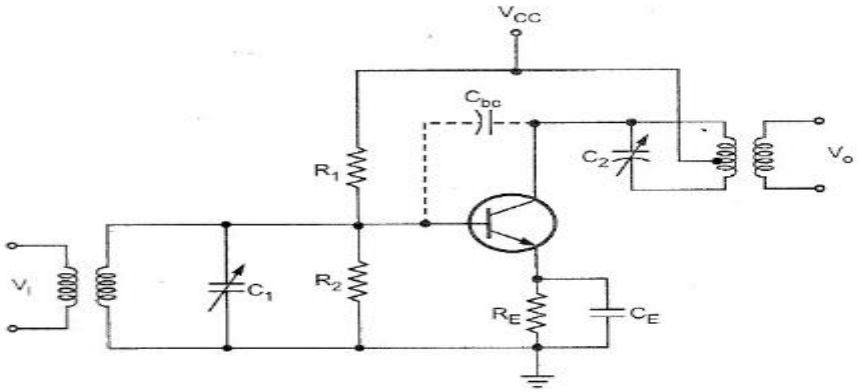
Bandwidth of the amplifier = $f_2 - f_1$

The frequency f_2 lies in high frequency region while frequency f_1 lies in low frequency region. These two frequencies are also called as half-power frequencies since gain or output voltage drops to 70.7% of maximum value and this represents a power level of one half the power at the reference frequency in mid-frequency region.

4.5 NEUTRALIZATION METHODS

In tuned RF amplifiers, transistors are used at the frequencies nearer to their unity gain bandwidths (i.e. f_T), to amplify a narrow band of high frequencies centred around a radio frequency. At this frequency, the inter junction capacitance between base and collector, C_{bc} of the transistor becomes dominant, i.e. its reactance becomes low enough to be considered, which is otherwise infinite to be neglected as open circuit. Being CE configuration capacitance C_{bc}, shown in the Fig. 3.35 come across input and output circuits of an amplifier. As reactance of C_{bc} at RF is low enough it provides the feedback path from collector to base. With this circuit condition, if some feedback signal manages to reach the input from output in a positive manner with proper phase shift, then there is possibility of circuit converted to an unstable one, generating its own oscillations and can stop working as an amplifier. This circuit will always oscillate if enough energy is fed back from the collector to the base in the correct phase to overcome circuit losses. Unfortunately, the conditions for best gain and selectivity are also those which promote oscillation. In order to prevent oscillations in tuned RF amplifiers it was necessary to reduce the stage gain to a level that ensured circuit stability. This could be accomplished in several ways such as lowering the Q of tune circuits; stagger tuning, loose coupling

V_{CC}



between the stages or inserting a 'loser' element into the circuit. While all these methods reduced gain, detuning and Q reduction had detrimental effects on selectivity. Instead of loosing the circuit performance to achieve stability, the professor L.A. Hazeltine introduced a circuit in which the troublesome effect of the collector to base capacitance of the transistor was neutralized by introducing a signal which cancels the signal coupled through the collector to base capacitance. He proved that the neutralization can be achieved by deliberately feding back a portion of the output signal to the input in such a way that it has the same amplitude as the unwanted feedback but the opposite phase. Later on many neutralizing circuits were introduced. Let us study some of these circuits.

3.10.1 Hazeltine Nèutralization

The Fig. 3.36 shows one variation of the Hazeltine circuit. In this circuit a small value of variable capacitance C_N is connected from the bottom of coil, point B, to the base. Therefore, the internal capacitance C_{bc}, shown dotted, feeds a signal from the top end of the coil, point A, to the transistor base and the C_N feeds a signal of equal magnitude but opposite polarity from the bottom of coil, point B, to the base. The neutralizing capacitor, C_N, can be adjusted correctly to completely nullify the signal fed through the C_{bc}.

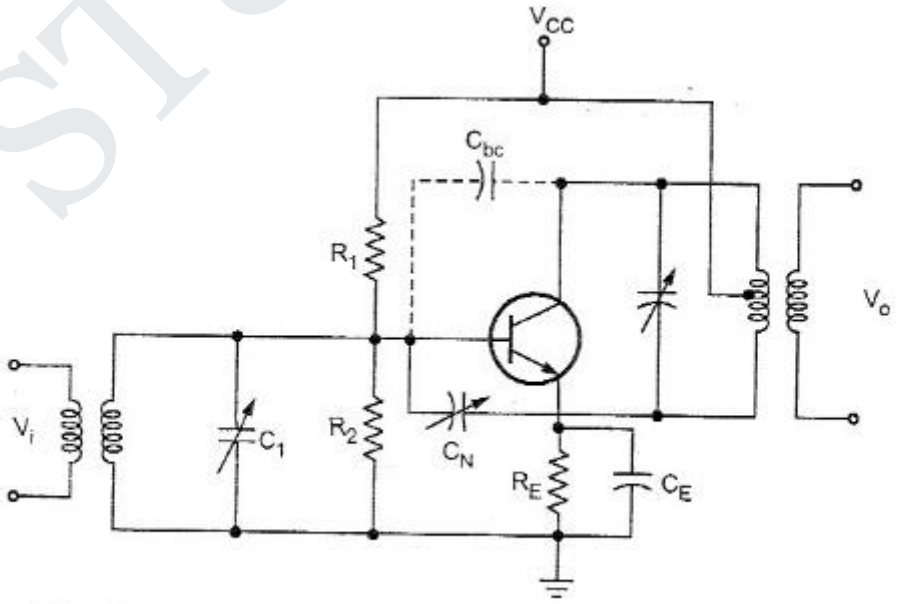


Fig. 3.36 Tuned RF amplifier with Hazeltine neutralization

4.5.1 Neutralization using coil

The Fig. 3.38 shows the neutralization of RF amplifier using coil. In this circuit, L part of the tuned circuit at the base of next stage is oriented for minimum coupling to the other windings. It is wound on a separate form and is mounted at right angles to the coupled windings. If the windings are properly polarized, the voltage across L due to the circulating current in the base circuit will have the proper phase to cancel the signal coupled through the base to collector, C_{bc} capacitance.

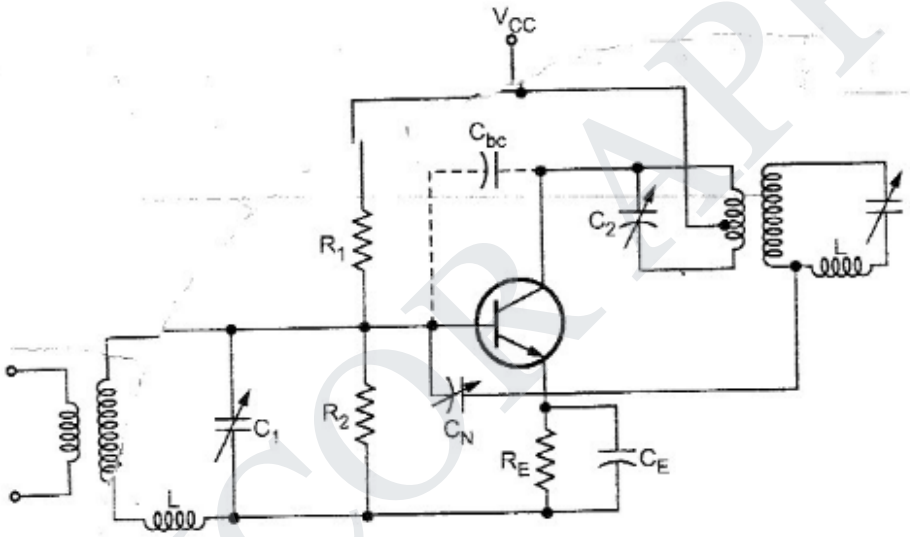


Fig. 3.38 Tuned RF amplifier using coil

4.6 POWER AMPLIFIERS :

The ideal amplifier would deliver 100 percent of the power it draws from the dc power supply to its load. In practice, 100 percent efficiency cannot be achieved (at this time) because every amplifier uses some percentage of the power it draws from the dc power supply.

The efficiency of an amplifier is the ratio of ac output power to dc input power, written as a percentage. By formula:

$$\eta = \frac{\text{ac output power}}{\text{dc input power}} \times 100$$

The lower the position of the Q-point on the dc load line, the higher the maximum theoretical efficiency of a given amplifier. Typical Q-point locations for class A, B, AB, and C amplifiers are shown in Figure 11.1 of the text.

AC Load Lines

The ac load line is a graph of all possible combinations of i_c and v_{ce} for a given amplifier. Under normal circumstances, the ac and dc load lines for a given amplifier are not identical (see Figure 11.3 of the text).

Amplifier Compliance

The compliance (PP) of an amplifier is the limit that the output circuit places on its peak-to-peak output voltage. The compliance for a given amplifier is found using the following equations:

$$PP = 2I_{CQ}r_C \text{ and } PP = 2V_{CEQ}$$

These equations are developed as illustrated in Figure 11.1.

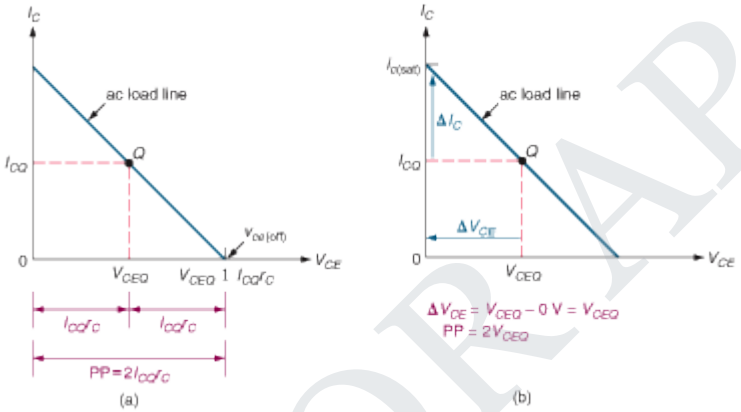


FIGURE 11.1 Amplifier compliance.

The compliance of an amplifier is determined by solving both PP equations and using the lower of the two results, as demonstrated in Example 11.1 of the text. Note the following:

- When an amplifier has a value of $PP = 2V_{CEQ}$, exceeding the value of PP results in saturation clipping.
- When an amplifier has a value of $PP = 2I_{CQ}r_C$, exceeding the value of PP results in cutoff clipping. However, the circuit will experience nonlinear distortion before the amplifier peak-to-peak output reaches the value of PP.

4.6.1 Transformer-Coupled Class A Amplifiers

A transformer-coupled class A amplifier is shown in Figure 11.2. The transformer is used to couple the amplifier output signal to its load.

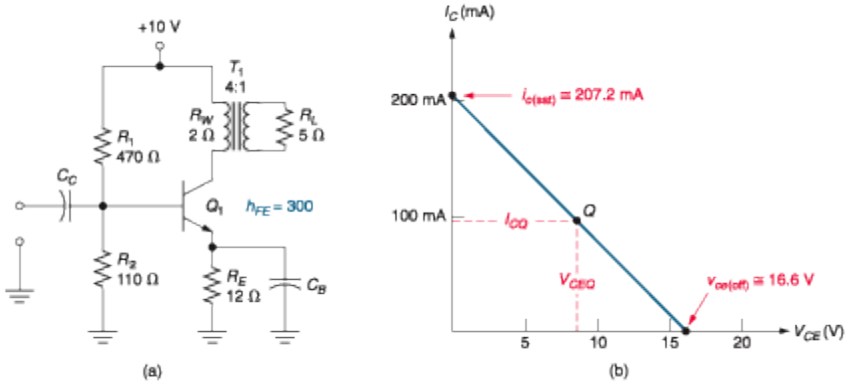


FIGURE 11.2 A transformer-coupled class A amplifier.

The dc biasing of the transformer-coupled class A amplifier is similar to that of other amplifiers, outside of the fact that the value of V_{CEQ} is designed to be as close as possible to the value of V_{CC}.

Plotting the ac load line of a transformer-coupled class A amplifier is demonstrated in Section 11.3.3 of the text. The following are typical characteristics for the transformer-coupled circuit:

- V_{CEQ} is very close to the value of V_{CC}.
- The maximum output voltage is very close to $2V_{CEQ}$ and therefore, can approach the value of $2V_{CC}$.

The maximum theoretical efficiency of a transformer-coupled class A amplifier is 50%. In practice, the transformer-coupled amplifier has a value of $\eta < 25\%$. The high theoretical value is a result of assuming that $V_{CEQ} = V_{CC}$ and ignoring transformer (and other) circuit losses. The efficiency of a transformer-coupled circuit is calculated as shown in Example 11.7 of the text.

The transformer-coupled class A amplifier has the following advantages over the RC-coupled circuit:

- Higher efficiency.
- It is relatively simple to match the amplifier and load impedance using a transformer.
- A transformer-coupled circuit can easily be converted to a tuned amplifier; that is, a circuit that provides a specific value of gain over a specified range of operating frequencies.

4.6.2 Class B Amplifiers

The class B amplifier is a two-transistor circuit that is designed to improve on the efficiency characteristics of class A amplifiers. A class B amplifier is shown in Figure 11.3. The Q-point values for the circuit in Figure 11.3 are found using

$$V_{ceQ} = \frac{V_{cc}}{2} \quad \text{and} \quad I_{cQ} = I_{CO} \cong 0 \text{ A}$$

where I_{CO} is the collector cutoff current rating for the transistor.

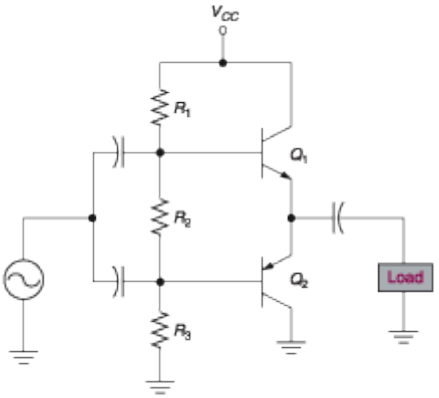


FIGURE 11.3 Class B amplifier.

The circuit shown in Figure 11.3 is a complementary-symmetry amplifier, or a push-pull emitter follower. The circuit contains one npn transistor (Q_1) and one pnp transistor (Q_2). The circuit contains complementary transistors; that is, npn and pnp transistors with identical characteristics

4.6.3 Class C Amplifiers

Class C amplifiers were briefly mentioned in Chapter 11. The transistor in a class C amplifier conducts for less than 180° of the input cycle. A basic class C amplifier is illustrated in Figure 17.14.

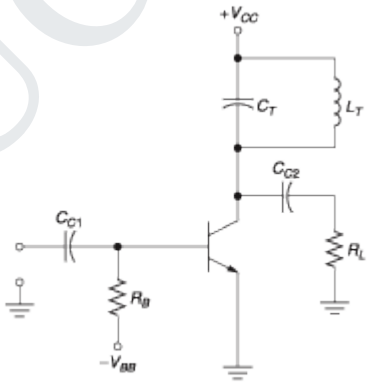


FIGURE 17.14 Class C amplifier.

The most important aspect of the dc operation of this amplifier is that it is biased deeply into cutoff, meaning that $V_{CEQ} \cong V_{CC}$ and $I_{CQ} \cong 0$ A. If a negative supply is used to bias the base circuit, the value of V_{BB} usually fulfills the following relationship:

$$-V_{BB} = 1\text{ V} - V_{in(pk)}$$

The ac operation of the class C amplifier is based on the characteristics of the parallel-resonant tank circuit. If a single current pulse is applied to the tank circuit, the result is a decaying sinusoidal waveform (as shown in Figure 17.43b of the text). The waveform

shown is a result of the charge/discharge cycle of the capacitor and inductor in the tank circuit, and is commonly referred to as the flywheel effect.

To produce a sine wave that does not decay, we must repeatedly apply a current pulse during each full cycle. At the peak of each positive alternation of the input signal, the tank circuit in a class C amplifier gets the current pulse it needs to produce a complete sine wave at the output. This concept is illustrated in Figure 17.44 of the text. Note that T_1, T_2, and T_3 are inverted at the output relative to the input. This is due to the fact that a common-emitter amplifier produces a 180° voltage phase shift. Note that the bandwidth, Q, and Q_L characteristics of a class C amplifier are the same as those for any tuned discrete amplifier.

One final point about the class C amplifier. In order for this amplifier to work properly, the tank circuit must be tuned to the same frequency as the input signal, or to some harmonic of that frequency. For instance, you could tune the class C amplifier to the third harmonic of the input and have an output that is three times the input frequency. As such, the class C amplifier can be used as a frequency multiplier.

Review questions:

1. How to eliminate the cross over distortion.
2. Explain the heat sink design.
3. Explain neutralization techniques
4. Explain working about differential amplifier and derive expression for CMRR
5. Explain transfer characteristics of differential amplifier and derive expression for the same.
6. Explain about single tuned amplifiers
7. Compare the characteristics power amplifiers.
8. Make complete analysis of single tuned amplifier &derive the necessary expressions.
9. Neutrodyne neutralization techniques
10. Hazeltine neutralization techniques
11. Draw a neat circuit diagram and explain working of cascade amplifier and derive the expression for gain and frequency.
12. Describe the input stages of FET amplifiers.

UNIT 5

UNIT – I

FEED BACK AMPLIFIERS AND OSCILLATORS

INTRODUCTION

A practical amplifier has a gain of nearly one million i.e. its output is one million times the input. Consequently, even a casual disturbance at the input will appear in the amplified form in the output. There is a strong tendency in amplifiers to introduce hum due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output. The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible. The noise level in amplifiers can be reduced considerably by the use of negative feedback i.e. by injecting a fraction of output in phase opposition to the input signal. The object of this chapter is to consider the effects and methods of providing negative feedback in transistor amplifiers.

5.1 Feedback

The process of injecting a fraction of output energy of some device back to the input is known as **feedback**. The principle of feedback is probably as old as the invention of first machine but it is only some 50 years ago that feedback has come into use in connection with electronic circuits. It has been found very useful in reducing noise in amplifiers and making amplifier operation stable. Depending upon whether the feedback energy aids or opposes the input signal, there are two basic types of feedback in amplifiers viz positive feedback and negative feedback.

(i) Positive feedback. When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called positive feedback. This is illustrated in Fig. 1.1. Both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop, causing the feedback voltage Vf to be in phase with the input signal Vin.

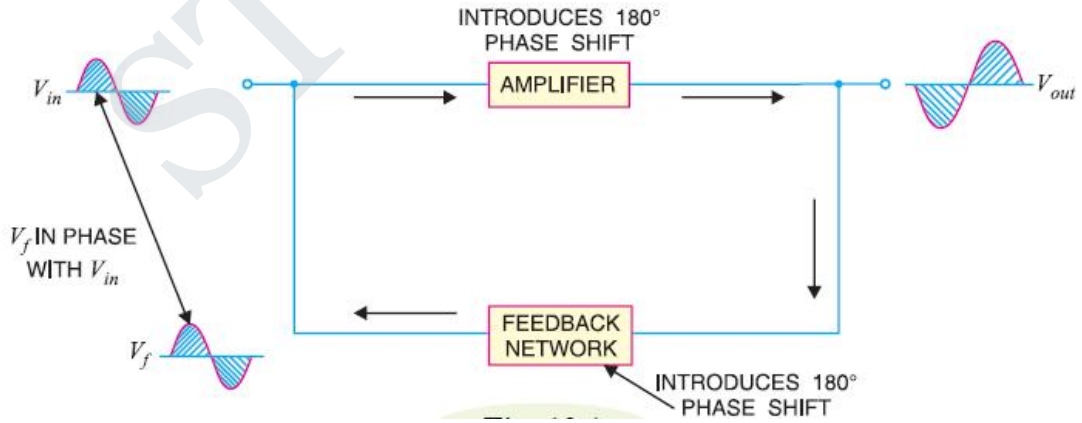


Figure 1.1

The positive feedback increases the gain of the amplifier. However, it has the disadvantages of increased distortion and instability. Therefore, positive feedback is seldom employed in amplifiers. One important use of positive feedback is in oscillators. As we shall see in the next chapter, if positive feedback is sufficiently

large, it leads to oscillations. As a matter of fact, an oscillator is a device that converts d.c. power into a.c. power of any desired frequency.

(ii) Negative feedback. When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called negative feedback. This is illustrated in Fig. 1.2. As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (i.e., 0° phase shift). The result is that the feedback voltage Vf is 180° out of phase with the input signal Vin.

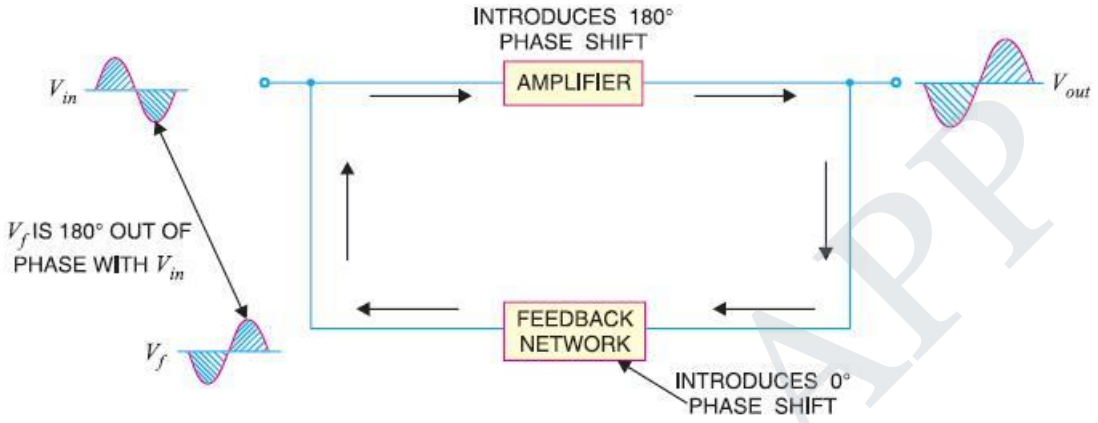


Figure 1.2

Negative feedback reduces the gain of the amplifier. However, the advantages of negative feedback are: reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances. It is due to these advantages that negative feedback is frequently employed in amplifiers.

5.2 Principles of Negative Voltage Feedback In Amplifiers

A feedback amplifier has two parts viz an amplifier and a feedback circuit. The feedback circuit usually consists of resistors and returns a fraction of output energy back to the input. Fig. 1.3 *shows the principles of negative voltage feedback in an amplifier. Typical values have been assumed to make the treatment more illustrative. The output of the amplifier is 10 V. The fraction mv of this output i.e. 100 mV is fedback to the input where it is applied in series with the input signal of 101 mV. As the feedback is negative, therefore, only 1 mV appears at the input terminals of the amplifier. Referring to Fig. 1.3, we have, Gain of amplifier without feedback,

$$A_v = \frac{10\ \text{V}}{1\ \text{mV}} = 10,000$$

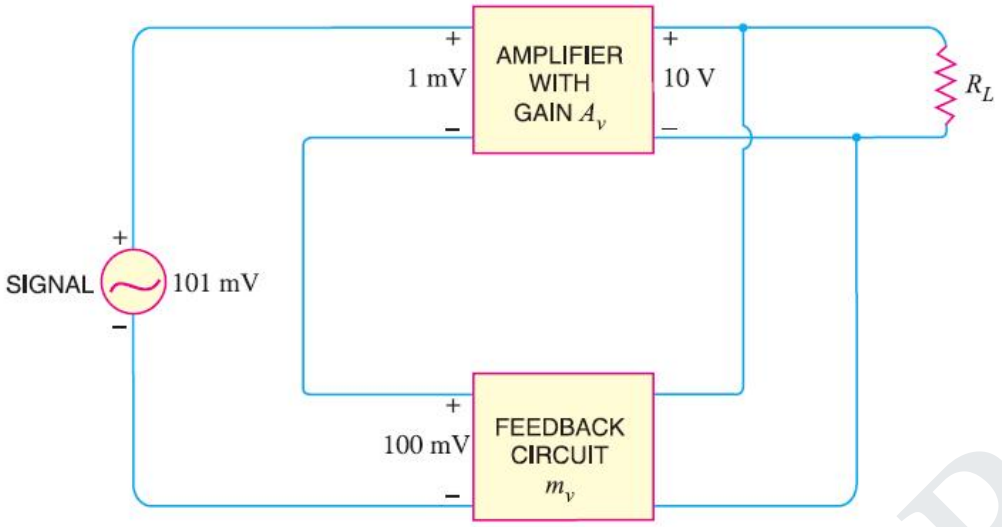


Figure 1.3

$$\text{Fraction of output voltage fedback, } m_v = \frac{100 \text{ mV}}{10 \text{ V}} = 0.01$$

$$\text{Gain of amplifier with negative feedback, } A_{vf} = \frac{10 \text{ V}}{101 \text{ mV}} = 100$$

The following points are worth noting :

✓ When negative voltage feedback is applied, the gain of the amplifier is reduced. Thus, the gain of above amplifier without feedback is 10,000 whereas with negative feedback, it is only 100.

✓ When negative voltage feedback is employed, the voltage actually applied to the amplifier is extremely small. In this case, the signal voltage is 101 mV and the negative feedback is 100 mV so that voltage applied at the input of the amplifier is only 1 mV.

✓ In a negative voltage feedback circuit, the feedback fraction mv is always between 0 and 1.

✓ The gain with feedback is sometimes called closed-loop gain while the gain without feedback is called open-loop gain. These terms come from the fact that amplifier and feedback circuits form a "loop". When the loop is "opened" by disconnecting the feedback circuit from the input, the amplifier's gain is Av, the "open-loop" gain. When the loop is "closed" by connecting the feedback circuit, the gain decreases to Avf , the "closed-loop" gain.

5.3 Gain of Negative Voltage Feedback Amplifier

Consider the negative voltage feedback amplifier shown in Fig. 1.4. The gain of the amplifier without feedback is Av. Negative feedback is then applied by feeding a fraction mv of the output voltage e0 back to amplifier input. Therefore, the actual input to the amplifier is the signal voltage eg minus feedback voltage mv e0 i.e.,

Actual input to amplifier = eg − mv e0

The output e0 must be equal to the input voltage eg − mv e0 multiplied by gain Av of

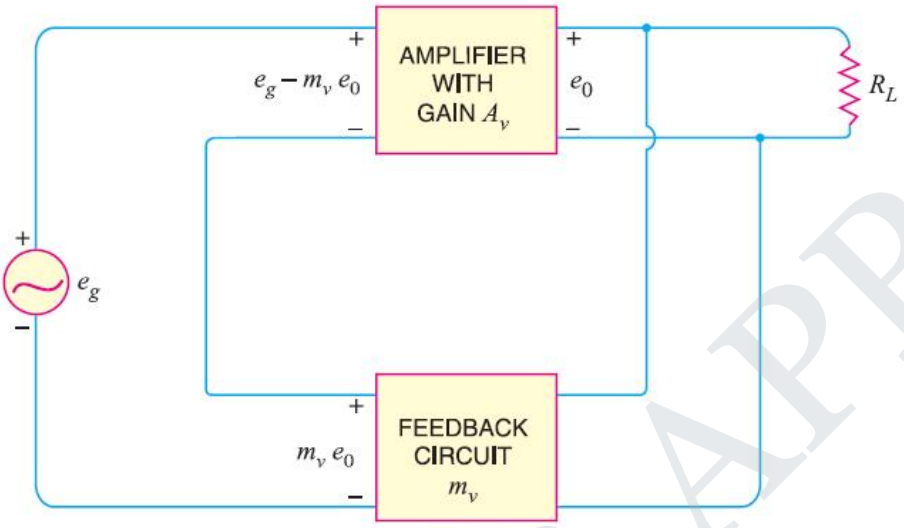
$$(e_g - m_v e_0) A_v = e_0$$

or $$A_v e_g - A_v m_v e_0 = e_0$$

or $$e_0 (1 + A_v m_v) = A_v e_g$$

or $$\frac{e_0}{e_g} = \frac{A_v}{1 + A_v m_v}$$

the amplifier i.e.,



But e0/eg is the voltage gain of the amplifier with feedback. Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

It may be seen that the gain of the amplifier without feedback is Av. However, when negative voltage feedback is applied, the gain is reduced by a factor 1 + Av mv. It may be noted that negative voltage feedback does not affect the current gain of the circuit.

5.4 Advantages of Negative Voltage Feedback

The following are the advantages of negative voltage feedback in amplifiers :

(i) Gain stability. An important advantage of negative voltage feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage variations.

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product Av mv much greater than unity. Therefore, in the above relation, 1 can be neglected as compared to Av mv and the expression becomes :

$$A_{vf} = \frac{A_v}{A_v m_v} = \frac{1}{m_v}$$

It may be seen that the gain now depends only upon feedback fraction mv i.e., on the characteristics of feedback circuit. As feedback circuit is usually a voltage divider (a resistive network), therefore, it is unaffected by changes in temperature, variations in transistor parameters and frequency. Hence, the gain of the amplifier is extremely stable.

(ii) Reduces non-linear distortion. A large signal stage has non-linear distortion because its voltage gain changes at various points in the cycle. The negative voltage feedback reduces the nonlinear distortion in large signal amplifiers. It can be proved mathematically that :

$$D_{vf} = \frac{D}{1 + A_v\, m_v}$$

where D = distortion in amplifier without feedback

D_{vf} = distortion in amplifier with negative feedback

It is clear that by applying negative voltage feedback to an amplifier, distortion is reduced by a factor 1 + Av mv.

(iii) Improves frequency response. As feedback is usually obtained through a resistive network, therefore, voltage gain of the amplifier is *independent of signal frequency. The result is that voltage gain of the amplifier will be substantially constant over a wide range of signal frequency. The negative voltage feedback, therefore, improves the frequency response of the amplifier.

(iv) Increases circuit stability. The output of an ordinary amplifier is easily changed due to variations in ambient temperature, frequency and signal amplitude. This changes the gain of the amplifier, resulting in distortion. However, by applying negative voltage feedback, voltage gain of the amplifier is stabilised or accurately fixed in value.

This can be easily explained. Suppose the output of a negative voltage feedback amplifier has increased because of temperature change or due to some other reason. This means more negative feedback since feedback is being given from the output. This tends to oppose the increase in amplification and maintains it stable. The same is true should the output voltage decrease. Consequently, the circuit stability is considerably increased.

(v) Increases input impedance and decreases output impedance. The negative voltage feedback increases the input impedance and decreases the output impedance of amplifier. Such a change is profitable in practice as the amplifier can then serve the purpose of impedance matching.

(a) Input impedance. The increase in input impedance with negative voltage feedback can be explained by referring to Fig. 13.5. Suppose the input impedance of the amplifier is Zin without feedback and Z ′in with negative feedback. Let us further assume that input current is i1. Referring to Fig. 13.5, we have,

$$e_g - m_v e_0 = i_1 Z_{in}$$

Now
$$e_g = (e_g - m_v e_0) + m_v e_0$$
$$= (e_g - m_v e_0) + A_v m_v (e_g - m_v e_0) \qquad [\because e_0 = A_v (e_g - m_v e_0)]$$
$$= (e_g - m_v e_0)(1 + A_v m_v)$$
$$= i_1 Z_{in} (1 + A_v m_v) \qquad [\because e_g - m_v e_0 = i_1 Z_{in}]$$

or
$$\frac{e_g}{i_1} = Z_{in} (1 + A_v m_v)$$

But eg/i1 = Z ′i n , the input impedance of the amplifier with negative voltage feedback.

$$Z'_{in} = Z_{in} (1 + A_v m_v)$$

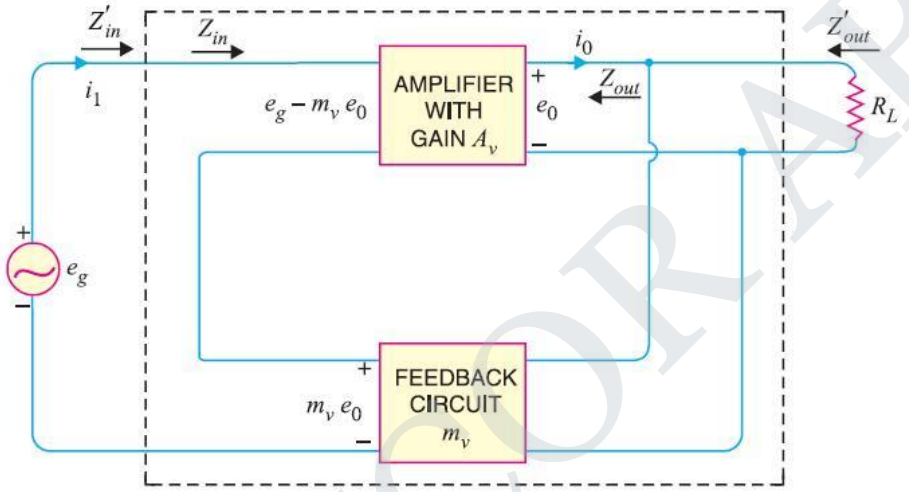


Figure 1.5

It is clear that by applying negative voltage feedback, the input impedance of the amplifier is increased by a factor 1 + Av mv. As Av mv is much greater than unity, therefore, input impedance is increased considerably. This is an advantage, since the amplifier will now present less of a load to its source circuit.

(b) Output impedance. Following similar line, we can show that output impedance with negative voltage feedback is given by :

$$Z'_{out} = \frac{Z_{out}}{1 + A_v m_v}$$

where
Z'_{out} = output impedance with negative voltage feedback
Z_{out} = output impedance without feedback

It is clear that by applying negative feedback, the output impedance of the amplifier is decreased by a factor 1 + Av mv. This is an added benefit of using negative voltage feedback. With lower value of output impedance, the amplifier is much better suited to drive low impedance loads.

Feedback Circuit

The function of the feedback circuit is to return a fraction of the output voltage to the input of the amplifier. Fig. 13.6 shows the feedback circuit of negative voltage feedback amplifier. It is essentially a potential divider consisting of resistances R1 and R2. The output voltage of the amplifier is fed to this potential divider which gives the feedback voltage to the input. Referring to Fig. 13.6, it is clear that :

$$\text{Voltage across } R_1 = \left(\frac{R_1}{R_1 + R_2}\right) e_0$$

$$\text{Feedback fraction, } m_v = \frac{\text{Voltage across } R_1}{e_0} = \frac{R_1}{R_1 + R_2}$$

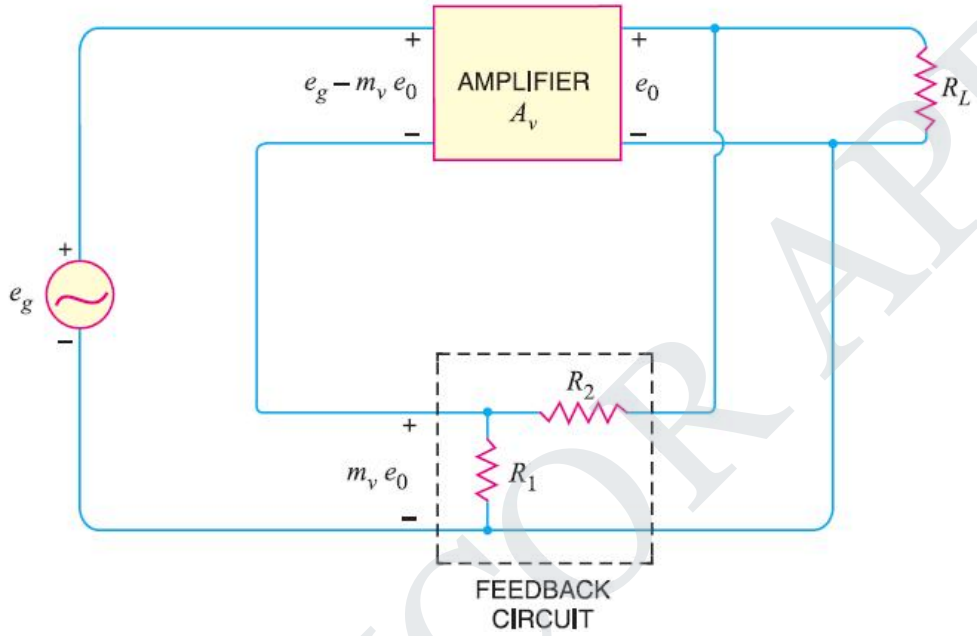


Figure 1.6

Principles of Negative Current Feedback

In this method, a fraction of output current is fedback to the input of the amplifier. In other words, the feedback current (If) is proportional to the output current (Iout) of the amplifier. Fig. 1.7 shows the principles of negative current feedback. This circuit is called current-shunt feedback circuit. A feedback resistor Rf is connected between input and output of the amplifier. This amplifier has a current gain of Ai without feedback. It means that a current I1 at the input terminals of the amplifier will appear as Ai I1 in the output circuit i.e., Iout = Ai I1.

Now a fraction mi of this output current is fedback to the input through Rf. The fact that arrowhead shows the feed current being fed forward is because it is negative feedback.

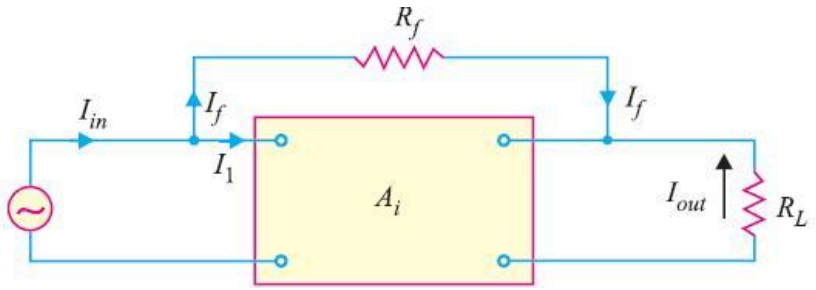


Figure 1.7

Feedback current, If = mi Iout

Note that negative current feedback reduces the input current to the amplifier and hence its current gain.

Current Gain with Negative Current Feedback

Referring to Fig. 13.6, we have, Iin = I1 + If = I1 + mi Iout

But Iout = Ai I1, where Ai is the current gain of the amplifier without feedback. Iin = I1

+ mi Ai I1 (ä Iout = Ai I1)

Current gain with negative current feedback is

$$A_{if} = \frac{I_{out}}{I_{in}} = \frac{A_i I_1}{I_1 + m_i A_i I_1}$$

$$\text{or } A_{if} = \frac{A_i}{1 + m_i A_i}$$

This equation looks very much like that for the voltage gain of negative voltage feedback amplifier. The only difference is that we are dealing with current gain rather than the voltage gain.

The following points may be noted carefully :

(i) The current gain of the amplifier without feedback is Ai. However, when negative current feedback is applied, the current gain is reduced by a factor (1 + mi Ai).

(ii) The feedback fraction (or current attenuation) mi has a value between 0 and 1.

(iii) The negative current feedback does not affect the voltage gain of the amplifier.

5.5 Effects of Negative Current Feedback

The negative current feedback has the following effects on the performance of amplifiers :

(i) Decreases the input impedance. The negative current feedback decreases the

input impedance of most amplifiers.

Let

Zin = Input impedance of the amplifier without feedback

Z ′in = Input impedance of the amplifier with negative current feedback

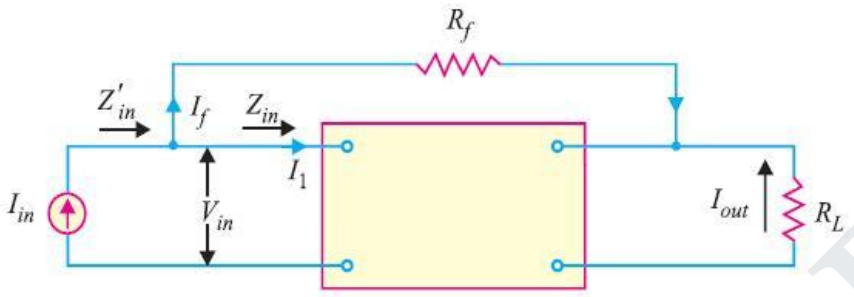


Figure 1.8

Referring to Fig. 1.8, we have,

$$Z_{in} = \frac{V_{in}}{I_1}$$

and

$$Z'_{in} = \frac{V_{in}}{I_{in}}$$

But $V_{in} = I_1 Z_{in}$ and $I_{in} = I_1 + I_f = I_1 + m_i I_{out} = I_1 + m_i A_i I_1$

$$\therefore \quad Z'_{in} = \frac{I_1 Z_{in}}{I_1 + m_i A_i I_1} = \frac{Z_{in}}{1 + m_i A_i}$$

or

$$Z'_{in} = \frac{Z_{in}}{1 + m_i A_i}$$

Thus the input impedance of the amplifier is decreased by the factor (1 + mi Ai). Note the primary difference between negative current feedback and negative voltage feedback. Negative current feedback decreases the input impedance of the amplifier while negative voltage feedback increases the input impedance of the amplifier.

Increases the output impedance. It can be proved that with negative current feedback, the output impedance of the amplifier is increased by a factor (1 + mi Ai).

$$Z'out = Zout (1 + mi Ai)$$

where

Zout = output impedance of the amplifier without feedback

Z ′out = output impedance of the amplifier with negative current feedback

The reader may recall that with negative voltage feedback, the output impedance of the amplifier is decreased.

Increases bandwidth. It can be shown that with negative current feedback, the bandwidth of the amplifier is increased by the factor (1 + mi Ai).

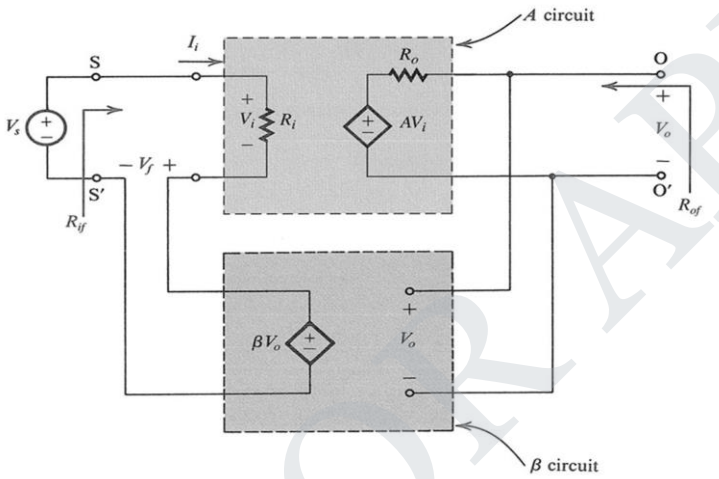
$$BW' = BW\ (1 + mi\ Ai)$$

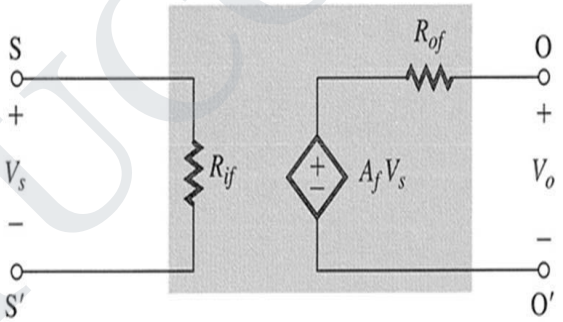
where

BW = Bandwidth of the amplifier without feedback

BW′ = Bandwidth of the amplifier with negative current feedback

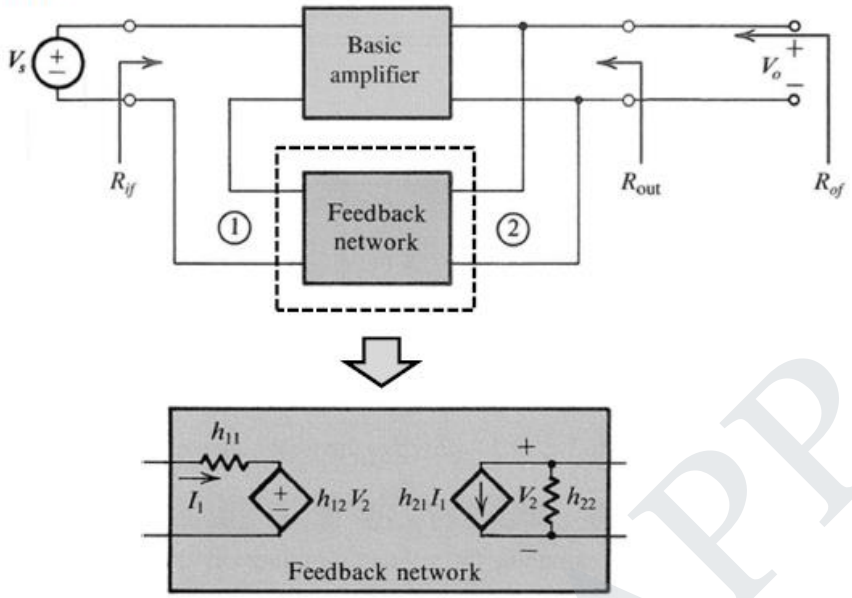
5.6 The Feedback Voltage Amplifier (Series-Shunt)





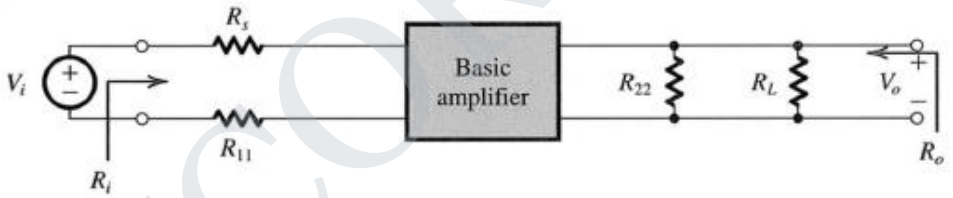
- Input resistance of the feedback amplifier $R_{if} = (1 + A\beta)R_i$
- Output resistance of the feedback amplifier $R_{of} = \dfrac{R_o}{1 + A\beta}$
- Voltage gain of the feedback amplifier $A_f = \dfrac{A}{1 + A\beta}$

The practical case

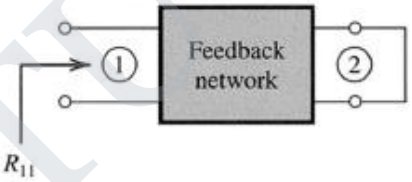


Analysis techniques

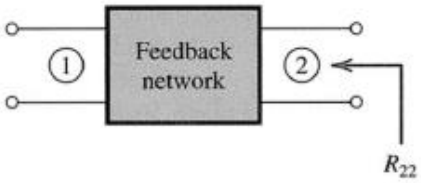
(a) The A circuit is



where R_{11} is obtained from

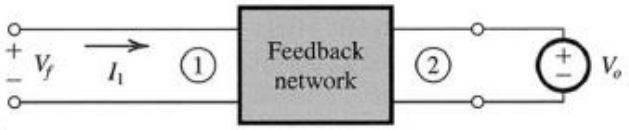


and R_{22} is obtained from



and the gain A is defined $A \equiv \frac{V_o}{V_i}$

(b) β is obtained from



$$\beta \equiv \frac{V_f}{V_o}\bigg|_{I_1 = 0}$$

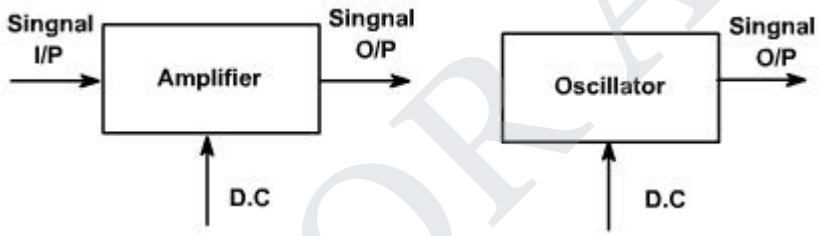
5.7 Oscillators:

An oscillator may be described as a source of alternating voltage. It is different than amplifier.

An amplifier delivers an output signal whose waveform corresponds to the input signal but whose power level is higher. The additional power content in the output signal is supplied by the DC power source used to bias the active device.

The amplifier can therefore be described as an energy converter, it accepts energy from the DC power supply and converts it to energy at the signal frequency. The process of energy conversion is controlled by the input signal, Thus if there is no input signal, no energy conversion takes place and there is no output signal.

The oscillator, on the other hand, requires no external signal to initiate or maintain the energy conversion process. Instead an output signals is produced as long as source of DC power is connected. **Fig. 1**, shows the block diagram of an amplifier and an oscillator.



Oscillators may be classified in terms of their output waveform, frequency range components, or circuit configuration.

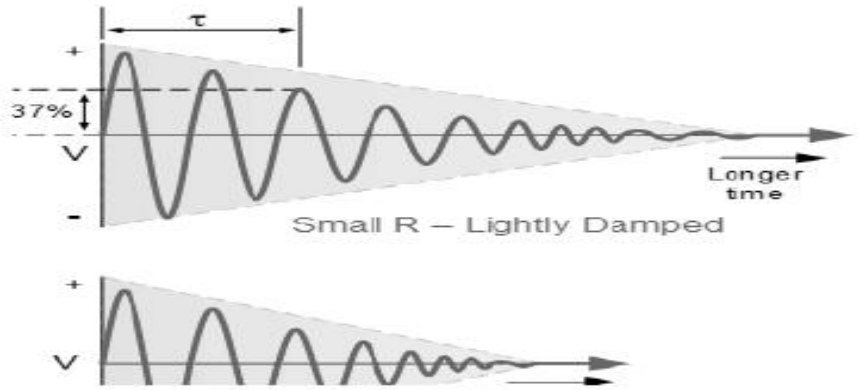
If the output waveform is sinusoidal, it is called harmonic oscillator otherwise it is called relaxation oscillator, which include square, triangular and saw tooth waveforms.

Oscillators employ both active and passive components. The active components provide energy conversion mechanism. Typical active devices are transistor, FET etc.

Passive components normally determine the frequency of oscillation. They also influence stability, which is a measure of the change in output frequency (drift) with time, temperature or other factors. Passive devices may include resistors, inductors, capacitors, transformers, and resonant crystals.

Capacitors used in oscillators circuits should be of high quality. Because of low losses and

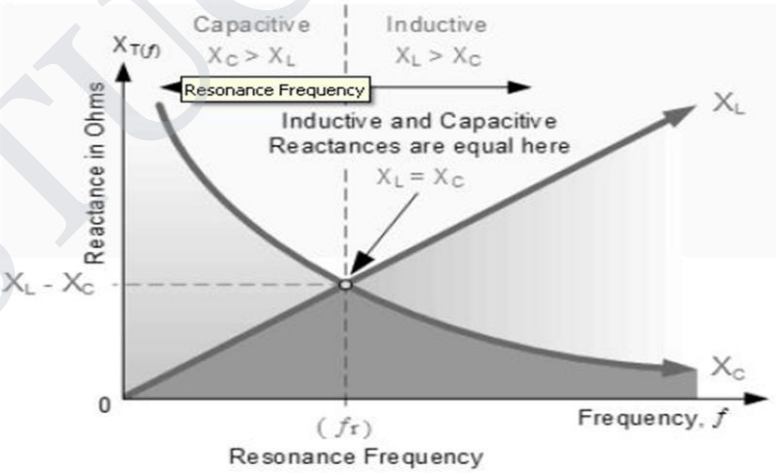
Damped Oscillations



The frequency of the oscillatory voltage depends upon the value of the inductance and capacitance in the LC tank circuit. We now know that for resonance to occur in the tank circuit, there must be a frequency point were the value of X_C, the capacitive reactance is the same as the value of X_L, the inductive reactance ($X_L = X_C$) and which will therefore cancel out each other out leaving only the DC resistance in the circuit to oppose the flow of current.

If we now place the curve for inductive reactance on top of the curve for capacitive reactance so that both curves are on the same axes, the point of intersection will give us the resonance frequency point, (fr or ωr) as shown below.

Resonance Frequency



where: f_r is in Hertz, L is in Henries and C is in Farads. Then the frequency at which this will happen is given as:

$$X_L = 2\pi f L \quad \text{and} \quad X_C = \frac{1}{2\pi f C}$$

$$\text{at resonance:} \quad X_L = X_C$$

$$\therefore \quad 2\pi f L = \frac{1}{2\pi f C}$$

$$2\pi f^2 L = \frac{1}{2\pi C}$$

$$\therefore \quad f^2 = \frac{1}{(2\pi)^2 LC}$$

$$f = \frac{\sqrt{1}}{\sqrt{(2\pi)^2 LC}}$$

Then by simplifying the above equation we get the final equation for **Resonant Frequency**, fr in a tuned LC circuit as:

Resonant Frequency of a LC Oscillator

$$f_R = \frac{1}{2\pi\sqrt{LC}}$$

Where:

L is the Inductance in Henries C is the Capacitance in Farads fr is the Output Frequency in Hertz

This equation shows that if either L or C are decreased, the frequency increases. This output frequency is commonly given the abbreviation of (fr) to identify it as the "resonant frequency". To keep the oscillations going in an LC tank circuit, we have to replace all the energy lost in each oscillation and also maintain the amplitude of these oscillations at a constant level.

The amount of energy replaced must therefore be equal to the energy lost during each cycle. If the energy replaced is too large the amplitude would increase until clipping of the supply rails occurs. Alternatively, if the amount of energy replaced is too small the amplitude would eventually decrease to zero over time and the oscillations would stop.

The simplest way of replacing this lost energy is to take part of the output from the LC tank circuit, amplify it and then feed it back into the LC circuit again. This process can be achieved using a voltage amplifier using an op-amp, FET or bipolar transistor as its active device.

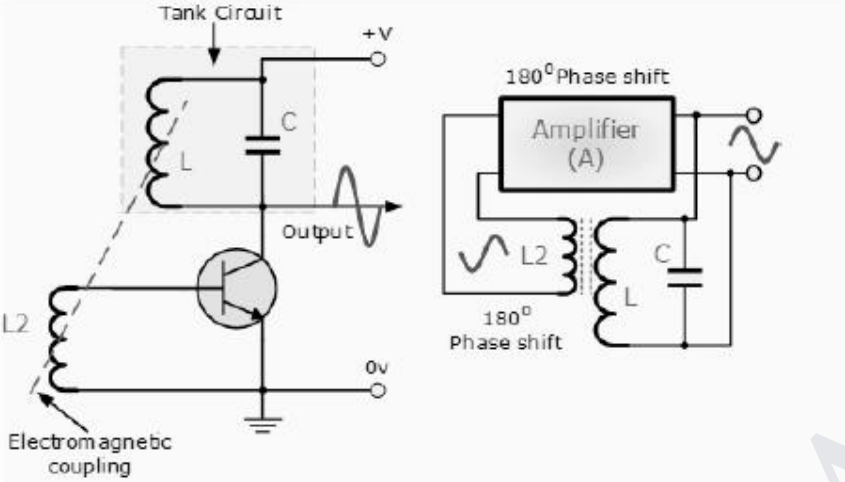
However, if the loop gain of the feedback amplifier is too small, the desired oscillation decays to zero and if it is too large, the waveform becomes distorted. To produce a constant oscillation, the level of the energy fed back to the LC network must be accurately controlled.

Then there must be some form of automatic amplitude or gain control when the amplitude tries to vary from a reference voltage either up or down. To maintain a stable oscillation the overall gain

of the circuit must be equal to one or unity. Any less and the oscillations will not start or die away to zero,

any more the oscillations will occur but the amplitude will become clipped by the supply rails causing distortion. Consider the circuit below.

Basic Transistor LC Oscillator Circuit



A Bipolar Transistor is used as the LC oscillators amplifier with the tuned LC tank circuit acts as the collector load. Another coil L2 is connected between the base and the emitter of the transistor whose electromagnetic field is "mutually" coupled with that of coil L. Mutual inductance exists between the two circuits.

The changing current flowing in one coil circuit induces, by electromagnetic induction, a potential voltage in the other (transformer effect) so as the oscillations occur in the tuned circuit, electromagnetic energy is transferred from coil L to coil L2 and a voltage of the same frequency as that in the tuned circuit is applied between the base and emitter of the transistor.

In this way the necessary automatic feedback voltage is applied to the amplifying transistor. The amount of feedback can be increased or decreased by altering the coupling between the two coils L and L2. When the circuit is oscillating its impedance is resistive and the collector and base voltages are 180 out of phase. In order to maintain oscillations (called frequency stability) the voltage applied to the tuned circuit must be "in-phase" with the oscillations occurring in the tuned circuit.

Therefore, we must introduce an additional 180^{o} phase shift into the feedback path between the collector and the base. This is achieved by winding the coil of L2 in the correct direction relative to coil L giving us the correct amplitude and phase relationships for the Oscillatorscircuit or by connecting a phase shift network between the output and input of the amplifier.

TheLC Oscillator is therefore a "Sinusoidal Oscillator" or a "Harmonic Oscillator" as it is more commonly called. LC oscillators can generate high frequency sine waves for use in radio frequency (RF) type applications with the transistor amplifier being of a Bipolar Transistor or FET.

Harmonic Oscillators come in many different forms because there are many different ways to construct an LC filter network and amplifier with the most common being the Hartley LC Oscillator, Colpitts LC Oscillator, Armstrong OscillatorandClapp Oscillator to name a few.

5.8 The Hartley Oscillator

The main disadvantages of the basic LC Oscillator circuit we looked at in the previous tutorial is that they have no means of controlling the amplitude of the oscillations and also, it is difficult to tune the oscillator to the required frequency.

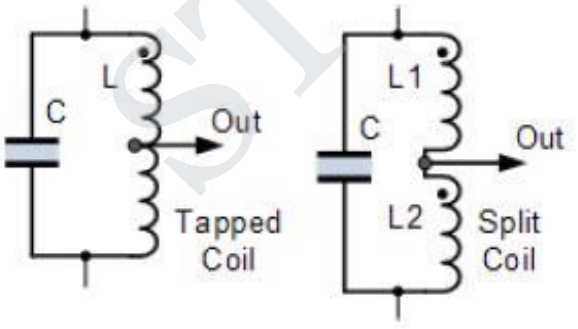
If the cumulative electromagnetic coupling between L1 and L2 is too small there would be insufficient feedback and the oscillations would eventually die away to zero Likewise if the feedback was too strong the oscillations would continue to increase in amplitude until they were limited by the circuit conditions producing signal distortion. So it becomes very difficult to "tune" the oscillator.

However, it is possible to feed back exactly the right amount of voltage for constant amplitude oscillations. If we feed back more than is necessary the amplitude of the oscillations can be controlled by biasing the amplifier in such a way that if the oscillations increase in amplitude, the bias is increased and the gain of the amplifier is reduced.

If the amplitude of the oscillations decreases the bias decreases and the gain of the amplifier increases, thus increasing the feedback. In this way the amplitude of the oscillations are kept constant using a process known as Automatic Base Bias**.**

One big advantage of automatic base bias in a voltage controlled oscillator, is that the oscillator can be made more efficient by providing a Class-B bias or even a Class-C bias condition of the transistor. This has the advantage that the collector current only flows during part of the oscillation cycle so the quiescent collector current is very small.

Then this "self-tuning" base oscillator circuit forms one of the most common types of LC parallel resonant feedback oscillator configurations called the Hartley Oscillator circuit.



Hartley Oscillator Tuned Circuit

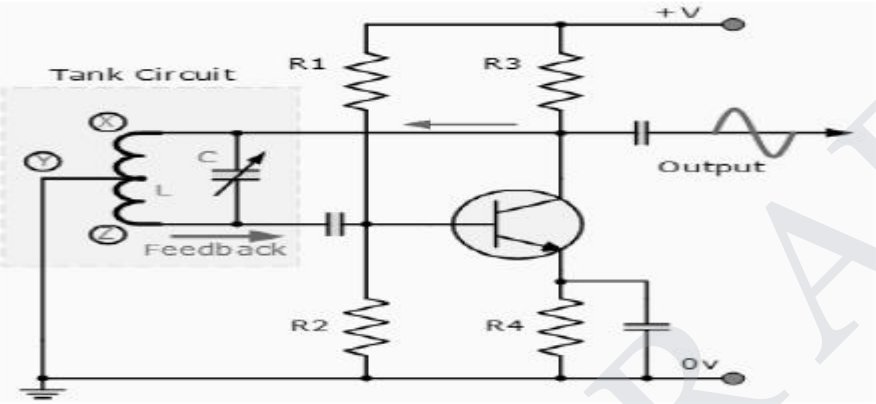
In the Hartley Oscillator the tuned LC circuit is connected between the collector and the base of the transistor amplifier. As far as the oscillatory voltage is concerned, the emitter is connected to a tapping point on the tuned circuit coil.

The feedback of the tuned tank circuit is taken from the centre tap of the inductor coil or even two separate coils in series which are in parallel with a variable capacitor, C as shown.

The Hartley circuit is often referred to as a split-inductance oscillator because coil L is centre-tapped. In effect, inductance L acts like two separate coils in very close proximity with the current flowing through coil section XY induces a signal into coil section YZ below.

An Hartley Oscillator circuit can be made from any configuration that uses either a single tapped coil (similar to an autotransformer) or a pair of series connected coils in parallel with a single capacitor as shown below.

Basic Hartley Oscillator Circuit



When the circuit is oscillating, the voltage at point X (collector), relative to point Y (emitter), is 180^{o} out-of-phase with the voltage at point Z (base) relative to point Y. At the frequency of oscillation, the impedance of the Collector load is resistive and an increase in Base voltage causes a decrease in the Collector voltage.

Then there is a 180 phase change in the voltage between the Base and Collector and this along with the original 180 phase shift in the feedback loop provides the correct phase relationship of positive feedback for oscillations to be maintained.

The amount of feedback depends upon the position of the "tapping point" of the inductor. If this is moved nearer to the collector the amount of feedback is increased, but the output taken between the Collector and earth is reduced and vice versa.

Resistors, R1 and R2 provide the usual stabilizing DC bias for the transistor in the normal manner while the capacitors act as DC-blocking capacitors.

In this Hartley Oscillator circuit, the DC Collector current flows through part of the coil and for this reason the circuit is said to be "Series-fed" with the frequency of oscillation of the Hartley Oscillator being given as.

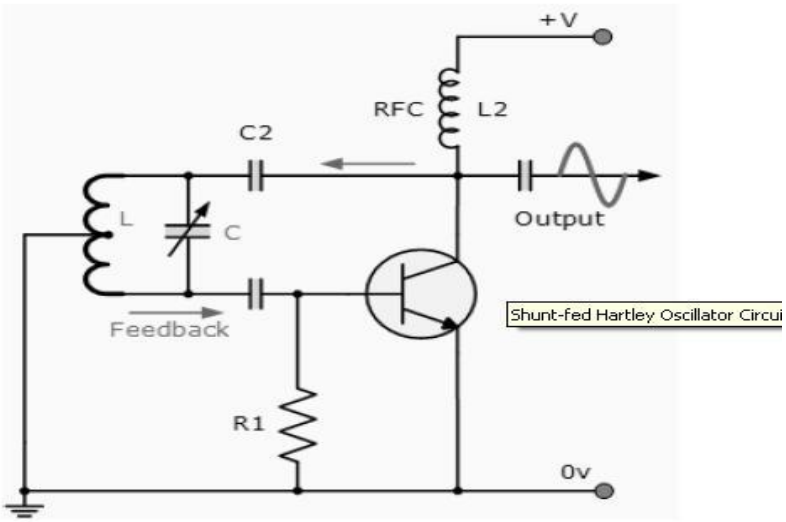
$$f = \frac{1}{2\pi\sqrt{L_T C}}$$

where: $L_T = L_1 + L_2 + 2M$

The frequency of oscillations can be adjusted by varying the "tuning" capacitor, C or by varying the position of the iron-dust core inside the coil (inductive tuning) giving an output over a wide range of frequencies making it very easy to tune. Also the Hartley Oscillator produces an output amplitude which is constant over the entire frequency range.

As well as the Series-fed Hartley Oscillator above, it is also possible to connect the tuned tank circuit across the amplifier as a shunt-fed oscillator as shown below.

Shunt-fed Hartley Oscillator Cricuit



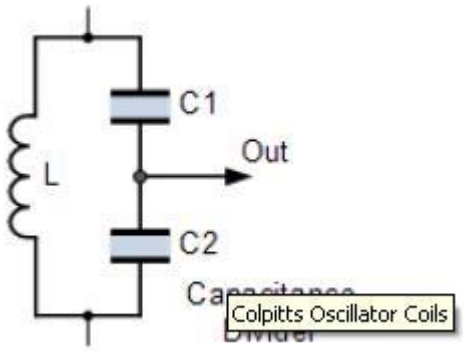
In the Shunt-fed Hartley Oscillator both the AC and DC components of the Collector current have separate paths around the circuit. Since the DC component is blocked by the capacitor, C2 no DC flows through the inductive coil, L and less power is wasted in the tuned circuit.

The Radio Frequency Coil (RFC), L2 is an RF choke which has a high reactance at the frequency of oscillations so that most of the RF current is applied to the LC tuning tank circuit via capacitor, C2 as the DC component passes through L2 to the power supply. A resistor could be used in place of the RFC coil, L2 but the efficiency would be less.

5.9 The Colpitts Oscillator

The Colpitts Oscillator, named after its inventor Edwin Colpitts is another type of LC oscillator design. In many ways, the Colpitts oscillator is the exact opposite of the Hartley Oscillator we looked at in the previous tutorial. Just like the Hartley oscillator, the tuned tank circuit consists of an LC resonance sub-circuit connected between the collector and the base of a single stage transistor amplifier producing a sinusoidal output waveform.

The basic configuration of the Colpitts Oscillator resembles that of the Hartley Oscillator but the difference this time is that the centre tapping of the tank sub-circuit is now made at the junction of a "capacitive voltage divider" network instead of a tapped autotransformer type inductor as in the Hartley oscillator.



Colpitts Oscillator Circuit

The Colpitts oscillator uses a capacitor voltage divider as its feedback source.

The two capacitors, C1 and C2 are placed across a common inductor, L as shown so that C1, C2 and L forms the tuned tank circuit the same as for the Hartley oscillator circuit.

The advantage of this type of tank circuit configuration is that with less self and mutual inductance in the tank circuit, frequency stability is improved along with a more simple design. As with the Hartley oscillator, the Colpitts oscillator uses a single stage bipolar transistor amplifier as the gain element which produces a sinusoidal output. Consider the circuit below.

Basic Colpitts Oscillator Circuit

The transistor amplifiers emitter is connected to the junction of capacitors, C1 and C2 which are connected in series and act as a simple voltage divider. When the power supply is firstly applied, capacitors C1 and C2 charge up and then discharge through the coil L. The oscillations across the capacitors are applied to the base-emitter junction and appear in the amplified at the collector output. The amount of feedback depends on the values of C1 and C2 with the smaller the values of C the greater will be the feedback.

The required external phase shift is obtained in a similar manner to that in the Hartley oscillator circuit with the required positive feedback obtained for sustained un-damped oscillations. The amount of feedback is determined by the ratio of C1 and C2 which are generally "ganged" together to provide a constant amount of feedback so as one is adjusted the other automatically follows.

The frequency of oscillations for a Colpitts oscillator is determined by the resonant frequency of the LC tank circuit and is given as:

$$f_r = \frac{1}{2\pi\sqrt{L\,C_T}}$$

where C_T is the capacitance of C1 and C2 connected in series and is given as:.

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} \quad \text{or} \quad C_T = \frac{C_1 \times C_2}{C_1 + C_2}$$

The configuration of the transistor amplifier is of a Common Emitter Amplifier with the output signal 180^o out of phase with regards to the input signal. The additional 180^o phase shift require for oscillation is achieved by the fact that the two capacitors are connected together in series but

in parallel with the inductive coil resulting in overall phase shift of the circuit being zero or ^{o} 360 .

Resistors, R1 and R2 provide the usual stabilizing DC bias for the transistor in the normal manner while the capacitor acts as a DC-blocking capacitors. The radio-frequency choke (RFC) is used to provide a high reactance (ideally open circuit) at the frequency of oscillation, (fr) and a low resistance at DC.

Colpitts Oscillator using an Op-amp

As well as using a bipolar junction transistor (BJT) as the amplifiers active stage of the Colpitts oscillator, we can also use either a field effect transistor, (FET) or an operational amplifier, (op- amp). The operation of an **Op-amp Colpitts Oscillator** is exactly the same as for the transistorised version with the frequency of operation calculated in the same manner. Consider the circuit below.

Colpitts Oscillator Op-amp Circuit

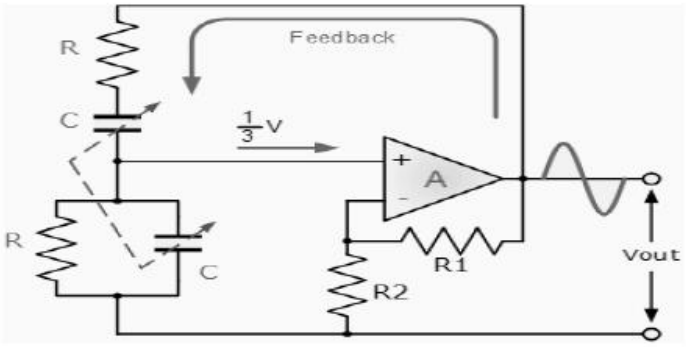
The advantages of the Colpitts Oscillatorover the Hartley oscillators are that the Colpitts oscillator produces a more purer sinusoidal waveform due to the low impedance paths of the capacitors at high frequencies. Also due to these capacitive reactance properties the Colpitts oscillator can operate at very high frequencies into the microwave region.

5.10 WIEN BRIDGE OSCILLATOR

One of the simplest sine wave oscillators which uses a RC network in place of the conventional LC tuned tank circuit to produce a sinusoidal output waveform, is the Wien Bridge Oscillator.

The Wien Bridge Oscillator is so called because the circuit is based on a frequency-selective form of the Whetstone bridge circuit. The Wien Bridge oscillator is a two-stage RC coupled amplifier circuit that has good stability at its resonant frequency, low distortion and is very easy to tune making it a popular circuit as an audio frequency oscillator

Wien Bridge Oscillator



The output of the operational amplifier is fed back to both the inputs of the amplifier. One part of the feedback signal is connected to the inverting input terminal (negative feedback) via the resistor divider network of R1 and R2 which allows the amplifiers voltage gain to be adjusted within narrow limits.

The other part is fed back to the non-inverting input terminal (positive feedback) via the RC Wien Bridge network. The RC network is connected in the positive feedback path of the amplifier and has zero phase shift a just one frequency. Then at the selected resonant frequency, (fr) the voltages applied to the inverting and non-inverting inputs will be equal and "in-phase" so the positive feedback will cancel out the negative feedback signal causing the circuit to oscillate.

Also the voltage gain of the amplifier circuit MUST be equal to three "Gain =3" for oscillations to start. This value is set by the feedback resistor network, R1 and R2 for an inverting amplifier and is given as the ratio -R1/R2.

Also, due to the open-loop gain limitations of operational amplifiers, frequencies above
1MHz are unachievable without the use of special high frequency op-amps. Then for oscillations to occur in a Wien Bridge Oscillator circuit the following conditions must apply.

1. With no input signal the Wien Bridge Oscillator produces output oscillations.

2. The Wien Bridge Oscillator can produce a large range of frequencies.

3. The Voltage gain of the amplifier must be at least 3.

4. The network can be used with a Non-inverting amplifier.

5. The input resistance of the amplifier must be high compared to R so that the RC network is not overloaded and alter the required conditions.

6. The output resistance of the amplifier must be low so that the effect of external loading

is minimised.

7. Some method of stabilizing the amplitude of the oscillations must be provided because if the voltage gain of the amplifier is too small the desired oscillation will decay and stop and if it is too large the output amplitude rises to the value of the supply rails, which saturates the op-amp and causes the output waveform to become distorted.

8**.** With amplitude stabilisation in the form of feedback diodes, oscillations from the oscillator can go on indefinitely.

5.11 Quartz Crystal Oscillators

One of the most important features of any oscillator is its frequency stability, or in other words its ability to provide a constant frequency output under varying load conditions. Some of the factors that affect the frequency stability of an oscillator include: temperature, variations in the load and changes in the DC power supply.

Frequency stability of the output signal can be improved by the proper selection of the components used for the resonant feedback circuit including the amplifier but there is a limit to the stability that can be obtained from normal LC and RC tank circuits.

To obtain a very high level of oscillator stability a Quartz Crystalis generally used as the frequency

Crystal Oscillator

When a voltage source is applied to a small thin piece of quartz crystal, it begins to change shape producing a characteristic known as the Piezo-electric effect.

This piezo-electric effect is the property of a crystal by which an electrical charge produces a mechanical force by changing the shape of the crystal and vice versa, a mechanical force applied to the crystal produces an electrical charge.

Then, piezo-electric devices can be classed as Transducersas they convert energy of one kind into energy of another (electrical to mechanical or mechanical to electrical).

This piezo-electric effect produces mechanical vibrations or oscillations which are used to replace the

LC tank circuit in the previous oscillators.

There are many different types of crystal substances which can be used as oscillators with the most important of these for electronic circuits being the quartz minerals because of their greater mechanical strength.

The quartz crystal used in a Quartz Crystal Oscillator is a very small, thin piece or wafer of cut quartz with the two parallel surfaces metallised to make the required electrical connections. The physical size and thickness of a piece of quartz crystal is tightly controlled since it affects the final frequency of oscillations and is called the crystals "characteristic frequency". Then once cut and shaped, the crystal can not be used at any other frequency. In other words, its size and shape determines its frequency.

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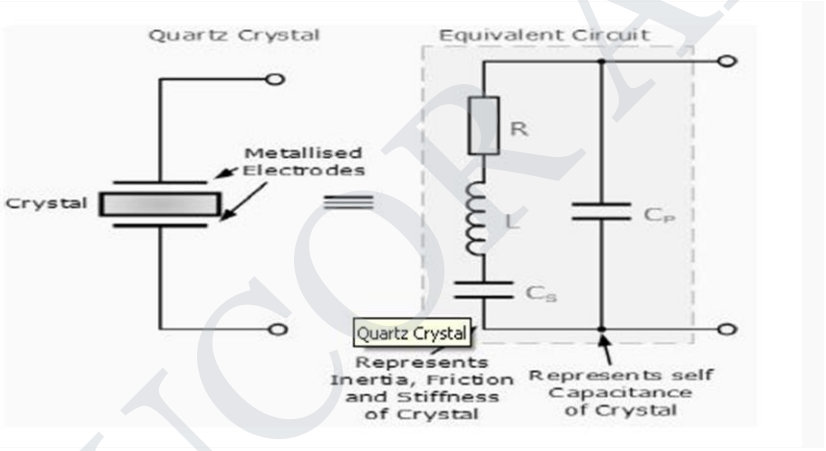
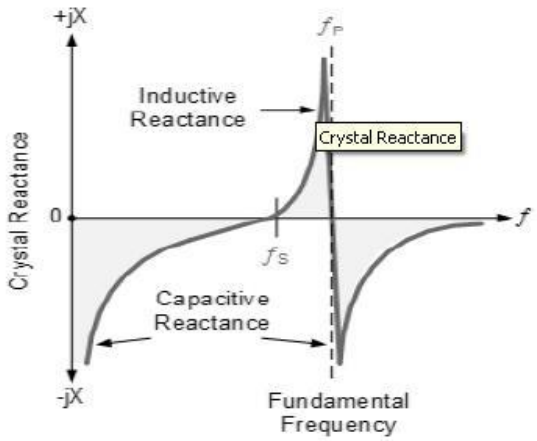
Quartz Crystal



The equivalent circuit for the quartz crystal shows an RLC series circuit, which represents the mechanical vibrations of the crystal, in parallel with a capacitance, Cp which represents the electrical connections to the crystal. Quartz crystal oscillators operate at "parallel resonance", and the equivalent impedance of the crystal has a series resonance where Cs resonates with inductance, L and a parallel resonance where L resonates with the series combination of Cs and Cp as shown.

Crystal Reactance

The slope of the reactance against frequency above, shows that the series reactance at frequency fs is inversely proportional to Cs because below fs and above fp the crystal appears capacitive, i.e. dX/df, where X is the reactance.



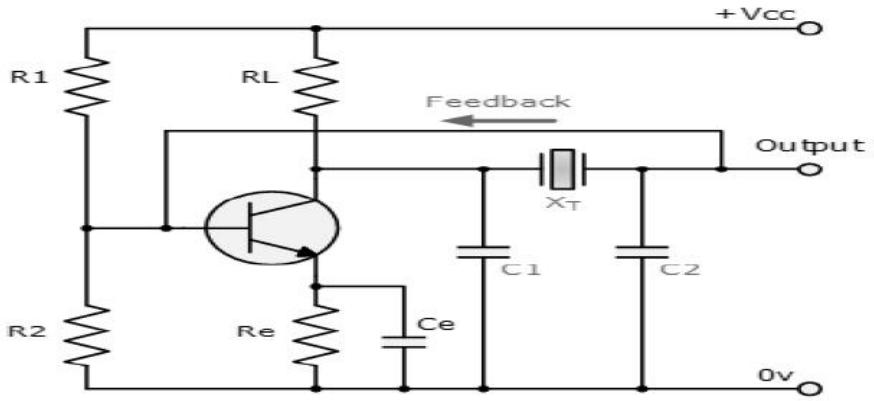
The slope of the reactance against frequency above, shows that the series reactance at frequency fs is inversely proportional to Cs because below fs and above fp the crystal appears capacitive, i.e. dX/d f, where X is the reactance. Between frequencies fs and fp, the crystal appears inductive as the two parallel capacitances cancel out. The point where the reactance values of the capacitances and inductance cancel each other out Xc = XL is the fundamental frequency of the crystal.

A quartz crystal has a resonant frequency similar to that of a electrically tuned tank circuit butwith a much higher Q factor due to its low resistance, with typical frequencies ranging from 4kHz to
10MHz. The cut of the crystal also determines how it will behave as some crystals will vibrate at more than one frequency. Also, if the crystal is not of a parallel or uniform thickness it has two or more resonant frequencies having both a fundamental frequency and harmonics such as second or third harmonics. However, usually the fundamental frequency is more stronger or pronounced than the others and this is the one used. The equivalent circuit above has three reactive components and there are two resonant frequencies, the lowest is a series type frequency and the highest a parallel type resonant frequency.

We have seen in the previous tutorials, that an amplifier circuit will oscillate if it has a loop gain greater or equal to one and the feedback is positive. In a Quartz Crystal Oscillator circuit the oscillator will oscillate at the crystals fundamental parallel resonant frequency as the crystal always wants to oscillate when a voltage source is applied to it.

Colpitts Crystal Oscillator:

The design of a Crystal Oscillator is very similar to the design of the Colpitts Oscillator we looked at in the previous tutorial, except that the LC tank circuit has been replaced by a quartz crystal as shown below.



These types of Crystal Oscillators are designed around the common emitter amplifier stage of a Colpitts Oscillator**.** The input signal to the base of the transistor is inverted at the transistors output.

The output signal at the collector is then taken through a 180^{o} phase shifting network which includes the crystal operating in a series resonant mode. The output is also fed back to the input which is "in-phase"

with the input providing the necessary positive feedback. Resistors, R1 and R2 bias the resistor in aClass
A type operation while resistor

Re is chosen so that the loop gain is slightly greater than unity.

Capacitors, C1 and C2 are made as large as possible in order that the frequency of oscillations can approximate to the series resonant mode of the crystal and is not dependant upon the values of these capacitors.

The circuit diagram above of the Colpitts Crystal Oscillator circuit shows that capacitors, C1 and C2 shunt the output of the transistor which reduces the feedback signal.

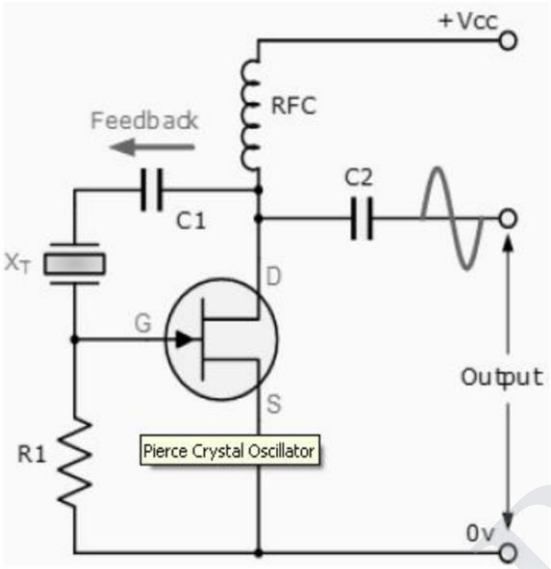
Therefore, the gain of the transistor limits the maximum values of C1 and C2.

The output amplitude should be kept low in order to avoid excessive power dissipation in the crystal otherwise could destroy itself by excessive vibration.

Pierce Oscillator

The Pierce oscillator is a crystal oscillator that uses the crystal as part of its feedback path and therefore has no resonant tank circuit. The Pierce Oscillator uses a JFET as its amplifying device as it provides a very high input impedance with the crystal connected between the output Drain terminal and the input Gate terminal as shown below.

Pierce Crystal Oscillator



In this simple circuit, the crystal determines the frequency of oscillations and operates on its series resonant frequency giving a low impedance path between output and input.

There is a 180° phase shift at resonance, making the feedback positive. The amplitude of the output sine wave is limited to the maximum voltage range at the Drain terminal.

Resistor, R1 controls the amount of feedback and crystal drive while the voltage across the radio frequency choke, RFC reverses during each cycle. Most digital clocks, watches and timers use a Pierce Oscillator in some form or other as it can be implemented using the minimum of components.

Review questions:

1. Explain voltage series and shunt feedback amplifier with an example. (16)
2. Describe the characteristics of Negative feedback. (8)
3. Describe the characteristics Positive feedback. (8)
4. Explain the current series and shunt feedback amplifier with an example. (16)
5. Explain the principle of operation and derive the expression for wein bridge oscillator.(16)
6. Explain the principle of operation and derive the expression for colpitts oscillator.(16)
7. Derive the expression and characteristics of oscillator i.

   RC Phase shift. (8)

   ii. Hartley. (8)
8. Explain the operation and advantages of crystal oscillators. (16)

9. Comparison of positive and negative feedback(8)
10. Explain the voltage series and current shunt feedback amplifier with an example. (16)
11. Explain the current series and voltage shunt feedback amplifier with an example. (16)
12. Explain about high frequency oscillator working principle.(16)