UNIT-1

PART A

1) What are basic properties of Boolean algebra?

The basic properties of Boolean algebra are commutative property, associative property and distributive property.

2) State the associative property of Boolean algebra.

The associative property of Boolean algebra states that the OR ing of several variables results in the same regardless of the grouping of the variables. The associative property is stated as follows:

$$A+ (B+C) = (A+B) +C$$

3) State the commutative property of Boolean algebra.

The commutative property states that the order in which the variables are OR ed makes no difference.

The commutative property is:

$$A+B=B+A$$

4) State the distributive property of Boolean algebra.

The distributive property states that AND ing several variables and OR ing the result with a single variable is equivalent to OR ing the single variable with each of the several variables and then AND ing the sums. The distributive property is:

$$A+BC= (A+B) (A+C)$$

5) State the absorption law of Boolean algebra.

The absorption law of Boolean algebra is given by

$$X+XY=X,\ X(X+Y)=X.$$

6) Simplify the following using De Morgan's theorem [((AB)'C)'' D]'

[((AB)'C)'' D]' = ((AB)'C)'' + D' [(AB)' = A' + B']

= (AB)' C + D'

= (A' + B') C + D'

7) State De Morgan's theorem.

De Morgan suggested two theorems that form important part of Boolean algebra. They are,

1) The complement of a product is equal to the sum of the complements.

(AB)' = A' + B'

2) The complement of a sum term is equal to the product of the complements.

(A + B)' = A'B'

8) Reduce A.A'C

A.A'C = 0.C [A.A' = 1]

= 0

9) Reduce A (A + B)

A (A + B) = AA + AB

= A (1 + B) [1 + B = 1]

= A.

10) Reduce A'B'C' + A'BC' + A'BC

A'B'C' + A'BC' + A'BC = A'C'(B' + B) + A'B'C

= A'C' + A'BC [A + A' = 1]

= A'(C' + BC)

= A'(C' + B) [A + A'B = A + B]

11) Reduce AB + (AC)' + AB'C (AB + C)

AB + (AC)' + AB'C (AB + C) = AB + (AC)' + AAB'BC + AB'CC

= AB + (AC)' + AB'CC [A.A' = 0]

= AB + (AC)' + AB'C [A.A = 1]

= AB + A' + C' =AB'C [(AB)' = A' + B']

= A' + B + C' + AB'C [A + AB' = A + B]

= A' + B'C + B + C' [A + A'B = A + B]

= A' + B + C' + B'C

=A' + B + C' + B'

=A' + C' + 1

= 1 [A + 1 =1]

12) Simplify the following expression Y = (A + B) (A + C') (B' + C')

Y = (A + B) (A + C') (B' + C')

= (AA' + AC +A'B +BC) (B' + C') [A.A' = 0]

= (AC + A'B + BC) (B' + C')

= AB'C + ACC' + A'BB' + A'BC' + BB'C + BCC'

= AB'C + A'BC'

13) Show that (X + Y' + XY) (X + Y') (X'Y) = 0

(X + Y' + XY)(X + Y')(X'Y)

= (X + Y' + X) (X + Y') (X' + Y) [A + A'B = A + B]

= (X + Y') (X + Y') (X'Y) [A + A = 1]

= (X + Y') (X'Y) [A.A = 1]

= X.X' + Y'.X'.Y

= 0 [A.A' = 0]

14) Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC

ABC + ABC' + AB'C + A'BC

=AB(C + C') + AB'C + A'BC

=AB + AB'C + A'BC

=A (B + B'C) + A'BC

=A (B + C) + A'BC

=AB + AC + A'BC

=B (A + C) + AC

=AB + BC + AC

=AB + AC +BC

15) Convert the given expression in canonical SOP form Y = AC + AB + BC

Y = AC + AB + BC

=AC (B + B') + AB (C + C') + (A + A') BC

=ABC + ABC' + AB'C + AB'C' + ABC + ABC' + ABC

=ABC + ABC' +AB'C + AB'C' [A + A =1]

16) Define duality property.

Duality property states that every algebraic expression deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

17) Find the complement of the functions F1 = x'yz' + x'y'z and F2 = x (y'z' + yz).

By applying De-Morgan's theorem.

$$F1' = (x'yz' + x'y'z)' = (x'yz')'(x'y'z)'$$

$$= (x + y' + z)\ (x + y + z')$$

$$F2' = [x\ (y'z' + yz)]' = x' + (y'z' + yz)'$$

$$= x' + (y'z')'(yz)'$$

$$= x' + (y + z)\ (y' + z')$$

18) Simplify the following expression

$$Y = (A + B)\ (A = C)\ (B + C)$$

$$= (A\ A + A\ C + A\ B + B\ C)\ (B + C)$$

$$= (A\ C + A\ B + B\ C)\ (B + C)$$

$$= A\ B\ C + A\ C\ C + A\ B\ B + A\ B\ C + B\ B\ C + B\ C\ C$$

$$= A\ B\ C$$

19) Define Canonical form

Boolean functions expressed as a sum of minterms ($\sum m$) or product of maxterms ($\prod M$) are said to be in canonical form

20) Define Minterm and Maxterm

Each individual term in standard SOP form is called a Minterm

Example: f (A, B, C) = AB'C +ABC +A'BC'

Each individual term in standard POS form is called a Maxterm

Example: f (A, B, C) = (A+B+C) (A+B'+C)

21) What are the methods adopted to reduce Boolean function?

i) Karnaugh map

ii) Tabular method or Quine Mc-Cluskey method

iii) Variable entered map technique.

22) State the limitations of karnaugh map.

i) Generally it is limited to six variable map (i.e.) more then six variable involving expressions are not reduced.

ii) The map method is restricted in its capability since they are useful for simplifying only Boolean expression represented in standard form.

23) What is a karnaugh map?

A karnaugh map or k map is a pictorial form of truth table, in which the map diagram is made up of squares, with each squares representing one minterm of the function.

24) Find the minterms of the logical expression Y = A'B'C' + A'B'C + A'BC + ABC'

Y = A'B'C' + A'B'C + A'BC + ABC'

=m0 + m1 +m3 +m6

$=\sum m(0, 1, 3, 6)$

25) Write the maxterms corresponding to the logical expression

$Y = (A + B + C') (A + B' + C') (A' + B' + C)$

$= (A + B + C') (A + B' + C') (A' + B' + C)$

$=M1.M3.M6$

$= \prod M(1, 3, 6)$

26) What are called don't care conditions?

In some logic circuits certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or'd' in the truth tables and are called don't care conditions or incompletely specified functions.

27) What is a prime implicant?

A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.

28) What is an essential implicant?

If a min term is covered by only one prime implicant, the prime implicant is said to be essential

29) What is a Logic gate?

Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function.

30) What are the basic digital logic gates?

The three basic logic gates are

AND gate, OR gate, NOT gate

31) Which gates are called as the universal gates? What are its advantages?

The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic application.

32) Classify the logic family by operation?

The Bipolar logic family is classified into Saturated logic and Unsaturated logic.

- ✓ The RTL, DTL, TTL, I2L, HTL logic comes under the saturated logic family.
- ✓ The Schottky TTL, and ECL logic comes under the unsaturated logic family.

33) State the classifications of FET devices.

FET is classified as

1. Junction Field Effect Transistor (JFET)
2. Metal oxide semiconductor family (MOS).

34) Mention the classification of saturated bipolar logic families.

The bipolar logic family is classified as follows:

RTL- Resistor Transistor Logic

DTL- Diode Transistor logic

I2L- Integrated Injection Logic

TTL- Transistor Transistor Logic

ECL- Emitter Coupled Logic

35) Mention the important characteristics of digital IC's?

Fan out

Power dissipation

Propagation Delay

Noise Margin

Fan In

Operating temperature

Power supply requirements

36) Define Fan-out?

Fan out specifies the number of standard loads that the output of the gate can drive without impairment of its normal operation.

37) Define power dissipation?

Power dissipation is measure of power consumed by the gate when fully driven by all its inputs.

38) What is propagation delay?

Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in ns.

39) Define noise margin?

It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts.

40) Define fan in?

Fan in is the number of inputs connected to the gate without any degradation in the voltage level.

41) What is Operating temperature?

All the gates or semiconductor devices are temperature sensitive in nature. The temperature in which the performance of the IC is effective is called as operating temperature. Operating temperature of the IC vary from 00 C to 700 c.

42) What is High Threshold Logic?

Some digital circuits operate in environments, which produce very high noise signals. For operation in such surroundings there is available a type of DTL gate which possesses a high threshold to noise immunity. This type of gate is called HTL logic or High Threshold Logic.

43) What are the types of TTL logic?

1. Open collector output 2. Totem-Pole Output

3. Tri-state output.

44) What is depletion mode operation MOS?

If the channel is initially doped lightly with p-type impurity a conducting channel exists at zero gate voltage and the device is said to operate in depletion mode.

45) What is enhancement mode operation of MOS?

If the region beneath the gate is left initially uncharged the gate field must induce a channel before current can flow. Thus the gate voltage enhances the channel current and such a device is said to operate in the enhancement mode.

46) Mention the characteristics of MOS transistor?

1. The n- channel MOS conducts when its gate- to- source voltage is positive.

2. The p- channel MOS conducts when its gate- to- source voltage is negative

3. Either type of device is turned off if its gate- to- source voltage is zero.

47) How schottky transistors are formed and state its use?

A schottky diode is formed by the combination of metal and semiconductor. The presence of schottky diode between the base and the collector prevents the transistor from going into saturation. The resulting transistor is called as schottky transistor. The use of schottky transistor in TTL decreases the propagation delay without a sacrifice of power dissipation.

48) List the different versions of TTL

1. TTL (Std.TTL) 2.LTTL (Low Power TTL) 3.HTTL (High Speed TTL)

4.STTL (Schottky TTL) 5.LSTTL (Low power Schottky TTL)

49) Why totem pole outputs cannot be connected together.

Totem pole outputs cannot be connected together because such a connection might produce excessive current and may result in damage to the devices.

50) State advantages and disadvantages of TTL

Adv:

Easily compatible with other ICs

Low output impedance

Disadv:

Wired output capability is possible only with tristate and open collector types Special circuits in Circuit layout and system design are required.

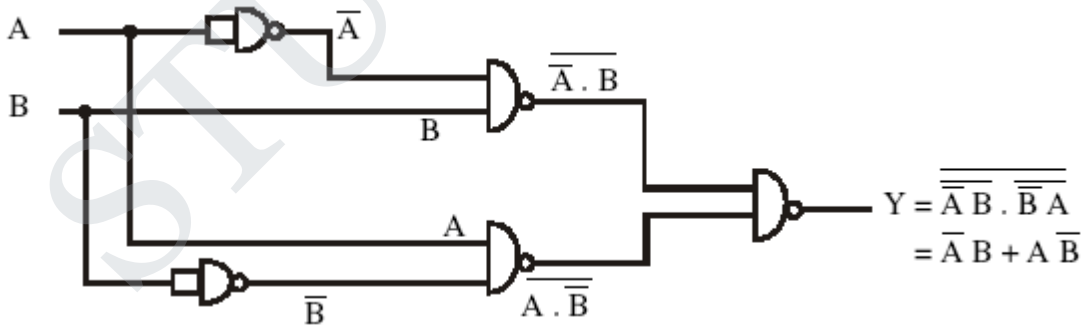
51) When does the noise margin allow digital circuits to function properly?

When noise voltages are within the limits of VNA (High State Noise Margin) and VNK for a particular logic family.

52) What happens to output when a tristate circuit is selected for high impedance.

Output is disconnected from rest of the circuits by internal circuitry.

53) Implement the Boolean Expression for EX – OR gate using NAND Gates.



UNIT-2

PART A

1. How logic circuits of a digital system are classified?

Logic circuits of a digital system are classified into two types as combinational and sequential.

2. Define combinational logic

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

3. Write down the design procedure for combinational circuits

- **The problem definition**
- **Determine the number of available input variables & required O/P variables.**
- **Assigning letter symbols to I/O variables**
- **Obtain simplified Boolean expression for each O/P.**
- **Obtain the logic diagram.**

4. Define Half adder and full adder

The logic circuit that performs the addition of two bits is a half adder. The circuit that performs the addition of three bits is a full adder.

5. Define Decoder?

A decoder is a multiple - input multiple output logic circuit that converts coded inputs into coded outputs where the input and output codes are different.

6. What is binary decoder?

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n out puts lines.

7. Define Encoder?

An encoder has 2n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

8. What is priority Encoder?

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

9. Define multiplexer?

Multiplexer is a digital switch. If allows digital information from several sources to be routed onto a single output line.

10. What do you mean by comparator?

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.

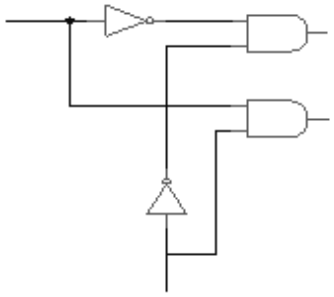
11. What is a demux? (Apr 2004)

A decoder with an enable input is referred to as a demultiplexer.

12. What is priority encoder?

A priority encoder is an encoder circuit that includes the priority function. The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

13. Draw a 1 to 2 demultiplexer circuit. (Nov 2003)

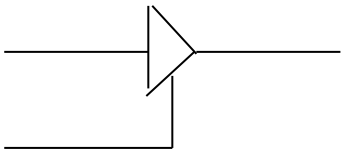


14. How can a decoder be converted into a demultiplexer? (Nov/Dec 2005)

A decoder can be converted into a demultiplexer by including enable input.

15. What are tri-state gates? (Apr 2005)

A three-state gate is a digital circuit that exhibits three states. Two of the states are signals equivalent to logic 1 and logic 0 and the third state is a high impedance state.



16. Distinguish between decoder and demultiplexer. (Apr / May 2003)

Decoder	Demultiplexer
A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. It is sometimes called as n-to-m-line decoder, where $m \leq 2^n$.	A demultiplexer is a circuit that receives information from a single line and transmits this information on one 2^n possible output lines.

17. How can a multiplexer be used to convert 8-bit parallel data into serial form? (May/June 2006).

- **A 8-to-1-line multiplexer is used to convert 8-bit parallel data into serial form.**
- **Each of the eight inputs, I_0 through I_7, is applied to one input of an AND gate.**

- **Selection lines S_0, S_1, S_2, and S_3 are decoded to select a particular AND gate.**
- **The outputs of the AND gates are applied to a single OR gate that provides the 1-line (serial form) output.**
- **Consider the case when the selection lines $S_2S_1S_0 = 011$.**
- **The AND gate associated with input I_3 has three of its inputs equal to 1 and the third input connected to I_3.**

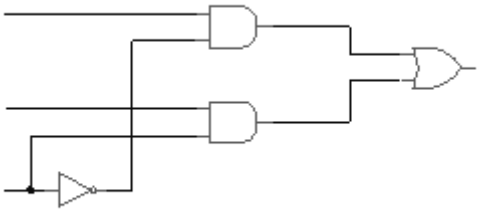
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4

- **The other seven AND gates have at least one input equal to 0, which makes their outputs**

  equal to 0.
- **The OR output is now equal to the value of I_2, providing a path from the selected input to the output. Thus it converts 8-bit parallel data into a serial form.**

18. Draw a 2 to 1 multiplexer circuit. (Nov 2003)

2 to 1 line Multiplexer



19. What is a combinational circuit? Give an example

Combinational logic circuits are circuits in which the output at any time depends upon the combination of the input signals present at that instant only and does not depend upon the past conditions

Example:

- **Decoder**
- **Multiplexer**
- **Adder**
- **Subtractor**

20. What is meant by multilevel gate network?

The multilevel gate networks are 2 level, 3level, 4level gate network, etc. The maximum number of gates cascaded in series between a network input and the output is referred to as the number of levels of gates

21. What is look-ahead carry addition?

The speed with which an addition is performed is limited by the time required for the

carries to propagate or ripple through all of the adder. One method of speeding up the

process is by eliminating the ripple carry delay and this is called look-ahead carry

addition. This method is based on two functions of the full adder, called the carry generate and carry propagate function.

UNIT-3

PART A

1. What is the classification of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types. They are,

1) Synchronous sequential circuit.

2) Asynchronous sequential circuit.

2. Define Flip flop.

The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

3. What are the different types of flip-flop?

There are various types of flip flops. Some of them are mentioned below they are,

- RS flip-flop
- SR flip-flop
- D flip-flop
- JK flip-flop
- T flip-flop

4. What is the operation of RS flip-flop?

• When R input is low and S input is high the Q output of flip-flop is set.

• When R input is high and S input is low the Q output of flip-flop is reset.

• When both the inputs R and S are low the output does not change

• When both the inputs R and S are high the output is unpredictable

5. What is the operation of SR flip-flop?

• When R input is low and S input is high the Q output of flip-flop is set.

• When R input is high and S input is low the Q output of flip-flop is reset.

• When both the inputs R and S are low the output does not change.

• When both the inputs R and S are high the output is unpredictable.

6. What is the operation of D flip-flop?

In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.

7. What is the operation of JK flip-flop?

• When K input is low and J input is high the Q output of flip-flop is set.

• When K input is high and J input is low the Q output of flip-flop is reset.

• When both the inputs K and J are low the output does not change

• When both the inputs K and J are high it is possible to set or reset the flip-flop (i.e.) the output toggle on the next positive clock edge.

8. What is the operation of T flip-flop?

T flip-flop is also known as Toggle flip-flop.

• When T=0 there is no change in the output.

• When T=1 the output switch to the complement state (i.e.) the output toggles.

9. Define race around condition.

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called 'race around condition'.

10. What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

11. What is a master-slave flip-flop?

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

12. Define rise time.

The time required to change the voltage level from 10% to 90% is known as rise time (t_r).

13. Define fall time.

The time required to change the voltage level from 90% to 10% is known as fall time (t_f).

14. Define skew and clock skew.

The phase shift between the rectangular clock waveforms is referred to as skew and

the time delay between the two clock pulses is called clock skew.

15. Define setup time.

The setup time is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t_{setup}.

16. Define hold time.

The hold time is the minimum time for which the voltage levels at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t_{hold}.

17. Define propagation delay.

A propagation delay is the time required to change the output after the application of the input. It is denoted as $t_{pd.}$

18. Define registers.

A register is a group of flip-flops flip-flop can store one bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

19. Define shift registers.

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

20. What are the different types of shift type?

There are five types. They are,

- **Serial In Serial Out Shift Register**
- **Serial In Parallel Out Shift Register**
- **Parallel In Serial Out Shift Register**
- **Parallel In Parallel Out Shift Register**
- **Bidirectional Shift Register**

21. Explain the flip-flop excitation tables for RS flip-flop.

In RS flip-flop there are four possible transitions from the present state to the next state. They are,

- **0 0 transition: This can happen either when R=S=0 or when R=1 and S=0.**

- **0 1 transition: This can happen only when S=1 and R=0.**
- **1 0 transition: This can happen only when S=0 and R=1.**
- **1 1 transition: This can happen either when S=1 and R=0 or S=0 and R=0.**

22. Explain the flip-flop excitation tables for JK flip-flop

In JK flip-flop also there are four possible transitions from present state to next state. They are,

- **0 0 transition: This can happen when J=0 and K=1 or K=0.**
- **0 1 transition: This can happen either when J=1 and K=0 or when J=K=1.**
- **1 0 transition: This can happen either when J=0 and K=1 or when J=K=1.**
- **1 1 transition: This can happen when K=0 and J=0 or J=1.**

23. Explain the flip-flop excitation tables for D flip-flop

In D flip-flop the next state is always equal to the D input and it is independent of the present state. Therefore D must be 0 if Qn+1 have to 0, and if Qn+1 have to be 1 regardless the value of Qn.

24. Explain the flip-flop excitation tables for T flip-flop

When input T=1 the state of the flip-flop is complemented; when T=0, the state of the flip-flop remains unchanged. Therefore, for 0_0 and 1_1 transitions T must be 0 and for 0_1 and 1_0 transitions must be 1.

25. Define sequential circuit?

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

26. Give the comparison between combinational circuits and sequential circuits.

Combinational circuits	Sequential circuits
Memory unit is not required	Memory unity is required
Parallel adder is a combinational circuit	Serial adder is a sequential circuit

27. What do you mean by present state?

The information stored in the memory elements at any given time defines the present state of the sequential circuit.

28. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

29. State the types of sequential circuits?

1. Synchronous sequential circuits

2. Asynchronous sequential circuits

30. Define synchronous sequential circuit

In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.

31. Define Asynchronous sequential circuit?

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

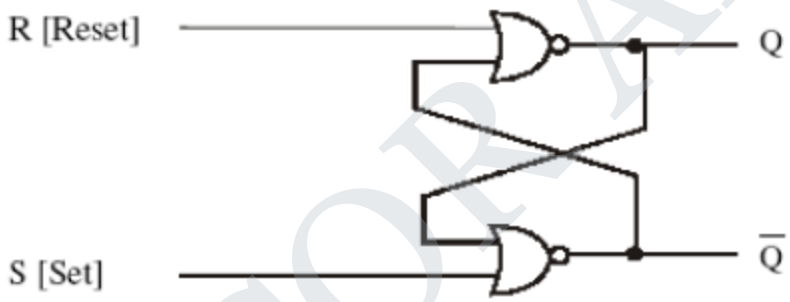
32. Give the comparison between synchronous & Asynchronous sequential circuits?

Synchronous sequential circuits	Asynchronous sequential circuits.
Memory elements are clocked flip-flops	Memory elements are either unlocked flip - flops or time delay elements.
Easier to design	More difficult to design

33. Define flip-flop

Flip - flop is a sequential device that normally samples its inputs and changes its outputs only at times determined by clocking signal.

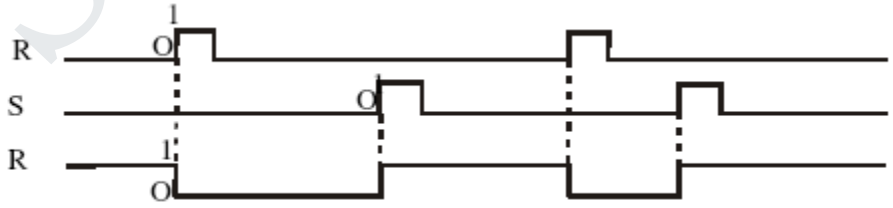
34. Draw the logic diagram for SR latch using two NOR gates.



35. The following wave forms are applied to the inputs of SR latch. Determine the

Q Waveform

Assume initially Q = 1



Here the latch input has to be pulsed momentarily to cause a change in the latch output state, and the output will remain in that new state even after the input pulse is over.

36. What is race around condition?

In the JK latch, the output is feedback to the input, and therefore changes in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

37. What are the types of shift register?

1. **Serial in serial out shift register?**
2. **Serial in parallel out shift register**
3. **Parallel in serial out shift register**
4. **Parallel in parallel out shift register**
5. **Bidirectional shift register shift register**

38. State the types of counter?

1. **Synchronous counter**
2. **Asynchronous Counter**

39. Give the comparison between synchronous & Asynchronous counters.

Asynchronous counters	Synchronous counters
In this type of counter flip-flops are connected in such a way that output of 1st flip-flop drives the clock for the next flip-flop.	In this type there is no connection between output of first flip-flop and clock input of the next flip - flop
All the flip-flops are Not clocked simultaneously	All the flip-flops are clocked simultaneously

40. The t pd for each flip-flop is 50 ns. Determine the maximum operating frequency for MOD - 32 ripple counter

$$f_{max\ (ripple)} = 5 \times 50\ ns = 4\ MHZ$$

UNIT-4

PART-A

1. **What are races?**

When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.

2. Define non critical race.

If the final stable state that the circuit reaches does not depend on the order in which the state variable changes, the race condition is not harmful and it is called a non critical race.

3. Define critical race?

If the final stable state depends on the order in which the state variable changes, the race condition is harmful and it is called a critical race.

4. What is a cycle?

A cycle occurs when an asynchronous circuit makes a transition through a series of unstable states. If a cycle does not contain a stable state, the circuit will go from one unstable to stable to another, until the inputs are changed.

5. Write a short note on fundamental mode asynchronous circuit.

Fundamental mode circuit assumes that. The input variables change only when the circuit is stable. Only one input variable can change at a given time and inputs are levels and not pulses.

6. Write a short note on pulse mode circuit.

Pulse mode circuit assumes that the input variables are pulses instead of level. The width of the pulses is long enough for the circuit to respond to the input and

the pulse width must not be so long that it is still present after the new state is reached.

7. Define secondary variables

The delay elements provide a short term memory for the sequential circuit. The present state and next state variables in asynchronous sequential circuits are called secondary variables.

8. Define flow table in asynchronous sequential circuit.

In asynchronous sequential circuit state table is known as flow table because of the behaviour of the asynchronous sequential circuit. The stage changes occur in independent of a clock, based on the logic propagation delay, and cause the states to flow from one to another.

9. What is fundamental mode.

A transition from one stable state to another occurs only in response to a change in the input state. After a change in one input has occurred, no other change in any input occurs until the circuit enters a stable state. Such a mode of operation is referred to as a fundamental mode.

10. Write short note on shared row state assignment.

Races can be avoided by making a proper binary assignment to the state variables. Here, the state variables are assigned with binary numbers in such a way that only one state variable can change at any one state variable can change at any one time when a state transition occurs. To accomplish this, it is necessary that states between which transitions occur be given adjacent assignments. Two binary are said to be adjacent if they differ in only

one variable.

11. Write short note on one hot state assignment.

The one hot state assignment is another method for finding a race free state assignment. In this method, only one variable is active or hot for each row in the original flow table, ie, it requires one state variable for each row of the flow table.

Additional row are introduced to provide single variable changes between internal state transitions.

12. Define hazard

Hazard is an unwanted transient i.e, spike or glitch that occurs due to unequal path or unequal propagation delays.

13. Define Static hazard

Static hazard is a condition which results in a single momentary incorrect output due to change in a single input variable when the output is expected to remain in the same state.

14. Define Static-0 hazard

When the output is to remain at the value 0 and a momentary 1 output is possible during the transition between the two input states, then the hazard is called a static-0 hazard.

15. Define Static-1 hazard

If the two input states both produce a 1 output in the steady state and a momentary 0 output is possible during the transition between the two input states, then the hazard is called a Static-1 hazard.

16. Define Dynamic hazard

A transient change occurring 3 or more times at an output terminal of a logic network when the output is supposed to change only once during a transition between two input states differing in the value of one variable.

17. How to eliminate a Dynamic hazard

Dynamic hazard can be eliminated by covering every pair of 1 cells and every pair of 0 cells in the K-map by at least one sub cube.

18. Define Essential hazard

Essential hazard is a type of hazard that exists only in asynchronous sequential circuits with two or more feedbacks. An essential hazard is caused by unequal delays along two or more paths that originate from the same input. An excessive delay through an inverter circuit in comparison to the delay associated with the feedback path may cause essential hazard.

19. How to eliminate Essential hazard

Essential hazard can be eliminated by adding redundant gates as in static hazards. They can be eliminated by adjusting the amount of delay in the affected path. For this, each feedback loop must be designed with extra care to ensure that the delay in the feedback path is long enough compared to the delay of other signals that originate from the input terminals.

20. How to eliminate static hazard

By covering the adjacent cells with a redundant grouping that overlaps both groupings.

21. Define a primitive flow table. (Nov-2005)

- In the design of asynchronous sequential circuits, it is easy to name the states by letter symbols. Such a table is called a flow table.
- If the flow table has only one stable state for each row in the table which is defined as primitive flow table.

22.What are excitation variables?

The next state variables in asynchronous sequential circuits are called as excitation variable.

23. What is fundamental mode sequential circuit?

-input variables changes if the circuit is stable

-inputs are levels, not pulses

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25. What are the significance of state assignment?

In synchronous circuits-state assignments are made with the objective of circuit reduction

Asynchronous circuits-its objective is to avoid critical races.

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28.What are the different techniques used in state assignment?

-shared row state assignment

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29.What are the steps for the design of asynchronous sequential circuit?

-construction of primitive flow table

-reduction of flow table

-state assignment is made

-realization of primitive flow table

30.What is the cause for essential hazards?

-unequal delays along 2 or more path from same input.

31.Give the comparison between state Assignment Synchronous circuit and state assignment

asynchronous circuit.

In synchronous circuit, the state assignments are made with the objective of circuit reduction. In asynchronous circuits, the objective of state assignment is to avoid critical races.

32.What is SM chart?

-describes the behavior of a state machine

-used in hardware design of digital systems.

33.What are the advantages of SM chart?

-easy to understand the operation

-east to convert to several equivalent forms.

34.What is state equivalence theorem ?

Two states SA and SB, are equivalent if and only if for every possible input X

sequence, the outputs are the same and the next states are equivalent

i.e., if SA (t + 1) = SB (t + 1) and ZA = ZB then SA = SB.

35.What do you mean by distinguishing sequences?

Two states, SA and SB of sequential machine are distinguishable if and only if their

exists at least one finite input sequence. Which, when applied to sequential machine causes

different output sequences depending on whether SA or SB is the initial state.

36. Prove that the equivalence partition is unique

Consider that there are two equivalence partitions exists : PA and PB, and PA) PB.

This states that, there exist 2 states Si & Sj which are in the same block of one partition and

not in the same block of the other. If Si & Sj are in different blocks of say PB, there exists at

least on input sequence which distinguishes Si & Sj and therefore, they cannot be in the same

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that affects the two states, the same output sequence, occurs whenever both outputs are

specified and regardless of whether Si on Sj is the initial state.

38.Define merger graph.

The merger graph is defined as follows. It contains the same number of vertices as the

state table contains states. A line drawn between the two state vertices indicates each

compatible state pair. It two states are incompatible no connecting line is drawn.

39.Define incompatibility

The states are said to be incompatible if no line is drawn in between them. If implied

states are incompatible, they are crossed & the corresponding line is ignored.

40.Explain the procedure for state minimization.

1. Partition the states into subsets such that all states in the same subsets are 1 -

equivalent.

2. Partition the states into subsets such that all states in the same subsets are 2 -

equivalent.

3. Partition the states into subsets such that all states in the same subsets are 3 -

equivalent.

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A Set of compatibles is said to be closed if, for every compatible contained in the set,

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M1, there is a corresponding equivalent state in M2 & vice versa.

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For the design of sequential counters we have to relate present states and next states.

The table, which represents the relationship between present states and next states, is called

state table.

44. Define total state

The combination of level signals that appear at the inputs and the outputs of the

delays define what is called the total state of the circuit.

45.What are the steps for the design of asynchronous sequential circuit?

1. Construction of a primitive flow table from the problem statement.

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reduction

3. State assignment is made

4. The primitive flow table is realized using appropriate logic elements.

46.What are the types of asynchronous circuits ?

1. Fundamental mode circuits

2. Pulse mode circuits

UNIT-4

PART-A

21. What are races?

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1. Fundamental mode circuits

2. Pulse mode circuits

UNIT-5

PART-A

1. What is RAM?

A memory Unit is a collection of storage cells together with associated circuits needed to transfer information in and out of the device. The time it takes to transfer information to or from any desired random location is always same. Hence, the name Random Access Memory abbreviated RAM

2. What are the different types of programming the PLA? [AU, DEC, 2008]

1. Mask programmable PLA
2. Field programmable PLA

3. List basic types of programmable logic devices?

3. Read only memory
4. Programmable logic Array
5. Programmable Array Logic

4. Explain ROM?

A read only memory (ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines. Each

bit combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is 2n.

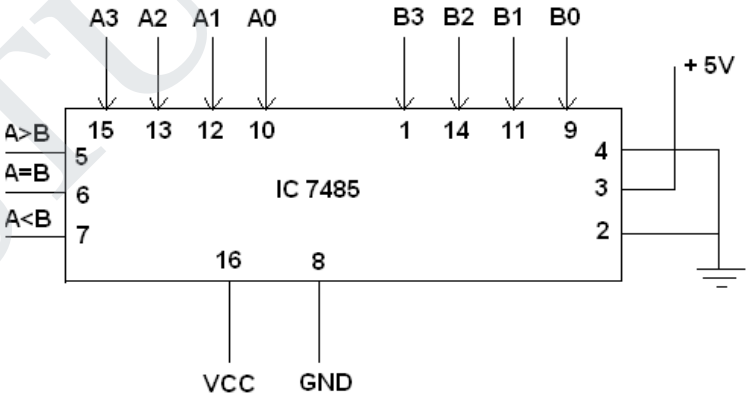
5. How does ROM retain information? [AU, APR/MAY, 2005]

ROM retains information since it is non – volatile memory.

6. Define address and word?

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

7. Using a single IC 7485, draw the logic diagram of a 4 bit comparator? [AU, APR/MAY, 2003]



8. What is programmable logic array? How it differs from ROM?

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to

a ROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the ROM.

9. State the types of ROM

6. Masked ROM.
7. Programmable Read only Memory
8. Erasable Programmable Read only memory.
9. Electrically Erasable Programmable Read only Memory

10. Explain PROM.

PROM (Programmable Read Only Memory):

It allows user to store data or program. PROMs use the fuses with material like nichrome and polycrystalline. The user can blow these fuses by passing around 20 to 50 mA of current for the period 5 to 20μs.The blowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent. (or) PROM is Programmable Read Only Memory. It consists of a set of fixed AND gates connected to a decoder and a programmable OR array.

11. Explain EPROM.

EPROM: (Erasable Programmable Read Only Memory)

EPROM use MOS circuitry. They store 1's and 0's as a packet of charge in a buried layer of the IC chip. We can erase the stored data in the EPROMs by exposing the chip to ultraviolet light via its quartz window for 15 to 20minutes. It is not possible to erase selective information. The chip can be reprogrammed.

12. Explain EEPROM.

EEPROM :(Electrically Erasable Programmable Read Only Memory)

EEPROM also use MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.

13. What is programmable logic array? How it differs from ROM?

[AU, NOV/ DEC 2005]

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the ROM.

14. List the major differences between PLA and PAL? (OR) Is the PAL same as the PLA? [AU, APR/MAY, 2004],[AU, NOV/DEC,2006]

Sl.no	PLA	PAL
1	Both AND and OR arrays are programmable and Complex	AND arrays are programmable OR arrays are fixed
2.	Costlier than PAL	Cheaper and Simpler.

15. Define PLD?

Programmable Logic Devices consist of a large array of AND gates and OR gates that can be programmed to achieve specific logic functions.

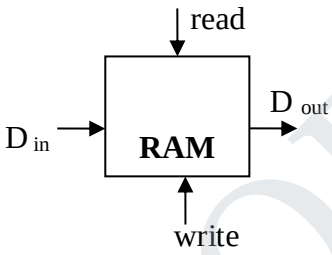
16. Give the classification of PLD's ?

PLDs are classified as PROM (Programmable Read Only Memory), Programmable Logic Array (PLA), Programmable Array Logic (PAL), and Generic Array Logic (GAL).

17. Define a memory cell. Give an example? (or) Draw a RAM cell?

[AU, NOV, 2004]

Memory cell or binary storage cell is the basic building block of a memory unit which is modeled by an SR latch with associated gates.



18. Define PLA?

PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a programmable AND array and a programmable OR array.

19. What is mask – programmable PLA?

With a mask programmable PLA, the user must submit a PLA program table to the manufacturer.

20. What is field programmable logic array?

The second type of PLA is called a field programmable logic array. The user by means of certain recommended procedures can program the FPLA.

21. Define PAL?

PAL is Programmable Array Logic. PAL consists of a programmable AND array and a fixed OR array with output logic.

22. Why was PAL developed?

It is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

23. What does PAL 10L8 specify?

PAL - Programmable Logic Array

10 - Ten inputs

L - Active LOW Output

8 - Eight Outputs

24. Why the input variables to a PAL are buffered?

The input variables to a PAL are buffered to prevent loading by the large number of AND gate inputs to which available or its complement can be connected.

25. Give the comparison between PROM and PLA. (AU- Sep -2009)

Sl.no	PROM	PLA
1	And array is fixed and OR array is programmable.	Both AND and OR arrays are Programmable.

2.	Cheaper and simple to use.	Costliest and complex than PROMS.

26. Comparison between RAM and ROM

RAM	ROM
RAM's have both read and write capability	ROM's have only read operation
RAM's are volatile memories	
They lose stored data when the power is turned off	ROM's are non-volatile memories
	They retain stored data even if power is turned off
RAM's are available in both bipolar and MOS technologies	ROM's are available in both bipolar and MOS technologies

27. Compare SRAM& DRAM

Static RAM	Dynamic RAM
SRAM consists of flip-flops. Each flip-flop stores one bit.	DRAM stores the data as charge on the capacitor. It consists of MOSFET and the

	capacitor for each cell
SRAM contains less memory cells per unit area	DRAM contains more memory cells per unit area
costly	Less costly
It's access time is less, hence faster memories	It's access time is greater than SRAM
Refreshing circuitry is not required	Refreshing circuitry is required

28. What are the advantages of RAM

- Fast operating speed (< 150 nS)
- Low power dissipation (< 1 mW)
- Compatibility
- Non-destructive readout

29. Write a note on advantages of ROM

- Ease and speed of design
- Faster than MSI devices PLD and FPGA
- The program that generates the ROM contents can easily be structured to handle unusual or undefined cases

- A ROM's function is easily modified just by changing the stored pattern, unusually without changing any external connections
- More economical

30. what are the disadvantages of ROM

- for functions more than 20 inputs, a ROM based circuit is impractical because of the limit on ROM sizes that are available
- For simple to moderately complex functions, ROM based circuit may costly, consume more power, run slower.

31. How is memory size is specified? (AU- Sep -2009)

Memory size is specified by the total number of words in a memory array which is in the form of (2^n X m).

Where, 2^n - total number of words

m- Number of bits in a word / number of output data lines