VALLIAMMAI ENGINEERING COLLEGE

SRM Nagar, Kattankulathur-603203

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

SUBJECT : EC8552-COMPUTER ARCHITECTURE AND ORGANIZATION

SEM/YEAR: V/III

UNIT I COMPUTER ORGANIZATION & INSTRUCTIONS

Basics of a computer system: Evolution, Ideas, Technology, Performance, Power wall, Uniprocessors to Multiprocessors. Addressing and addressing modes. Instructions: Operations and Operands, Representing instructions, Logical operations, control operations.

PART-A

Q.No	Questions	BT Level	Competence
1	Express the equation for the dynamic power required per transistor.	BTL 2	Understanding
2	Identify general characteristics of Relative addressing mode with an example.	BTL 4	Analyzing
3	List the eight great ideas invented by computer architects.	BTL 1	Remembering
4	Tabulate are the components of computer system.	BTL 1	Remembering
5	Distinguish Pipelining from Parallelism.	BTL 2	Understanding
6	Interpret the various instructions based on the operations they perform and give one example to each category.	BTL 2	Understanding
7	Differentiate DRAM and SRAM.	BTL 4	Analyzing
8	Give the components of a computer system and list their functions.	BTL 2	Understanding
9	What is the MIPS code for the statement f= (g+h)-(i+j).	BTL 1	Remembering
10	Calculate throughput and response time.	BTL 3	Applying
11	Compose the CPU performance equation.	BTL 6	Creating
12	Measure the performance of the computers: If computer A runs a program in 10 seconds, and computer B runs the same program in 15 seconds, how much faster is A over B?	BTL 5	Evaluating
13	Formulate the equation of CPU execution time for a program.	BTL 6	Creating
14	State the need for indirect addressing mode. Give an example.	BTL 1	Remembering
15	Show the formula for CPU clock cycles required for a program.	BTL 3	Applying
16	Define Stored Program Concept.	BTL 1	Remembering
17	Name the different addressing modes.	BTL 1	Remembering
18	Compare multi-processor and uniprocessor.	BTL 4	Analyzing
19	Illustrate relative addressing mode with example.	BTL 3	Applying
20	Consider the following performance measurements for a program Which computer has the higher MIPS rating	BTL 5	Evaluating

Measurement	Computer A	Computer B
Instruction Count	10 billion	8 billion
Clock rate	4GHz	4GHz
CPI	1.0	1.1

	PART B			
1	i).Summarize the eight great ideas of computer Architecture. ii). Explain the technologies for Building Processors.	(7) (6)	BTL 5	Evaluating
2	List the various components of computer system and explain with neat diagram.	(13)	BTL 1	Remembering
3	i).Define addressing mode. ii).Describe the basic addressing modes for MIPS and give one suitable example instruction to each category.	(4) (9)	BTL 1	Remembering
4.	Examine the operands and operations of computer hardware.	(13)	BTL 1	Remembering
5	i).Discuss the logical operations and control operations of computer. ii). Express the concept of Powerwall processor.	(7) (6)	BTL 2	Understanding
6	Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. i).Which processor has the highest performance expressed in instructions per second? ii).If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions? iii).We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?	 (3) (5) (5)	BTL 4	Analyzing
7	Assume a program requires the execution of 50 × 106 FP instructions,110 × 106 INT instructions, 80 × 106 L/S instructions, and 16 × 106 branch instructions The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate. i).By how much must we improve the CPI of FP instructions if we want the program to run two times faster? ii).By how much must we improve the CPI of L/S instructions? iii).By how much is the execution time of the program improved if the CPI of INT and FP Instructions are reduced by 40% and the CPI of L/S and Branch is reduced by 30%?	 (4) (4) (5)	BTL 3	Applying
8	Recall how performance is calculated in a computer system and derive the necessary performance equations.	(13)	BTL 2	Understanding
9	i).Formulate the performance of CPU. ii).Compose the factors that affect performance.	(7) (6)	BTL 6	Creating
10	i).Illustrate the following sequence of instructions and identify the addressing modes used and the operation done in every instruction (1) Move (R5)+, R0 (2) Add(R5)+, R0 (3) Move R0, (R5) (4) Move 16(R5),R3 (5) Add #40, R5 ii).Calculate which code sequence will execute faster according to execution time for the following conditions: Consider the computer with three instruction classes and CPI measurements as given below and instruction counts for each	(7) (6)	BTL 3	Applying

<table>
<tr><td></td><td>instruction class for the same program from two different compilers are given. Assume that the computer's clock rate is 1GHZ.
<table>
<tr><td>Code from</td><td colspan="3">CPI for the instruction class</td></tr>
<tr><td></td><td>A</td><td>B</td><td>C</td></tr>
<tr><td>CPI</td><td>1</td><td>2</td><td>3</td></tr>
<tr><td>Code from</td><td colspan="3">CPI for the instruction class</td></tr>
<tr><td></td><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Compiler1</td><td>2</td><td>1</td><td>2</td></tr>
<tr><td>Compiler2</td><td>2</td><td>1</td><td>1</td></tr>
</table></td><td></td><td></td></tr>
<tr><td>11</td><td>Consider two different implementation of the same instruction set architecture, The instruction can be divided into four classes according to their CPI (class A,B,C and D). P1 with clock rate 2.5 Ghz and CPI s of 1,2,3, and 3 respectively and P2 with clock rate 3 Ghz and CPI s of 2,2,2and 2 respectively. Given a program with a dynamic instruction count of $1.0*10^6$ instruction divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster? What is the global CPI for each implementation? Find the clock cycles required in both cases.</td><td>(13)</td><td>BTL 1</td><td>Remembering</td></tr>
<tr><td>12</td><td>i). Compare uni-processors and multi- processors.
ii). Analyze how instructions that involve decision making are executed with an example.</td><td>(3)
(10)</td><td>BTL 4</td><td>Analyzing</td></tr>
<tr><td>13</td><td>Analyze the various instruction formats and illustrate with an example.</td><td>(13)</td><td>BTL 4</td><td>Analyzing</td></tr>
<tr><td>14</td><td>(i)With suitable examples, Summarize the compilation of assignment statements into MIPS.
(ii)Translate the following C code to MIPS assembly code .Use a minimum number of instructions. Assume that I and k correspond to register $s3 and $s5 and the base of the array save is in $s6.What is the MIPs assembly code corresponding to this is C segment
While(save[i]==k) i+=1;</td><td>(8)
(5)</td><td>BTL 2</td><td>Understanding</td></tr>
<tr><td colspan="4">PART C</td></tr>
<tr><td>1</td><td>Assume that the variables f and g are assigned to register $s0 and $s1 respectively. Assume that base address of the array A is in register $s2. Assume f is zero initially.
f- -g – A[4]
A[5]=f + 100
Translate the above C statement into MIPS code . how many MIPS assembly instructions are needed to perform the C statements and how many different registers are needed to carry out the C statements ?</td><td>(15)</td><td>BTL 6</td><td>Creating</td></tr>
<tr><td>2</td><td>Integrate the eight ideas from computer architecture to the following ideas from other fields:
i). Assembly lines in automobile manufacturing.
ii). Express elevators in buildings.
iii).Aircraft and marine navigation systems that incorporate wind information.</td><td>(5)
(5)
(5)</td><td>BTL 6</td><td>Creating</td></tr>
</table>

3	Evaluate a MIPS assembly instruction in to a machine instruction, for the add $to, $s1,$s2 MIPS instruction. (15)	BTL 5	Evaluating
4	Explain the steps to convert the following high level language such as C into a MIPS code. (15) a=b+e; c=b+f;	BTL 5	Analyzing
UNIT II -ARITHMETIC			
Fixed point Addition, Subtraction, Multiplication and Division. Floating Point arithmetic, High performance arithmetic, Subword parallelism			
PART-A			
Q.No	**Questions**	**BT Level**	**Competence**
1	Calculate the following: Add 5_{10} to 6_{10} in binary and Subtract -6_{10} from 7_{10} in binary.	BTL 3	Applying
2	Analyze overflow conditions for addition and subtraction.	BTL 4	Analyzing
3	Construct the Multiplication hardware diagram.	BTL 3	Applying
4	List the steps of multiplication algorithm.	BTL 1	Remembering
5	What is meant by ALU fast multiplication?	BTL 1	Remembering
6	Subtract $(11011)_2 - (10011)_2$ using 1's complement and 2's complement method.	BTL 2	Understanding
7	Illustrate scientific notation and normalization with example.	BTL 3	Applying
8	Perform X-Y using 2's complement arithmetic for the given two 16-bit numbers X=0000 1011 1110 1111 and Y=1111 0010 1001 1101.	BTL 4	Analyzing
9	Contrast overflow and underflow with examples.	BTL 2	Understanding
10	State the rules to add two integers.	BTL 6	Creating
11	Name the floating point instructions in MIPS.	BTL 1	Remembering
12	Formulate the steps of floating point addition.	BTL 6	Creating
13	Evaluate the sequence of floating point multiplication.	BTL 5	Evaluating
14	Define scientific notation and normalized notation.	BTL 1	Remembering
15	Express the IEEE 754 floating point format.	BTL 2	Understanding
16	State sub-word parallelism and the data path in CPU.	BTL 1	Remembering
17	Interpret single precision floating point number representation with example and the representation of double precision floating point number.	BTL 2	Understanding
18	Divide 1,001,010 by 1000.	BTL 4	Analyzing
19	Describe edge triggered clocking.	BTL 1	Remembering
20	For the following MIPS assembly instructions above, decide the corresponding C statement? add f, g, h & add f, i, f	BTL 5	Evaluating
PART-B			
1	i).Discuss the multiplication algorithm its hardware and its sequential version with diagram. (6) ii).Express the steps to Multiply 2*3. (7)	BTL 2	Understanding
2	Illustrate the multiplication of signed numbers using Booth algorithm. $A=(-34)_{10}=(1011110)_2$ and $B=(22)_{10}=(0010110)_2$ where B is multiplicand and A is multiplier. (13)	BTL 3	Applying
3	Describe about basic concepts of ALU design. (13)	BTL 1	Remembering
4	Develop algorithm to implement A*B. Assume A and B for a pair of signed 2's complement numbers with values: A=010111, B=101100 (13)	BTL 6	Creating

5	i).State the division algorithm with diagram and examples. (6) ii).Divide 00000111 by 0010. (7)	BTL 1	Remembering
6	i).Express in detail about Carry looks ahead Adder. (8) ii).Divide $(12)_{10}$ by $(3)_{10}$ (7)	BTL 2	Understanding
7	Point out how ALU performs division with flow chart and block diagram. (13)	BTL 4	Analyzing
8	i).Examine with a neat block diagram how floating point addition is carried out in a computer system. (10) ii).Give an example for a binary floating point addition. (3)	BTL 1	Remembering
9	Tabulate the IEEE 754 binary representation of the number- 0.75_{10} i).Single precision. (6) ii).Double precision. (7)	BTL 1	Remembering
10	i).Design an arithmetic element to perform the basic floating point operations. (7) ii).Discuss sub word parallelism. (6)	BTL 2	Understanding
11	i).Explain floating point addition algorithm with diagram. (6) ii).Assess the result of the numbers $(0.5)_{10}$ and $(0.4375)_{10}$ using binary Floating point Addition algorithm. (7)	BTL 5	Evaluating
12	Calculate using single precision IEEE 754 representation. i). 32.75 (6) ii).18.125 (7)	BTL 4	Analyzing
13	Arrange the given number 0.0625 i). Single precision. (6) ii). Double precision formats. (7)	BTL 4	Analyzing
14	Solve using Floating point multiplication algorithm i). A= 1.10_{10} X 10^{10} B= $9.200X10^{-5}$ (7) ii). 0.5_{10} X 0.4375_{10} (6)	BTL 3	Applying
	PART C		
1	Create the logic circuit for CLA. What are the disadvantages of Ripple carry addition and how it is overcome in carry look ahead adder? (15)	BTL 6	Creating
2.	Evaluate the sum of 2.6125 * 101 and 4.150390625 * 101 by hand, assuming A and B are stored in the 16-bit half precision. Assume 1 guard, 1 round bit and 1 sticky bit and round to the nearest even. Show all the steps. (15)	BTL 5	Evaluating
3	Summarize 4 bit numbers to save space, which implement the multiplication algorithm for 0010_2 , 0011_2 with hardware design. (15)	BTL 5	Evaluating
4	Design 4 bit version of the algorithm to save pages, for dividing 00000111_2 by 0010_2 with hardware design. (15)	BTL 6	Creating
	UNIT III- THE PROCESSOR		
Introduction, Logic Design Conventions, Building a Datapath - A Simple Implementation scheme - An Overview of Pipelining - Pipelined Datapath and Control. Data Hazards: Forwarding versus Stalling, Control Hazards, Exceptions, Parallelism via Instructions.			
	PART-A		
Q.No	**Questions**	**BT Level**	**Competence**
1	Express the truth table for AND gate and OR gate.	BTL 2	Understanding
2	Define hazard. Give an example for data hazard.	BTL 2	Understanding

3	Recall pipeline bubble.	BTL 1	Remembering
4	List the state elements needed to store and access an instruction.	BTL 1	Remembering
5	Describe the main idea of ILP.	BTL 2	Understanding
6	Distinguish the hazards with respect to processor function.	BTL 2	Understanding
7	Name the use of different logic gates.	BTL 1	Remembering
8	Evaluate branch taken and branch not taken in instruction execution.	BTL 5	Evaluating
9	State the ideal CPI of a pipelined processor.	BTL 1	Remembering
10	Design the instruction format for the jump instruction.	BTL 6	Creating
11	Classify the different types of hazards with examples.	BTL 4	Analyzing
12	Illustrate the two steps that are common to implement any type of instruction.	BTL 3	Applying
13	Assess the methods to reduce the pipeline stall.	BTL 5	Evaluating
14	Tabulate the use of branch prediction buffer.	BTL 1	Remembering
15	Show the 5 stages pipeline.	BTL 3	Applying
16	Point out the concept of exceptions. Give one example of MIPS exception.	BTL 4	Analyzing
17	What is pipelining?	BTL 1	Remember
18	Illustrate how to organize a multiple issue processor?	BTL 3	Applying
19	Neatly sketch three primary units of dynamically scheduled pipeline.	BTL 4	Analyzing
20	Generalize Exception. Give one example for MIPS exception.	BTL6	Creating
	PART-B		
1	Discuss the basics of logic design conventions. (13)	BTL 2	Understanding
2	i) State the MIPS implementation in detail with necessary multiplexers and control lines. (7) ii) Examine and draw a simple MIPS datapath with the control unit and the execution of ALU instructions. (6)	BTL 1	Remembering
3	i).Define parallelism and its types. (3) ii).List the main characteristics and limitations of Instruction level parallelism. (10)	BTL 1	Remembering
4	Design and develop an instruction pipeline working under various situations of pipeline stall. (13)	BTL 6	Creating
5	i).What is data hazard? (3) ii). Explain stalls with neat diagrams and suitable examples. (10)	BTL 1	Remembering
6	i).Summarize the speculation scheme. (3) ii).Distinguish static and dynamic techniques for speculation. (10)	BTL 2	Understanding
7	i).Differentiate sequential execution and pipelining. (3) ii). Explain the process of building single data path with neat diagram. (10)	BTL 4	Analyzing
8	Recommend the techniques for i).Dynamic branch prediction. (7) ii).Static branch prediction. (6)	BTL 5	Evaluating
9	Examine the approaches would you use to handle exceptions in MIPS. (13)	BTL 3	Applying
10	i).Analyze the hazards caused by unconditional branching statements and pipelining a processor using an example. (7) ii).Describe operand forwarding in a pipeline processor with a diagram. (6)	BTL 4	Analyzing

11	Express the simple data path with control unit and modified data path to accommodate pipelined executions with a diagram.	(13)	BTL 2	Understanding
12	With a suitable set of sequence of instructions show what happens when the branch is taken, assuming the pipeline is optimized for branches that are not taken and that we moved the branch execution to the ID stage.	(13)	BTL 3	Applying
13	i) Define multiple issue. ii) Differentiate static and dynamic multiple issues.	(3) (10)	BTL 1	Remembering
14	i).Explain single cycle and pipelined performance with examples. ii).Point out the advantages of pipeline over single cycle and limitations of pipelining a processor's datapath. Suggest the methods to overcome the later part	(7) (6)	BTL 4	Analyzing
	PART C			
1	Assume the following sequence of instructions are executed on a 5 stage pipelined processor Or r1,r2,r3 Or r2,r1,r4 Or r1,r1,r2 i) Indicate dependences and their type. ii) Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them. iii) Assume there is a full forwarding .Indicate hazard and add NOP instructions to eliminate them.	 (5) (5) (5)	BTL6	Creating

2	Consider the following code segment in C: A=b+e; c=b+f; Here is the generated MIPS code for this segment, assuming all variables are in memory and are addressable as off sets from $t0:
	lw $t1, 0($t0)
	lw $t2, 4($t0)
	add $t3, $t1, $t2
	sw $t3, 12($t0)
	lw $t4, 8($t0)
	add $t5, $t1, $t4
	sw $t5, 16($t0)
	Find the hazards in the preceding code segment and reorder the instructions to avoid any pipeline stalls.
		(15)	BTL 5	Evaluating

3	Consider the following loop: Loop: lw r1,0(r1) and r1,r1,r2 lw r1,0(r1) lw r1,0(r1) beq r1,r0,loop Assume that perfect branch prediction is used (no stalls) that there are no delay slots, and that the pipeline has full forwarding support. Also assume that many iterations of this loop are executed before the loop exits. i).Assess a pipeline execution diagram for the third iteration of this loop. ii).Show all instructions that are in the pipeline during these cycles (for all iterations).	 (8) (7)	BTL 5	Evaluating

4	Plan the pipelining in MIPS architecture and generate the exceptions handled in MIPS. (15)	BTL 6	Creating

UNIT IV- MEMORY AND I/O ORGANIZATION

Memory hierarchy, Memory Chip Organization, Cache memory, Virtual memory. Parallel Bus Architectures, Internal Communication Methodologies, Serial Bus Architectures, Mass storage, Input and Output Devices

PART-A

Q.No	Questions	BT Level	Competence
1	Distinguish the types of locality of references.	BTL 2	Understanding
2	Define the structure of memory hierarchy in a typical computer system and draw its diagram.	BTL 1	Remembering
3	Give how many total bits are required for a direct mapped cache with 16KB of data and 4-word blocks, assuming a 32 bit address.	BTL 2	Understanding
4	Compare and contrast SRAM and DRAM.	BTL 4	Analyzing
5	What is miss penalty?	BTL 1	Remembering
6	Describe Rotational Latency.	BTL 1	Remembering
7	State is direct-mapped cache.	BTL 1	Remembering
8	Evaluate Hit Ratios and Effective Access Times in cache	BTL 5	Evaluating
9	Formulate Fragmentation in virtual memory	BTL 6	Creating
10	Analyze the writing strategies in cache memory.	BTL 4	Analyzing
11	Integrate the functional steps required in an instruction cache miss.	BTL 6	Creating
12	State hit rate and miss rate.	BTL 1	Remembering
13	Summarize the various block placement schemes in cache memory.	BTL 2	Understanding
14	Identify the purpose of Dirty/Modified bit in Cache memory.	BTL 1	Remembering
15	Point out the use of parallel bus architecture?	BTL 4	Analyzing
16	Show the role of TLB in virtual memory.	BTL 3	Applying
17	Illustrate the advantages of virtual memory.	BTL 3	Applying
18	Assess the use of Overlays in memory.	BTL 5	Evaluating
19	Differentiate Paging and segmentation.	BTL 2	Understanding
20	Demonstrate the sequence of events involved in handling Direct Memory Access.	BTL 3	Applying

PART-B

1	i).Define parallelism and its types. (7) ii).List the main characteristics and limitations of Instruction level parallelism. (6)	BTL 1	Remembering
2	i).Define virtual memory and its importance. (7) ii).Examine TLB with necessary diagram .What is its use? (6)	BTL 2	Understanding
3	i).List the various memory technologies and examine its relevance in architecture design. (7) ii). Identify the characteristics of memory system. (6)	BTL 2	Understanding
4	Apply how Internal Communication Methodologies is useful in developing computer architecture. (13)	BTL 3	Applying
5	i).Demonstrate the DMA controller. Discuss how it improves the overall performance of the system. (7) ii).Illustrate how DMA controller is used for direct data transfer between memory and peripherals? (6)	BTL 1	Remembering

6	Point out the need for cache memory. Explain the following three mapping methods with examples. i). Direct. ii).Associative. iii).Set associative.	(13)	BTL 4	Analyzing
7	Evaluate the features of Bus Arbitration-Masters and Slaves.	(13)	BTL 5	Evaluating
8	Generalize the Bus Structure, Protocol, and Control in Parallel Bus Architecture	(13)	BTL 6	Creating
9	i).Classify the types of memory chip organization. ii).Analyze the advantages of cache and virtual memory	(7) (6)	BTL 4	Analyzing
10	Elaborate in detail about the following in Parallel Bus Architectures i). The Synchronous Bus ii). The Asynchronous Bus	(7) (6)	BTL 1	Remembering
11	i).Give the advantages of cache. ii).Identify the basic operations of cache in detail with diagram.	(6) (7)	BTL 4	Analyzing
12	Describe the principle approaches of Serial Bus Architectures with necessary diagrams.	(13)	BTL 1	Remembering
13	Illustrate the following in detail i). Magnetic Disks ii). Magnetic Tape iii). Optical Disks	 (5) (4) (4)	BTL 3	Applying
14	Discuss the following in detail i). Input Devices. ii). Output Devices.	 (7) (6)	BTL 2	Understanding

PART C

1	Generalize the merits and demerits of Parallel Bus Architectures, Bridge-Based Bus Architectures and Serial Bus Architectures.	(15)	BTL 6	Creating
2	For a direct mapped cache design with a 32 bit address, the following bits of the address are used to access the cache. Tag : 31-10 Index: 9-5 Offset: 4-0 i). Judge what is the cache block size? ii).Decide how many entries does the cache have? iii).Assess what is the ratio between total bits required for such a cache implementation over the data storage bits?	 (5) (5) (5)	BTL 5	Evaluating
3	Develop methods to constructing large RAMS from small RAMS and commercial memory modules	(15)	BTL 6	Creating
4	Summarize the virtual memory organization followed in digital computers.	(15)	BTL 5	Evaluating

UNIT V- ADVANCED COMPUTER ARCHITECTURE

Parallel processing architectures and challenges, Hardware multithreading, Multicore and shared memory multiprocessors, Introduction to Graphics Processing Units, Clusters and Warehouse scale computers - Introduction to Multiprocessor network topologies.

PART-A

Q.No	Questions	BT Level	Competence
1	Describe the main idea of Parallel processing architectures.	BTL 2	Understanding
2	Illustrate how to organize a clusters.	BTL 3	Applying
3	List the network topologies in parallel processor.	BTL 1	Remembering

4	Analyze the main characteristics of SMT processor.	BTL 4	Analyzing
5	Quote the importance of Graphics Processing Units.	BTL 1	Remembering
6	Define multicore microprocessor.	BTL 1	Remembering
7	Express Warehouse scale computers.	BTL 2	Understanding
8	State the overall speedup if a webserver is to be enhanced with a new CPU which is 10 times faster on computation than an old CPU .The original CPU spent 40% of its time processing and 60% of its time waiting for I/O.	BTL 1	Remembering
9	Differentiate between SIMD and MIMD.	BTL 2	Understanding
10	Show the performance of cluster organization.	BTL 3	Applying
11	Compare SMT and hardware multithreading.	BTL 5	Evaluating
12	Identify the Flynn classification and give an example for each class in Flynn's classification.	BTL 1	Remembering
13	Integrate the ideas of multistage network and cross bar network.	BTL 6	Creating
14	Discriminate UMA and NUMA.	BTL 5	Evaluating
15	Describe fine grained multithreading.	BTL 1	Remembering
16	Express the need for instruction level parallelism.	BTL 2	Understanding
17	Formulate the various approaches to hardware multithreading.	BTL 6	Creating
18	Categorize the various multithreading options.	BTL 4	Analyzing
19	Compare fine grained multithreading and coarse grained multithreading.	BTL 4	Analyzing
20	Classify shared memory multiprocessor based on the memory access latency.	BTL 3	Applying
	PART-B		
1	i).Define parallelism and its types. (4) ii).List the main characteristics and limitations of Instruction level parallelism. (9)	BTL 1	Remembering
2	i).Give the software and hardware techniques to achieve Instruction level parallelism. (4) ii).Summarize the facts or challenges faced by parallel processing in enhancing computer architecture. (9)	BTL 2	Understanding
3	Express in detail about hardware multithreading. (13)	BTL 2	Understanding
4	Apply your knowledge on graphics processing units and explain how it helps computer to improve processor performance. (13)	BTL 3	Applying
5	Describe data level parallelism in i).SIMD. (6) ii).MISD. (7)	BTL 1	Remembering
6	i).Point out how will you classify shared memory multi-processor based on memory access latency. (7) ii).Compare and contrast Fine grained, Coarse grained multithreading and Simultaneous Multithreading. (8)	BTL 4	Analyzing
7	Evaluate the features of Multicore processors. (13)	BTL 5	Evaluating
8	i).Classify the types of multithreading. (9) ii).Analyze the advantages in multithreading. (4)	BTL 4	Analyzing
9	Formulate the classes in Flynn's Taxonomy of computer Architecture classification with example. (13)	BTL 6	Creating
10	Elaborate in detail about the following		

	i).SISD. (8) ii).MIMD (5)		BTL 1	Remembering
11	Explain simultaneous Multithreading with example.	(13)	BTL 4	Analyzing
12	Describe the four principle approaches to multithreading with necessary diagrams.	(13)	BTL 1	Remembering
13	Illustrate the following in detail i). Clusters (7) ii). Wharehouse scale computers (6)		BTL 3	Applying
14	Discuss the multiprocessor network topologies in detail.	(13)	BTL 2	Understanding
	PART C			

1	Evaluate the below C code using MIMD and SIMD machine as efficient as possible:
	For(i=0;i<2000;i++)
	For(j=0;j<3000;j++)
	X_array[i][j]=y_array[j][i]+200;
		(15)	BTL 5	Evaluating

2	Write down a list of your daily activities that you typically do on a weekday. For instance get out of bed, take a shower, get dressed, eat breakfast, brush your teeth, dry your hair etc (minimum ten activities). Which of these activities can be done in form of parallelism. For each activity discuss if they are working in parallel, but if not, why they are not. Estimate how much shorter time it will take to complete all the activities if it is done in parallel.	(15)	BTL 6	Creating
3	Consider the following portions of two different programs running at the same time on four processors in a symmetric multicore processor (SMP). Assume that before this code is run, both x and y are 0? Core 1: x=2; Core 2: y=2; Core 3: w= x + y +1; Core 4: z= x + y; i. What if all the possible resulting values of w,x,y,z ? For each possible outcomes, explain how we might arrive at those values. (8) ii. Develop the execution more deterministic so that only one set of values is possible? (7)		BTL 6	Creating
4	Summarize the merits and demerits of clusters and warehouse scales computer.	(15)	BTL 5	Evaluating