Microprocessor and microcontrollers

2 Marks – Question & Answers

Unit-I (8086)

1. **What are the modes in which 8086 can operate?**

   The 8086 can operate in two modes and they are minimum (or uniprocessor) mode and maximum (or multiprocessor) mode.

2. **What are the hardware interrupts of 8086?**

   The interrupts of 8085 are INTR and NMI. The INTR is general maskable interruput and NMI is non-maskable interrupt.

3. **How clock signal is generated in 8086? What is the maximum internal clock frequency of 8086?**

   The 8086 does not have on-chip clock generation circuit. Hence the clock generator chip, 8284 is connected to the CLK pin of8086. The clock signal supplied by 8284 is divided by three for internal use. The maximum internal clock frequency of8086 is 5MHz.

4. **What is pipelined architecture?**

   In pipelined architecture the processor will have number of functional units and the execution time of functional units is overlapped. Each functional unit works independently most of the time.

5. **What are the functional units available in 8086 architecture?**

   The bus interface unit (BIU) and execution unit (EU) are the two functional units available in 8086 processor.

6. **List the segment registers of 8086.**

   The segment registers of 8086 are, Code segment (CS), Data segment (DS), Stack segment (SS) and Extra segment (ES) registers.

7. **What is the difference between segment register and general purpose register?**

   The segment registers are used to store 16 bit segment base address of the four memory segments. The general purpose registers are used as the source or destination register during data transfer and computation, as pointers to memory and as counters.

8. **What is queue? How queue is implemented in 8086?**

   A data structure which can be accessed on the basis of first in first out is called queue. The 8086 has six numbers of 8-bit FIFO registers, which is used for instruction queue.

9. Write the special functions carried by the general purpose registers of 8086.

The special functions carried by the registers of 8086 are the following.

Register	Special function
AX	16-bit Accumulator
AL	8-bit Accumulator
BX	Base Register
CX	Count Register
DX	Data Register

10. Write the flags of 8086.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	O	D	I	T	S	Z	-	Ac	-	P	-	Cy

The 8086 has nine flags and they are

1. Carry Flag (CF)
2. Parity Flag (PF)
3. Auxiliary carry Flag (AF)
4. Zero Flag (ZF)
5. Sign Flag (SF)
6. Overflow Flag (OF)
7. Trace Flag (TF)
8. Interrupt Flag (IF)
9. Direction Flag (DF)

11. What are control bits?

The flags TF, IF and DF of 8086 are used to control the processor operation and so they are called control bits.

12. Describe the difference between the instructions MOV AX, 2437H and MOV AX,[2437H].

Difference between the instructions MOV AX, 2437H and MOV AX,[2437H] are former instruction takes 2437 as 16-bit data and latter instruction takes 2437 as 16-bit address.

13. State the function of Direction flag in 8086.

Direction flag is used with string instructions. If DF= 0, the string is processed from its beginning with the first element having the lowest address. Otherwise, the string is processed from the high address towards the low address.

14. What happens in 8086 processor, when

a. overflow of sum occurs during addition of signed numbers. *(Ans: Ov Flag is Set)*
b. overflow of quotient occurs during division operation. *(Ans: type0-divide by zero interrupt is generated).*

15. In 8086 processor the code segment contains 4000H and instruction pointer contains 9F20H. Find the memory location addressed by the processor.

Segment address 4000	-	0100 0000 0000 0000	
Shifted to left by four bits	-	0100 0000 0000 0000 0000	
(+) Offset address	-	1001 1111 0010 0000	

Physical address -	-	0100 1001 1111 0010 0000	= $49F20_H$

∴The Calculated Physical address = $49F20_H$

16. Discuss the functions of the following prefixes: LOCK, ESCAPE

LOCK :

In a multiprocessor system each microprocessor has its own local buses and memory. The individual microprocessors are connected together by a system bus so that each can access system resources such as disk drives or memory. Each microprocessor only takes control of the system bus when it needs to access some system resources.

The LOCK prefix allows a microprocessor to make sure that another processor does not take control of the system bus while it is in the middle of a critical instruction which uses the system bus.

ESCAPE:

This instruction is used to pass instructions to a coprocessor such as the 8087 math coprocessor which shares the address and data bus with an 8086.

17. What are the flag manipulation instructions of 8086?

LAHF : Load AH from low byte of flag register.
SAHF : Store AH to low byte of flag register
PUSHF : Push content of flag to the stack.
POPF : Pop content of stack and load it in the flag register.

18.Give the contents of the flag register after execution of following addition.

```
   0110 0101 1101 0001
+  0010 0011 0101 1001
   -------------------
   1000 1001 0010 1010
   -------------------
```

SF = 1, ZF = 0, PF = 1, CF = 0, AF = 0, OF=1.

19. What are the three groups of signals in 8086?

The 8086 signals are categorized in three groups. They are :
i. The signals having common function in minimum and maximum mode.
ii. The signals having special functions for minimum mode,
iii. The signals having special functions for maximum mode.

20. What are the uses of AD0 – AD15 lines?

These are the time multiplexed memory 15 address and data lines. Address remains on the line during T I state ,while data is available on the data bus during T2, T3, TW and T4. Here T1, T2, T3, T4 and Tw are the clock states of a machine cycle. Tw is a wait state. These lines are active high and float to a tristate during interrupt acknowledge and local bus hold acknowledge cycles.

21. What is the operation of RD signal?

Read signal RD when low, indicates the peripherals that the processor is performing a memory (or) I/O read operation.

22. What is the function of READY signal?

This is the acknowledgment from the slow devices (or) memory that they have completed the data transfer. The signal made available by the devices is synchronized by the 8284A clock generator to provide ready input to the 8086. The signal is active high.

23.What is the function of INTR signal?

INTR- Interrupt Request: This is a level triggered input. This is sampled during the last clock cycle of each instruction to determine the availability of the request, If any interrupt request is pending, the processor enters the interrupt acknowledge cycle. This can be internally masked by resetting he interrupt enable flag. This signal is active high and 1ternally synchronized.

24. What is the operation performed when TEST input pin is low?

If the TEST input goes low, execution will continue, else, the processor remains in an idle state. The input is synchronized internally during each clock cycle on leading edge of clock.

25. What is the purpose of ALE signal in minimum mode?

ALE -Address Latch Enable: This output signal indicates the availability of the valid address on the address / data lines, and is connected to latch enable input of latches. This signal is active high and is never tristated.

26. What is the function of RESET pin?

RESET input causes the processor to terminate the current activity and start execution from FFFFOH. This signal is active high and must be active for at least four clock cycles. It restarts execution when the RESET return low. RESET is also internally synchronized.

27. What is the function of DEN signal in minimum mode?

This signal indicates the availability of valid data over the address / data lines. It is used to enable the Transceivers to separate the data from the multiplexed address / data signal. It is active from the middle of T2 until the middle of T4 DEN is tristated during hold acknowledge cycle.

28. What is the significance of $\overline{MX}$/MN pin in 8086?

The above said pin is used for selecting the mode of the operation of the processor. HIGH in that pin declares that the system comprises of uni-processor (Minimum Mode) and LOW declares that the system comprises of multi-processor (Maximum Mode).

29. What are the differences between maximum mode and minimum mode?

	Minimum mode	Maximum mode
1	A processor is in minimum mode when MN /MX pin is strapped to +5v	A processor is in maximum mode when MN /MX is grounded
2.	All control signals are given out by. microprocessor chip it self	The processor derive the status signals S2, Sl and So. Another chip called bus controller derives control signals using this status information
3.	There is a single micro processor	There may be more than one microprocessor

30. What is multi micro-processor architecture?

The maximum clock frequency at which a system operate may be considered as one of the measure of the processor capability of the system. An appropriate system involving several microprocessors connected using a certain topology may provide high processing capacity. The study of such a system known as multi micro processor architecture.

31. What is meant by numeric processor?

The numeric processor 8087 is a coprocessor which has been designed to work under the control of the processor 8086 and offer it additional numeric processing capabilities.

32. Explain the tightly coupled (closely coupled) system.

In a tightly coupled system, the microprocessor (either coprocessor or independent processors) may share a common clock & bus control logic The two processors in a closely coupled system may communicate using a common system bus or common memory The microprocessor in a closely coupled system either uses a status bit in memory / interrupt the host to inform it about the completion of the task allotted to it.

33. Explain the loosely coupled multiprocessor system.

In a loosely coupled multiprocessor system, each CPU may have its own bus control logic. The bus arbitration is handled by an external circuit. The loosely coupled system configurations like LAN and WAN can be spreaded over a large area.

34. Give the advantage of loosely coupled system over the tightly coupled system.

The loosely coupled system has the following advantage over the tightly coupled system,

- More number of CPUs can be added in a loosely coupled system to improve the system performance.
- The system structure is modular and hence easy to maintain and troubleshoot.
- A fault in a single module does not lead to a complete system breakdown.
- Due to the independent processing modules used in the system, it is more fault -tolerant.
- More suitable to parallel applications due to its modular organization.

8255 – PROGRAMMABLE PERIPHERAL INTERFACE (PPI)

1. What is a programmable peripheral device?

If the functions performed by a peripheral device can be altered or changed by a program instruction then the peripheral device is called programmable device. Usually the programmable devices will have control registers. The device can be programmed by sending control word in the prescribed format to the control register.

2. What is the need for a Port?

The I/O devices are generally slow devices and their timing characteristics do not match with processor timings. Hence the I/O devices are connected to system bus through the ports.

3. What is handshake port?
Explain the working of a handshake input port and output port.

In handshake port, signals are exchanged between I/O device and port or between port and processor for checking or informing various condition of the device.

In handshake input operation, the input device will check whether the port is empty or not. If the port is empty, then the data is loaded into the port. When the port receives the data, it will inform the processor for read operation. Once the data have been read by the processor, the port will signal the input device that it is empty. Now the input device can load another data to port and the above process is repeated.

In handshake output operation, the processor will load a data to port. When the port receives the data, it will inform the output device to collect the data. Once the output device accepts the data, the port will inform the processor that it is empty. Now the processor can load another data to port and the above process is repeated.

4. What are the internal devices of 8255?

The internal devices of 8255 are port-A, port-B, port-C and Control register.
The ports can be programmed for either input or output function in different operating modes.

5. What are the operating modes of port -A 8255?

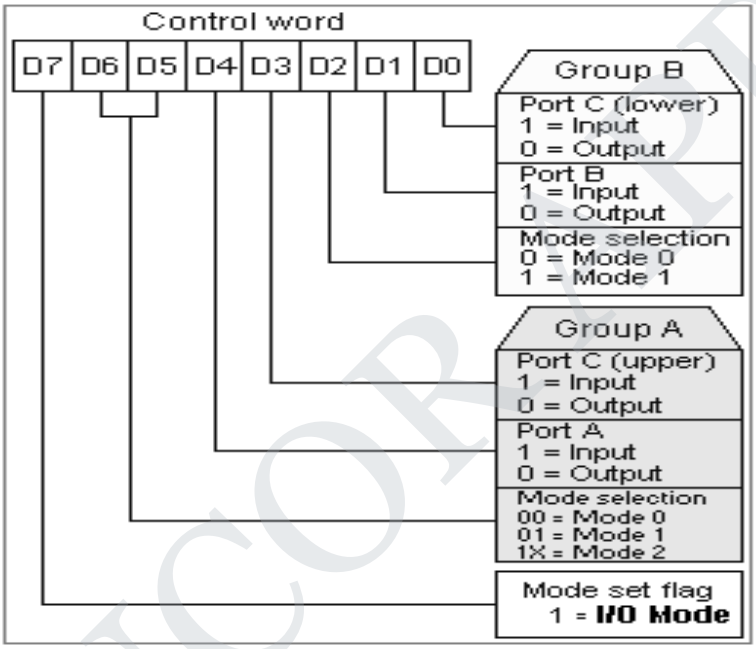
The port-A of 8255 can be programmed to work in anyone of the following operating modes as input or output port.

Mode-0 : Simple 1/0 port.
Mode-l : Handshake 1/0 port
Mode-2 : Bidirectional 1/0 port

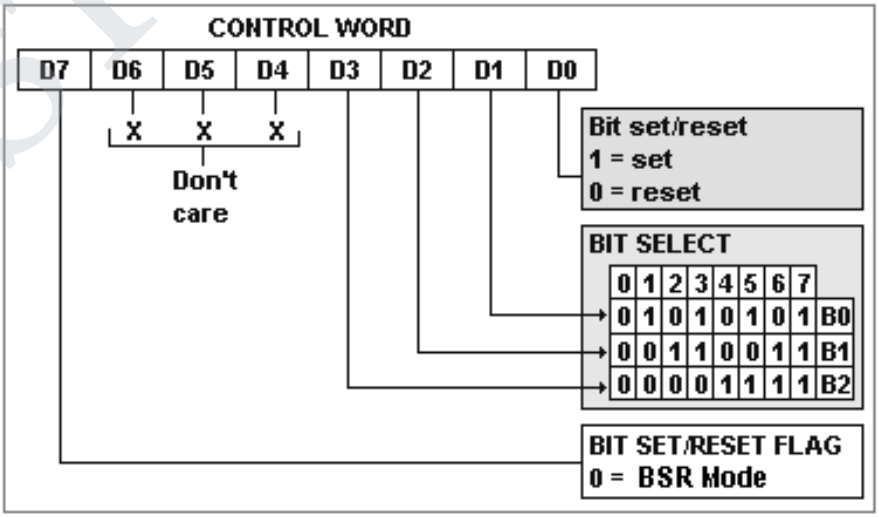
6. What are the functions performed by port-C of 8255?

1. The port-C pins are used for handshake signals.
2. Port-C can be used as an 8-bit parallel 1/0 port in mode-0.
3. It can be used as two numbers of 4-bit parallel port in mode-0.
4. The individual pins of port-C can be set or reset for various control applications.

7. Draw the control word format for I/O mode.



8. Draw the control word format for BSR (Bit Set Reset) Mode.



8251 – USART:

9. What is baud rate?

The baud rate is the rate at which the serial data is transmitted (expressed as bits per second).

Baud rate is also defined as l/(Tb - time period for a symbol). In some systems, one data bit may be represented through one symbol. Then, on such occasions, the baud rate and bits/sec are same.

10. What is USART? What are the functions performed by INTEL 8251A?

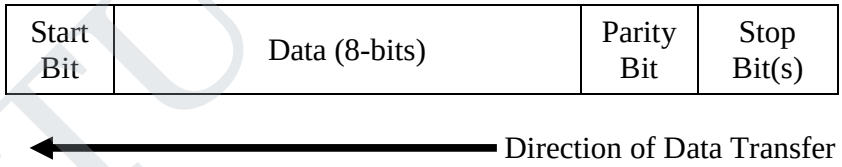
The device which can be programmed to perform Synchronous or Asynchronous serial communication is called USART (Universal Synchronous Asynchronous Receiver Transmitter). The INTEL 8251A is an example of USART.

The INTEL 825lA is used for serial data transmission or reception either asynchronously or synchronously. The 8251A can be used to interface MODEM for serial communication through telephone lines.

11. What is asynchronous data transfer scheme?

In asynchronous data transfer scheme, first the processor sends a request to the device for read/write operation. Then the processor keeps on polling the status of the device. Once the device is ready, the processor executes a data transfer instruction to complete the process.

The frame format in Asynchronous data transfer is given below.



12. What is synchronous data transfer scheme?

For synchronous data transfer scheme, the processor does not check the readiness of the device after a command has been issued for read/write operation. In this scheme, the processor will request the device to get ready and then read/write to the device immediately after the request. In some synchronous schemes a small delay is allowed after the request.

Data is sent continuously in blocks either without any time interval or in fixed time intervals.

13. What are the control words of 8251A and what are its functions?

The control words of 8251A are Mode word and Command word. The mode word informs 8251 about the baud rate, character length, parity and stop bits. The command word can be send to enable the data transmission and reception.

14. What are the functions performed by INTEL 8251A?

The INTEL 825lA is used for converting parallel data to serial or vice versa. The data transmission or reception can be either asynchronously or synchronously. The 8251A can be used to interface MODEM and establish serial communication through MODEM over telephone lines.

15. What is the information that can be obtained from the status word of 8251?

The status word can be read by the CPU to check the readiness of the transmitter or receiver and to check the character synchronization in synchronous reception. It also provides information regarding various errors in the data received. The various error conditions that can be checked from the status word are parity error, overrun error and framing error.

16. What are the different types of errors that can occur in asynchronous serial communication?

1. Framming Error
2. Over run Error
3. Parity Error

17. What is the significance of $\overline{C/D}$ signal in 8251?

This pin is used to select either Control register for configuring or Data bus buffer for read / write operations.

8279 – KEYBOARD & DISPLAY CONTROLLER:

18. What are the different scan modes of 8279?

The different scan modes of 8279 are Decoded scan and Encoded scan.

In decoded scan mode, the output of scan lines will be similar to a 2-to-4 decoder.

In encoded scan mode, the output of scan lines will be binary count, and so an external decoder should be used to convert the binary count to decoded output.

19. What is debouncing?

When a key is pressed, it bounces after a short time. If a key code is generated immediately after sensing a key actuation, then the processor will generate the same keycode a number of times. (A key typically bounces for 10 to 20 msec). Hence the processor has to wait for the key bounces to settle before reading the keycode. This process is called keyboard debouncing.

20. What is the difference in programming the 8279 for encoded scan and decoded scan?

If the 8279 is programmed for decoded scan then the output of scan lines will be decoded output and if it is programmed for, encoded scan then the output of scan lines will be binary count. In encoded mode, an external decoder should be used to decode the scan lines.

21. What is scanning in keyboard and what is scan time?

The process of sending a zero to each row of a keyboard matrix and reading the columns for key actuation is called scanning. The scan time is the time taken by the processor to scan all the rows one by one starting from first row and coming back to the first row again.

22. What are the tasks involved in keyboard interface?

The tasks involved in keyboard interfacing are sensing a key actuation, debouncing the key and generating key codes (Decoding the key). These tasks are performed by software if the keyboard is interfaced through ports and they are performed by hardware if the keyboard is interfaced through 8279.

23. How a keyboard matrix is formed in keyboard interface using 8279?

The return lines, RLo to RL7 of 8279 are used to form the columns of keyboard matrix. In decoded scan the scan lines SLo to SL3 of 8279 are used to form the rows of keyboard matrix. In encoded scan mode, the output lines of external decoder are used as rows of keyboard matrix.

24. What is scanning in display and what is the scan time?

In display devices, the process of sending display codes to 7 –segment LEDs to display the LEDs one by one is called scanning (or multiplexed display). The scan time is the time taken to display all the 7-segment LEDs one by one, starting from first LED and coming back to the first LED again.

25. What is meant by 2-key lockout and N-key rollover?

2-Key Lockout: When two keys are pressed simultaneously, one key pressed first will be recognized and code will be generated.

N-Key Rollover: When a key is pressed continuously, the same key will be recognized several times, after each debounce.

26. List the functions performed by 8279.

a. Keyboard scanning.
b. Keyboard debouncing.
c. Keycode generation.
d. Intimating key pressing to CPU through Interrupt.
e. Storing display codes.
f. Output display codes to LED/LCDs.
g. Display refreshing.

ADC / DAC:

27. What are the different types of ADC?

The different types of ADC are successive approximation ADC, counter type ADC flash type ADC, integrator converters and voltage-to-frequency converters.

28. What is settling or conversion time in DAC?

The time taken by the DAC to convert a given digital data to corresponding analog signal is called conversion time.

29. What is most commonly employed circuit in DAC?

The most commonly employed circuit in DAC is R/2R ladder network.

30. What are the internal devices of typical DAC?

The internal devices of DAC are R/2R ladder network, an internal latch and Current to Voltage converting amplifier.

31. What is the significance of address bus A0, A1 & A2 in ADC?

The analog input voltage may be taken for conversion into digital output from eight input channels. A particular input channel is selected by providing appropriate signals in the three address buses, A0, A1 & A2.

SERIAL COMMUNICATION STANDARDS:

32. What is RS-232C Standard?

The RS232C is a serial bus consisting of a maximum of 25 signals, which are standardized by EIA (Electronic Industry Association). The first 9 signals are sufficient for most of the serial data transmission.

33. What is the voltage level used in RS232C standard?

The voltage levels are

Logic LOW (0) : –3V to –15V

Logic HIGH (1) : +3V to +15V

Commonly used voltage levels are +12V (logic HIGH) and –12V (logic LOW).

34. What is the importance of Level converters?

The RS-232C signal levels are not compatible with TTL logic levels. Hence for interfacing TTL devices, level converters or RS-232C line drivers are employed. The popularly used level converters are

- **MCI488** - TTL to RS232C level converter
- **MCI489** - RS232C to TTL level converter
- **MAX 232** - Bi-directional level converter.

(Max 232 is equivalent to a combination of MC1488 and MC1489 in single IC)

35. What are two important lines in I2C Standard?

a) SDA

b) SCA

Unit – IV

1. What is mean by microcontroller?

A device which contains the microprocessor with integrated peripherals like memory, serial ports, parallel ports, timer/counter, interrupt controller, data acquisition interfaces like ADC, DAC is called microcontroller.

CPU	ROM	RAM
Timers	I/O Ports	Serial Port

Internal blocks of Microcontroller

2. Explain DJNZ instructions of intel 8051 microcontroller?

a. DJNZ Rn, rel - Decrement the content of the register Rn and jump if not zero.
b. DJNZ direct , rel - Decrement the content of direct 8-bit address and jump if not zero.

3. Explain the contents of the accumulator after the execution of the following program segments:
MOV A,#3CH
MOV R4,#66H
ANL A,R4
A -> 3C
R4 -> 66
A -> 24

4. State the function of RS1 and RS0 bits in the flag register of Intel 8051 microcontroller?

RS1 , RS0 – Register bank select bits

RS1	RS0	Bank Selection
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

5. Write a program using 8051 assembly language to change the data 55H stored in the lower byte of the data pointer register to AAH using rotate instruction.

```
        MOV DPL, #55H
        MOV A, DPL
        RL A
Label : SJMP Label
```

6. Give the alternate functions for the port pins of port3?
RD WR T1 T0 INT1 INT0 TXD RXD
RD – Read data control output.
WR – Write data control output.

T1 – Timer / Counter1 external input or test pin.
T0 – Timer / Counter0 external input or test pin.
INT1- Interrupt 1 input pin.
INT 0 – Interrupt 0 input pin.
TXD – Transmit data pin for serial port in UART mode.
RXD - Receive data pin for serial port in UART mode.

7. Specify the single instruction, which clears the most significant bit of B register of 8051, without affecting the remaining bits.
Single instruction, which clears the most significant bit of B register of 8051, without affecting the remaining bits is CLR B.7.

8. Explain the function of the pins PSEN and EA of 8051.
PSEN: PSEN stands for program store enable. In 8051 based system in which an external ROM holds the program code, this pin is connected to the OE pin of the ROM.
EA: EA stands for external access. When the EA pin is connected to Vcc, program fetched to addresses 0000H through 0FFFH are directed to the internal ROM and program fetches to addresses 1000H through FFFFH are directed to external ROM/EPROM. When the EA pin is grounded, all addresses fetched by program are directed to the external ROM/EPROM.

9. Explain the 16-bit registers DPTR and SP of 8051.
DPTR: DPTR stands for data pointer. DPTR consists of a high byte (DPH) and a low byte (DPL). Its function is to hold a 16-bit address. It may be manipulated as a 16-bit data register or as two independent 8-bit registers. It serves as a base register in indirect jumps, lookup table instructions and external data transfer.
SP: SP stands for stack pointer. SP is a 8- bit wide register. It is incremented before data is stored during PUSH and CALL instructions. The stack array can reside anywhere in on-chip RAM. The stack pointer is initialized to 07H after a reset. This causes the stack to begin at location 08H.

10. Name the special functions registers available in 8051.
a. Accumulator
b. B Register
c. Program Status Word.
d. Stack Pointer.
e. Data Pointer.
f. Port 0
g. Port 1
h. Port 2
i. Port 3
j. Interrupt priority control register.
k. Interrupt enable control register.

11. Write down the different operating modes for serial communication of 8051.
Serial communication of 8051 operate under four modes. They are mode 0 , mode 1, mode 2 and mode3 .SM0 and SM1 bits of SCON register specifies the mode.

SM0	SM1	Mode	
0	0	0	Baud rate fixed.
0	1	1	8-bit data, 1 stop bit, 1 start bit. Baud rate variable.
1	0	2	8-bit data, 9th programmable bit,1 stop bit, 1 start bit, Baud rate fixed.
1	1	3	8-bit data, 9th programmable bit,1 stop bit, 1 start bit, Baud rate variable.

12. Explain the register IE format of 8051.

EA	-	ET2	ES	ET1	EX1	ET0	EX0

EA- Enable all control bit.
ET2- Timer 2 interrupt enable bit.
ES – Enable serial port control bit.
ET1 – Enable Timer1 control bit.
EX1- Enable external interrupt1 control bit.
ET0 – Enable Timer0 control bit.
EX0- Enable external interrupt0 control bit.

13. Compare Microprocessor and Microcontroller.

Sl. No	Microprocessor	Microcontroller
1	Microprocessor contains ALU,general purpose registers,stack pointer, program counter, clock timing circuit and interrupt circuit.	Microcontroller contains the circuitry of microprocessor and in addition it has built- in ROM, RAM, I/O devices, timers and counters.
2	It has many instructions to move data between memory and CPU.	It has one or two instructions to move data between memory and CPU.
3	It has one or two bit handling instructions.	It has many bit handling instructions.
4	Access times for memory and I/O devices are more.	Less access times for built-in memory and I/O devices.
5	Microprocessor based system requires more hardware.	Microcontroller based system requires less hardware reducing PCB size and increasing the reliability.

14. Name the five interrupt sources of 8051?
The interrupts are:

		Vector address
• External interrupt 0	: IE0 :	0003H
• Timer interrupt 0	: TF0 :	000BH
• External interrupt 1	: IE1 :	0013H
• Timer Interrupt 1	: TF1 :	001BH
• Serial Interrupt		
Receive interrupt : RI	:	0023H
Transmit interrupt: TI	:	0023H

15. Write a program to load accumulator A, DPH and DPL with 30H.
MOV A,#30
MOV DPH,A
MOV DPL,A

16. Write a program to subtract the contents of R1 of Bank0 from the contents of R0 of Bank2.
MOV PSW, #10
MOV A, R0
MOV PSW, #00
SUBB A, R1

17. How the RS -232C serial bus is interfaced to TTL logic device?
The RS-232C signal voltage levels are not compatible with TTL logic levels. Hence for interfacing TTL devices to RS-232C serial bus, level converters are used. The popularly used level converters are MC 1488 & MC 1489 or MAX 232.

18. List some of the features of 8096 microcontroller.
a. The 8096 is a 16-bit microcontroller.
b. The 8096 is designed to use in applications which require high speed calculations and fast I/O operations.
c. The high speed I/O section of an 8096 includes a 16 bit timer, a 16 bit counter, a 4 input programmable edge detector, 4 software timers and a 6-output programmable event generator.
d. It has 100 instructions, which can operate on bit, byte, word, double words.
e. The bit operations are possible and these can be performed on any bit in the register file or in the special function register.

19. What is HS0 of 8096?
HS0:
The High Speed Output unit (HS0) is used to trigger events at specific times with minimal CUP overhead. These events include : starting an A to D conversion, resetting Timer2, setting 4 software flags, and switching up to 6 output lines.

20. List the features of 8051 microcontroller?
The features are
*single_supply +5 volt operation using HMOS technology.
*4096 bytes program memory on chip(not on 8031)
*128 data memory on chip.

*Four register banks.
*Two multiple mode,16-bit timer/counter.
*Extensive boolean processing capabilities.
*64 KB external RAM size
*32 bidirectional individually addressible I/O lines.
*8 bit CPU optimized for control applications.

21 .Explain the operating mode0 of 8051 serial ports?
In this mode serial enters &exits through RXD, TXD outputs the shift clock.8 bits are transmitted/received: 8 data bits(LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

22. Explain the operating mode2 of 8051 serial ports?
In this mode 11 bits are transmitted(through TXD)or received (through RXD):a start bit(0), 8 data bits(LSB first),a programmable 9th data bit ,& a stop bit(1).ON transmit the 9th data bit (TB* in SCON) can be assigned the value of 0 or 1.
For eg:, the parity bit(P, in the PSW) could be moved into TB8.On receive the 9th data bit go in to the RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32or1/64 the oscillator frequency.

23. Write a program to perform multiplication of 2 nos using 8051?
MOV A, #data 1
MOV B, #data 2
MUL AB
MOV DPTR, #5000
MOV @DPTR, A (lower value)
INC DPTR
MOV A,B
MOVX @ DPTR,A

24. Write a program to mask the 0th &7th bit using 8051?

```
        MOV A, #data
        ANL A, #81
        MOV DPTR, #4500
        MOVX @DPTR, A
LOOP:SJMP LOOP
```

25. Write about CALL statement in 8051?
There are two subroutine CALL instructions. They are
*LCALL(Long CALL)
*ACALL(Absolute CALL)
Each increments the PC to the 1st byte of the instruction & pushes them in to the stack.

26. Write about the jump statement?
There are three forms of jump. They are
LJMP(Long jump)-address 16
AJMP(Absolute Jump)-address 11
SJMP(Short Jump)-relative address

27. Write program to load accumulator, DPH & DPL using 8051?
MOV A, #30

MOV DPH, A
MOV DPL, A

28. Write a program to find the 2's complement using 8051?
MOV A, R0
CPL A
INC A

29. Write a program to add 2 8-bit numbers using 8051?
MOV A, #30H
ADD A, #50H

30. Write a program to swap two numbers using 8051?
MOV A, #data
SWAP A

31. Write a program to subtract 2 8-bit numbers & exchange the digits using 8051?
MOV A, #9F
MOV R0, #40
SUBB A, R0
SWAP A

32. Write a program to subtract the contents of R1 of Bank0 from the contents of R0 of Bank2 using 8051?
MOV PSW, #10
MOV A, R0
MOV PSW, #00
SUBB A, R1

33. What is an Interrupt?
Interrupt is a signal send by an external device to the processor so as to request the processor to perform a particular task or work.

34. What is program counter? How is it useful in program execution?
The program counter keeps track of program execution. To execute a program the starting address of the program is loaded in program counter. The PC sends out an address to fetch a byte of instruction from memory and increments its content automatically.

35. Define stack.
Stack is a sequence of RAM memory locations defined by the programmer.

UNIT - I

1.With neat sketch explain the architecture of 8086 processor.
-Block Diagram
-Explanation about all blocks in the block diagram

2.Draw the Pin Diagram of 8086 and explain the function of various signals.
-Pin Diagram
-Explanation about all signals

3.List the various Instruction available in 8086 processor.
-Data Transfer Instructions
-Arithmetic Instructions
-Bit Manipulation Instructions
-String Instructions
-Program Execution Transfer Instructions
-Processor Control Instructions

4. Describe the interrupt system of 8086 processor.

5. Explain the addressing modes of 8086 processor.

6.With neat sketch explain the architecture of 8086 in minimum mode.
-Block Diagram
-Explanation about all blocks in the block diagram

7.With neat sketch explain the architecture of 8086 in maximum mode.
-Block Diagram
-Explanation about all blocks in the block diagram

8. With neat sketch explain the architecture of 8087 coprocessor.
-Block Diagram
-Explanation about all blocks in the block diagram

9.With neat sketch explain the architecture of 8089 I/O processor.
-Block Diagram
-Explanation about all blocks in the block diagram

10.With neat sketch explain the multiprocessor configurations.
-Explanation about all Configurations
-Loosely Coupled and Tightly Coupled

1.With neat sketch explain the functions of 8255 PPI.
-Block Diagram
-Explanation about all the ports available.
-Explanation about the modes of transfer
-Explain the control Word Register

2. With neat sketch explain the functions of 8251.
-Block Diagram
-Types of data transfer
-Explanation about all the blocks.
-Explain the control Word Register, Status Register

3. With neat sketch explain the function of DMA contoller.
-Block Diagram
-Explanation about all blocks in the block diagram

4.With neat sketch explain the function of Programmable Interrupt Controller.
-Block Diagram
-Explanation about all blocks in the block diagram

5.With neat sketch explain the function of Keyboard and display controller.
-Block Diagram
-Types of Display Available
-Types of keys available
-Explanation about all blocks in the block diagram

6.With neat sketch explain the function of A/D converter.
-Fundamental steps
-Figure
-Explain the functions.

7.With neat sketch explain the function of D/A converter.
-Fundamental steps
-Figure
-Explain the functions.

UNIT – IV

1.With neat sketch explain the architecture of 8051 microcontroller.
-Block Diagram
-Explanation about all blocks in the block diagram

2.Draw the Pin Diagram of 8051 and explain the function of various signals.
-Pin Diagram
-Explanation about all signals

3.List the various Instruction available in 8051 microcontroller.
-Data Transfer Instructions
-Arithmetic Instructions
-Logical Instructions
-Boolean variable Manipulation Instructions
-Program and Machine Control Instructions

4. With neat sketch explain the architecture of 8096 microcontroller.
-Block Diagram
-Explanation about all blocks in the block diagram

5.Draw the Pin Diagram of 8096 and explain the function of various signals.
-Pin Diagram
-Explanation about all signals