ST.ANNE'S

COLLEGE OF ENGINEERING AND TECHNOLOGY
(Approved by AICTE, New Delhi. Affiliated to Anna University, Chennai)
(An ISO 9001: 2015 Certified Institution)
ANGUCHETTYPALAYAM, PANRUTI – 607 106.

QUESTION BANK

PERIOD : JULY - NOV 2019 **BATCH**: 2018 – 2022

BRANCH : EEE **YEAR/SEM:** II/III

SUB CODE/NAME: EE8351- DIGITAL LOGIC CIRCUITS

UNIT I - NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES

PART – A

1. Convert $(101.01)_2$ to decimal number.***[Apr/May-2019]***
2. Give each one example for error detecting code and error correcting code. ***[Apr/May-2019]***
3. Draw the DTL based NAND gate. ***[Nov/Dec-2018]***
4. Perform subtraction on the following unsigned binary numbers using the 2's- complement of the subtrahend (a) 11011 – 11001 (b) 110100 -10101***[Nov/Dec-2018]***
5. Convert a binary number $(1101101)_2$ to decimal and octal numbers. ***[EE6301-Apr/May-2019]***
6. Define Tri-state gates. ***[EE6301-Apr/May-2019]***
7. Convert $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers. ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
8. Write about a gray code and mention it's advantages. [***EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
9. State the associative property of Boolean algebra. ***[EE6301-Apr/May-2018]***
10. Reduce A(A + B). ***[EE6301-Apr/May-2018]***
11. Reduce a(b+bc')+ab' . ***[EE6301-Apr/May-2017]***
12. Convert 143_{10} into its binary and binary coded decimal equivalent. ***[EE6301-Apr/May-2017]***
13. Construct OR gate and AND gate using NAND gate's. [***EE6301-Nov/Dec-2016]***
14. Convert the following Excess - 3 numbers into decimal numbers. ***[EE6301-Nov/Dec-2016]***
    (a)1011 (b)1001 0011 0111
15. Convert the following binary code into a Gray Code : $(1010111000)_2$. ***[EE6301-Apr/May-2016]***\
16. Define fan-in and fan-out. ***[EE6301-Apr/May-2016]***
17. What is an unit distance code? Give an example***.[EE6301-Nov/Dec-2015]***
18. Define Fan-out.***[EE6301-Nov/Dec-2015]***
19. Convert: ***[EE6301-Apr/May-2015]***
    (a)$(475.25)_8$ to its decimal equivalent.
    (b)$(549.B4)_{16}$ to its binary equivalent.
20. Define propagation delay. ***[EE6301-Apr/May-2015]***
21. Determine $(377)_{10}$ in Octal and Hexa-Decimal equivalent. ***[EE6301-Nov/Dec-2014]***
22. Compare the totem-pole output with open-collector output? ***[EE6301-Nov/Dec-2014]***

PART – B

1. Design a 3-input NAND gate circuit using TTL logic.(7) ***[Apr/May-2019]***
2. Explain in detail, the generation of Hamming code for 4-bit data. (6) ***[Apr/May-2019]***
3. Design a 2 input NOR gate using CMOS logic.(7) ***[Apr/May-2019]***
4. Explain the operation of RTL inverter circuit with relevant diagrams.(6) ***[Apr/May-2019]***
5. Given the following Boolean function F = A' C + A' B + AB' C + BC . (13) ***[Nov/Dec-2018]***

   (i)Express it in sum of minterms.

   (ii)Find the minimal. sum of products expression.
6. Draw the logic diagram of a 2-to-4 line decoder using NOR gates only. Include an enable input. (13) ***[Nov/Dec-2018]***
7. Define Binary code. Demonstrate the Hamming code with an example. (13) ***[EE6301-Apr/May-2019]***
8. Explain TTL logic in detail along with its types.(13) ***[EE6301-Apr/May-2019]***
9. Explain in detail about error detecting and error correcting code.(13) ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
10. Write short notes on following : (13) ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***

    (i)RTL (ii)DTL (iii)TTL (iv)ECL.
11. Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC . ii) Convert the given expression in canonical SOP form Y = AC + AB + BC. (13) ***[EE6301-Apr/May-2018]***
12. Designing a 4-bit Adder-Subtractor circuit. (13) ***[EE6301-Apr/May-2018]***
13. Design a odd-parity hamming code generator and detector for 4-bit data and explain their logic. ***[EE6301-Apr/May-2017]***
14. Convert $FACE_{16}$ into its binary, octal and decimal equivalent. ***[EE6301-Apr/May-2017]***
15. With circuit schematic explain the working of a two-input TTL NAND gate. ***[EE6301-Apr/May-2017]***
16. Compare Totem Pole and open collector outputs. ***[EE6301-Apr/May-2017]***
17. Explain with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families.(10) ***[EE6301-Nov/Dec-2016]***
18. Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction Y - X by using 2's complements.(3) ***[EE6301-Nov/Dec-2016]***
19. Explain in detail the usage of Hamming codes for error. detection and error correction with an example considering the data bits as 0101. (10) ***[EE6301-Nov/Dec-2016]***
20. Convert $(23.625)_{10}$ to octal (base 8).(3) ***[EE6301-Nov/Dec-2016]***
21. Convert $(10101110111011)_2$, into its octal, decimal and hexadecimal equivalent.(6) ***[EE6301-Apr/May-2016]***
22. Deduce the odd parity hamming code for the data : 1010. Introduce an error in the LSB of the hamming code and deduce the steps to detect the error.(10) ***[EE6301-Apr/May-2016]***
23. With circuit schematic explain the operation of a two input TTL NAND gate.(8) ***[EE6301-Apr/May-2016]***

24. With circuit schematic and explain the operation anti characteristics of a ECL gate.(a) ***[EE6301-Apr/May-2016]***
25. Draw the CMOS logic circuit for NOR gate and explain its operation.(8)***[EE6301-Nov/Dec 2015]***
26. Perform the following operation $(756)_8$ - $(437)_8$ + $(725)_{16}$. Express the answer in octal form.(8) ***[EE6301-Nov/Dec 2015]***
27. A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8 bit data word that was written into memory if the 12 bit word read out is as (i) 101110010100 and (ii) 111111110100.(12) ***[EE6301-Nov/Dec 2015]***
28. Briefly discuss weighted Binary code.(4) ***[EE6301-Nov/Dec 2015]***
29. Perform the following addition using BCD and Excess-3 addition (205+569). (8) ***[EE6301-Apr/May 2015]***
30. Encode the binary word 1011 into seven bit even parity Hamming code. (8) ***[EE6301-Apr/May 2015]***
31. With circuit schematic, explain the operation of a two input TTL NAND gate with totem-pole output. (10) ***[EE6301-Apr/May 2015]***
32. Compare totem pole and open collector outputs.(6) ***[EE6301-Apr/May 2015]***
33. Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010. Determine the method of detecting the error using any one error detecting code.(8) ***[EE6301-Nov/Dec 2014]***
34. Draw the MOS logic circuit for NOT gate and explain its operation.(8) ***[EE6301-Nov/Dec 2014]***
35. Explain Hamming code with an example. State its advantages over parity codes. (8) ***[EE6301-Nov/Dec 2014]***
36. Design a TTL logic circuit for a 3-input NAND gate.(8) ***[EE6301-Nov/Dec 2014]***

PART – C

1. Simplify the following function and implement it using NAND gates only: (15) ***[Apr/May-2019]***
   F(w, x, y, z)= Σ(1, 3, 5, 7, 9,11, 13,15) with don't care states d(w, x, y, z) = Σ(0, 2, 4, 6, 8)
2. Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out power dissipation, propagation delay and noise margin. Compare its advantages over other logic families.(15) ***[EE6301-Apr/May-2017]***

UNIT II - COMBINATIONAL CIRCUITS

PART – A

1. Determine the exact number of half adders and full adders required for performing the addition of two binary numbers of 5-bits length each. ***[Apr/May-2019]***
2. Find the result of A + A' D + AC'. ***[Apr/May-2019]***
3. Mention the dependency of output in combinational circuits. ***[Nov/Dec-2018]***
4. Draw the NAND gate circuit using NOT, AND & OR Gates. ***[Nov/Dec-2018]***
5. Write the logic expression for Full adder and Full subtractor. ***[EE6301-Apr/May-2019]***
6. What is meant by canonical form? Give an example for POS and SOP canonical forms. ***[EE6301-Apr/May-2019]***
7. Define K-map. ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
8. Compare decoder and Demultiplexer. ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
9. Define duality property. ***[EE6301-Apr/May-2018]***
10. What is a karnaugh map? ***[EE6301-Apr/May-2018]***
11. Write the POS form of the SOP expression f (x, y, z) = x'yz + xyz' + xy'z. ***[EE6301-Apr/May-2017]***
12. Design a Half Subtractor.***[EE6301-Apr/May-2017]***
13. Convert the given expression in canonical SOP form Y = AB + A'C + BC'. ***[EE6301-Nov/Dec-2016]***
14. Draw the truth table of 2 :1 MUX. ***[EE6301-Nov/Dec-2016]***
15. Write the POS representation of the following SOP function: ***[EE6301-Apr/May-2016]***
    f(x,y, z) = Σm (0, 1, 3, 5, 7).
16. Design a half subtractor. ***[EE6301-Apr/May-2016]***
17. Convert the given expression in canonical SOP form Y = AB + A'C+ BC' . ***[EE6301-Nov/Dec-2015]***
18. Draw the logical diagram of EX-OR gate using NAND gates. ***[EE6301-Nov/Dec-2015]***
19. Convert the given expression in canonical SOP form Y=AC+AB+BC. ***[EE6301-Apr/May-2015]***
20. Simplify the expression Z = AB + AB.(A.C). ***[EE6301-Apr/May-2015]***
21. Given F = B' + A' B + A' C': Identify redundant term using K-Map. ***[EE6301-Nov/Dec-2014]***
22. Give one application each Multiplexer and Decoder. ***[EE6301-Nov/Dec-2014]***

PART – B

1. Design a 3 x 8 decoder using 2 x 4 decoders. Draw the truth table. (7) ***[Apr/May-2019]***
2. Design a full adder circuit using logic gates. (6)***[Apr/May-2019]***
3. Simplify and implement the logic function F(A, B, C) =Σ(0, 1, 4, 5, 7) using logic gates.(7) ***[Apr/May-2019]***
4. Design a 4 x 2 priority encoder using logic gates.(6) ***[Apr/May-2019]***
5. Given the following Boolean function F = A' C + A' B + AB' C + BC. (13) ***[Nov/Dec-2018]***
   (i) Express it in sum of minterms.
   (ii) Find the minimal sum of products expression.

6. Draw the logic diagram of a 2-to-4 line decoder using NOR gates only. Include an enable input. (13) ***[Nov/Dec-2018]***
7. Design a Combinational logic circuit to convert Binary to Gray code and write its truth table.(13) ***[EE6301-Apr/May-2019]***
8. Implement the following Boolean function using 4:1 Multiplexer. (13) ***[EE6301-Apr/May-2019]***
   F (W, X, Y, Z)=Σm (0, 1, 2, 4, 6, 9, 12, 14)
9. Plot the logical expression ABCD + A' B' C' D' + AB'C + AB on a 4-variable K-map; obtain the simplified expression from the map. (7). ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
10. Express the function Y=A+B'C in canonical SOP and canonical POS form.(6) ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
11. Design a 4-bit gray code to binary converter and express using logic gates.(13) ***[EE6301-Nov/Dec-2018]***
12. Write down the steps in implementing a Boolean function with levels of AND gates.(13) ***[EE6301-Apr/May-2018]***
13. Give the general procedure for converting a Boolean expression in to multilevel NAND diagram (13) ***[EE6301-Apr/May-2018]***
14. Design a 4-bit gray code to binary converter and express using logic gates. (13) ***[EE6301-Nov/Dec-2017]***
15. Reduce the following minterms using Karnaugh – Map: (7) ***[EE6301-Apr/May-2017]***
    f(w, x, y, z)=Σm(0, 1, 3, 5, 6, 7, 8, 12, 14) + d(9, 15) .
16. Implement the following function using a suitable multiplexer
    f(a,b,c) = Σm (3, 7, 4, 5). ***(6) [EE6301-Apr/May-2017]***
17. Design a 3 x 8 decoder and explain its operation as a minterm generator. (7) ***[EE6301-Apr/May-2017]***
18. Design a full adder using only NOR gates. (6) ***[EE6301-Apr/May-2017]***
19. Simplify the logical expression using K-map in SOP and POS form[EE6301-Nov/Dec-2016] F(A,B, C, D) = ∑m (0, 2 , 3, 6, 7) + d(8, 10, 11, 15) . (13) ***[EE6301-Nov/Dec-2016]***
20. Design a full subtractor and realise using logic gates. Also, implement the same using half subtractors. (13) ***[EE6301-Nov/Dec-2016]***
21. Simplify the Billowing function using Karnaugh Map.
    F(w, x, y, z) = Σm(0, 1, 3, 9. 10, 12, 13, 14) + Σd(2. 5, 6, 11) (8) ***[EE6301-Apr/May-2016]***
22. Implement the following function using only NAND gates : f(x,y, z) = Σm(0, 2, 4, 6)(8)***[EE6301-Apr/May-2016]***
23. Design a BCD to Excess-3 code converter.(8) ***[EE6301-Apr/May-2016]***
24. Design a full adder and implement it using suitable multiplexer.(8) ***[EE6301-Apr/May-2016]***
25. Simplify the boolean function using K-map and implement using only NAND gates.
    F(A, B, C, D) =Σm(0,8,11,12,15) + Σd(1,2,4,7,10,14).
    Mark the essential and non-essential prime implicants.(8***) [EE6301-Nov/Dec 2015]***
26. Design a full subtractor and implement using logic gates.(8) ***[EE6301-Nov/Dec 2015]***

27. Design a 4 bit BCD to excess 3 code converter and implement using logic gates.(8)***[EE6301-Nov/Dec 2015]***
28. What is a multiplexer? Implement the following using Boolean function with 8 x 1 MUX and external gates.
    F(A, B, C, D) = Σm(1,3,4,11,12,13,14,15) .(8) ***[EE6301-Nov/Dec 2015]***
29. Reduce the following function using K-map, f (A, B,C,D)= πM(0,2,3,8,9,12,13,15). (8***) [EE6301-Apr/May 2015]***
30. Design a full adder using half-adders and an OR gate.(8) ***[EE6301-Apr/May 2015]***
31. Design a BCD to Excess 3 code converter. (8) ***[EE6301-Apr/May 2015]***
32. Implement the following Boolean function using 8:1 Mux : F(A,B,C,D)= Σm(0,1, 3, 4, 8,9,15) . (8) ***[EE6301-Apr/May 2015]***
33. Minimize the function F(a, b, c, d) = Σ(0, 4, 6, 8, 9, 10, 12) with d = Σ(2, 13). Implement the function using only NOR gates. (8) ***[EE6301-Nov/Dec 2014]***
34. (Design a Full Subtractor and implement it using logic gates. (8) ***[EE6301-Nov/Dec 2014]***
35. Implement the function F(p, q, r, s)=Σ(0, 1, 2, 4, 7, 10, 11, 12) using Decoder. (8) ***[EE6301-Nov/Dec 2014]***
36. Design a 4-bit Binary ray code converter and implement it using logic gates.(8) ***[EE6301-Nov/Dec 2014]***

PART – C

1. Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. when the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary' input is 4, 5, 6, or 7, the binary output is one less than the input.(15) ***[Nov/Dec-2018]***
2. Design a logic circuit that has three inputs, A, B, 0 and whose output will be HIGH only when a majority of the inputs are HIGH. (15) ***[EE6301-Nov/Dec-2018]***
3. Apply K-map and simplify the following. y = C'(A'B'D'+ D)+ AB'C +D'.(15) [EE6301-Nov/Dec-2018]
4. Design a full adder using 4 x 1 multiplexer, also write its truth table and draw the logical diagram. (8) ***[EE6301-Nov/Dec-2017]***

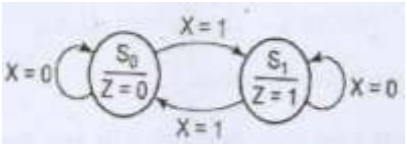
UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS

PART – A

1. Write down the characteristic table of JK. ***[Apr/May-2019]***
2. What is FSM? List its two basic types. ***[Apr/May-2019]***
3. Write the role of master clock generator in synchronous circuits. ***[Nov/Dec-2018]***
4. Comment about a preset table counter & ripple counter. ***[Nov/Dec-2018]***
5. Draw the sequential logic diagram for Parallel In-Serial Out Shift register. ***[EE6301-Apr/May-2019]***
6. Write the characteristic equation of JK flip flop and its truth table. ***[EE6301-Apr/May-2019]***
7. Mention about race around condition in a flip-flop. ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
8. What is a presettable counter and ripple counter? ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
9. What is a master-slave flip-flop? ***[EE6301-Apr/May-2018]***
10. Give the comparison between synchronous and asynchronous counters. ***[EE6301-Apr/May-2018]***
11. Give the characteristic equation and characteristic table of a T Flip Flop. ***[EE6301-Apr/May-2017]***
12. State the differences between Moore and Melay state machines. ***[EE6301-Apr/May-2017]***
13. Differentiate Mealy and Moore model. ***[EE6301-Nov/Dec-2016]***
14. Draw the state diagram of JK flip flop. ***[EE6301-Nov/Dec-2016]***
15. Give the characteristic equation and characteristic table of SR flip-flop. ***[EE6301-Apr/May-2016]***
16. State any two differences between Moore and Mealy state machines. ***[EE6301-Apr/May-2016]***
17. Draw the truth table and state diagram of SR flip-flop. ***[EE6301-Nov/Dec-2015]***
18. What is edge triggered flip fops? ***[EE6301-Nov/Dec-2015]***
19. Convert T Flip Flop to D Flip Flop. ***[EE6301-Apr/May-2015]***
20. State the rules for state assignment. ***[EE6301-Apr/May-2015]***
21. Show how the JK flip flop can be modified into a D flip flop or a T flip flop. ***[EE6301-Nov/Dec-2014]***
22. Differentiate between Mealy and Moore models. ***[EE6301-Nov/Dec-2014]***

PART – B

1. Design a 2-bit synchronous sequential down counter.(7) ***[Apr/May-2019]***
2. Explain the operation of a 3-bit universal shift register.(6) ***[Apr/May-2019]***
3. Explain Moore and Mealy models with the help of block diagrams.(7) ***[Apr/May-2019]***
4. Draw the state table for the following state diagram. (6) ***[Apr/May-2019]***



5. Explain the operation, state diagram and characteristics of a T flip-flop and master slave JK flip-flop.(13) ***[Nov/Dec-2018]***
6. Describe the design procedure with neat diagram about 4 bit bidirectional shift register with parallel load.(13) ***[Nov/Dec-2018]***

7. Synthesis a 3 bit counter using T Flip Flop (State diagram, Excitation table, K-map, Logic diagram.(13) ***[EE6301-Apr/May-2019]***
8. What is meant by a Flip Flop? Write the characteristics equation, characteristics table and draw logic of SR, JK and D flip flops. (2+4+4+3) ***[EE6301-Apr/May-2019]***
9. Explain the operation, state diagram and characteristics of T flip-flop and master-slave JK flip-flop.(13) ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
10. Explain in detail about different shift registers.(13) ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
11. Explain the operation of SR flip-flop, T flip-flop and JK.(13) ***[EE6301-Apr/May-2018]***
12. Explain the flip-flop excitation tables for JK flip-flop and RS flip-flop.(13) ***[EE6301-Apr/May-2018]***
13. Draw and explain the operation of a Master – Slave JK Flip Flop.(7) ***[EE6301-Apr/May-2017]***
14. Design a 5-bit ring counter and mention its applications.(6) ***[EE6301-Apr/May-2017]***
15. Design a 4-bit parallel-in serial-out shift register using D FlipFlops.(7) ***[EE6301-Apr/May-2017]***
16. Using partitioning minimization procedure reduce the following state table :(6) ***[EE6301-Apr/May-2017]***

Present state	Next state		Output
	w =0	w=1	2
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

17. Design a sequence detector that produces an output '1' whenever the non-overlapping sequence 101101 is detected.(13) ***[EE6301-Nov/Dec-2016]***
18. Explain the realization of JK flip flop from T flip flop.(7) ***[EE6301-Nov/Dec-2016]***
19. Write short notes on SIPO and draw the output waveforms. (6) ***[EE6301-Nov/Dec-2016]***
20. Explain the operation of a JK master slave flip flop. (8) ***[EE6301-Apr/May-2016]***
21. Design a MOD-5 counter using T Flip Flops.(8) ***[EE6301-Apr/May-2016]***
22. Design a serial adder using Mealy state model.(8) ***[EE6301-Apr/May-2016]***
23. Explain the state minimization using partitioning procedure with a suitable example.(8) ***[EE6301-Apr/May-2016]***
24. A sequential circuit with two D flip flops A and B, input X and output Y is specified by the following next state and output equations

    A(t+1)=AX+BX

    B(t+1)=A'X

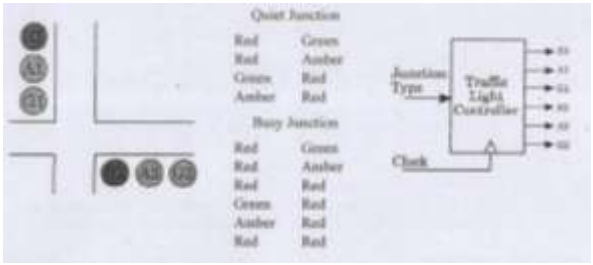
    Y=(A+B)X'

    Draw the logic diagram; derive state table and state diagram. (12) ***[EE6301-Nov/Dec 2015]***
25. Realize T flip-flop using JK flip-flop.(4) ***[EE6301-Nov/Dec 2015]***

26. Design a synchronous decade counter using T flip flop and construct the timing diagram (8)***[EE6301-Nov/Dec 2015]***
27. Design a mealy model of sequence detector to detect the pattern 1001. (8) ***[EE6301-Nov/Dec 2015]***
28. Explain the operation of a master slave JK flip flop.(8) ***[EE6301-Apr/May 2015]***
29. Design a 3-bit bidirectional shift register.(8) ***[EE6301-Apr/May 2015]***
30. Design a MOD-5 synchronous counter using JK flip-flops. (8) ***[EE6301-Apr/May 2015]***
31. Design a sequence detector to detect the sequence 101 using JK flip flop. (8) ***[EE6301-Apr/May 2015]***
32. Design an asynchronous Modulo-8 Down counter using JK flipflops. (8) ***[EE6301-Nov/Dec 2014]***
33. Explain the circuit of a SR flip-flop and explain its operation.(8) ***[EE6301-Nov/Dec 2014]***
34. Design synchronous sequential circuit that goes through the count sequence 1,3,4,5 repeatedly. Use T flip-flops for your design.(8) ***[EE6301-Nov/Dec 2014]***
35. Explain the various types of triggering with suitable diagrams. Compare their merits and demerits.(8) ***[EE6301-Nov/Dec 2014]***

PART – C

1. Design and explain and bit shift register. Also give its truth table with its input and output waveform.(15)***[EE6301-Apr/May-2018]***
2. Describe level triggering and edge triggering.(7) ***[EE6301-Nov/Dec-2017]***
3. Design a synchronous sequential logic circuit that goes through the sequence 0, 2, 4, 6, 8, 10, 12,14 repeatedly. Use D flip flops for your design. (15) ***[Apr/May-2019]***
4. Design a sequential circuit with two D flip-flops A and B, and one input x . When x = 0 , the state of the circuit remains the same. When x = 1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats. (15) ***[Nov/Dec-2018]***
5. Design a synchronous digital circuit, a Moore machine, which operates this traffic light at two types of road crossing.(15) ***[EE6301-Apr/May-2019]***



6. Assume that there is a parking area in a shop whose capacity is 10. No more than 10 cars are allowed inside the parking area and the gate is closed as soon as the capacity is reached. There is a gate sensor to detect the entry of car which is to be synchronized with the clock pulse. Design and implement a suitable counter using JK flip flops. Also, determine the number of flip flops to be used if the capacity is increased to 50. (15) ***[EE6301-Nov/Dec-2016]***

UNIT IV- ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABILITY LOGIC DEVICES

PART – A

1. Define metastable state. ***[Apr/May-2019]***
2. Draw the structure of PAL. ***[Apr/May-2019]***
3. Draw the block diagram of asynchronous sequential circuit. ***[Nov/Dec-2018]***
4. Outline about PLA. ***[Nov/Dec-2018]***
5. Define race condition. How it can be eliminated. ***[EE6301-Apr/May-2019]***
6. Describe PROM. ***[EE6301-Apr/May-2019]***
7. What happens to the information stored in a memory location after it has been, read and write operation? ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
8. What is Programmable Logic Array? ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
9. Define address and word. ***[EE6301-Apr/May-2018]***
10. Why was PAL developed? ***[EE6301-Apr/May-2018]***
11. What is a flow table? Give example. ***[EE6301-Apr/May-2017]***
12. State the difference between PROM, PAL and PLA. ***[EE6301-Apr/May-2017]***
13. What is static hazard and dynamic hazard? ***[EE6301-Nov/Dec-2016]***
14. Define races in asynchronous sequential circuits. ***[EE6301-Nov/Dec-2016]***
15. What are the two types of asynchronous sequential circuits? ***[EE6301-Apr/May-2016]***
16. State the difference between PROM, PLA and PAL. ***[EE6301-Apr/May-2016]***
17. What is PROM? ***[EE6301-Nov/Dec-2015]***
18. Compare pulsed mode and fundamental mode asynchronous circuit. ***[EE6301-Nov/Dec-2015]***
19. State the difference between static 0 and static 1 hazard. ***[EE6301-Apr/May-2015]***
20. What is a PROM? ***[EE6301-Apr/May-2015]***
21. What is a deadlock condition? ***[EE6301-Nov/Dec-2014]***
22. Draw the block diagram of PLA. ***[EE6301-Nov/Dec-2014]***

PART – B

1. Design a 2-bit synchronous sequential down counter.(7) ***[Apr/May-2019]***
2. Design a Modulo-6 asynchronous binary up-counter.(7) ***[Apr/May-2019]***
3. Implement the functions, (6) ***[Apr/May-2019]***

   $F1(X, Y, Z) = \Sigma(1, 2, 4, 5)$

   $F2(X, Y, Z) = \Sigma(0, 1, 3, 4)$

   $F3(X, Y, Z) = \Sigma(23, 6, 7)$ using a single PROM grid.
4. Differentiate PAL and PLA implementations with the help of the same example: **(7) [Apr/May-2019]**

   $F2(a, b, c) = \Sigma(0, 1, 3, 4, 6, 7)$.
5. Explain the structure of CPLD with the help of a block diagram. (6) ***[Apr/May-2019]***

6. Discuss the operation of SR Latch with NOR and NAND gate8 analysis.(13) ***[Nov/Dec-2018]***
7. Illustrate about hazards in sequential circuits and the steps to avoid hazards in it. (13) ***[Nov/Dec-2018]***
8. Explain the steps for the design of Asynchronous sequential circuits with an example. (13)***[EE6301-Apr/May-2019]***
9. Draw a PLA circuit to implement the functions (13) ***[EE6301-Apr/May-2019]***

   F_1= AB' +AC +A' BC' and F_2 = (AC +BC)'
10. Discuss about the hazards in asynchronous sequential circuit and the ways to eliminate them. (13) ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
11. Design an asynchronous circuit that will operate only for the first pulse received whenever a control input is asserted from LOW to HIGH state. Further pulses will be ignored.(13) ***[EE6301-Nov/Dec-2018]***
12. Elaborate the concept of PROM, EPROM, EEPROM in detail.(13) ***[EE6301-Apr/May-2018]***
13. Explain the operation of bipolar RAM cell with suitable diagram.(13) ***[EE6301-Apr/May-2018]***
14. Write short notes on PLA and PAL.(7) ***[EE6301-Nov/Dec-2017]***
15. What is hazards? Explain hazards in digital circuits. (6) ***[EE6301-Nov/Dec-2017]***
16. A control mechanism for a vending machine accepts nickels and dimes. It dispense merchandise when 20 cents is deposited; it does not give change if 25 cents is deposited.. Design the FSM that implements the required control, using as few states as possible. Find a suitable assignment and derive next-state and output expressions.(13) ***[EE6301-Apr/May-2017]***
17. Implement the following logic and analyse for the pressure of any hazard f = xlx2 +x1'x3. If hazard is present briefly explain the type of hazard and design a hazard-free circuit. (7) ***[EE6301-Apr/May-2017]***
18. Implement the following functions using programmable logic array: (6) ***[EE6301-Apr/May-2017]***

    F1 (x, y, z)= Σm (0, 1, 3, 5, 7)

    F2 (x, y, z)= Σm (2, 4, 6)
19. Design an asynchronous circuit that has two inputs x1 and x2 and one output z. The circuit is required to give an output whenever the input sequence (0,0), (0,1) and (1, 1) received but only in that order (13) ***[EE6301-Nov/Dec-2016]***
20. Design a PLA structure using AND and OR logic for the following functions.(10) ***[EE6301-Nov/Dec-2016]***

    F1= Σm(0, 1, 2, 3, 4, 7, 8, 11, 12, 15)
    F2 = Σm (2, 3, 6, 7, 8, 9, 12, 13)
    F3 = Σm (1, 3, 7, 8, 11, 12, 15)
    F4= Σm (0, 1, 4, 8, 11, 12, 15)
21. Compare PLA and PAL circuits.(3) ***[EE6301-Nov/Dec-2016]***
22. What are Static-0 and Static- 1 hazards? Explain the removal of hazards using hazard covers in K-map. (8) ***[EE6301-Apr/May-2016]***
23. Explain cycles and races in asynchronous sequential circuits.(8) ***[EE6301-Apr/May-2016]***
24. What are transition table and flow table? Give suitable examples.(6) ***[EE6301-Apr/May-2016]***
25. Implement the following function using PLA and PAL :(10) ***[EE6301-Apr/May-2016]***

F(x,y,z) =Σm (0, 1, 3, 5, 7)

26. Design an asynchronous sequential circuit (with detailed steps involved) that has 2 inputs x1 and x2 and one output z. The circuit is required to give an output z = 1 when x1 =1, x2 = 1 and x1 = 1 being first. (16) ***[EE6301-Nov/Dec 2015]***
27. Show how to program the fusible links to get a 4 bit Gray code from the binary inputs using PLA and PAL and compare the design requirements with PROM. (16) ***[EE6301-Nov/Dec 2015]***
28. Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z . When X_1 = 0, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. (16) ***[EE6301-Apr/May 2015]***
29. Implement the following function using PLA: (8) ***[EE6301-Apr/May 2015]***

    F(x,y,z)=Σm(1,2,4,6)
30. For the given boolean function, obtain the hazard-free circuit F(A,B,C,D)=Σm(1,3,6,7,13,15).(8) ***[EE6301-Apr/May 2015]***
31. Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples.(16) ***[EE6301-Nov/Dec 2014]***
32. Describe with reasons, the effect of races in asynchronous sequential circuit design. Explain its types with illustrations. Show the method of race-free state assignments with examples. (16) ***[EE6301-Nov/Dec 2014]***

PART – C

1. Design an asynchronous circuit that has two inputs X1 and X2 and one output Z. The circuit is required to give an output whenever the input sequence (0, 0) (0, 1) and (1, 1) received but only in that order. Design it using T flip flop. (15) ***[EE6301-Apr/May-2019]***
2. Design an asynchronous sequential circuit with two inputs x1 and x2 and one output Z. Initially, both inputs are equal to zero. When x1 or x2 becomes 1, the output Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state.(15) ***[EE6301-Nov/Dec-2017]***

UNIT-V VHDL

PART – A

1. State the purpose of test bench. ***[Apr/May-2019]***
2. Write a VHDL program for an EX-NOR gate using behavioral coding. ***[Apr/May-2019]***
3. Draw the basic structure of MOS transistor. ***[Nov/Dec-2018]***
4. List the languages that are combined together to get VHDL language. ***[Nov/Dec-2018]***
5. List the purpose of Test bench. ***[EE6301-Apr/May-2019]***
6. Design a Half adder using HDL. ***[EE6301-Apr/May-2019]***
7. Define modularity. ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
8. List the languages that are combined together to get VHDL, language. ***[EE6301-Nov/Dec-2018] [EE6301-Nov/Dec-2017]***
9. Define Cache memory. ***[EE6301-Apr/May-2018]***
10. Infer the concept of switch-level modeling. ***[EE6301-Apr/May-2018]***
11. Give the syntax for package declaration and package body in VHDL. ***[EE6301-Apr/May-2017]***
12. Write the VHDL code for a 2 x 1, multiplexer using behavioral modeling. ***[EE6301-Apr/May-2017]***
13. Write VHDL behavioral model for D flip flop. ***[EE6301-Nov/Dec-2016]***
14. Write the VHDL code for a logical gate which gives high output only when both the inputs are high. ***[EE6301-Nov/Dec-2016]***
15. What is data flow modeling in VHDL ? Give its basic mechanism. ***[EE6301-Apr/May-2016]***
16. Write the VHDL code to realize a 2 x 1 multiplexer. ***[EE6301-Apr/May-2016]***
17. Write the behavioral model of D flip flop. ***[EE6301-Nov/Dec-2015]***
18. List out the operators present in VHDL. ***[EE6301-Nov/Dec-2015]***
19. What is a package in VHDL? ***[EE6301-Apr/May-2015]***
20. Write the behavioral modeling code for a D Flip Flop. ***[EE6301-Apr/May-2015]***
21. Write a VHDL code for 2 x 1 MUX. ***[EE6301-Nov/Dec-2014]***
22. State the advantage of package declaration over component declaration. ***[EE6301-Nov/Dec-2014]***

PART – B

1. Draw the VLSI design flow chart used for IC design and fabrication. (7) ***[Apr/May-2019]***
2. Write down a VHDL code for 8 x 1 Demultiplexer.(6) ***[Apr/May-2019]***
3. Illustrate the two approaches used in VHDL coding with full adder design as your example.(7) ***[Apr/May-2019]***
4. What are components in VHDL? Show step-by-step how a NOR gate component can be created and added in the library. (6) ***[Apr/May-2019]***
5. Explain the structure and working principles of TTL based Totem-pole output configuration.(13) ***[Nov/Dec-2018]***
6. Write a VHDL code to realize a half adder using behavioral modeling and structural modeling. (13) ***[Nov/Dec-2018]***

7. Describe RTL in HDL with an example.(13) ***[EE6301-Apr/May-2019]***
8. Write the HDL program for 2:1 multiplexer in Dataflow and Behavioral Description.(6) ***[EE6301-Apr/May-2019]***
9. Write program in HDL to design 2 bit up/down counter.(7) ***[EE6301-Apr/May-2019]***
10. Implement a full adder circuit using PLA having three inputs, eight product terms, and two outputs.(13) ***[EE6301-Nov/Dec-2018]***
11. Briefly explain the operations involved using RAM and compare Static RAMandDynamicRAM.(13)***EE6301-Nov/Dec-2018]***
12. Give the different arithmetic operators and bitwise operators.(13) ***[EE6301-Apr/May-2018]***
13. Explain in detail about the principal of operation of RTL design. (13) ***[EE6301-Apr/May-2018]***
14. Write a VHDL code to realize a full adder using behavioral modeling and structural modeling. (13) ***[EE6301-Nov/Dec-2017]***
15. Discuss briefly the packages in VHDL. (6) ***[EE6301-Nov/Dec-2017]***
16. Write a VHDL coding for realization of clocked SR flip-flop.(7) ***[EE6301-Nov/Dec-2017]***
17. Design a 3 –bit magnitude comparator and write the VHDL code to realize it using structural modeling. (13) ***[EE6301-Apr/May-2017]***
18. Design a 4 x 4 array multiplier and write the VHDL code to realize it using structural modeling,(13) ***[EE6301-Apr/May-2017]***
19. Explain in detail the concept of structural modeling in VHDL with an example of full adder.(13) ***[EE6301-Nov/Dec-2016]***
20. Write short notes on built- in operators used in VHDL programming. (6) ***[EE6301-Nov/Dec-2016]***
21. Write VHDL coding for 4 x 1 Multiplexer. (7) ***[EE6301-Nov/Dec-2016]***
22. Explain the various operators supported by VHDL.(8) ***[EE6301-Apr/May-2016]***
23. Write the VHDL code to realize a decade counter with behavioral modeling.(8) ***[EE6301-Apr/May-2016]***
24. Explain functions and subprograms with suitable examples.(6) ***[EE6301-Apr/May-2016]***
25. Write the VHDL code to realize a 4-bit parallel binary adder with structural modeling and write the test bench to verify its functionality.(10) ***[EE6301-Apr/May-2016]***
26. Write a VHDL program for 1 to 4 Demux using dataflow modeling.(8) ***[EE6301-Nov/Dec 2015]***
27. Write a VHDL program for Full adder using structural modeling.(8) ***[EE6301-Nov/Dec 2015]***
28. Explain in detail the RTL design procedure.(16) ***[EE6301-Nov/Dec 2015]***
29. Write the VHDL code to realize a full adder using, (16) ***[EE6301-Apr/May 2015]***

    (i)Behavioral modeling (8)

    (ii)Structural modeling.(8)
30. Write the VHDL code to realize a 3-bit Gray code counter using case statement. (16) ***[EE6301-Apr/May 2015]***

31. Explain the digital system design flow sequence with the help of a flow chart. (8) ***[EE6301-Nov/Dec 2014]***
32. Write a VHDL code for a 4-bit universal shift register. (8) ***[EE6301-Nov/Dec 2014]***
33. Explain the concept of behavioral modeling and Structural modeling in VHDL. Take the example of full Adder design for both and write the coding.(16) ***[EE6301-Nov/Dec 2014]***

PART – C

1. Draw the circuit of CMOS AND gate and explain its operation. Also implement using VHDL. (15) ***[EE6301-Apr/May-2018]***
2. Design a 4 bit code converter which converts given binary code into a code in which the adjacent number differs by only 1 by the preceding number. Also, develop VHDL coding for the above mentioned code converter. (15) ***[EE6301-Nov/Dec-2016]***
3. Write the VHDL code for the given state diagram, using behavioral modeling. Design it using one-hot state -assignment and implement it using Programmable Array Logic (PAL). (15) ***[EE6301-Apr/May-2017]***