UNIT I IC FABRICATION 9

IC classification, fundamental of monolithic IC technology, epitaxial growth, masking and etching, diffusion of impurities. Realisation of monolithic ICs and packaging. Fabrication of diodes, capacitance, resistance, FETs and PV Cell.

Part-A (10×2 = 20 marks)

1. What are the major categories of integrated circuits?

Type of integration	Number of gates	Number of transistors	Example
SSI(or) Small Scale Integration	12	10	Single chip Amplifier IC , BIFET Preamplifier, Logic Gates
MSI or Medium Scale Integration	99	500	Shift Register , Adder , Counters
LSI or Large Scale Integration	9999	20000	4-bit microprocessor 4004 , 8-bit microprocessors such as 8080 , 8085
VLSI or Very Large Scale Integration	99,999	1000000	8-bit Microcontroller 8051 , 16-bit Microprocessor 8086 , 32-bit Microprocessor Motorola 68000
ULSI or Ultra Large Scale Integration	> 100,000	> 1000000	Intel Core i3/i5/i7

2. Mention the advantages of Integrated circuits over discrete circuits?

- Extremely small size
- Extremely light weight
- Very low cost because of simultaneous production of hundreds of similar circuits on a semiconductor wafer
- Low power consumption

Eg. AT89S52 microcontroller , a flash memory variant of 8051 microcontroller(8-bit microcontroller), has a size of 676 mm^2 , weight of 6 g , cost of Rs.250 , power consumption of 165 mW.

3. What is ion implantation ? Give its advantages.

- Silicon Wafers placed in a vacuum chamber called as target chamber and exposed to a beam of high energy dopant ions(Boron for P-type ; Phosphorous for N-type).
- Accelerating voltage for the ions is between 20 kV to 250 kV.
- Ions striking the wafer penetrate some small distance into the wafer. Depth of penetration increases with increase in accelerating voltage.

Advantages:

- Low temperature process.
- Less lateral diffusion of impurities
- Accelerating potential and beam current electrically controlled from outside.

4. Mention different available IC package configurations.

Through Hole Package:

Example : SIP (Single Inline Package) ; DIP(Dual Inline Package) ; ZIP(Zigzag Inline PackMSBage).

Surface Mounting Technology(SMT) or Planar Mounting Package :
Example : SOD(Small Outline Diode) , MELF(Metal Electrode Leadless Face), LGA(Land Grid Array).

Chip Carrier Package:
Example : BCC(Bump Chip Carrier) , PLCC(Plastic Leaded Chip Carrier) , DLCC(Dual Leadless Chip Carrier)

PGA(Pin Grid Array**)**:
Example : OPGA (Organic Pin Grid Array) , PAC(Pin Array Catridge) , CGPA(Ceramic Pin Grid Array)

5. State the limitations of IC Technology

- Limited Power rating
- Low voltage operation
- More noise during operation
- Voltage dependence of resistors and capacitors.

6. Distinguish between dry etching and wet etching.

Parameters	Dry Etching	Wet Etching
Directionality	Good for most materials	Suitable for crystal materials having an aspect ratio of 100
Production Automation	Good	Poor
Environmental Impact	Low	High
Selectivity	Poor	Very Good

7. What is meant by parasitic capacitance?
Parasitic capacitance or stray capacitance or mutual capacitance is an unavoidable and unwanted capacitance existing between the parts of an electronic device or circuit due to their proximity**.**

8. What are the advantages of NPN transistor over PNP transistor in IC technology
NPN transistors are preferred over PNP transistors in integrated circuits due to the following reasons:
→ In vertical pnp transistor , collector has to be held at FIXED NEGATIVE VOLTAGE.
→ NPN transistor has high current gain (50 to 300) compared to PNP transistor current gain(1.5 to 30).
→ N-type collector in NPN transistor moves very little compared to P-type collector in PNP transistor during base and emitter diffusion process. Hence NPN has superior performance than PNP transistor

9. Define the term Encapsulation
Putting a cap over the IC and sealing it in inert atmosphere is called **Encapsulation**.

10. List the advantages of thin film resistors.

- Tight tolerance to 0.05%
- Low capacitance
- Low noise
- Low temperature coefficient(1 ppm to 2 ppm)

11. How diodes are realized in IC wafer fabrication.

Monolithic diodes are realized by **joining any two of three terminals of a BJT and leaving one of the terminals open.**

12. Classify ICs based on the Manufacturing techniques. Name any two merits.
Based on Manufacturing techniques ICs can be classified as follows:

- Thick and Thin Film ICs
- Monolithic ICs
- Hybrid or Multichip ICs

13. List the steps used for preparation of Silicon Wafer.
(i) Crystal Growth and Doping
(ii) Ingot Trimming and Grounding:
(iii) Ingot Slicing
(iv) Wafer polishing and etching:
(v) Wafer cleaning

14. Classify IC on the basis of application, device used and chip complexity.
Based on Application:

- Commercial grade IC [0˚C to 45˚C]
- Industrial Grade IC[-20˚C to +85˚C]
- Automotive Grade IC[-40˚C to +125˚C]
- Military Grade IC [-55˚C to +125˚C]

Based on Device Used for IC Fabrication:

- Unipolar IC[FET based IC]
- Bipolar IC[BJT based IC]

Based on chip complexity:

Type of integration	Number of gates	Number of transistors	Example
SSI(or) Small Scale Integration	12	10	Single chip Amplifier IC , BIFET Preamplifier, Logic Gates
MSI or Medium Scale Integration	99	500	Shift Register , Adder , Counters
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15. Explain the importance of SiO_2 layer?

To allow selective diffusion of dopant atoms into certain regions of wafer and protection of wafer from unwanted impurity diffusion.

16. What is meant by substantial diffusion
Addition of impurities to silicon chip at very high temperature.

17. What step is taken to avoid material defect in ion-implantation
- Controlling depth of penetration of dopants
- Control of dopant concentration.

Part-B

1. With neat illustrations explain the various steps involved in IC fabrication process.(13)

A.) Crystal Growth and Doping

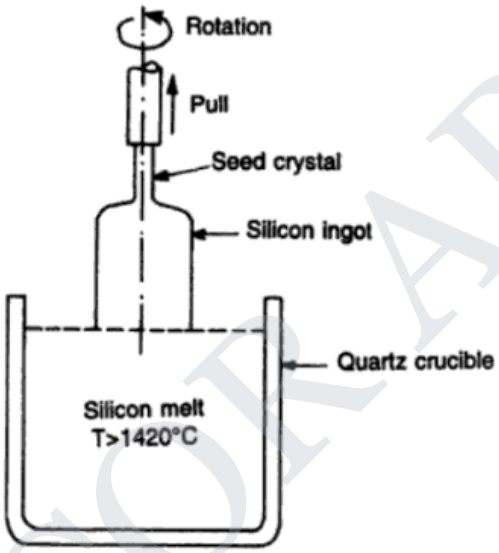
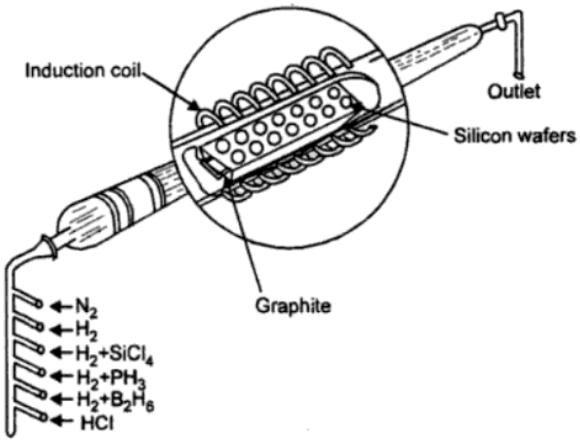


Fig. Czochralski Crystal Growth

The process of fabricating a **silicon ingot is called crystal growth.** In this method , a 99.5% pure polycrystalline silicon is doped with suitable impurity and heated in a crucible to form a melt.
A seed crystal is dipped into the melt and slowly taken out while the crucible is made to rotate in a direction opposite to that of seed crystal. This is called **crystal pulling.**
The silicon ingot is sliced into suitable diameters using (D = 10 or 12.5 or 15 cm) using stainless steel with diamonds embedded in it.
Once sliced , one of the faces of the wafer is given **highly polished mirror finish** and its other face is lapped on a abrasive machine to an acceptable degree of flatness. Then the wafers are rinsed and dried.

B.) Epitaxial Growth:
In this process , a group of wafers are mounted on a rectangular graphite rod called boat and heated in a **gaseous atmosphere of suitable impurity in** reaction chamber at a temperature of 1200˚C by **RF induction coils** encircled around the chamber.
For n-type epitaxial layer , **phosphine (PH_3) gas** is doped into the **silicon tetrachloride hydrogen gas stream.**

$$SiCl_4 + 2H_2 \rightleftharpoons Si + 4\ HCl$$



All the active and passive components are fabricated within this layer.

C.) Oxidation or Thermal Oxidation:

A SiO_2 [silicon dioxide] layer of 0.02 µm to 2 µm thickness is grown on the n-type epitaxial layer as follows:

The silicon wafers are stacked up in a quartz boat and then inserted into a quartz furnace tube. The temperature of the wafers are raised between 950˚C to 1115˚C and exposed to a gas containing O_2 or H_2O or both.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

D.) Photolithography:

Photolithography is the process of using UV rays or X-rays to develop microscopic circuit and devices on semiconductor wafers.

Making of photolithographic mask and photo-etching are the two processes involved in **photolithographic process**

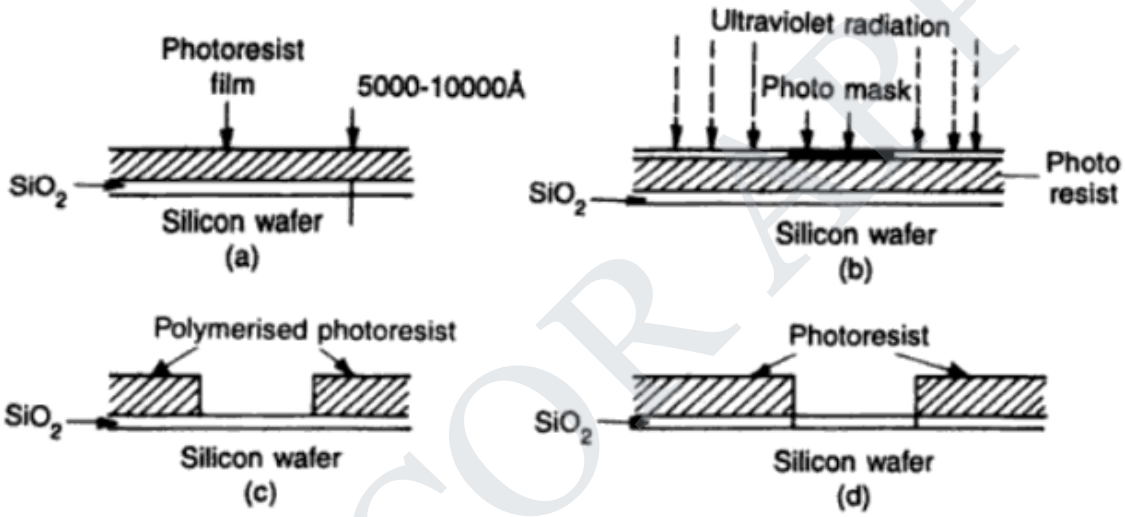
Making of a photographic mask or Masking:

- **Initial Layout or Artwork of an IC normally done at several hundred times larger than the final dimension of the finished monolithic circuit. For a finished monolithic chip of area 50 mils × 50 mils (1 mil = 25 µm) , the artwork will be made on an area of about 60 cm × 60 cm.**
- **The initial layout then decomposed into several mask layers , each corresponding to a step in fabrication. Eg. Mask for base diffusion , Mask for emitter diffusion , Mask for collector diffusion , Mask for metallization.**
- **The artwork is usually produced on a precision drafting machine called as CO-ORDINATOGRAPH. This device outlines the pattern cutting through a red mylar(opaque regions) coated over the artwork without damaging the clear region lying below the opaque region.**
- **This rubylith pattern of individual mask is photographed and then reduced in steps by a factor of 5 or 10 times to finally obtain the exact image size. The final image is photo-repeated many times by a step and repeat camera in a matrix fashion for mass production of ICs.**
- **The step and repeating camera is a device with a photographic plate on a movable platform. Between the exposure , the plate is moved in equal steps so that successive images form in a array or matrix.**

Photo-etching or Wet Etching:

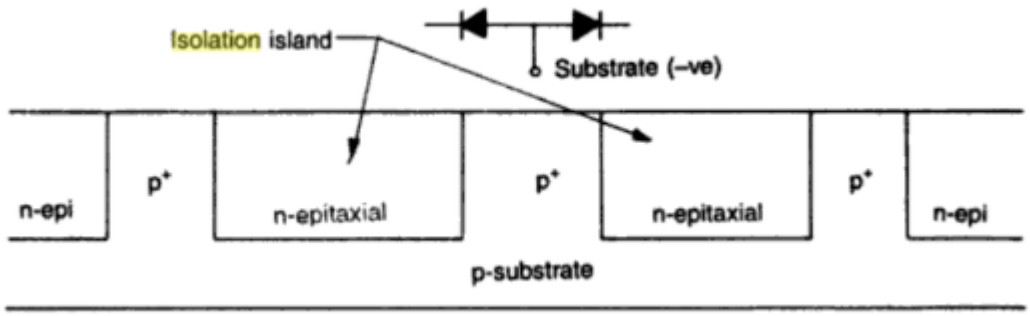
- **This a method of removing silicon dioxide from desired regions so that desired impurities can be diffused.**

- The wafer is coated with photosensitive film namely **KPR(Kodak Photo Resist**) and having a thickness of 5000 $\dot{A}$ to 10,000 $\dot{A}$. The mask negative of the desired pattern is placed over the photo-resist coated wafer.
- Now the mask is exposed to UV rays, so that **KPR becomes polymerized beneath the transparent regions of the mask**.
- The mask is then removed and the wafer is chemically treated with **tricholoroethylene** in order to remove the **unpolymerized regions on the photo-resist**.
- The polymerized photoresist is next cured so that it becomes immune to chemicals called **etchants in the subsequent processing steps.**
- The chip is then immersed in **hydrofluoric acid (etchant)** for removing SiO_2 from areas not protected by KPR.
- After diffusion of impurities , the photo-resist is removed by chemically treating with hot H_2SO_4 (sulfuric acid) and mechanical abrasion.



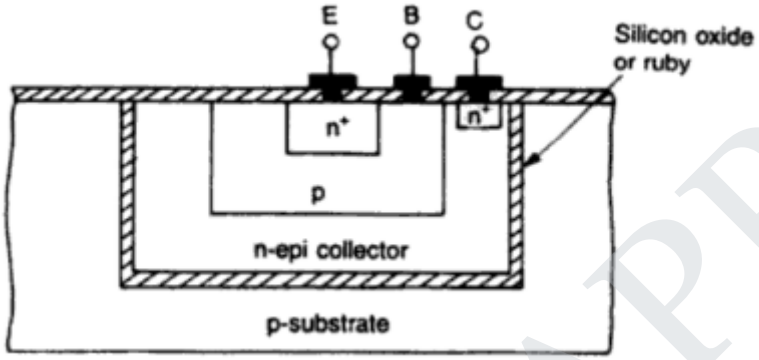
E.) Isolation Techniques:
PN Junction Isolation:
For this , SiO_2 is removed from 5 different places through photolithographic technique.
The wafer is then subjected to heavy p-type diffusion for a long time interval such that they penetrate the n-type epitaxial layer and reach the p-type substrate.
The area under the SiO_2 are n-type islands and are completely surrounded by p-type moats.
Now two things are done:

- **PN junction between the isolation islands are reverse biased (p-type substrate at negative potential and n-type island at positive potential) , so that the islands are electrically isolated from each other**.
- **Acceptor Density in the region between isolation islands ($\approx 5\times 10^{20}$ atoms per cm^{-3}) is generally kept higher than that of p-type substrate(($\approx 1.4\times 10^{15}$ atoms per cm^{-3}) to ensure the reverse biased junctions does not short circuit two adjacent islands.**



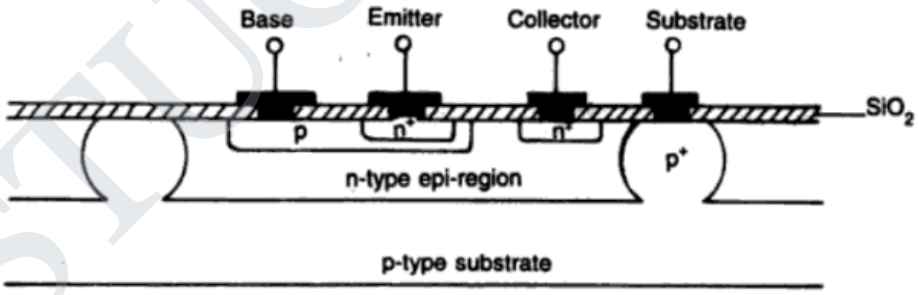
Dielectric Isolation:

- A layer of silicon dioxide (SiO_2) or Ruby(Al_2O_3) is placed around each of the components to provide electrical and physical isolation.
- Due to large thickness of dielectric , capacitance of dielectric is negligible.
- With this method , both npn and pnp transistors can be fabricated within the same silicon substrate.
- This technique is expensive and is usually used for fabrication of professional grade ICs required for applications like military and aerospace.



F.) Diffusion or Thermal Diffusion:

- 20 cleaned wafers are placed in a quartz boat and both of them placed in a quartz furnace and heated to a temperature of 1000˚C.
- Now either p-type or n-type impurities introduced into the wafer in the vapour form.
- N-type impurities such as phosphorous are introduced in the form of $POCl_3$ (Phosphorous Oxychloride) or P_2O_5 (Phosphorous Pentoxide).
- P-type impurities such as boron are introduced in the form of B_2O_3 (Boron Trioxide) or BCl_3 (Boron Tricholride).
- Dry Oxygen or Dry nitrogen used to carry the impurities to the furnace.
- Time taken for diffusion is usually of the order of 2 hours ; Diffusion of impurities usually takes place laterally(Horizontally) or Vertically.



H.) Ion Implantation :

- Silicon Wafers placed in a vacuum chamber called as target chamber and exposed to a beam of high energy dopant ions(Boron for P-type ; Phosphorous for N-type).
- Accelerating voltage for the ions is between 20 kV to 250 kV.
- Ions striking the wafer penetrate some small distance into the wafer. Depth of penetration increases with increase in accelerating voltage.

Advantages:

- Low temperature process.
- Less lateral diffusion of impurities
- Accelerating potential and beam current electrically controlled from outside.

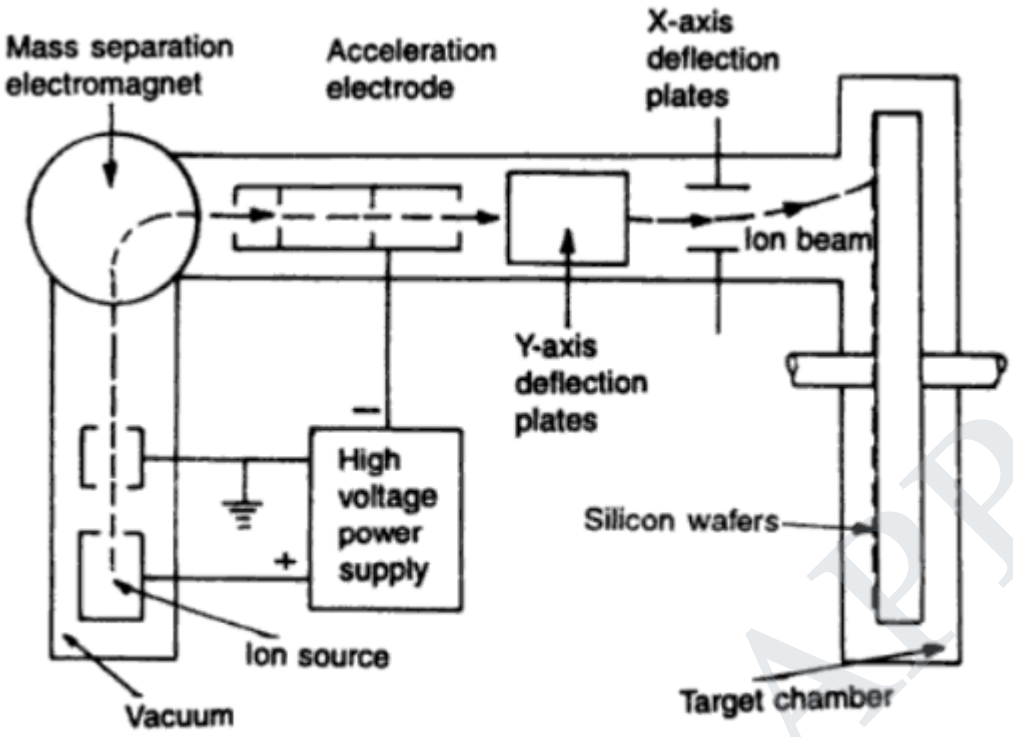


Fig. 1.10 Ion implantation system

I.) Metallization:

Producing a thin aluminium film layer (1 μm) on the substrate to make interconnection of various components on the chip.

Advantages of Aluminium for metallization:

- Good conductor
- Can be easily deposited using vacuum deposition technique.
- Makes good mechanical bond with silicon.
- Forms low resistance ohmic contact with lightly doped p-type silicon and heavily doped n-type silicon.

Process of metallization:

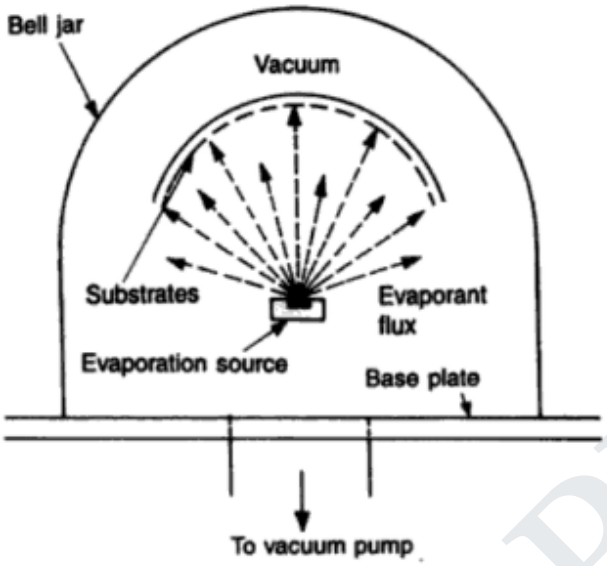


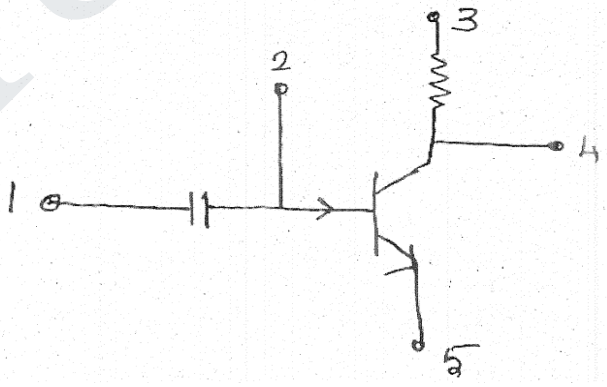
Fig. 1.12 Vacuum evaporation for metallization

- Pressure in the vacuum chamber reduced to 10^{-6} to 10^{-7} torr (1 torr = 760 mm of mercury).
- Aluminium is placed in a resistance-heated tungsten coil or basket ; A very high power density electron beam is focussed at the surface of aluminium.
- The aluminium gets vaporized , flows in a straight line path in all directions , hit the substrate and condense to form a thin film.
- The aluminium film is patterned by photolithographic process to produce required connections and bonding pad configuration.
- Unwanted aluminium films during photolithography process removed by treating with H_3PO_4 (Phosphoric Acid).

J.) Assembly Processing and Packaging:

- A diamond tipped tool taken and create cut lines on the surface of the wafer along the rectangular grid. The cut lines separate the individual chips. This process is called **scribing and cleaving**.(Scribing is to create cut lines ; Cleaving is separating the cut lines).
- Each individual chip mounted on a ceramic wafer and attached to a suitable package.

2. Explain the fabrication process in the following circuit diagram (Figure 1) (10)



(Or)

Briefly explain the various process involved in fabrication of monolithic IC which integrates diode , capacitance and FET (13)

(Or)

Explain in detail the recent fabrication methods of diode and capacitance for industrial applications. (15)

[In case of **FET replace base region with Gate region and base diffusion as gate diffusion ; Collector region as drain region ; Emitter region as Source region].**

Step 1 : Silicon Wafer Preparation

P-type substrate prepared as follows:

(i) Crystal Growth and Doping

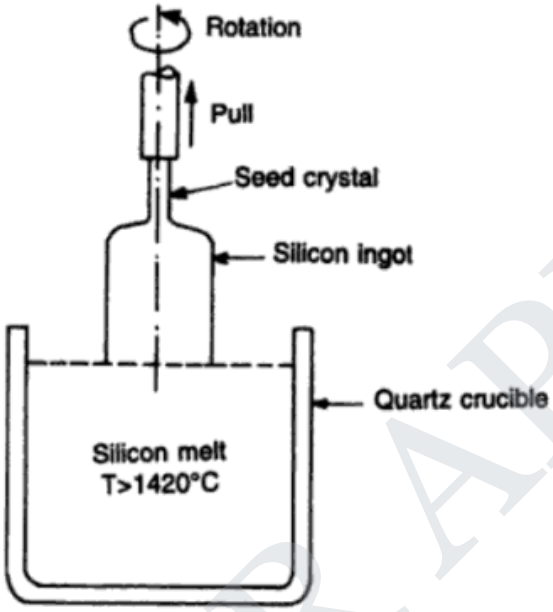


Fig. Czochralski Crystal Growth

The process of fabricating a **silicon ingot is called crystal growth.** In this method , a 99.5% pure polycrystalline silicon is doped with suitable impurity and heated in a crucible to form a melt.

A seed crystal is dipped into the melt and slowly taken out while the crucible is made to rotate in a direction opposite to that of seed crystal. This is called **crystal pulling.**

The silicon ingot is sliced into suitable diameters using (D = 10 or 12.5 or 15 cm) using stainless steel with diamonds embedded in it.

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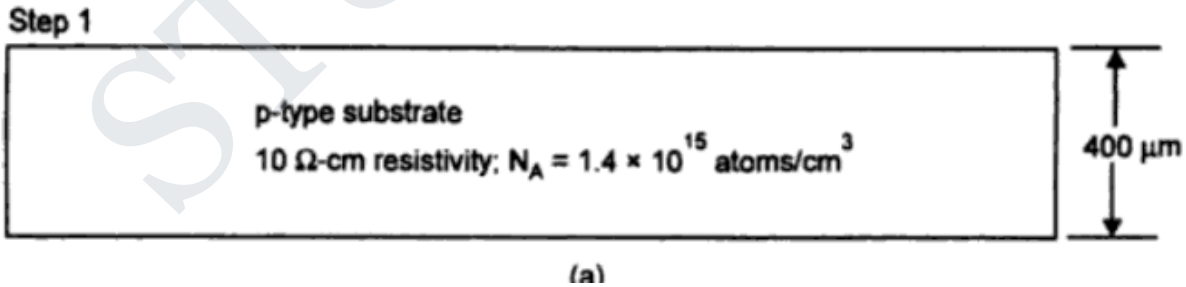


(a)

Step 2: Epitaxial Growth:

A n-type epitaxial film (5-25µm) is grown over the p-type substrate by the following process:

In this process , a group of wafers are mounted on a rectangular graphite rod called boat and heated in a **gaseous atmosphere of suitable impurity in** reaction chamber at a temperature of 1200˚C by **RF induction coils** encircled around the chamber.

For n-type epitaxial layer , **phosphine (PH_3) gas** is doped into the **silicon tetrachloride hydrogen gas stream.**

$$SiCl_4 + 2H_2 \rightleftharpoons Si + 4\ HCl$$

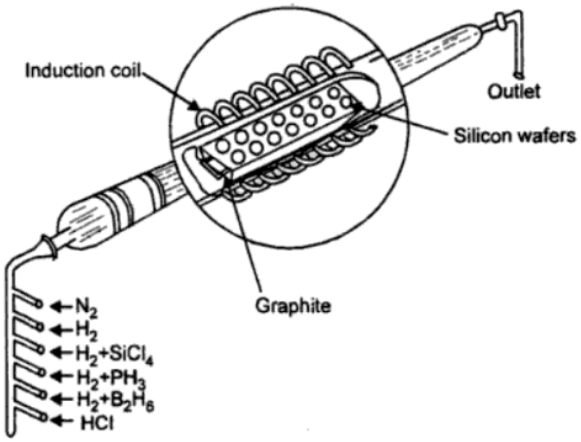
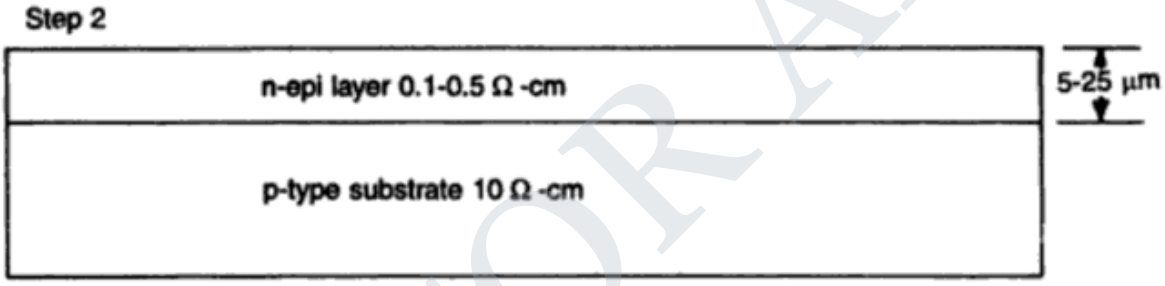


Fig. System for growing silicon epitaxial films

The resistivity of the n-type epitaxial layer is 0.1 to 0.5 Ω-cm. This layer serves as the

→ **Collector region of the BJT**
→ **Element of a diode**
→ **Diffused capacitor**



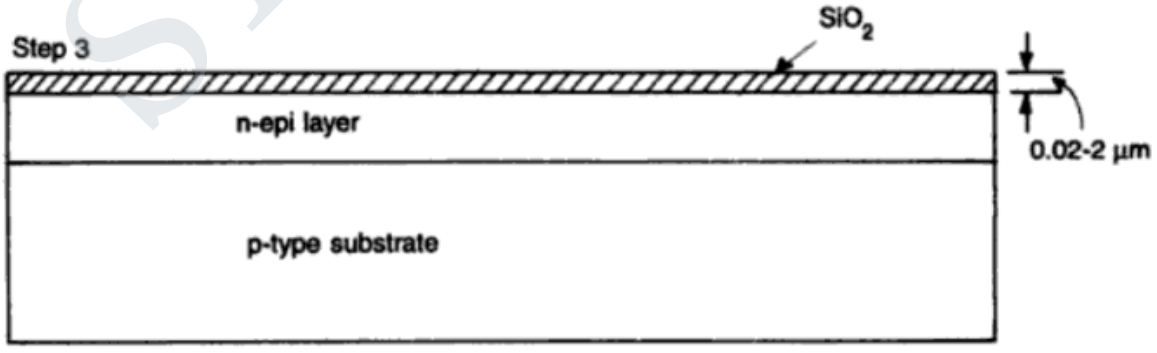
All the active and passive components are fabricated within this layer.

Step 3: Oxidation or Thermal Oxidation:

A SiO_2 [silicon dioxide] layer of 0.02 µm to 2 µm thickness is grown on the n-type epitaxial layer as follows:

The silicon wafers are stacked up in a quartz boat and then inserted into a quartz furnace tube. The temperature of the wafers are raised between 950˚C to 1115˚C and exposed to a gas containing O_2 or H_2O or both.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$



(c)

Step 4: Isolation Diffusion:

The process of physically separating the components on a silicon substrate is called **isolation diffusion.** The wafer is subjected to heavy p-type diffusion for a long time interval such that they penetrate the n-type epitaxial layer and reach the p-type substrate.

The area under the SiO_2 are n-type islands and are completely surrounded by p-type moats.
Now two things are done:

- **PN junction between the isolation islands are reverse biased (p-type substrate at negative potential and n-type island at positive potential) , so that the islands are electrically isolated from each other**.
- **Acceptor Density in the region between isolation islands (≈ 5× 10^{20} atoms per cm^{-3}) is generally kept higher than that of p-type substrate((≈ 1.4× 10^{15} atoms per cm^{-3}) to ensure the reverse biased junctions does not short circuit two adjacent islands.**

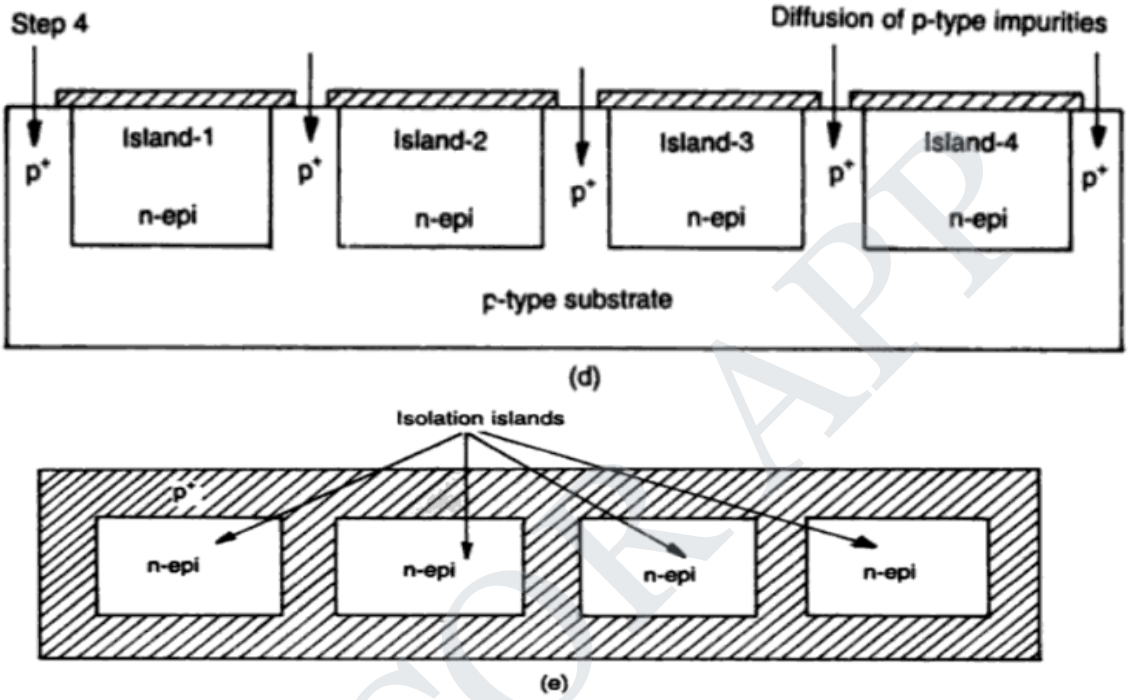
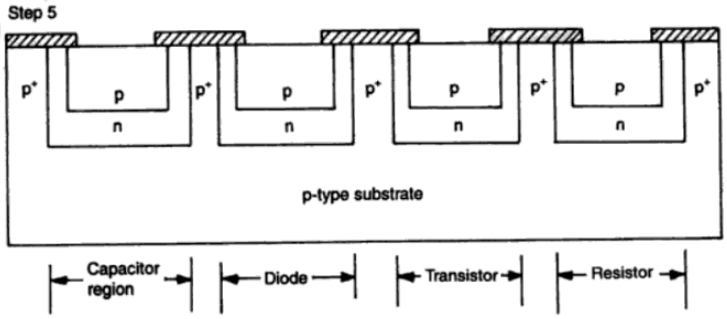


Fig. 1.14 (a-e) Steps in the fabrication of the circuit shown in Fig. 1.3

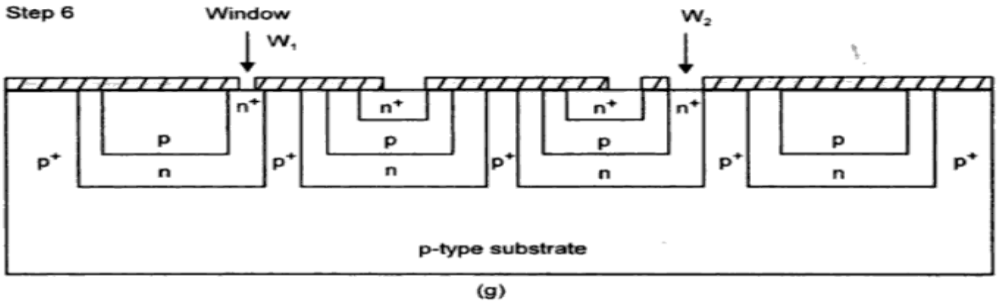
Step 5 : Base Diffusion:
A new layer of silicon dioxide is grown over the entire wafer and a new pattern of openings formed through photolithographic technique through which p-type impurities (such as boron) is introduced into the n-type epitaxial silicon. This diffusion is used to form the following:

→ Base region of the transistor
→ Resistor
→ Anode of the diode
→ Junction Capacitor



Step 6: Emitter Diffusion:
A new layer of silicon dioxide is grown over the entire wafer and a new pattern of openings formed through photolithographic technique through which heavily doped (≈2 × 10^{20} cm^{-3}) n-type impurities (such as phosphorous) is introduced into the n-type epitaxial silicon. This diffusion is used to form the following:

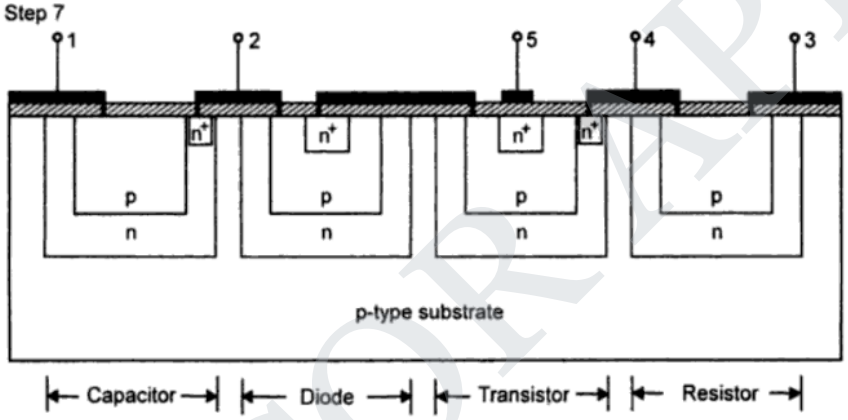
→ **Emitter region of the transistor**
→ **Cathode region of the diode**



(g)

Step 7: Aluminium Metallization

A new layer of silicon dioxide is grown over the entire wafer and a new pattern of openings formed through photolithographic technique where interconnections have to be made between the components. A thin coating of aluminium is **vacuum deposited** over the entire surface of the wafer and the interconnection pattern between the components made by **photo-resist technique**.



3. Discuss the different ways to fabricate the diodes (10)

Grown Junction Diode:

- Diodes formed from crystal pulling process
- P-type and N-type impurities alternately added to the molten semiconductor in the crucible. When pulled , a crystal with grown PN junction obtained.
- Slice the obtained ingot into smaller pieces.
- Diodes are suitable for only low frequency operation.
- Capable of handling large currents.

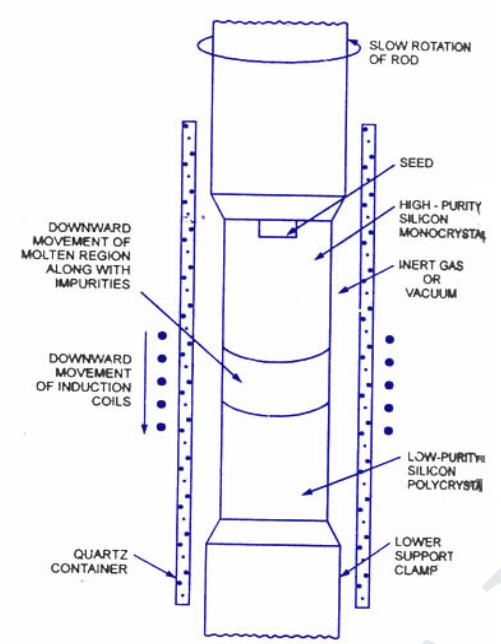
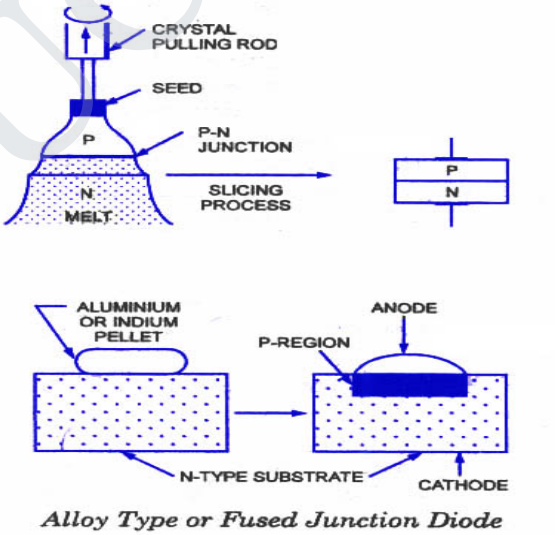


Fig. Grown Junction Diode

Alloy Type or Fused Junction Diode:

- P-type impurity placed over a N-type crystal and heated till liquefaction occurs and two materials meet.
- On cooling , a PN junction formed at the boundary of alloy substrate.
- Alternately a N-type impurity placed over a P-type crystal and heated till liquefaction occurs and two materials meet.
- Alloy type diodes have large current and PIV(Peak Inverse Voltage) rating.
- Suitable for low frequency operation

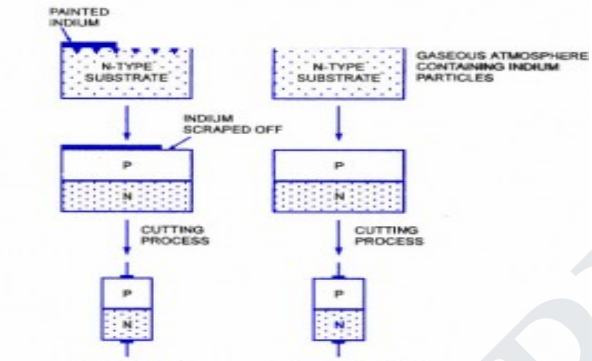


Alloy Type or Fused Junction Diode

Diffused Junction Diode

- Diodes formed due to either solid diffusion or gaseous diffusion.
- In solid diffusion , a p-type layer formed on n-type substrate and both heated till the impurity diffuses into the n-type layer.
- Formed PN junction device cut into smaller pieces.
- Metallic contacts made for forming anode and cathode.

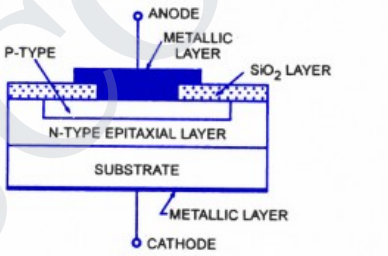
- In gaseous diffusion, the n-type substrate is placed in a atmosphere of P-type impurity gas and both heated till the impurity diffuses into the n-type layer.
- Diffusion takes more time than alloy formation of diode , but less expensive and can be accurately controlled.
- Diffusion process allows simultaneous fabrication of multiple diodes over a semiconductor disc and is the most commonly followed discrete diode fabrication method.



Diffusion Process

Epitaxial Growth or Planar Diffused Diode:

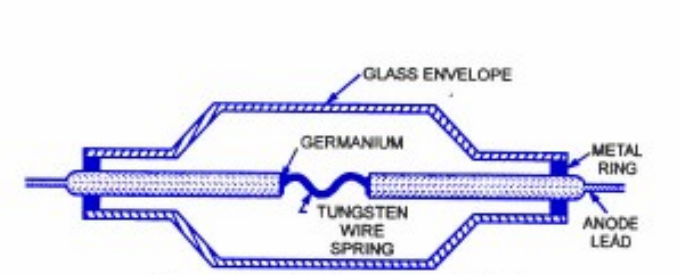
- A heavily doped n-type semiconductor layer grown on heavily doped substrate. Both the layer and substrate are made out of the same material.
- P-type semiconductor material diffused into the n-type semiconductor layer.
- Silicon dioxide thermally grown on top surface , photo-etched and then aluminium contact made to P-region. Metallic layer formed over the P-region ; Anode terminal is attached to it.
- Metallic layer formed at the bottom of the substrate; Cathode terminal is attached to it.
- Most commonly followed Diode IC fabrication method.



Epitaxially Grown or Planar Diffused Diode

Point Contact Diode:

- One of the faces of N-type semiconductor soldered to a metallic base by RF heating Another face pressed against a phosphor bronze or tungsten spring; Tungsten spring placed inside a glass envelope.
- A pulsating current causes P-type region to be formed around the tungsten spring or wire ; Formed PN junction is hemispherical in shape.
- Forming process cannot be controlled by precision.
- Handles small currents and suitable for very high frequency applications.



Germanium Point Contact Diode

4. Explain how a monolithic capacitor can be fabricated (6)

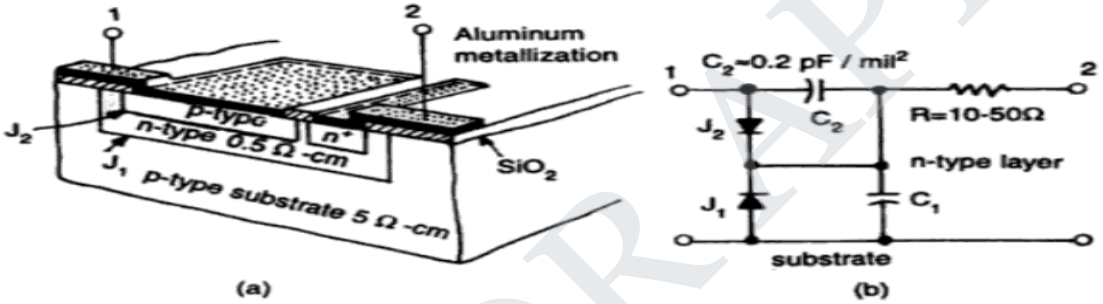
Following are the two methods of obtaining integrated capacitor:

(i) Junction Capacitor

(ii) MOS Capacitor

(iii) Thin Film Capacitor

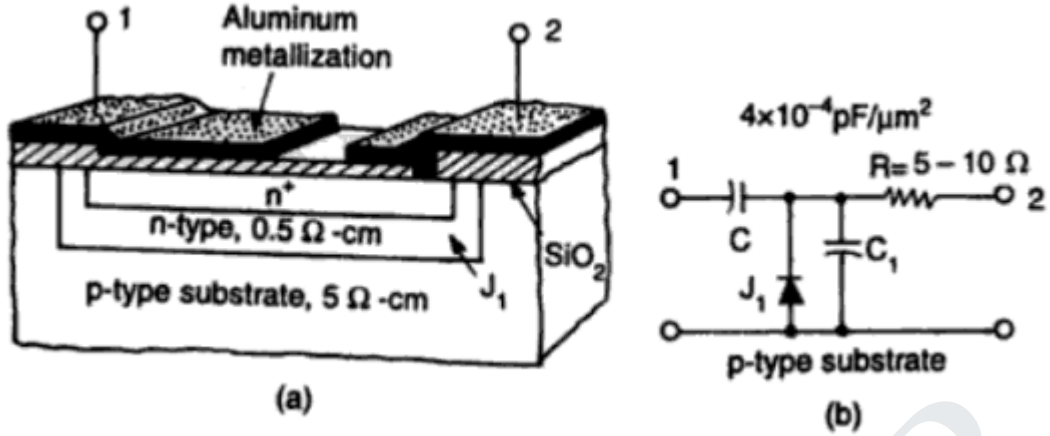
(i) Junction Capacitor:



- Two junctions J_1 and J_2 are present .
- Reverse biasing J_2 produces desired polarised capacitance C_2 ; C_1 is the parasitic capacitance between n-type epitaxial layer and substrate ; R is the series resistance due to the n-region.
- C_1 minimized by keeping the substrate at most negative potential.
- C_2 depends on (a) Area of J_2 (b) Impurity concentration of n-type epitaxial layer (c) Voltage across J_2.

(ii) MOS Capacitor:

- Parallel plate capacitor with silicon dioxide as dielectric.
- Heavily doped n+ region formed during emitter diffusion forms the lower plate.
- Thin film of aluminium metal forms the upper plate .
- The parasitic elements involved are (i) Series resistance due to n+ region (ii) Series resistance due to collector junction J_1 (iii) Capacitance of J_1.
- Non-polar capacitor and capacitance independent of applied voltage.
- Alternative to silicon dioxide , silicon nitride can be used as dielectric.
- Silicon nitride has high dielectric constant compared to Silicon dioxide.



(iii) Thin Film Capacitor

- Aluminium or tantalum used as capacitor plates.
- Aluminium Oxide(Al_2O_3) used as dielectric for small capacitors ; Tantalum Oxide (Ta_2O_5) used as dielectric for large capacitors.
- Gets irreversibly destroyed when voltage rating exceeds breakdown value of dielectric.

5. What is thick and thin film technology ? Explain various methods used for deposition of thin film technology (16)

Thin and Thick film technology is used to make passive components like resistors and capacitors. Thin films are the ones with thickness 50 *Å* (0.0001 mil)to 20000 *Å* (0.08 mil), whereas thick films vary from 1,25,000 *Å* (0.5 mil) to 6,25,000 *Å* (2.5 mil).

Various methods used in the deposition of thin film are

→ Vacuum Evaporation
→ Sputtering
→ Gas Plating
→ Electroplating
→ Electroless plating
→ Silk Screening

Vacuum Evaporation:

Producing a thin aluminium film layer (1 μm) on the substrate to make interconnection of various components on the chip.

Advantages of Aluminium for metallization:

- Good conductor
- Can be easily deposited using vacuum deposition technique.
- Makes good mechanical bond with silicon.
- Forms low resistance ohmic contact with lightly doped p-type silicon and heavily doped n-type silicon.

Process of metallization:

- Pressure in the vacuum chamber reduced to 10^{-6} to 10^{-7} torr (1 torr = 760 mm of mercury).
- Aluminium is placed in a resistance-heated tungsten coil or basket ; A very high power density electron beam is focussed at the surface of aluminium.
- The aluminium gets vaporized , flows in a straight line path in all directions , hit the substrate and condense to form a thin film.
- The aluminium film is patterned by photolithographic process to produce required connections and bonding pad configuration.
- Unwanted aluminium films during photolithography process removed by treating with H_3PO_4 (Phosphoric Acid).

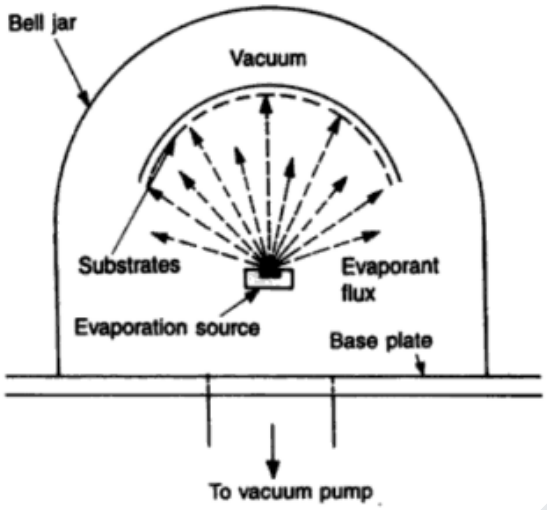


Fig. 1.12 Vacuum evaporation for metallization

Cathode Sputtering:

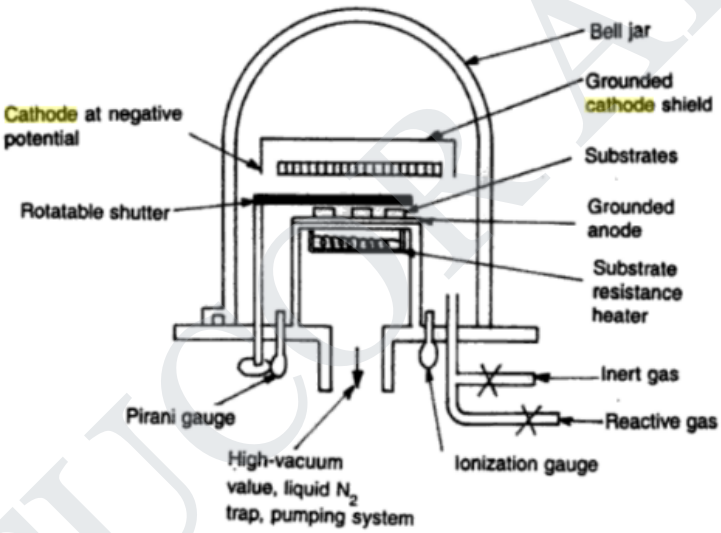


Fig. 1.30 The principal parts of sputtering system

- This method is slower than vacuum evaporation technique and involves minutes to hours deposition of micron-thick film.
- Sputtering method is superior and costlier compared to vacuum evaporation technique.
- Cathode sputtering is generally carried out at a pressure of 10^{-12} torr. The material to be sputtered is first intensely bombarded by argon gas particles. These gas ions are accelerated by making material to be sputtered as the cathode.
- The high energy gas particles then emitted from the cathode , diffuse through the low pressure gas and deposited as a thin film on a nearby substrate. This results in a very uniform thin film with **good crystal structure and adhesion**.
- A potential typically 2 kV to 5 kV is applied between cathode(material to be sputtered or source material) and anode. During the sputtering process , **glow is produced in the space between anode and cathode**.

Plating Technique:

Two types of plating technique are commonly followed:

Electroplating:

- Involves coating an object with one or more layers of different metals

- Cathode is a substrate and Anode is a metal. Both are immersed in a electrolytic solution. When dc is passed through the solution , positive metal ions migrate from anode to cathode and get deposited there. This method is useful for making **conductive gold or copper films**.

Electroless plating:

- Metal ion in the solution reduced to free metal and deposited as a metallic coating without passing dc. This method is useful for depositing metals of considerable thickness on any substrate such as glass , ceramic , plastic etc.

6. Explain the different types of IC packages (8)

Or

Write a note on classification of IC and IC packages (13)

Through Hole Package:

- Components are placed onto drilled holes on a bare PCB.
- Best suited for products that require strong connection between layers.
- Through hole components can withstand more environmental stress when compared to surface mounted components.
- Through Hole packages are of two types : (i) Axial Leads (ii) Radial Leads. In axial leads , the pins protrude horizontally on either side of the package. In radial leads , the pins protrude vertically from the package.

Example : SIP (Single Inline Package) ; DIP(Dual Inline Package) ; ZIP(Zigzag Inline Package).

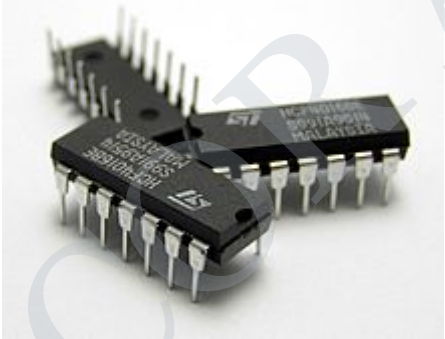
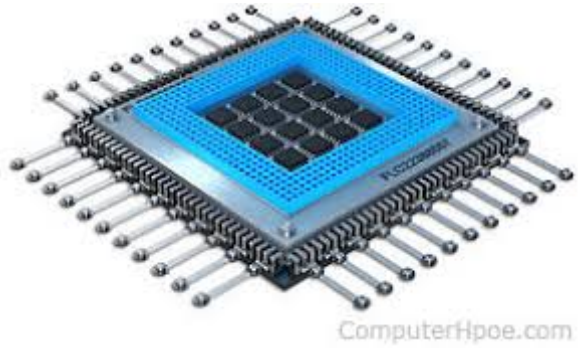


Fig. DIP

Surface Mounting Technology(SMT) or Planar Mounting Package :

- Components are placed directly on the surface of bare PCB.
- Has better electromagnetic compatibility due to smaller radiation loop area.
- Has lower R-L value at the connection points.
- Fewer holes needs to be drilled.

Example : SOD(Small Outline Diode) , MELF(Metal Electrode Leadless Face), LGA(Land Grid Array).



Chip Carrier Package:

- Rectangular Package with contacts on all four edges.

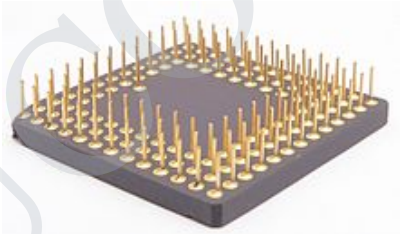
- Two types of chip carrier : (i) Leaded Chip Carrier (ii) Leadless Chip Carrier
- In leaded chip carriers , metal leads are wrapped around the edge of the package.
- In leadless chip carriers , metal pads are wrapped around the edge of the package.
- Chip carriers usually made out of ceramic or plastic.
- Placed in a PCB through the process of soldering

Example : BCC(Bump Chip Carrier) , PLCC(Plastic Leaded Chip Carrier) , DLCC(Dual Leadless Chip Carrier)

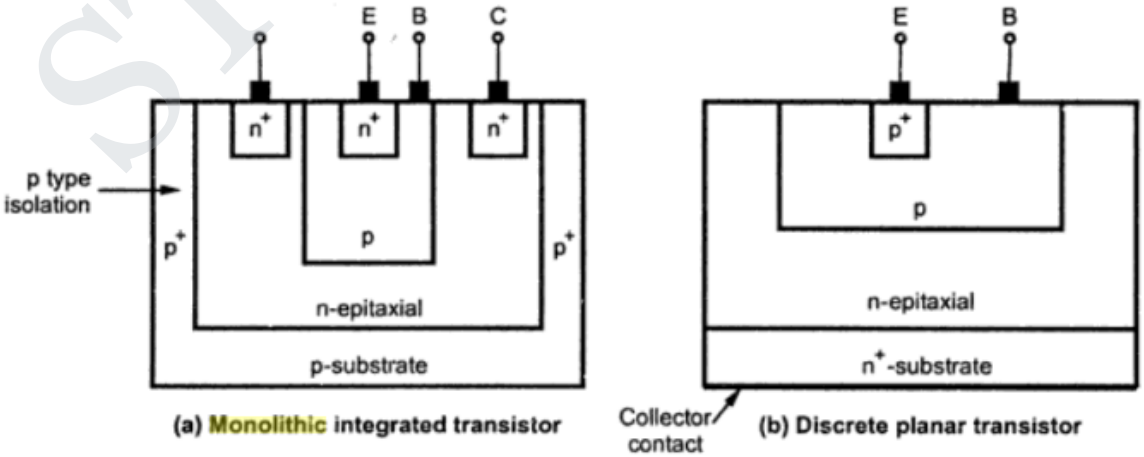
PGA(Pin Grid Array**)**:

- Square or Rectangular package , in which the pins are placed on bottom side of the package.
- Mounted on PCBs either through through hole technology or into a socket.
- Preferred for microprocessors with larger width data-buses.
- Cheaper than BGA(Ball Grid Array) and other grid arrays.

Example : OPGA (Organic Pin Grid Array) , PAC(Pin Array Catridge) , CGPA(Ceramic Pin Grid Array)



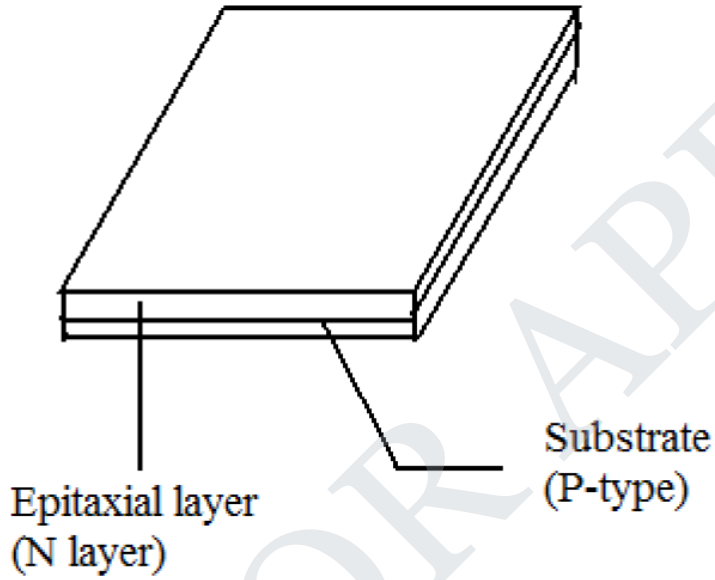
7. Explain the various steps involved in the fabrication of typical transistor in monolithic ICs (13)



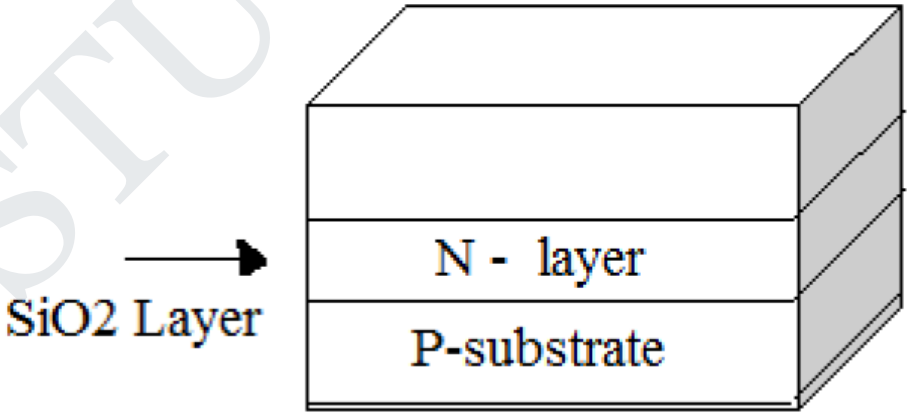
Fabrication of monolithic transistors (BJT) include the following:

Epitaxial Growth:

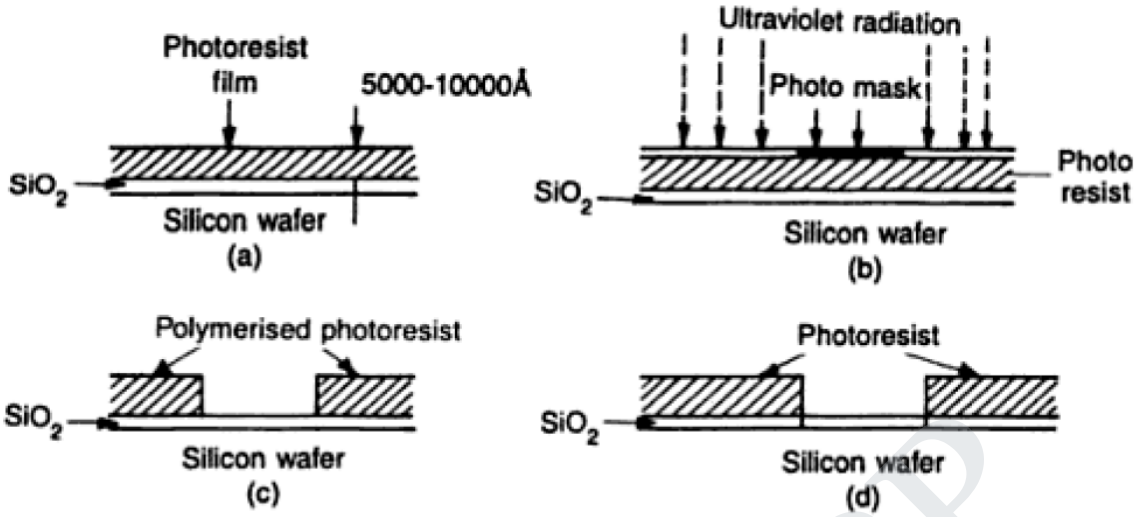
- First step in fabrication of BJT is to create collector region.
- A P-type silicon substrate of acceptor density $N_A = 1.4 \times 10^{15}$ atoms/cm^3 and resistivity is fabricated using **czhochraski technique**.
- A **heavily doped n-type region called as** buried layer is grown over the substrate by diffusion process.
- Another N-type layer is grown over the **buried region** through **epitaxial process**. This epitaxial region is called **active region or collector region of BJT.**
- The **buried layer reduces the collector resistance of BJT**.



Oxidation :
A silicon dioxide layer is grown over the **epitaxial layer by exposing the silicon substrate to a oxygen atomosphere at 1000˚C.**



Photolithography:



- The silicon dioxide layer in the wafer is coated with a thin **photo-emulsive solution called as photo-resist.**
- Then a mask , black and white negative of the required pattern placed over the photo-resist and the silicon wafer is exposed to **UV rays**.
- The photo-resist under the transparent region(white) of the mask gets polymerized. The photo-resist under the opaque(black) region of the mask remains unpolymerized.
- The polymerized region is cured so that it becomes resistant to corrosion. The unpolymerized regions are removed by dipping the wafer in **HF(Hydro Fluoric)** acid. This creates opening for the diffusion of P-type and N-type impurities to be diffused.
- Once P-type and N-type impurities are diffused , the polymerized region is removed by dipping the wafer in **H_2SO_4 (Sulphuric Acid)** and by mechanical abrasion.

PN Junction Isolation Diffusion:
The PN junction Isolation diffusion involves creation of **heavily doped p-type region around the transistor. This region is called MOAT**.
The epitaxial layer and the p-type moat forms a back-to-back PN junction.
When the P-type substrate is held at negative potential , the two back to back PN diodes gets reverse biased thereby providing the required **electrical and physical isolation between BJT and its adjacent components.**

Base Diffusion:
A new layer of silicon dioxide is grown over the entire wafer and a new pattern of openings formed through photolithographic technique through which p-type impurities (such as boron) is introduced into the n-type epitaxial silicon. This diffusion is used to form the b**ase region of the transistor**

Emitter Diffusion:
A new layer of silicon dioxide is grown over the entire wafer and a new pattern of openings formed through photolithographic technique through which heavily doped ($\approx 2 \times 10^{20}$ cm^{-3}) n-type impurities (such as phosphorous) is introduced into the n-type epitaxial silicon. This diffusion is used to form the e**mitter region of the transistor.**

Aluminium Metallization
A new layer of silicon dioxide is grown over the entire wafer and a new pattern of openings formed through photolithographic technique where interconnections have to be made between the components. A thin coating of aluminium is **vacuum deposited** over the entire surface of the wafer and the interconnection pattern between the components made by **photo-resist technique**.

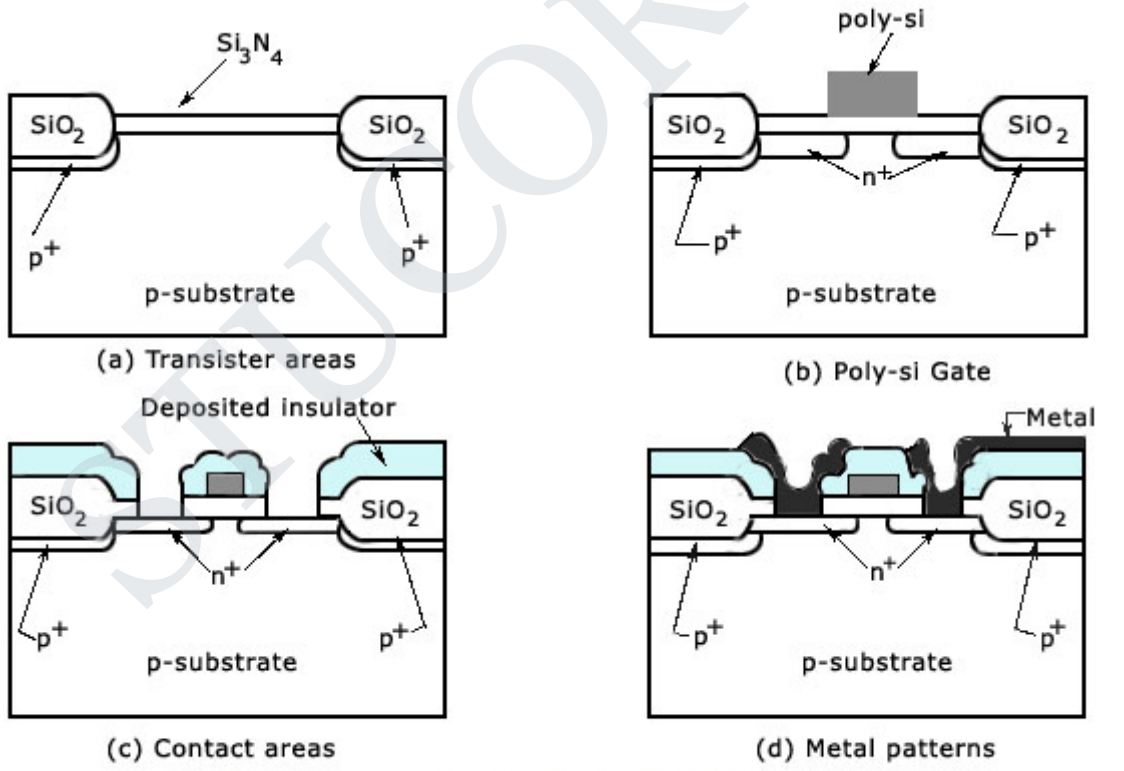
Assembly Processing and Packaging:

- A diamond tipped tool taken and create cut lines on the surface of the wafer along the rectangular grid. The cut lines separate the individual chips. This process is called **scribing and cleaving**.(Scribing is to create cut lines ; Cleaving is separating the cut lines).
- Each individual chip mounted on a ceramic wafer and attached to a suitable package.

8. Elaborate the fabrication of MOS ICs with suitable diagram (13)

The fabrication sequence of NMOS ICs is as follows:

- By the process of chemical vapor deposition , silicon nitride (Si_3N_4) deposited on the entire wafer surface. Through photolithographic process , the area where MOS IC has to be fabricated is defined. Si_3N_4 is removed from regions outside the area defined for transistor. This region is called **inactive or field region**. Boron is implanted in the inactive region to avoid short circuit between MOS IC and adjacent circuit.
- Now the wafer is subjected to **local or selective oxidation.** 1 μm SiO_2 grow in the inactive regions and not in the area defined for transistor. Si_3N_4 prevents oxidation.
- Si_3N_4 is removed from transistor areas. 0.1 μm SiO_2 grown in the transistor area. Then polysilicon grown over the entire wafer. Through photolithographic process , pattern for gate electrode formed in the transistor region. The polysilicon outside the transistor region removed by **chemical or plasma etching**.
- The polysilicon regions where source and drain regions are to be fabricated within the transistor area made **heavily doped n-type** by **diffusion or ion-implantation**.



Sectional views showing in MOS fabrication process

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- Again a SiO_2 layer grown over the entire wafer by **local or selective oxidation**. Through photolithography process , the regions for making **electrical contacts(terminals)** for the gate , source and drain regions are made.

- Through **plasma or chemical etching** , the contact regions are exposed for **aluminium metallization**.
- The SiO_2 used as the insulating field oxide between gate electrode and n-channel has high resistance of 10^{10} Ω to 10^{15} Ω.
- The gate electrode made out of either **aluminium or polycrystalline silicon**. If gate electrode made out of aluminium , MOSFET called **Metallic Gate Electrode MOSFET**. If gate electrode made out of **polysilicon(or polycrystalline silicon)**, MOSFET called **Silicon Gate Electrode MOSFET**.
- Aluminium Gate electrode MOSFET has threshold voltage between 3 V to 6 V. Polysilicon Gate electrode MOSFET has threshold voltage between 1 V to 2 V.
- Two types of field oxide present in MOSFET. **Thick field oxide (5000 *Å* to 10,000 *Å*) outside drain and source regions. Thin field oxide (300 *Å* to 800 *Å*) below the gate electrode**.

Advantages of Polysilicon Gate electrode MOSFET:

- In conventional(**aluminium)** gate electrode MOSFET , gate electrode overlaps with the edges of drain and source regions to avoid **masking errors**. The C_{GD}(Gate-Drain Overlap capacitance) and C_{GS}(Gate-Source Overlap capacitance) of the order of 1 pF to 3 pF lower the operating speed of MOSFET.
- Two diodes formed: (i) Between Drain and Substrate (ii) Between Source and Substrate. By applying positive voltage to drain , these two diodes are reverse biased , thereby allowing the current to flow through n-channel. Therefore separate isolation islands are not required.

9. Explain the fabrication of FET in detail

JFET Fabrication:

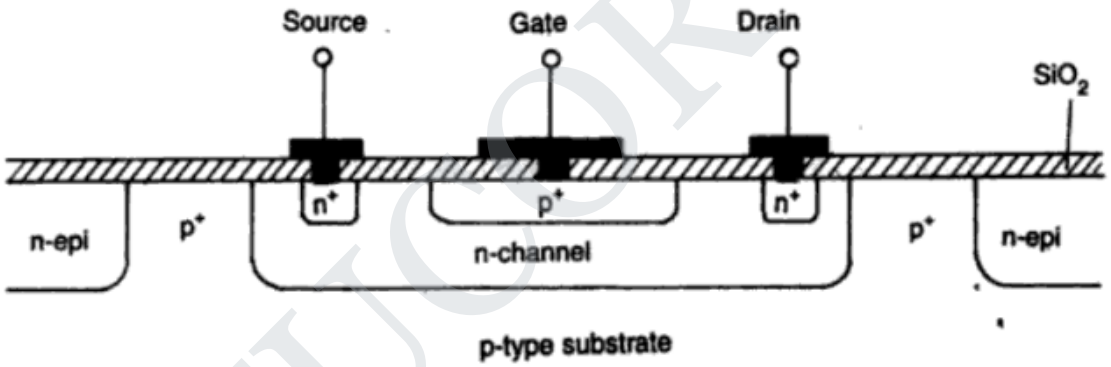

Fig. N-channel JFET Structure

- The process used for fabrication of JFET same as fabrication of BJT.
- Epitaxial layer serves as the n-channel of JFET.
- The p^+ gate is formed in n-channel by the process of **diffusion or ion implantation**.
- The n^+ regions formed under the drain and source contact regions for providing **ohmic or non-rectifying contacts**.

MOSFET(Enhancement NMOS) Fabrication:

The fabrication sequence of NMOS ICs is as follows:

- By the process of chemical vapor deposition , silicon nitride (Si_3N_4) deposited on the entire wafer surface. Through photolithographic process , the area where MOS IC has to be fabricated is defined. Si_3N_4 is removed from regions outside the area defined for transistor. This region is called **inactive or field region**. Boron is implanted in the inactive region to avoid short circuit between MOS IC and adjacent circuit.
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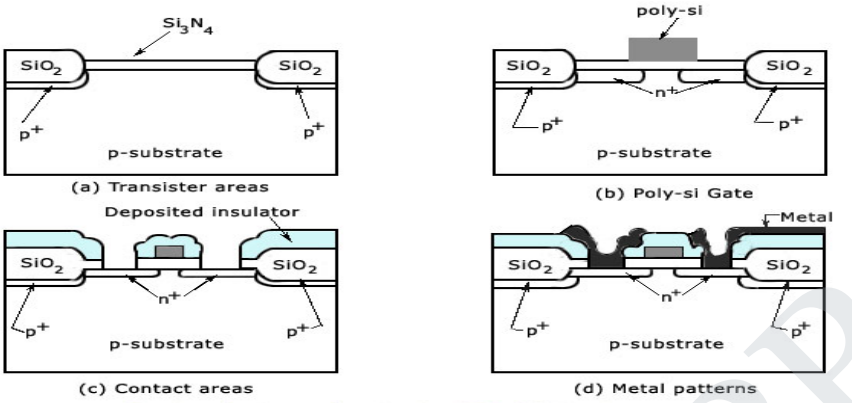

Sectional views showing in MOS fabrication process

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- Again a SiO_2 layer grown over the entire wafer by **local or selective oxidation**. Through photolithography process , the regions for making **electrical contacts(terminals)** for the gate , source and drain regions are made.
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- Two diodes formed: (i) Between Drain and Substrate (ii) Between Source and Substrate. By applying positive voltage to drain , these two diodes are reverse biased , thereby allowing the current to flow through n-channel. Therefore separate isolation islands are not required.

CMOS(Complementary MOSFET) Fabrication:

Series connection of NMOS and PMOS transistors yield CMOS transistors.

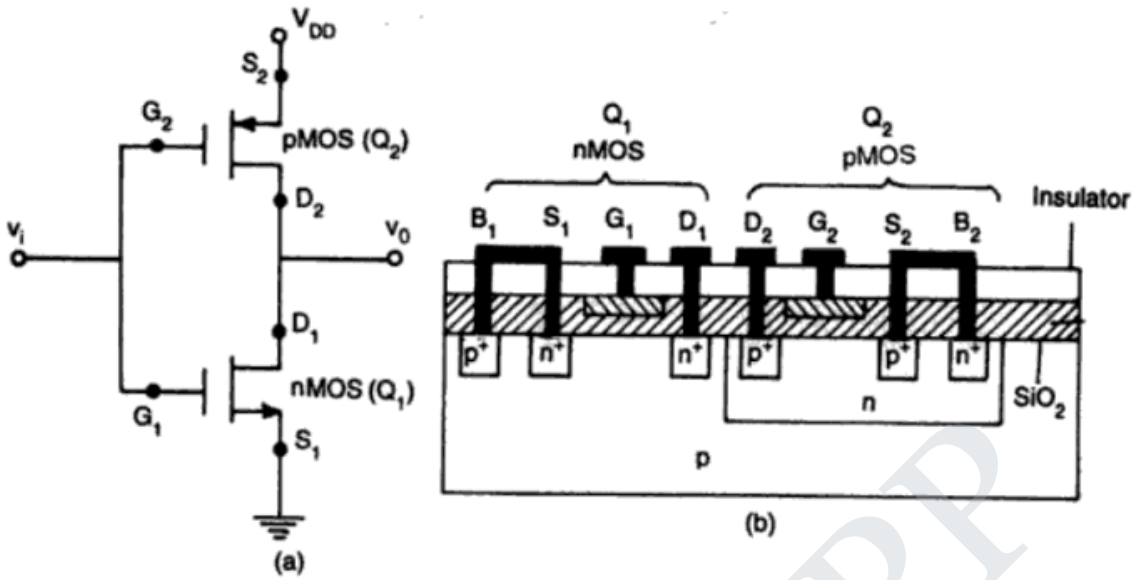


Fig. 1.29 (a) CMOS inverter, (b) Cross-section of CMOS IC

- Polysilicon Gate electrode NMOSFET fabricated within the p-type substrate. Polysilicon Gate electrode PMOSFET fabricated within a n-type tub or well formed in p-type substrate.
- P-type substrate forms the **body terminal of NMOS transistor**. N-type tub or well forms the **body terminal of PMOS transistor**.
- Formation of n-type tub or well and diffusion or ion implantation of p-type drain and source regions are additional steps required for fabrication of PMOS when compared to NMOS.
- Two diodes are formed : (i) Between **body and source terminals of NMOS transistor** (ii) Between **body and source terminals of PMOS transistor**.
- By connecting body terminal of NMOS transistor(B_1) to GND and body terminal of PMOS transistor (B_2) to V_{DD} , the diodes are reverse biased thereby isolating the NMOS and PMOS transistors.

10. Describe the methods in thick film technology? (13)

Screen Printing:

- Stainless steel wire based screen woven to a mesh size of 320 and mounted on a aluminium frame under uniform tension.
- Photo-emulsive solution coated over the screen and polymerized by exposure to light.
- Mask of the desired pattern kept over the photo-emulsion and developed on exposure to light.
- Screen is clear wherever thick film to be deposited and blocked by photoresist in other regions.
- Screen now placed on a substrate and carefully aligned components are deposited on the substrate by moving a constant velocity squeegee over the screen.
- Squegee forces an ink in the form of a paste through the patterned screen.

Ceramic Firing:

- The desired thermal and electrical properties of thick film deposited by screen printing achieved through **ceramic firing** process.
- The thick film placed in a furnace or kiln operating at 500 ˚C to 1000 ˚C and having four to eight control zones.
- Organic binders of thick film vaporizes and remaining material fuses with substrate , thereby becoming part of ceramic structure.
- Since structure and dimensions of thick films not compatible with monolithic circuits , thick film technology mostly suitable for fabrication of **Hybrid IC**s.

11. Explain in detail about photolithography process with neat diagram (7)

Photolithography:

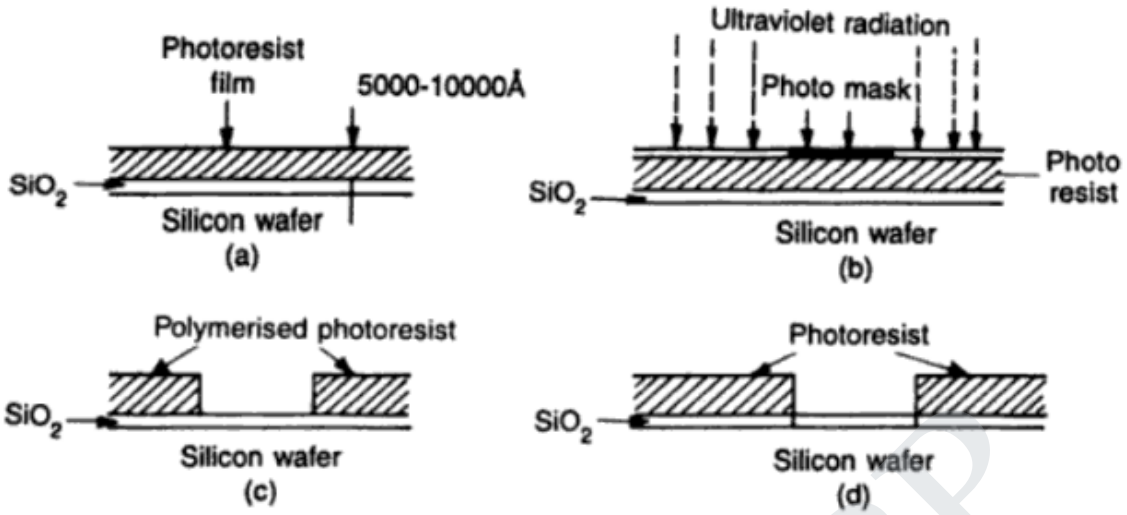
Photolithography is the process of using UV rays or X-rays to develop microscopic circuit and devices on semiconductor wafers.
Making of photolithographic mask and photo-etching are the two processes involved in **photolithographic process**

Making of a photographic mask or Masking:

- **Initial Layout or Artwork of an IC normally done at several hundred times larger than the final dimension of the finished monolithic circuit. For a finished monolithic chip of area 50 mils × 50 mils (1 mil = 25 µm) , the artwork will be made on an area of about 60 cm × 60 cm.**
- **The initial layout then decomposed into several mask layers , each corresponding to a step in fabrication. Eg. Mask for base diffusion , Mask for emitter diffusion , Mask for collector diffusion , Mask for metallization.**
- **The artwork is usually produced on a precision drafting machine called as CO-ORDINATOGRAPH. This device outlines the pattern cutting through a red mylar(opaque regions) coated over the artwork without damaging the clear region lying below the opaque region.**
- **This rubylith pattern of individual mask is photographed and then reduced in steps by a factor of 5 or 10 times to finally obtain the exact image size. The final image is photo-repeated many times by a step and repeat camera in a matrix fashion for mass production of ICs.**
- **The step and repeating camera is a device with a photographic plate on a movable platform. Between the exposure , the plate is moved in equal steps so that successive images form in a array or matrix.**

Photo-etching or Wet Etching:

- **This a method of removing silicon dioxide from desired regions so that desired impurities can be diffused.**
- The wafer is coated with photosensitive film namely **KPR(Kodak Photo Resist**) and having a thickness of 5000 $\dot{A}$ to 10,000 $\dot{A}$. The mask negative of the desired pattern is placed over the photo-resist coated wafer.
- Now the mask is exposed to UV rays, so that **KPR becomes polymerized beneath the transparent regions of the mask**.
- The mask is then removed and the wafer is chemically treated with **tricholoroethylene** in order to remove the **unpolymerized regions on the photo-resist**.
- The polymerized photoresist is next cured so that it becomes immune to chemicals called **etchants in the subsequent processing steps.**
- The chip is then immersed in **hydrofluoric acid (etchant)** for removing SiO_2 from areas not protected by KPR.
- After diffusion of impurities , the photo-resist is removed by chemically treating with hot H_2SO_4 (sulfuric acid) and mechanical abrasion.



12. Describe Epitaxial Growth process (8)

Epitaxy refers to growing of a silicon layer over the substrate.

A n-type epitaxial film (5-25μm) is grown over the p-type substrate by the following process:

→ The silicon wafers are placed on **rectangular graphite rod** called **boat** which then placed in a **long cylindrical quartz tube** called as **reaction chamber** and heated by means of RF induction coil encircled around it to a temperature of 1200˚C.

→ The various gases required for the growth of desired epitaxial layers are introduced into the system through a control console. For n-type epitaxial layer , **phosphine (PH_3) gas** is doped into the **silicon tetrachloride hydrogen gas stream.**

$$SiCl_4 + 2H_2 \rightleftharpoons Si + 4\ HCl$$

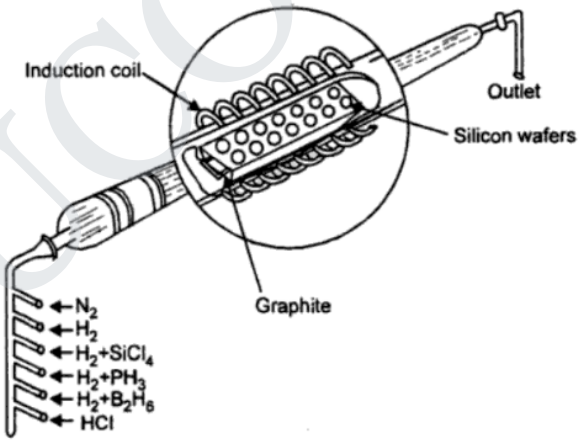


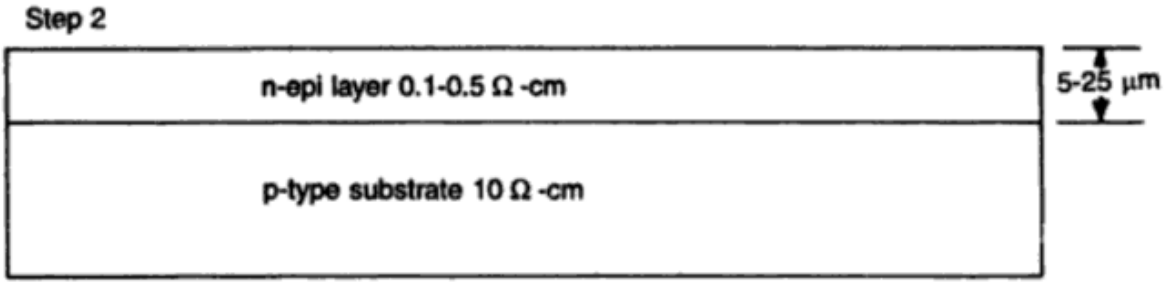
Fig. System for growing silicon epitaxial films

The resistivity of the n-type epitaxial layer is 0.1 to 0.5 Ω-cm. This layer serves as the

→ **Collector region of the BJT**

→ **Element of a diode**

→ **Diffused capacitor**



All the active and passive components are fabricated within this layer.

13. What are new trends in integrated circuit technologies and explain about its scope for future generation. (15)

- Integrated electronics or **microelectronics** is the outcome of continuous research and improvement in the characteristics and miniaturization of solid state devices and components.
- **Microelectronics** can be considered as logical extension of silicon device technology.
- Today the integrated electronics realize complete circuits on a silicon chip. These circuits are called **Integrated circuits**.
- The main semiconductor material utilized is silicon but for special applications GaAs(Gallium Arsenide) and other compound semiconductor materials may also be utilized.
- A single silicon chip may be of the order of 1 cm^2 and contain over 1 million transistors and components.
- Intense research on silicon processing and increased automation in design and manufacturing have led to the low cost and higher fabrication yields of integrated circuits.
- There are various advantages of integrated circuits over their discrete counterparts. They are:
  → Size of an IC is 1000 times smaller than discrete circuit. Therefore an IC has high equipment density.
  → Mass production of wafers possible , each containing millions of components, simultaneously. Therefore cost of IC is low.
  → Weight of an IC is very much less than discrete circuit containing same number of components.
  → Since ICs operate at low voltage , power consumption is low.
  → Since soldered joints are absent , ICs are highly reliable than their discrete counterparts.
  → Effects of parasitic capacitances are minimised in ICs. Therefore their operating speed is high.
- Depending upon the **functional utility** , the ICs are classified as **Linear(Analog or Continuous Time) ICs and Digital(Discrete or Discontinuous Time) ICs.**
- Depending upon the structure of ICs , they are classified as **Monolithic IC , Thick-Thin Film IC , Hybrid IC.** In monolithic IC all the active and passive components and their interconnections are made on a silicon chip. They are mainly preferred in **low power applications**.
- **Thick-thin film ICs** are fabricated by first depositing various resistor or capacitor films on a **glass or ceramic substrate** and then **adding pre-fabricated active components onto the substrate.** Thin film ICs are costlier than Thick Film ICs.
- **Combination of monolithic ICs or monolithic ICs with thick-thin film ICs** are called **Hybrid ICs** and are mainly preferred for **high power applications**.
- Depending upon the active device (BJT or FET) employed for fabrication , the ICs are classified as **Bipolar ICs (BJT based) and Unipolar ICs(FET based)**.
- Depending upon the type of isolation technique employed , the ICs are classified as **pn junction isolation ICs and Dielectric Isolation ICs**
- Depending upon the number of active devices per chip[**called as Level of Integration]** , the ICs are classified as

Type of integration	Number of gates	Number of transistors	Example

SSI(or) Small Scale Integration	12	10	Single chip Amplifier IC , BIFET Preamplifier, Logic Gates
MSI or Medium Scale Integration	99	500	Shift Register , Adder , Counters
LSI or Large Scale Integration	9999	20000	4-bit microprocessor 4004 , 8-bit microprocessors such as 8080 , 8085
VLSI or Very Large Scale Integration	99,999	1000000	8-bit Microcontroller 8051 , 16-bit Microprocessor 8086 , 32-bit Microprocessor Motorola 68000
ULSI or Ultra Large Scale Integration	> 100,000	> 1000000	Intel Core i3/i5/i7

14. What are the new trends in integrated circuit technologies and explain about its scope for future generation. (15)

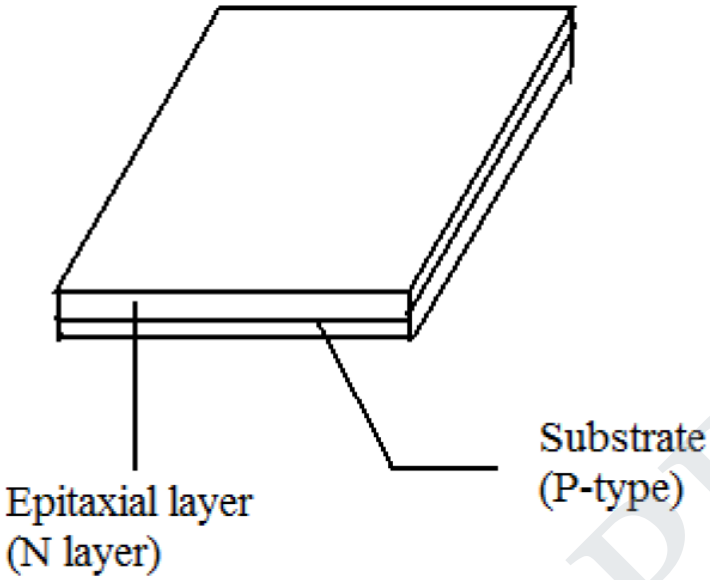
Fabrication of Monolithic Diodes :

- In a **grown junction diode** , the diode is fabricated using Czhochralski technique by controlled doping of p-type and n-type impurities in the silicon ingot.
- In **alloy type diode ,** a p-type impurity is placed over a N-type substrate and heated till liquefaction occurs and two materials meet.
- In **diffused type diode** , the pn diode is formed by either placing a p-type impurity over n-type substrate till the impurity diffuses into the substrate[**solid diffusion**] or diffusing a gaseous p-type impurity into the n-type substrate in a gas chamber[**gaseous diffusion**]
- In **point contact diode** , one of the faces of N-type semiconductor is attached to a metallic body by RF heating and another face is provided with p-type region by passing current through a **phosphor bronze or tungsten wire**.

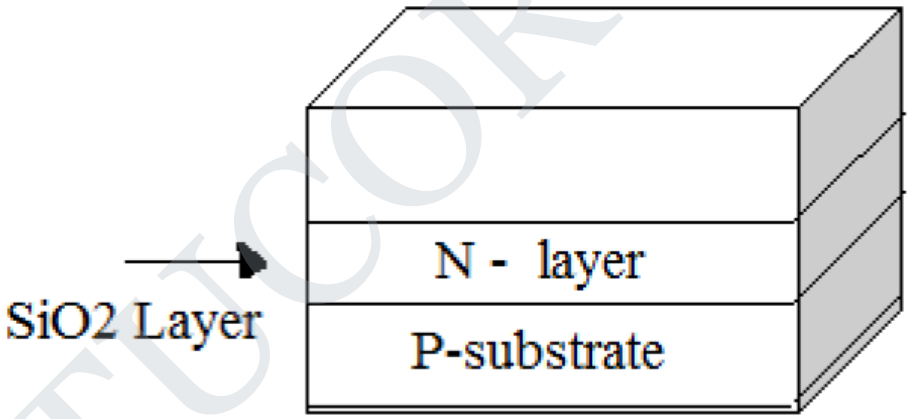
Fabrication of Monolithic BJT:

Epitaxial Growth:

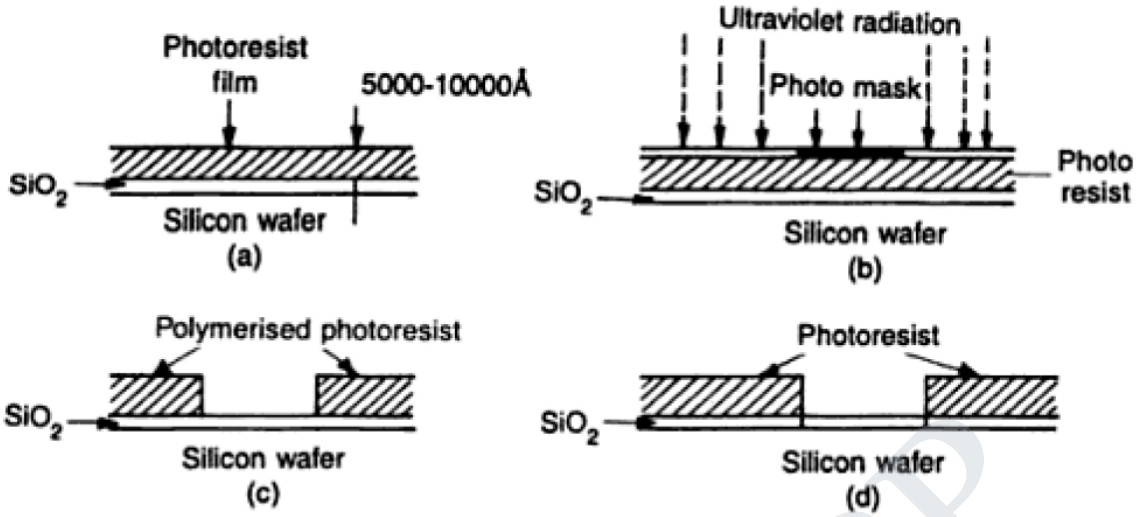
- First step in fabrication of BJT is to create collector region.
- A P-type silicon substrate of acceptor density $N_A = 1.4 \times 10^{15}$ atoms/cm^3 and resistivity is fabricated using **czhochraski technique**.
- A **heavily doped n-type region called as** buried layer is grown over the substrate by diffusion process.
- Another N-type layer is grown over the **buried region** through **epitaxial process**. This epitaxial region is called **active region or collector region of BJT.**
- The **buried layer reduces the collector resistance of BJT**.



Oxidation :
A silicon dioxide layer is grown over the **epitaxial layer by exposing the silicon substrate to a oxygen atomosphere at 1000˚C.**



Photolithography:



- The silicon dioxide layer in the wafer is coated with a thin **photo-emulsive solution called as photo-resist.**
- Then a mask , black and white negative of the required pattern placed over the photo-resist and the silicon wafer is exposed to **UV rays**.
- The photo-resist under the transparent region(white) of the mask gets polymerized. The photo-resist under the opaque(black) region of the mask remains unpolymerized.
- The polymerized region is cured so that it becomes resistant to corrosion. The unpolymerized regions are removed by dipping the wafer in **HF(Hydro Fluoric)** acid. This creates opening for the diffusion of P-type and N-type impurities to be diffused.
- Once P-type and N-type impurities are diffused , the polymerized region is removed by dipping the wafer in **H_2SO_4 (Sulphuric Acid)** and by mechanical abrasion.

PN Junction Isolation Diffusion:
The PN junction Isolation diffusion involves creation of **heavily doped p-type region around the transistor. This region is called MOAT**.
The epitaxial layer and the p-type moat forms a back-to-back PN junction.
When the P-type substrate is held at negative potential , the two back to back PN diodes gets reverse biased thereby providing the required **electrical and physical isolation between BJT and its adjacent components.**

Base Diffusion:
A new layer of silicon dioxide is grown over the entire wafer and a new pattern of openings formed through photolithographic technique through which p-type impurities (such as boron) is introduced into the n-type epitaxial silicon. This diffusion is used to form the b**ase region of the transistor**

Emitter Diffusion:
A new layer of silicon dioxide is grown over the entire wafer and a new pattern of openings formed through photolithographic technique through which heavily doped ($\approx 2 \times 10^{20}$ cm^{-3}) n-type impurities (such as phosphorous) is introduced into the n-type epitaxial silicon. This diffusion is used to form the e**mitter region of the transistor.**

Aluminium Metallization
A new layer of silicon dioxide is grown over the entire wafer and a new pattern of openings formed through photolithographic technique where interconnections have to be made between the components. A thin coating of aluminium is **vacuum deposited** over the entire surface of the wafer and the interconnection pattern between the components made by **photo-resist technique**.

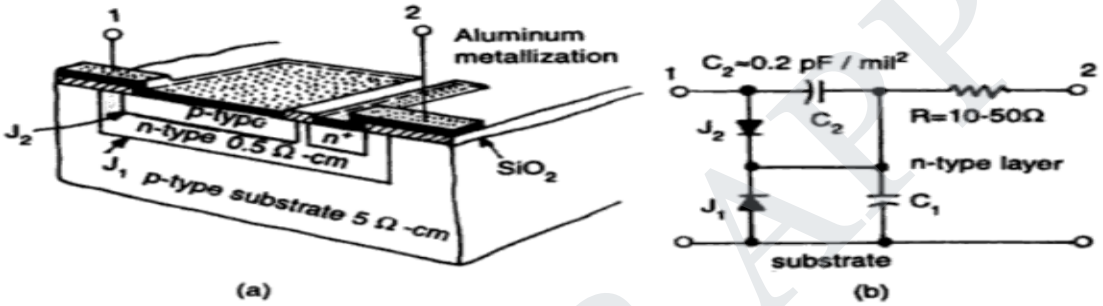
Assembly Processing and Packaging:

- A diamond tipped tool taken and create cut lines on the surface of the wafer along the rectangular grid. The cut lines separate the individual chips. This process is called **scribing and cleaving**.(Scribing is to create cut lines ; Cleaving is separating the cut lines).
- Each individual chip mounted on a ceramic wafer and attached to a suitable package.

Fabrication of Monolithic Capacitor:

Following are the two methods of obtaining integrated capacitor:
(i) Junction Capacitor
(ii) MOS Capacitor
(iii) Thin Film Capacitor

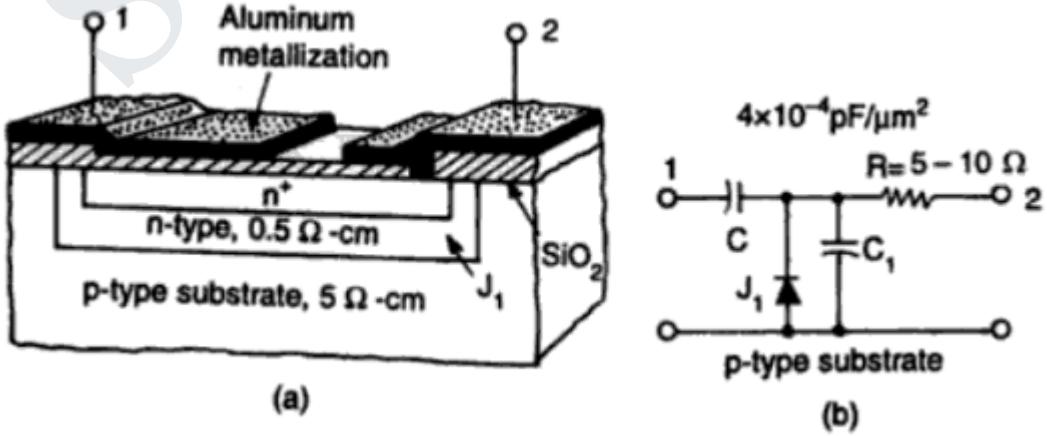
(i) Junction Capacitor:



- Two junctions J_1 and J_2 are present .
- Reverse biasing J_2 produces desired polarised capacitance C_2 ; C_1 is the parasitic capacitance between n-type epitaxial layer and substrate ; R is the series resistance due to the n-region.
- C_1 minimized by keeping the substrate at most negative potential.
- C_2 depends on (a) Area of J_2 (b) Impurity concentration of n-type epitaxial layer (c) Voltage across J_2.

(ii) MOS Capacitor:

- Parallel plate capacitor with silicon dioxide as dielectric.
- Heavily doped n+ region formed during emitter diffusion forms the lower plate.
- Thin film of aluminium metal forms the upper plate .
- The parasitic elements involved are (i) Series resistance due to n+ region (ii) Series resistance due to collector junction J_1 (iii) Capacitance of J_1.
- Non-polar capacitor and capacitance independent of applied voltage.
- Alternative to silicon dioxide , silicon nitride can be used as dielectric.
- Silicon nitride has high dielectric constant compared to Silicon dioxide.



(iii) Thin Film Capacitor

- Aluminium or tantalum used as capacitor plates.
- Aluminium Oxide(Al_2O_3) used as dielectric for small capacitors ; Tantalum Oxide (Ta_2O_5) used as dielectric for large capacitors.
- Gets irreversibly destroyed when voltage rating exceeds breakdown value of dielectric.

Fabrication of JFET

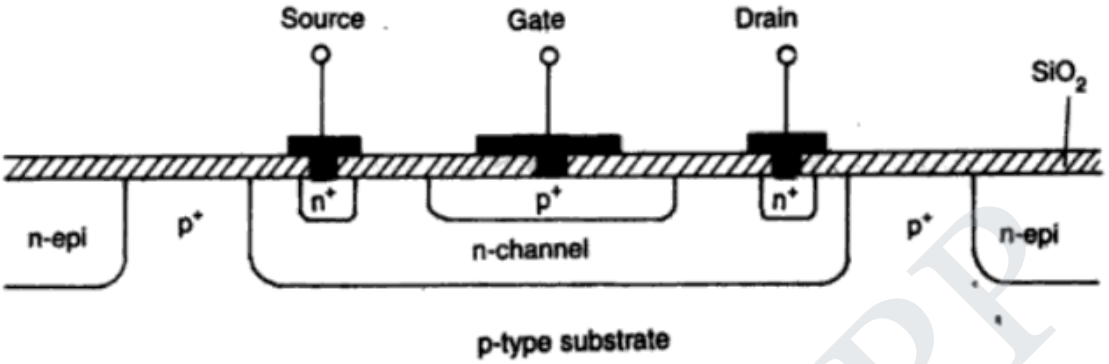


Fig. N-channel JFET Structure

- The process used for fabrication of JFET same as fabrication of BJT.
- Epitaxial layer serves as the n-channel of JFET.
- The p^+ gate is formed in n-channel by the process of **diffusion or ion implantation**.
- The n^+ regions formed under the drain and source contact regions for providing **ohmic or non-rectifying contacts**.

UNIT II CHARACTERISTICS OF OPAMP 9

Ideal OP-AMP characteristics, DC characteristics, AC characteristics, differential amplifier; frequency response of OP-AMP; Basic applications of op-amp – Inverting and Non-inverting Amplifiers, summer, differentiator and integrator-V/I & I/V converters.

Part-A(10×2 = 20 marks)

1. Draw an adder circuit using an OP-AMP to get the output expression as $V_0 = -(0.1\,V_1 + V_2 + 10\,V_3)$ where V_1, V_2 and V_3 are inputs?

The output expression for the circuit in fig. a is

$$V_O = -\left[\left(\frac{R_F}{R_1}\right) V_1 + \frac{R_F}{R_2}\right) V_2 + \frac{R_F}{R_3}\right) V_3\ ] \ldots..(1)$$

Assume $R_F = 10\ k\Omega$, $R_1 = 100\ k\Omega$, $R_2 = 10\ k\Omega$, $R_3 = 1\ k\Omega$

Substituting these values in eqn(1) we obtain

$V_0 = -(0.1\,V_1 + V_2 + 10\,V_3)$

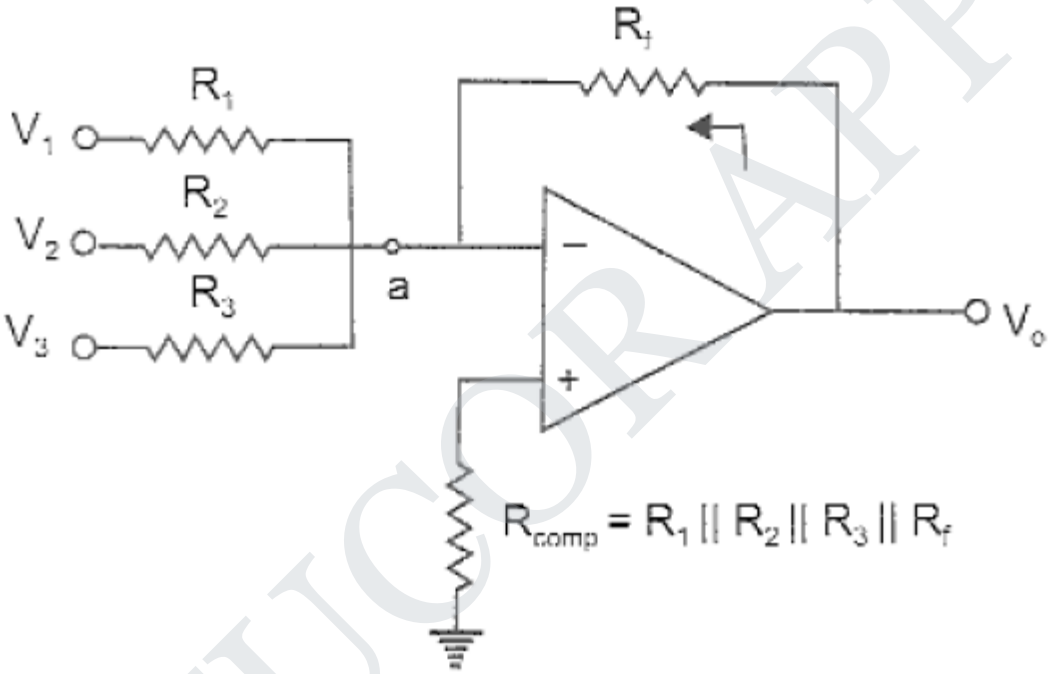


Fig. a Inverting Summing Amplifier

2. A 100 pF capacitor has a maximum charging current of 150 microamps. What is the slew rate?

$$\text{Slew rate} = \frac{I_{max}}{C} = \frac{150 \times 10^{-6}}{100 \times 10^{-12}} = 1.5 \times 10^6\ \text{V/s} = 1.5\ \text{MV/s}\ [\ 10^6 = \text{M} = 1\ \text{Mega}]$$

3. What do you mean by input offset current and offset voltage?

Input Offset Current : Absolute algebraic difference between the **bias or base currents flowing into the inverting and non-inverting input terminals of op-amp.**

$$\mathbf{I_{IOS} = |I_B^- - I_B^+|}$$

Input offset current is of the order of 200 nA for BJT based OP-AMP and 10 pA for FET based OP-AMP.

Input Offset Voltage : Small voltage that has to be applied between the input terminals of OP-AMP under zero input condition to make the output voltage zero ; It is the absolute algebraic difference between the **voltages at the inverting and non-inverting terminals.**

$$\mathbf{V_{IOS} = |V_{IN} - V_{NIN}|}$$

Output Offset Voltage : Small voltage that appears at the output due to input offset voltage under zero input condition and is given by

$$V_{OOS} = [1+\frac{R_F}{R_1}]\ V_{IOS}$$

Total Output Offset Voltage : $V_{OST} = V_{OOS} + R_F I_B$

4. Define CMRR

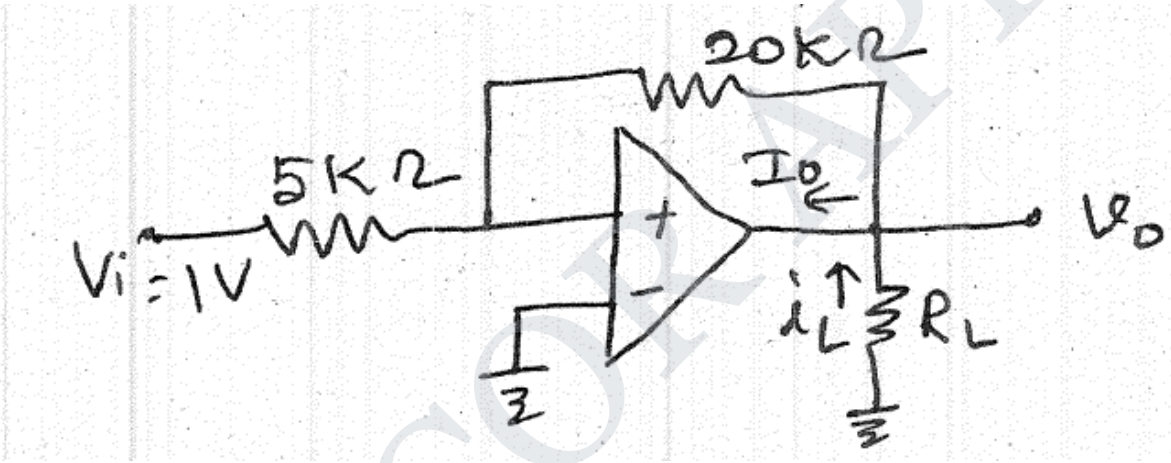
CMRR is the abbreviation for **C**ommon **M**ode **R**ejection **R**atio and is the absolute ratio of Differential mode and Common Mode Gain.

$$CMRR = |\frac{A_{DM}}{A_{CM}}| = 2\ g_M R_E .$$

5. What are the ideal characteristics of an OP-AMP ?

- Infinite Voltage Gain
- Infinite Input Impedance
- Zero Output Impedance
- Gain Independent of Frequency
- Zero Input Offset Voltage

6.



In the circuit shown in the above figure , calculate V_0 , A_{CL} , load current i_L output current i_0. **(Example 2.4 Pg.49 Roy Chodhury)**

Solution:

(i) Output Voltage of the Non-Inverting Amplifier , $V_0 = [1+\frac{R_F}{R_1}]\ V_I = [1+\frac{20\ k\Omega}{5\ k\Omega}]\ (1V)$

$= 5V$

(ii) Closed Loop Gain of the Non-Inverting Amplifier , $A_{CL} = \frac{V_0}{V_I} = \frac{5}{1} = 5$

(iii) Load Current of the Non-Inverting Amplifier , $I_L = \frac{V_0}{R_L} = \frac{5\ V}{5\ k\Omega} = 1$ mA

(iv) Input Current of the Non-Inverting Amplifier , $I_I = \frac{V_I}{R_1}$ or $\frac{V_o - V_I}{R_F} = \frac{1\ V}{5\ k\Omega}$ or $\frac{5-1}{20\ k\Omega} = 0.2$ mA .

Therefore Output Current of the Non-Inverting Amplifier , $I_O = I_L + I_I = 1$ mA + 0.2 mA = 1.2 mA.

The output current of the OP-AMP flows away from the output junction.

7. Why IC 741 is not used in high frequency applications.

Ans. IC 741 OP-AMP has **low slew rate (0.5 V/µs)** and therefore **cannot be used for high frequency applications**.

8. Draw the circuit diagram of an integrator and give its output equation.

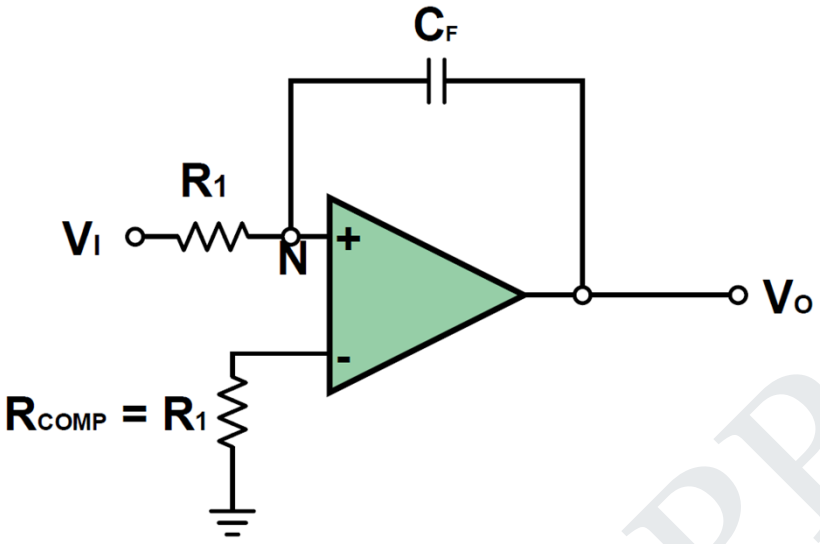


Fig. a **Inverting OP-AMP Integrator**

$$V_0(t) = -\frac{1}{R_1 C_F}\int V_i\, dt + V_O(0)$$

9. Write some applications of operational amplifier
   - Adder
   - Subtractor
   - Voltage to Current Converter or Transconductance amplifier or Current Series Negative Feedback Amplifier or Voltage Controlled Current Source.
   - Current to Voltage Converter or Transresistance amplifier or Transimpedance amplifier or Voltage Shunt Negative Feedback Amplifier or Current Controlled Voltage Source.
   - Voltage Follower or Buffer

10. What is integrator.

An integrator is a op-amp based circuit that provides an output voltage proportional to the **time integral of the** input voltage.

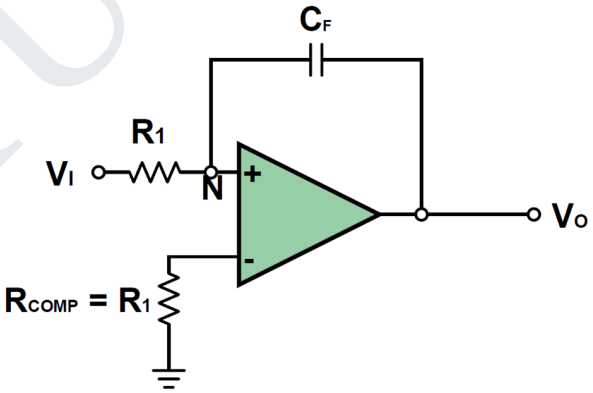


Fig. a **Inverting OP-AMP Integrator**

$$V_0(t) = -\frac{1}{R_1 C_F}\int V_i\, dt + V_O(0)$$

$V_O(0)$ is the initial output voltage (Voltage at t =0)

11. What is drawback of IC741 ?
   - Output voltage is limited to a minimum and maximum value closer to the power supply voltages.

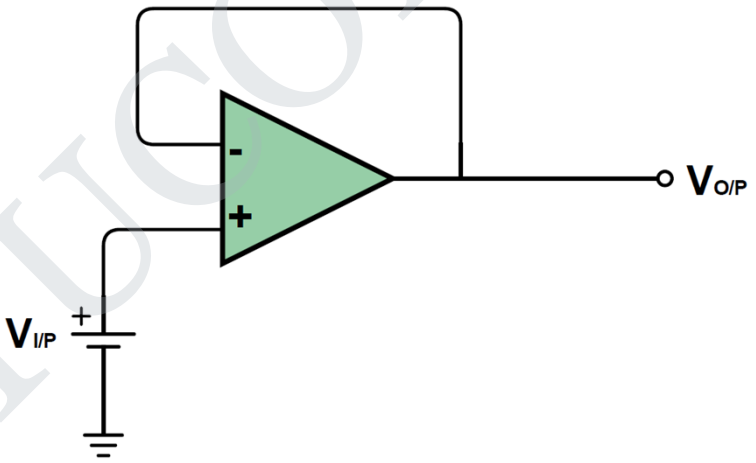
- Not suitable for high frequency applications
- Suitable for low power applications
- Turns off when the load resistance is below a certain value

12. Compare the ideal and practical op-amp characteristics

S.No	Ideal OP-AMP	Practical OP-AMP
1.	Infinite Voltage Gain , so that it can amplify signals of any amplitude	Voltage gain varies between 10^5 to 10^8. It cannot amplify signals < 100 µV
2.	Infinite Input resistance , so no loading effect occurs for the preceding stage	Input resistance varies between 10^6 to $10^{12}\Omega$. Not all source can drive it.
3.	Zero output resistance , so no loading effect occurs for the succeeding stage	Output resistance is of the order of 75Ω. Therefore it can drive only limited number of output devices
4.	Zero output voltage when input voltage is zero(Zero Output Offset Voltage)	Small output voltage exist under zero input conditions due to **unavoidable mismatch between the transistors**

13. How an op-amp can be used as a voltage follower.

In the non-inverting amplifier , if $R_F = 0$ and $R_1 = \infty$, we get the voltage follower or **unity gain amplifier or buffer.** It produces an output voltage which is equal in magnitude and phase with the input voltage. Its main purpose is to connect a **high impedance source with a low impedance load.[i.e. suitable for sagging voltage or current source**]



14 . Write the concept of virtual ground

Virtual ground means the inverting terminal of inverting amplifier will be at the same ground potential as the non-inverting terminal , even though both of them are not physically connected with each other.

15. Define slew rate

Slew rate is a type of **AC characteristic of OP-AMP and is** defined as the maximum rate of change of output voltage caused by a **step input voltage and is usually specified in V/µs. A slew rate of 1V/µs means the output voltage rises or falls by 1V in one microsecond.Practical IC op-amps have a slew rate between 0.1 V/µs to 1000 V/µs.**

16. Give the various types of frequency compensation

- External Frequency Compensation
  → Pole-Zero Compensation

→ Dominant Pole Compensation

- Internal Frequency Compensation

17 . The output voltage of a certain op-amp circuit changes by 20 V in 4 μs. What is its slew rate.

$$\textbf{Slew rate} = 2\pi \times \frac{1}{4 \times 10^{-6}} \times 20 = 31.5\ \text{V/μs}$$

18. List any four non-ideal DC characteristics of OP-AMP

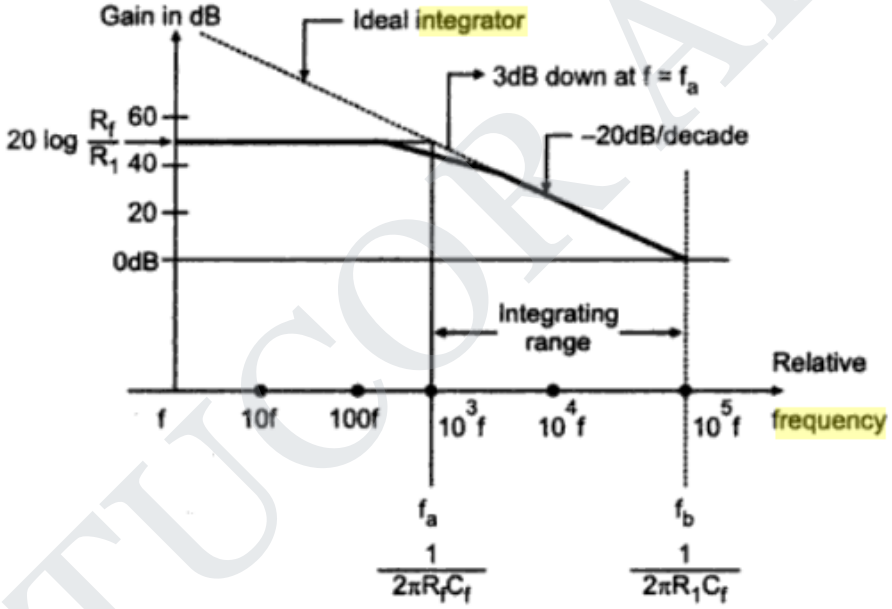
(i) **Input Bias Current**
(ii) **Input Offset Current**
(iii) **Input Offset Voltage**
(iv) **Output Offset Voltage**

19. State the causes for slew rate in an OP-AMP ? How it is indicated

Causes of Slew Rate:

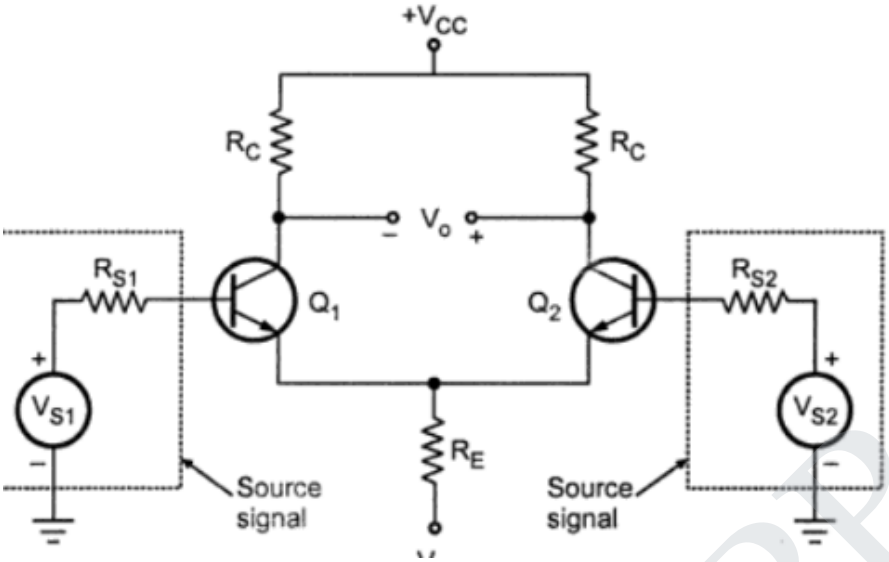
- Limited charging rate of the compensating capacitor
- Current limiting in the internal stages of the op-amp

The slew rate is indicated through the frequency response of the OP-AMP

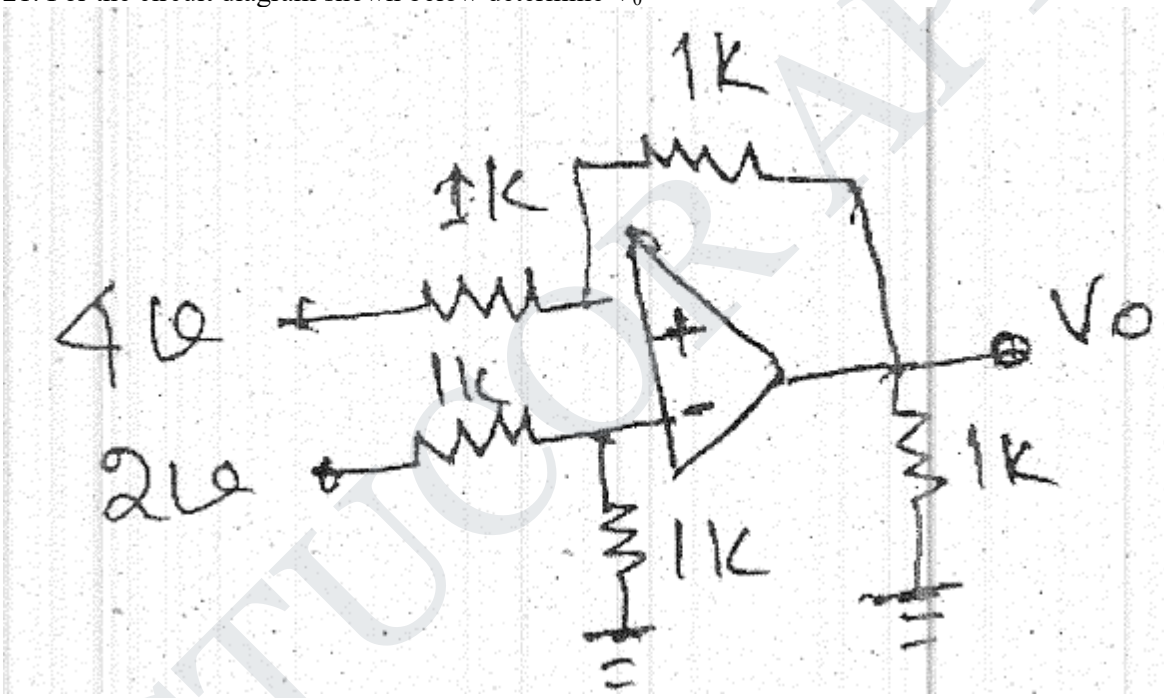


20. Draw the circuit of a symmetrical emitter coupled differential amplifier.

Symmetrical Emitted Coupled Differential amplifier is also called Dual Input Balanced Output Differential Amplifier.



21. For the circuit diagram shown below determine V_0



The given circuit is a OP-AMP based **subtractor circuit , also called as difference amplifier. The output voltage is $V_O = V_1 – V_2 = 4 – 2 = 2V$**

22. What is meant by virtual ground of an op-amp?

When the output voltages are below the saturation values , the OP-AMP behaves as a linear amplifier. Under this condition , no differential voltage exist between the inverting and non-inverting terminals. The value of voltages in these two terminals are same. Thus if non-inverting terminal is grounded , inverting terminal is also grounded. This is called **virtual ground or virtual short.**

Part-B

1. Consider the lossy integrator as shown in Figure 2. For the component values R_1 = 10 kΩ , R_F = 100 kΩ and C_F = 1nF , Determine the lower frequency limit of integration and study the response for inputs. (Eg. 4.4 **Roy Choudhury**)

(i) step input

(ii) square input
(iii) sine input

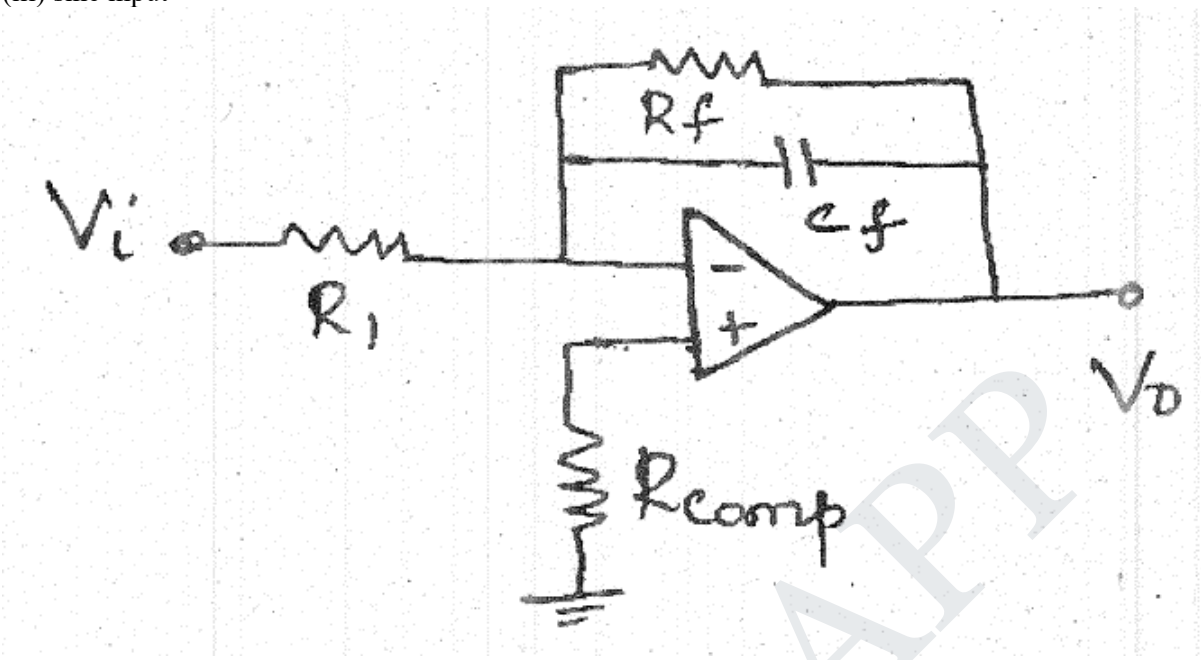


Figure 2.

Solution:

For the given component values , the lower frequency limit of integration $\mathbf{f_A}$ is

$$f_A = \frac{1}{2\pi R_F C_F} = \frac{1}{2\pi \times 100 \times 10^3 \times 10 \times 10^{-9}} = 159 \text{ Hz.}$$

For 99% accuracy , **the input frequency should be atleast 1 decade above f_A i.e. 1.59 kHz. Accurate integration can be achieved beyond 1.59 kHz. But the upper frequency limit of integration is determined by frequency response of OP-AMP**.

(i) Sine wave input :

For an input of 1 V peak sine wave at 5 kHz, the output V_O is

$$V_0 = -\frac{1}{R_1 C_F}\int V_1(t)dt$$

$$= -\frac{1}{100 \times 10^3 \times 10 \times 10^{-9}}\int 1 \sin(2\pi\, 5000t)\, dt$$

$$= -10^4 \int \sin(2\pi\, 5000t)\, dt = -\frac{10^4}{2\pi \times 5000}[-\cos(2\pi\, 5000t)]$$

$$= 0.318 \cos(2\pi\, 5000t)$$

The output is a cosine wave with peak amplitude of 0.318 V. If the frequency of the input is raised by a factor of 10 to 50 kHz , the output would be cosine wave of frequency 50 kHz and amplitude of 31.8 mV.

(ii) Step input:

For an input of 1 V step input voltage between t = 0 to 0.3 ms , the output voltage of integrator at t = 0.3 ms is

$$V_0 = -\frac{1}{R_1 C_F}\int V_1(t)dt$$

$$= \frac{1}{100 \times 10^3 \times 10 \times 10^{-9}}\int_0^{0.3\ ms} 1\ dt$$

$$= -10^4\,[t] = -10^4\,[0.3\text{-}0] = -10^4 \times 0.3 \times 10^{-3} = -3\ V$$

The output is a ramp voltage with a slope of 10 V/ms.

(iii) Square wave input:

For an square wave input voltage with amplitude + 1V between t = 0 to 0.1 ms and -1V between t = 0.1 ms to 0.2 ms. Thus the square wave is a combination of two step inputs (i) One step input above x-axis and another step input below x-axis. So the output voltage will be having accordingly ramps (i) One ramp signal above x-axis and (ii) Another ramp signal below x-axis.

$$V_0 = -\frac{1}{R_1 C_F}\int V_1(t)dt$$

$$= \frac{1}{100 \times 10^3 \times 10 \times 10^{-9}}\int_0^{0.1\ ms} 1\ dt$$

$$-10^4\,[t] = -10^4\,[0.1\text{-}0] = -10^4 \times 0.1 \times 10^{-3} = -1\ V$$

(i.e. For positive square wave negative ramp is obtained and for negative square wave positive ramp is obtained).

$$V_0 = -\frac{1}{R_1 C_F}\int V_1(t)dt$$

$$= \frac{1}{100 \times 10^3 \times 10 \times 10^{-9}}\int_{0.1}^{0.2\ ms} -1\ dt$$

$$10^4\,[t] = 10^4\,[0.2\text{-}0.1] = 10^4 \times 0.1 \times 10^{-3} = 1\ V$$

(ii) Design an adder-subtractor circuit for $V_0 = 2V_1 + 5V_2 - 10V_3$ (6)

Solution:

In the first step , design an adder to get $2V_1 + 5V_2$

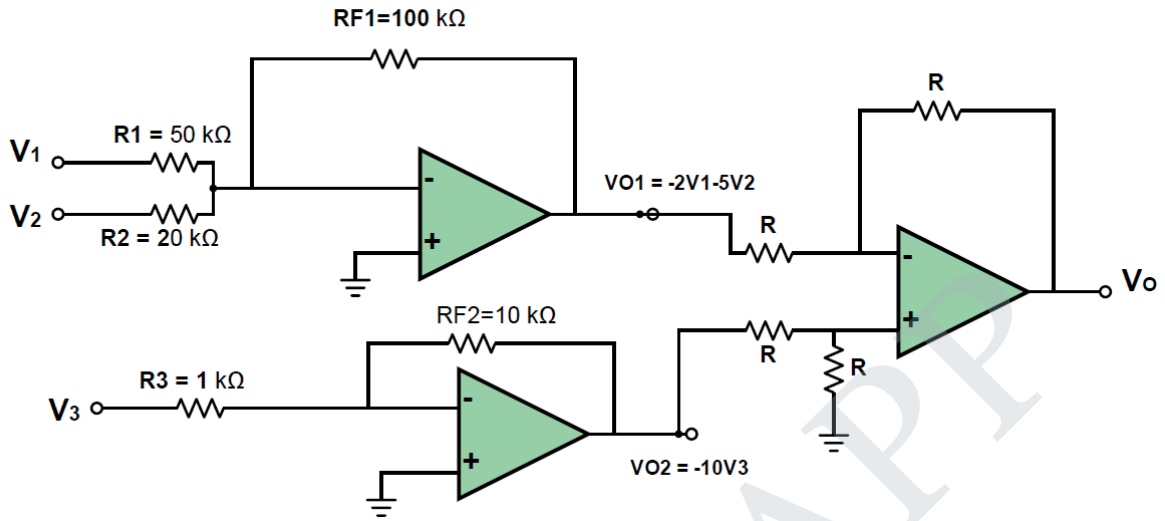
Therefore $V_{O1} = -[\frac{R_{F1}}{R_1} V_1 + \frac{R_{F1}}{R_2} V_2]$

Therefore $\frac{R_{F1}}{R_1} = 2$; $\frac{R_{F1}}{R_2} = 5$; Choose $R_{F1} = 100\ k\Omega$. Therefore $R_1 = 50\ k\Omega$, $R_2 = 20\ k\Omega$

Now generate 10 V_3 by using an inverting amplifier of gain 10.

$V_{O2} = -\frac{R_{F2}}{R_3} V_3$; $\frac{R_{F2}}{R_3} = 10$ Choose $R_{F2} = 10$ kΩ. Therefore $R_3 = 1$ kΩ

Now use subtractor for getting $V_O = V_{O2} - V_{O1} = -10\ V_3 - (-2V_1 - 5V_2) = 2V_1 + 5V_2 - 10\ V_3$



2. For a V-I converter shown in figure 3 , $V_{IN} = 5$ V , R = 10 kΩ and $V_1 = 1$ V, find the load current and output voltage V_0 . Assume the op-amp is initially nulled (6)

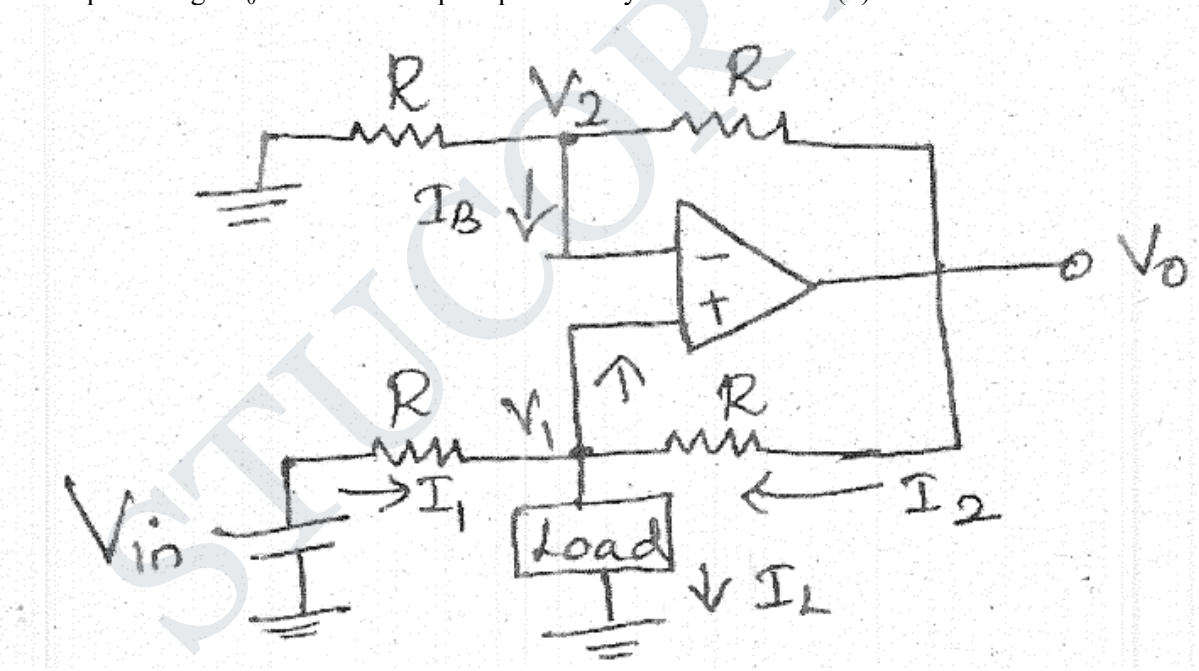


Figure 3

Solution:

$$\mathbf{I_L = \frac{V_{IN}}{R} = \frac{5}{10 \times 10^3} = 0.5\ mA}$$

$$\mathbf{\text{Load current } I_L = I_1 + I_2}$$

$$\mathbf{= \frac{V_{IN} - V_1}{R} + \frac{V_{OUT} - V_1}{R}}$$

$$\mathbf{0.5\ mA = \frac{5 - 1}{10 \times 10^3} + \frac{V_{OUT} - 1}{10 \times 10^3}}$$

$0.5\ mA = 0.4\ mA + 0.1(V_{OUT} - 1)$
$0.1\ mA = 0.1(V_{OUT} - 1)$
$1 = V_{OUT} - 1$
$V_{OUT} = 1+1 = 2V$
Therefore
Load current , $I_L = 0.5\ mA$
$V_{OUT} = 2\ V$

3. For a maximum frequency of 100 Hz , design a differentiator circuit and draw the frequency response for the same.(**Example 4.3 , Pg. 167 , Roy Choudhury)**
(16)

Solution:

Select $f_A = f_{MAX} = 100\ Hz = \frac{1}{2\pi R_F C_1}$

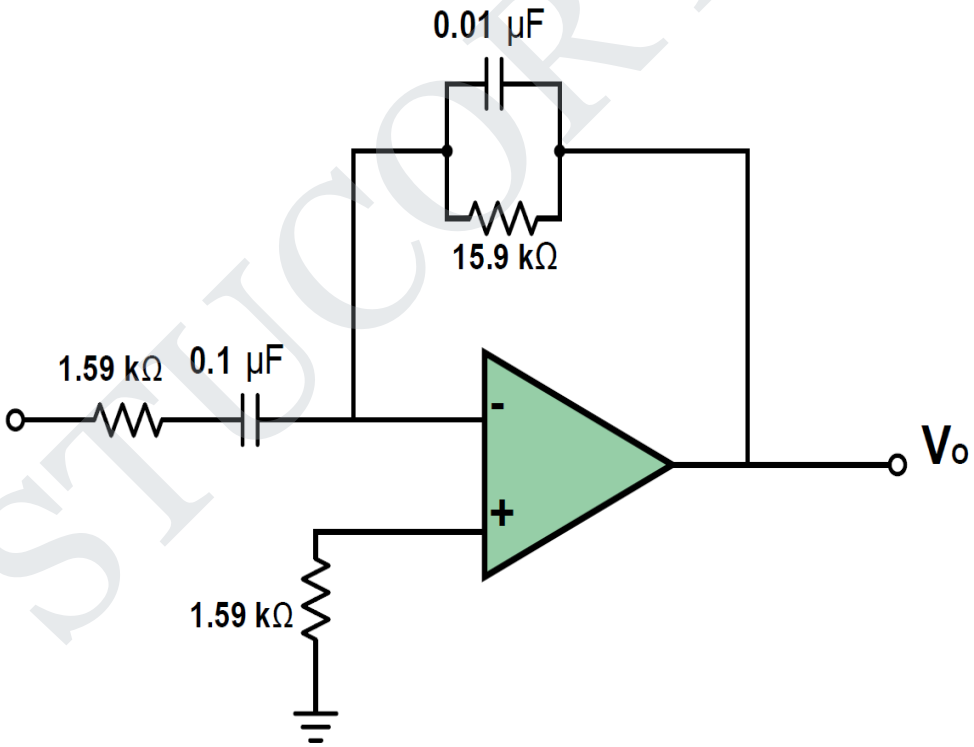
Let $C_1 = 0.1\ \mu F$

Then $R_F = \frac{1}{2\pi f C_1} = \frac{1}{2\pi \times 100 \times 0.1 \times 10^{-6}} = 15.9\ k\Omega$

Now choose $f_B = 10\ f_A = 1\ kHz = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi 1 \times 10^3 \times 0.1 \times 10^{-6}} = 1.59\ k\Omega$

Since $R_F C_F = R_1 C_1$

We get $C_F = \frac{1.59 \times 10^3 \times 0.1 \times 10^{-6}}{15.9 \times 10^3} = 0.01\ \mu F.$



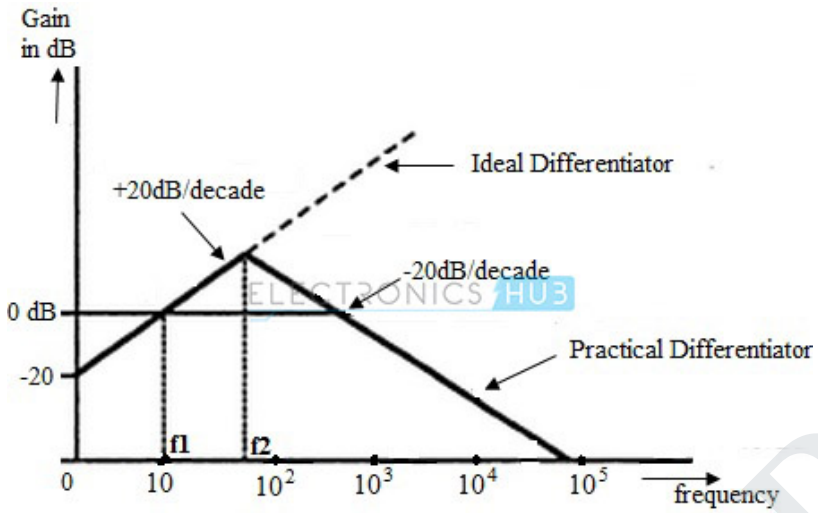


Fig: Frequency Response of Practical Differentiator

4. Design an OP-AMP circuit to give an output voltage $V_0 = 4V_1 - 3V_2 + 5V_3 - V_4$, where V_1 , V_2 , V_3 and V_4 are inputs. (8)

In the first step , design an adder to get $4V_1 + 5V_3$

Therefore $V_{O1} = -[\frac{R_{F1}}{R_1} V_1 + \frac{R_{F1}}{R_3} V_3]$

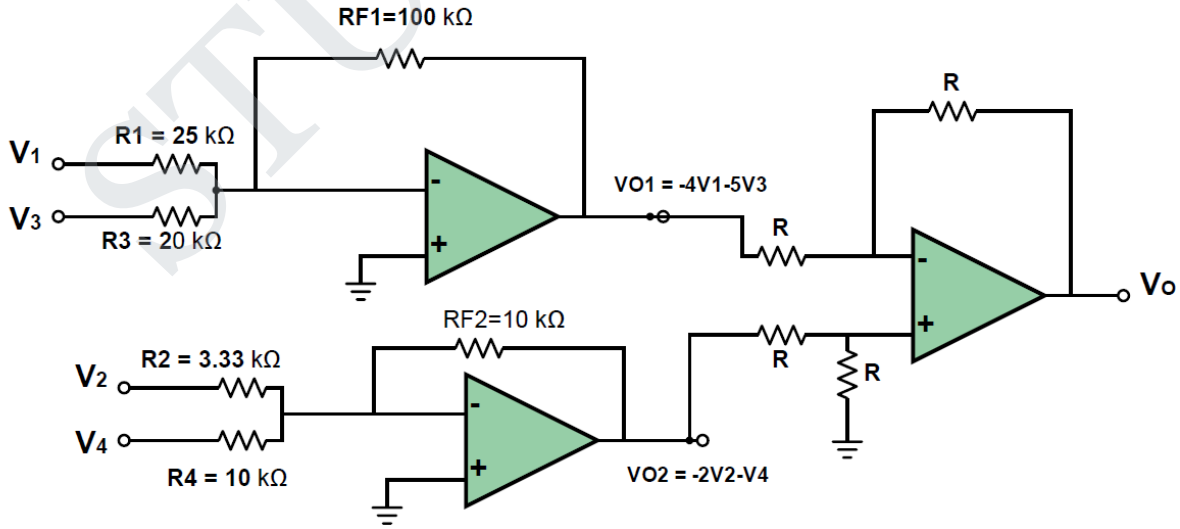
Therefore $\frac{R_{F1}}{R_1} = 4$; $\frac{R_{F1}}{R_2} = 5$; Choose $R_{F1} = 100$ kΩ . Therefore $R_1 = 25$ kΩ , $R_3 = 20$ kΩ

Now generate $-3V_2$ by using an inverting amplifier of gain 3 and V_4 with a gain of 1.

$V_{O2} = -[\frac{R_{F2}}{R_2} V_2 + \frac{R_{F2}}{R_4} V_4]$

$\frac{R_{F2}}{R_2} = 3$; $\frac{R_{F2}}{R_4} = 1$ Choose $R_{F2} = 10$ kΩ. Therefore $R_2 = 3.33$ kΩ ; $R_4 = 10$ kΩ

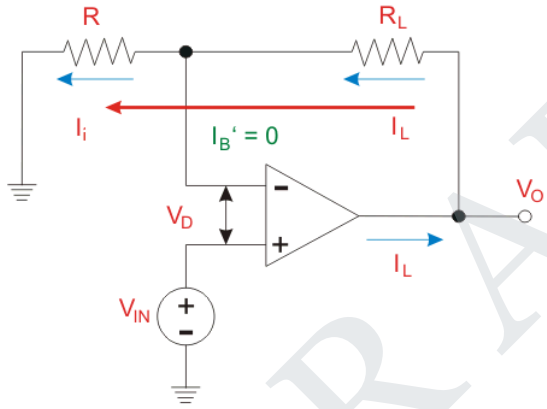
Therefore $V_O = V_{O2} - V_{O1} = -3V_2 - V_4 - (-4V_1 - 5V_3) = 4V_1 - 3V_2 + 5V_3 - V_4$



5. Explain the voltage to current converter using operational amplifier. Also explain the application of OP-AMP as integrator. (8)

Voltage to Current Converter : [Transconductance Amplifier or Voltage Controlled Current Source]

The V/I Converter circuit generates an output current proportional to the input voltage or feedback.
V/I converter classified into two types based on the type of load connected to it. They are:
→ Floating Load V/I Converter
→ Grounded Load V/I Converter
Floating Load V/I Converter:[**Current Series Negative Feedback Amplifier**]
Floating load means the **load resistor R_L (in case of DC source applied to non-inverting terminal) or Z_L(in case of AC source applied to non-inverting terminal)** is not connected to ground.
The inverting input terminal is driven by the feedback voltage [Voltage across R_L] determined by the load current I_L and the feedback voltage is in series with V_D (Input Difference Voltage – Potential Difference between inverting and Non-inverting terminal voltages].



Applying KVL to the input loop formed by V_{IN} , V_D and V_F(Feedback Voltage) , we obtain

$$V_{IN} = V_D + V_F$$

Since the gain is very large for the op-amp , $V_D = 0$

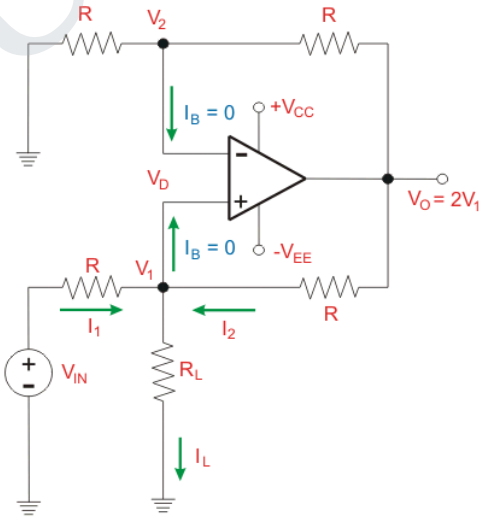
$$\text{Therefore } V_{IN} = V_F$$

Assuming the bias current into the inverting terminal I_B^- is zero,

$$V_{IN} = V_F = I_L.R = I_I.R \text{ [R is the input resistance and } I_I \text{ is the input current]}$$

$$\text{Therefore } I_L = I_I = \frac{V_{IN}}{R} = \frac{V_F}{R}$$

Grounded Load V/I Converter [Howland Current Converter]



Grounded Load means the **load resistor R_L (in case of DC source applied to non-inverting terminal) or Z_L(in case of AC source applied to non-inverting terminal)** is connected to ground.

Applying KCL at node 1

$$I_1 + I_2 = I_L$$

$$\frac{V_{IN} - V_1}{R} + \frac{V_{OUT} - V_1}{R} = I_L.$$

Therefore $V_{IN} + V_{OUT} - 2V_1 = I_L \cdot R$

Therefore $V_1 = \frac{V_{IN} + V_{OUT} - I_L.R}{2}$

Since the op-amp is used as non-inverting amplifier , the gain is $(1+\frac{R}{R} = 2)$

Therefore the output voltage of the non-inverting amplifier is $V_{OUT} = 2V_1 = V_{IN} + V_{OUT} - I_L.R$

Therefore $0 = V_{IN} - I_L.R$

$V_{IN} = I_L.R$

$I_L = \frac{V_{IN}}{R}$

Applications of V/I Converter:

- Low voltage AC and DC Voltmeter
- Zener Diode Tester
- LED tester

6. Explain the application of OP-AMP as integrator

Integrator:[Ideal or Lossless Integrator]

An integrator is a op-amp based circuit that provides an output voltage proportional to the **time integral of the** input voltage.

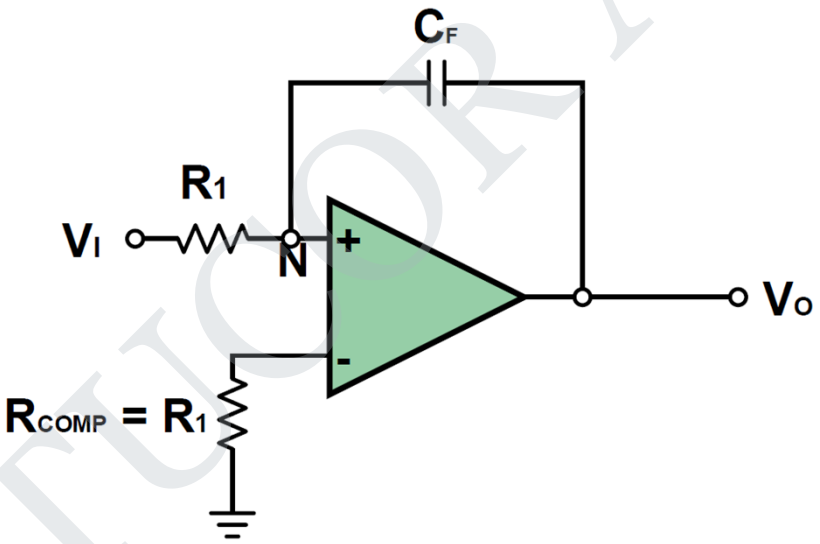


Fig. a **Inverting OP-AMP Integrator**

$V_0(t) = -\frac{1}{R_1 C_F} \int V_i \, dt + V_O(0)$

$V_O(0)$ is the initial output voltage (Voltage at t =0)

Based on the terminal where the input voltage V_I is given , the integrator can be classified as **(i) inverting integrator (ii) Non-inverting integrator**. In inverting integrator , input voltage applied to inverting input terminal of OP-AMP whereas in non-inverting integrator. The R_{COMP} (Compensating resistor provided in inverting integrator minimizes the effect of input bias current.

Derivation for Inverting Integrator:

At the inverting node , N

$$\frac{V_I}{R_1} + C_F \frac{dV_0}{dt} = 0$$

$$\frac{dV_0}{dt} = -\frac{V_I}{R_1 C_F}$$

Integrating both sides we get

$$\int_0^t dV_0 = -\frac{1}{R_1C_F}\int_0^t V_i\,dt$$

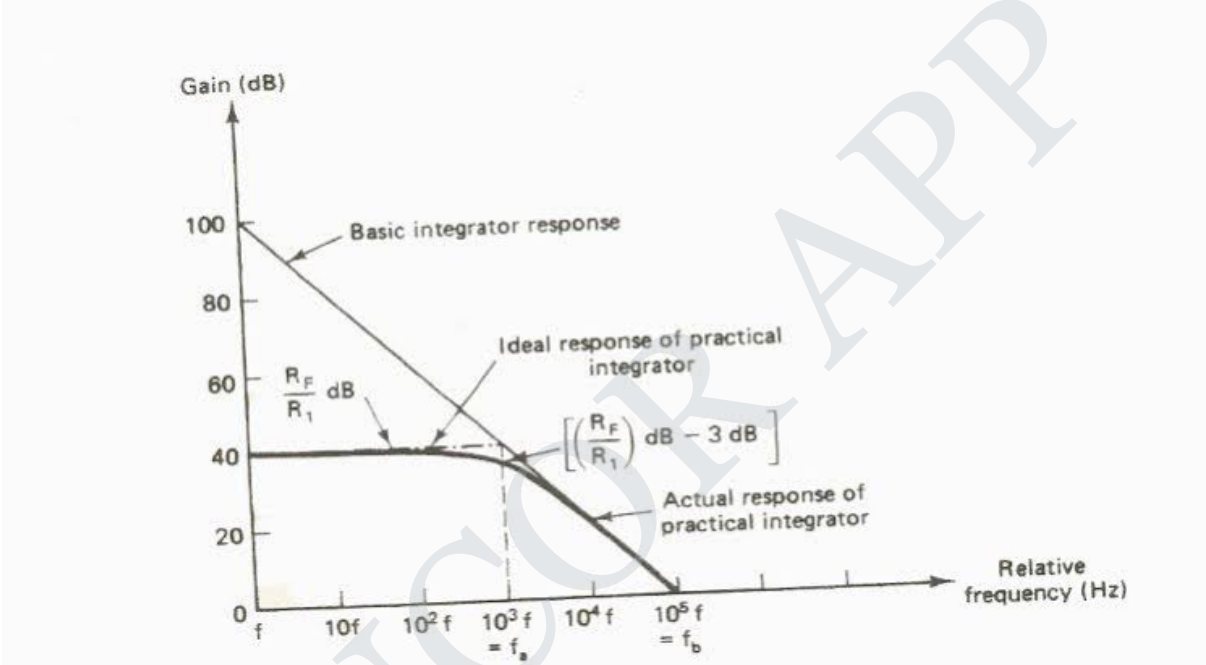
$$V_0(t) = -\frac{1}{R_1C_F}\int V_i\,dt + V_O(0)$$

$V_O(0)$ is the initial output voltage (Voltage at t =0)

R_1C_F is the time constant of an integrator. **The negative sign in the output expression indicates 180° phase shift between input and output.**

The frequency at which the gain of the integrator is 0 db[High Frequency Limit] is given by

$$f_B = \frac{1}{2\pi R_1C_F}$$



One of the main demerit of this lossless integrator is at 0 Hz , the integrator gain and the output becomes infinite. To avoid infinite gain at low frequency , a resistor R_F which is very much greater than R_1 [R_F = 10 R_1] is placed in parallel to C_F. The resulting integrator is called **practical or lossy or dc stabilized** integrator. The resistor R_F makes the low frequency gain to be $-\frac{R_F}{R_1}$.(i.e. equal to the gain of inverting amplifier). The value of feedback capacitance C_F is of the order of 0.001 µF to 10 µF and consist of Teflon[C_2F_4] or Polystyrene[C_8H_8] or Mylar[$C_{10}H_8O_4$] as dielectric.

The frequency at which the gain of the integrator is $-\frac{R_F}{R_1}$ dB[Low Frequency Limit] is given by

$$f_A = \frac{1}{2\pi R_FC_F}$$

If the input voltage frequency is less than f_A , the circuit acts as a simple **inverting amplifier and does not do integration**. If the input voltage frequency is equal to f_A , the circuit acts as an **integrator with 50% accuracy**. If the input voltage frequency is equal to $10f_A$, the circuit acts as an **integrator with 99% accuracy.**

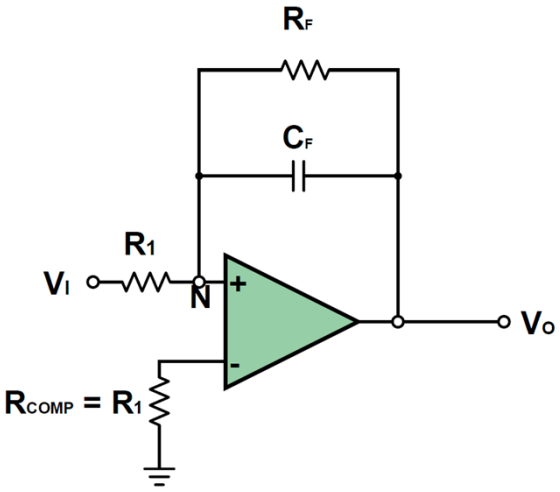


Fig. Practical Integrator

Transfer function of ideal integrator , $|A| = \frac{V_O(j\omega)}{V_I(j\omega)} = \frac{1}{\omega R_1 C_F}$

Transfer function of practical integrator , $|A| = \frac{V_O(j\omega)}{V_I(j\omega)} = \frac{R_F/R_1}{\sqrt{1+(\omega R_F C_F)^2}}$

7. Explain the methods of frequency compensation used in operational amplifiers. (10)

The method of modifying loop gain response of OP-AMP so that it behaves like single break frequency response which provides sufficient positive phase margin is called **frequency compensation**. OP-AMP circuits with **high closed loop gain** are **easy to compensate than OP-AMP with low closed loop gain**. There are two types of frequency compensation technique:

External Frequency Compensation:

In this method , the compensating network is connected to the system externally to alter the response as per the requirement. There are three types of external compensation technique:

(i) **Dominant Pole Compensation:**

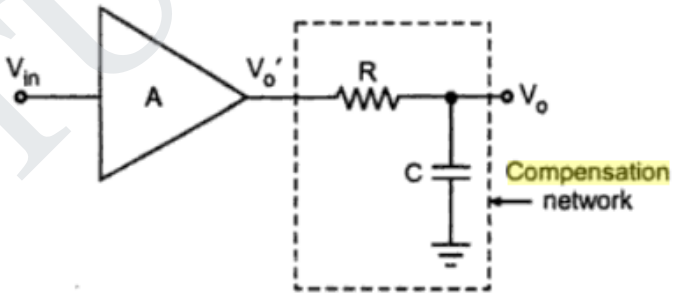


Fig. 4.11 Dominant pole compensation

Consider an OP-AMP with three break frequencies and loop gain A.

$$A = \frac{A_{OL}}{(1+j\frac{f}{f_1})(1+j\frac{f}{f_2})(1+j\frac{f}{f_3})}$$

In this method , the **transfer function or closed loop gain A** is modified by introducing a dominant pole through addition of a RC network at the output of OP-AMP.

Dominant Pole means the pole with magnitude much smaller than the existing ones. Therefore the break frequency of the compensating network is lesser than the existing ones.

The transfer function of the compensating network can be obtained as :

A_1 = Transfer function of compensating network

$$= \frac{V_o}{V_o'}$$

V_o

By the voltage divider rule applied to the network,

$$A_1 = \frac{V_o}{V_o'} = \frac{-jX_C}{R - jX_C} \quad \ldots (1)$$

$$= \frac{-\frac{j}{2\pi f C}}{R - \frac{j}{2\pi f C}} = \frac{1}{\frac{R}{\left(-\frac{j}{2\pi f C}\right)} + 1} \quad \ldots (2)$$

As $\frac{1}{-j} = +j$, we can write

$$\therefore \quad A_1 = \frac{1}{1 + j2\pi f R C} \quad \ldots (3)$$

Let $$f_d = \frac{1}{2\pi R C} \quad \ldots (4)$$

$$\boxed{A_1 = \frac{1}{1 + j\left(\frac{f}{f_d}\right)}} \quad \ldots (5)$$

Where f_d = break frequency of the compensating network

Hence the compensated transfer function becomes

$$A' = AA_1 \quad \ldots (6)$$

$$\therefore \quad \boxed{A' = \frac{A_{OL}}{(1 + j\frac{f}{f_d})(1 + j\frac{f}{f_1})(1 + j\frac{f}{f_2})(1 + j\frac{f}{f_3})}} \quad \ldots (7)$$

Values of R and C selected in such a way closed loop gain drops to 0 dB with a slope of -20 dB per decade and at a frequency where the poles of UNCOMPENSATED SYSTEM contributes a small phase shift.

Generally f_D is selected in such a way the magnitude plot of compensated transfer function passes through 0 dB at the pole f_1 of A.[A- uncompensated transfer function]

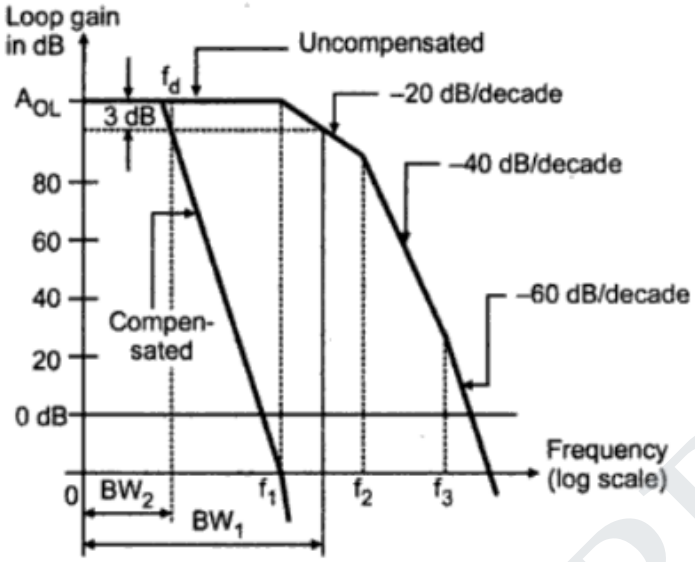


Fig. 4.12 Dominant pole compensation

Merits:

- As the noise frequency components are outside the smaller bandwidth , the noise immunity of the system improves.
- Adjusting the value of f_D , adequate phase margin and stability of the system is ensured.

Demerits:

- 3 dB down bandwidth reduces drastically for the compensated OP-AMP when compared to the uncompensated OP-AMP.

Pole Zero Compensation: **(Lag Compensation)**

Consider an OP-AMP with three break frequencies and loop gain A.

$$A = \frac{A_{OL}}{(1+j\frac{f}{f_1})(1+j\frac{f}{f_2})(1+j\frac{f}{f_3})}$$

In this method , the **transfer function or closed loop gain A** is modified by introducing a pole and zero through addition of a RC network at the output of OP-AMP. The **zero is added at higher frequency while the pole is added at lower frequency**.

The transfer function of the compensating network is say A_1.

$$A_1 = \frac{V_o}{V_o'}$$

By the voltage divider rule,

$$A_1 = \frac{Z_1}{Z_1 + Z_2} \quad \ldots (8)$$

Now $$Z_2 = R_2 - jX_{C2} \quad \ldots (9)$$

And $$Z_1 = R_1 \quad \ldots (10)$$

$$\therefore \quad A_1 = \frac{R_2 - jX_{C2}}{R_1 + R_2 - jX_{C2}} = \frac{R_2 - \frac{j}{2\pi f C_2}}{R_1 + R_2 - \frac{j}{2\pi f C_2}} = \frac{\frac{R_2}{\left[\frac{-j}{2\pi f C_2}\right]} + 1}{\frac{R_1 + R_2}{\left[\frac{-j}{2\pi f C_2}\right]} + 1}$$

Now $$-\frac{1}{j} = +j$$

$$\therefore \quad \boxed{A_1 = \frac{1 + j2\pi f R_2 C_2}{1 + j2\pi f (R_1 + R_2) C_2}} \quad \ldots (11)$$

Now let $$f_1 = \frac{1}{2\pi R_2 C_2} \quad \ldots (12)$$

And $$f_o = \frac{1}{2\pi (R_1 + R_2) C_2} \quad \ldots (13)$$

$$\therefore \quad \boxed{A_1 = \frac{1 + j\left(\frac{f}{f_1}\right)}{1 + j\left(\frac{f}{f_o}\right)}} \quad \ldots (14)$$

The values of R_1 , R_2 and C_2 are selected in such a way **the break frequency for the zero matches with first corner frequency f_1 of the uncompensated system while the break frequency of the pole matches with second corner frequency f_2 of the uncompensated system**.

$$A' = AA_1$$

$$\boxed{A_1 = \frac{A_{OL}\left(1 + j\frac{f}{f_1}\right)}{\left(1 + j\frac{f}{f_o}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}} \quad \ldots (15)$$

where $0 < f_o < f_1 < f_2 < f_3$

The values of R_1 , R_2 and C_2 are selected in such a way the loop gain of the compensated system(**A'**) passes through 0 dB at f_2.

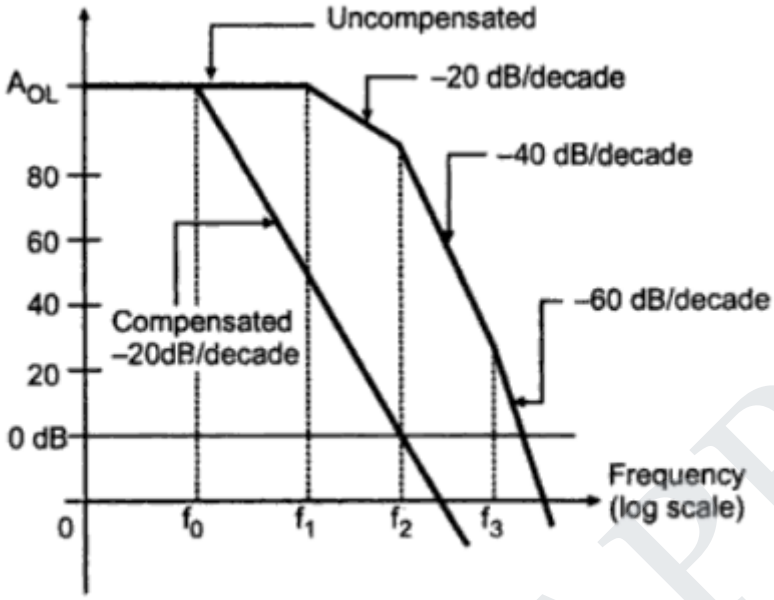


Fig. 4.14 Pole-zero compensation

As compared to **dominant pole compensation , this method improves the bandwidth by $f_2 - f_1$. The value of the compensation capacitor is generally large , therefore the compensating elements are connected externally.**

Internal Frequency Compensation: (Miller Effect Compensation)

In OP-AMPs like IC 741 , built-in lag compensation is provided. A capacitor ranging from 10 pF to 30 pF is placed between input and output stage to achieve the necessary compensation.

In Miller effect compensation , a capacitor is connected in the feedback path of the Darlington pair used in the output stage of the op-amp.

The C_c is the compensating capacitor, R_i is the input resistance and R_o is the output resistance of the Darlington stage. The gain of the Darlington stage is given by,

$$a_2 = -G_{mc} R_o$$

Where G_{mc} = Transconductance of the stage

Looking through the input terminal C_c appears as the Miller capacitance C_M and from the results of Miller effect we can write,

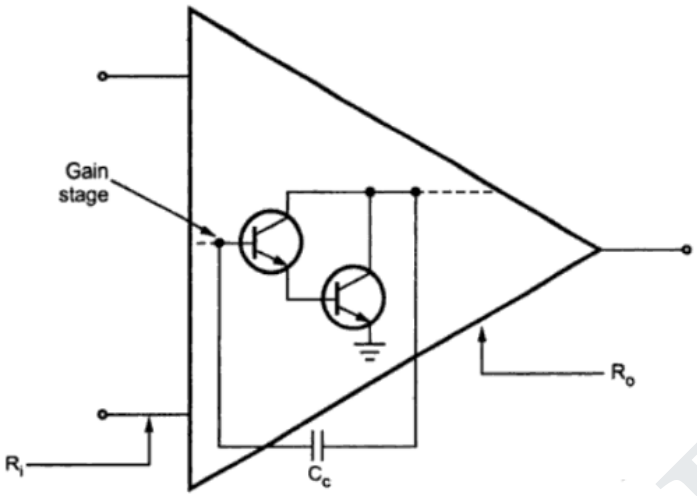


Fig. 4.20 Miller effect compensation

$$Z_{CM} = \frac{Z_{C_c}}{1+a_2}$$

Where $Z_{CM} = \frac{1}{j\omega C_M}$ and $Z_{C_c} = \frac{1}{j\omega C_c}$

$$\therefore \quad \frac{1}{j\omega C_M} = \frac{\frac{1}{j\omega C_c}}{(1+a_2)}$$

$$\therefore \quad C_M = (1 + a_2)\, C_c$$

Thus effectively C_c gets multiplied by $(1 + a_2)$ where a_2 is the gain of the stage which is large, as viewed through the input terminals. Thus practically small C_c values can be used, which is helpful from monolithic fabrication point of view.

This Miller equivalent capacitance C_M forms a low pass RC section with input resistance R_i whose corner frequency is given by,

$$f_d = \frac{1}{2\pi C_M R_i} \qquad \ldots (16)$$

In addition to the multiplying the capacitance, Miller effect has another advantage. It causes rearrangement of original poles and cause **Pole splitting**. This means due to Miller effect compensation, f_1 gets lowered while f_2 gets raised. Thus poles get diverged. This increases the bandwidth compared to dominant pole compensation.

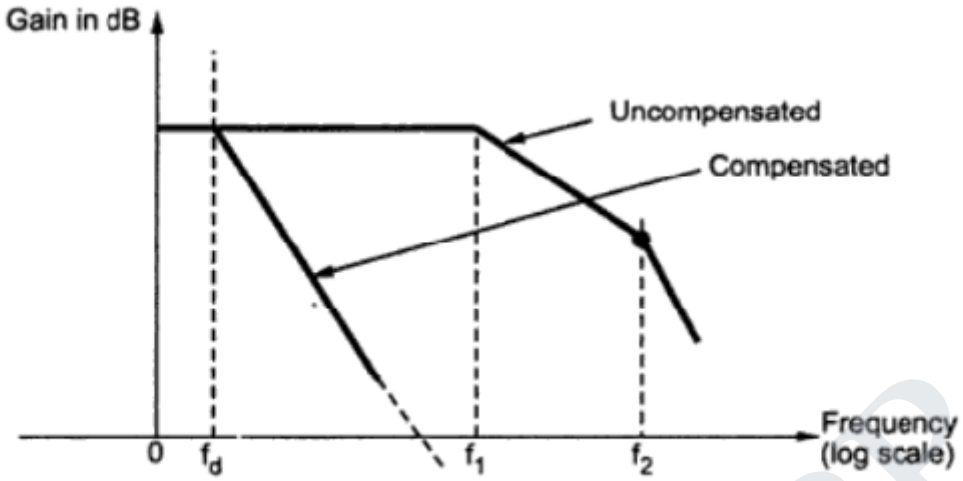


Fig. 4.21 Miller effect compensation

Such compensated op-amps usually have single break frequency and are inherently stable in nature irrespective of value of closed loop gain. External compensating network is not required for such op-amps.

Some internally compensated op-amps are Fairchild's μA 741, National semiconductor's LM 107, LM 741, LM 112 and Motorola's MC 1858.

8. What is slew rate and how it can be improved (6)

Slew rate is a type of **AC characteristic of OP-AMP and is** defined as the maximum rate of change of output voltage caused by a **step input voltage and is usually specified in V/μs. A slew rate of 1V/μs means the output voltage rises or falls by 1V in one microsecond. Practical IC op-amps have a slew rate between 0.1 V/μs to 1000 V/μs.**

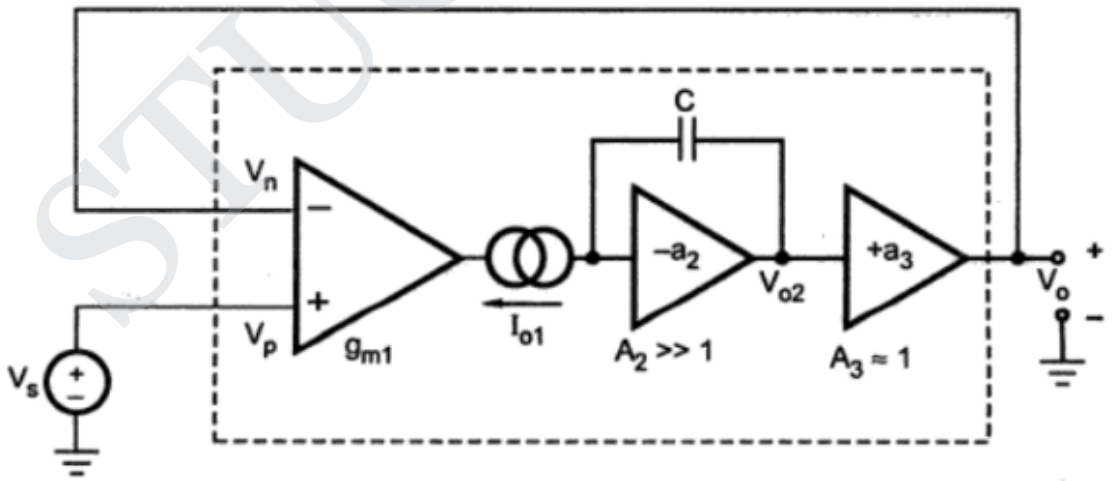


Fig. 4.16 Op-amp model for slew rate analysis

Different methods to improve slew rate are as follows:

(i) **Increasing gain-bandwidth product or unity-gain bandwidth(f_T) of OP-AMP:**

- Higher the gain bandwidth product of OP-AMP , higher is the slew rate.
- To increase the gain-bandwidth product , the internal capacitor value has to be reduced.
- Frequency compensation schemes like feed-forward compensation is used for achieving high gain-bandwidth product.

(ii) **Increasing $I_{O1(SAT)}$ [Input Stage Saturation Current Level]of OP-AMP**:

- Higher the $I_{O1(SAT)}$ of OP-AMP , higher is the slew rate. The $I_{O1(SAT)}$ cannot be externally controlled by the user.
- To increase $I_{O1(SAT)}$ without affecting g_M and f_T , we need to add an additional transistor pair at input which goes into conduction during large signal conditions and causes rapid charging and discharging of C.
- This type of adjustments are possible in **programmable OP-AMPs** where the operating point of the device can be set by the user with a **external current setting pin I_{SET}**

(iii) **Reducing g_{M1} (Input Stage Transconductance)of OP-AMP:**

- Lower the g_{M1} of OP-AMP , higher is the slew rate. This is achieved through employing **emitter degeneration in OP-AMP(**i.e. adding resistors in series with the coupled emitter of input differential pair).
- Another method of reducing g_{M1} , is to replace the BJT differential pair at input with FET differential pair. The transconductance value of FETs are less than that of BJT. Added merit of using FET differential pair is low input bias and input offset currents when compared to BJT differential pair.

9. Discuss the second order high pass filter with its frequency response and design the circuit with a cut-off frequency of 5 kHz (8)

Second Order High Pass Butterworth Filter:

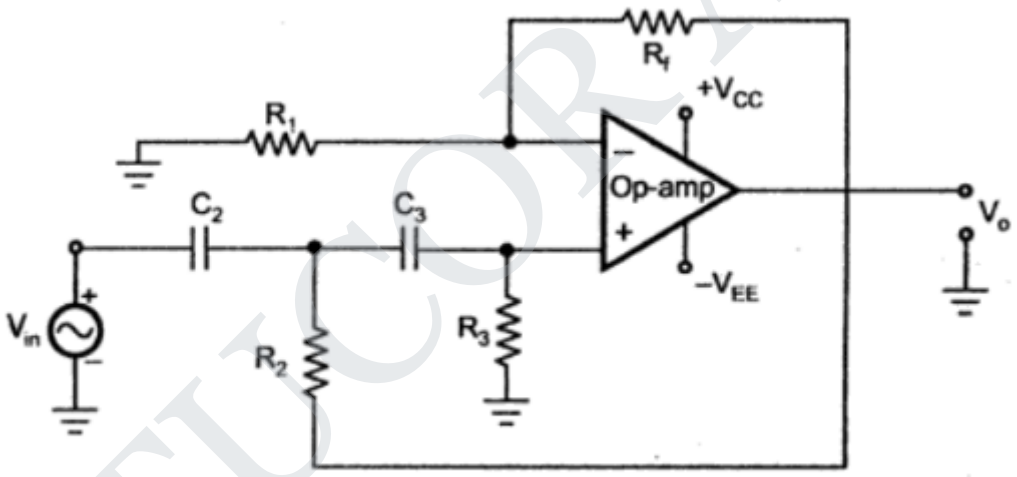


Fig. 5.22 Second order high pass Butterworth filter

- The second order high pass butterworth filter has gain roll-off[lower down] at the rate of +40 dB per decade in the stop band.
- The second order high pass butterworth filter can also be realized by interchanging the positions of resistors and capacitors in a second order low pass filter.

Expression for cut-off frequency:

The input RC network in Laplace domain

$$I_1 = I_2 + I_3 \quad \ldots\ldots(A)$$

$$\frac{V_{in} - V_1}{R_2} = \frac{V_1 - V_o}{\left(\frac{1}{sC_2}\right)} + \frac{V_1 - V_A}{R_3} \quad \ldots\ldots(B)$$

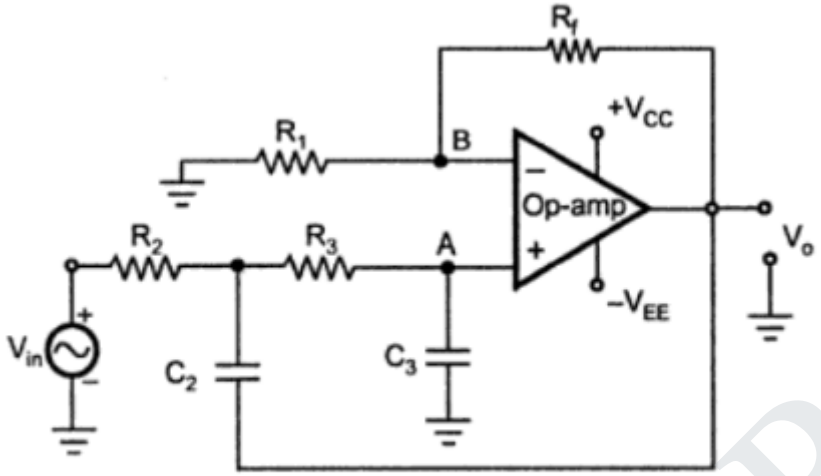


Fig. 9.20 Second order low pass Butterworth filter

Using potential divider rule we can write

$$V_A = V_1 \left[\frac{\frac{1}{sC_3}}{R_3 + \frac{1}{sC_3}} \right] \quad \ldots (3)$$

$$V_A = \frac{V_1}{1 + sR_3 C_3} \quad \ldots (4)$$

$$V_1 = V_A (1 + s R_3 C_3)$$

$$\frac{V_{in} - V_A (1+sR_3 C_3)}{R_2} = \frac{V_A (1+s R_3 C_3) - V_o}{\left(\frac{1}{sC_2}\right)} + \frac{V_A (1+s R_3 C_3) - V_A}{R_3}$$

$$\frac{V_{in}}{R_2} + V_o (s C_2) = V_A \left[\frac{(1+s R_3 C_3)}{R_2} + s C_2 (1+s R_3 C_3) + \frac{(1+s R_3 C_3)}{R_3} - \frac{1}{R_3} \right]$$

$$\therefore \frac{V_{in}}{R_2} + V_o (s C_2) = V_A \left[\frac{R_3 (1+s R_3 C_3) + R_2 R_3 s C_2 (1+s R_3 C_3) + R_2 (1+s R_3 C_3) - R_2}{R_2 R_3} \right]$$

$$\therefore (R_3 V_{in} + V_o s R_2 R_3 C_2) = V_A [(1 + s R_3 C_3) (R_3 + R_2 R_3 s C_2 + R_2) - R_2]$$

$$V_A = \frac{R_3 V_{in} + V_o s R_2 R_3 C_2}{[(1+s R_3 C_3)(R_3 + R_2 R_3 C_2 s + R_2) - R_2]} \quad \ldots (5)$$

For non-inverting op-amp

$$V_o = A_F V_A$$

where $A_F = 1 + \frac{R_f}{R_1}$

and V_A = the voltage at the noninverting terminal

$$\therefore \quad V_o = A_F \left[\frac{R_3 V_{in} + V_o\, s R_2 R_3 C_2}{(1+s R_3 C_3)(R_3 + R_2 R_3 C_2 s + R_2) - R_2} \right]$$

$$\therefore \quad \frac{A_F R_3 V_{in}}{(1+s R_3 C_3)(R_3 + R_2 R_3 C_2 s + R_2) - R_2} = V_o \left[1 - \frac{s R_2 R_3 C_2}{(1+s R_3 C_3)(R_3 + R_3 R_2 C_2 s + R_2) - R_2} \right]$$

$$\therefore A_F R_3 V_{in} = V_o \left[(1 + s R_3 C_3)(R_3 + R_3 R_2 C_2 s + R_2) - R_2 - s R_2 R_3 C_2 \right]$$

$$\therefore \frac{V_o}{V_{in}} = \frac{A_F}{s^2 + \frac{(R_3 C_3 + R_2 C_3 + R_2 C_2 - A_F R_2 C_2)\, s}{R_2 R_3 C_2 C_3} + \frac{1}{R_2 R_3 C_2 C_3}} \quad \ldots (7)$$

As the highest degree of the polynomial in the denominator is 2 , the given filter is a **second order filter**

The standard form of transfer function of second order system

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad \ldots..(8)$$

A = overall gain

ξ – Damping ratio

ω_N – natural frequency or resonant frequency of oscillations

$$\omega_n^2 = \frac{1}{R_2 R_3 C_2 C_3} \quad \ldots.(9)$$

$$\therefore \quad \omega_H^2 = \frac{1}{R_2 R_3 C_2 C_3} \quad \ldots\ldots.(10)$$

$$\therefore \quad (2\pi f_H)^2 = \frac{1}{R_2 R_3 C_2 C_3}$$

$$\therefore \quad f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

Since the positions of R and C in this high pass filter are the interchanged ones than those existing in low pass filter , f_H becomes f_L.

f_L is the **lower cut-off frequency**

Replacing s by jω, the transfer function can be written in the frequency domain and hence, finally, can be expressed in the polar form as

$$\frac{V_o}{V_{in}} = \left|\frac{V_o}{V_{in}}\right| \angle \phi$$

Where $\left|\frac{V_O}{V_{IN}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$

A_F = Passband gain = 1.586 to ensure second order butterworth response

$R_F = 0.586\, R_1$

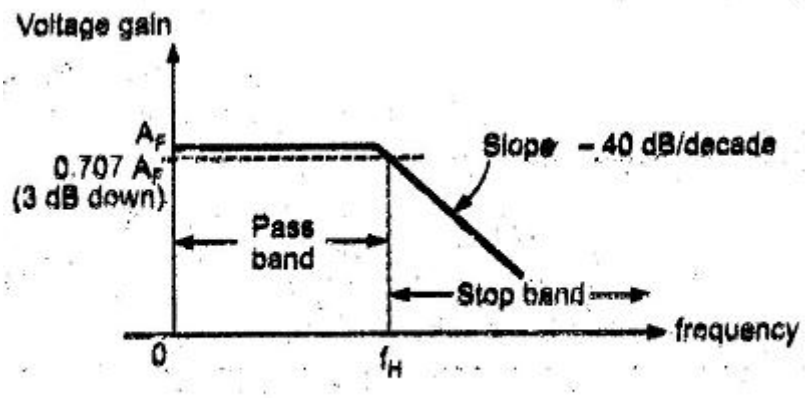


Fig. 2.78 Frequency response

Design a second order highpass butterworth filter with a cut-off frequency 5 kHz:

Solution : i) A second order Butterworth active high pas filter for a cut-off frequency of 5 kHz : The cut-cíf frequency is $f_o = 5$ kHz

$$\text{Choose } R = 10\,k\Omega$$

$$\therefore \quad f_0 = \frac{1}{2\pi RC}$$

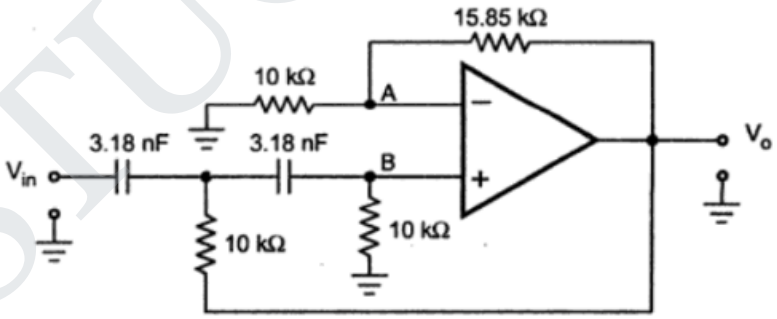
$$\text{i.e.} \quad C = \frac{1}{2\pi \times 10 \times 10^3 \times 5 \times 10^3} = 3.18\ nF$$

For second order Butterworth filter,

$$\frac{R_f}{R_1} = 1.585$$

Choose R = 10 kΩ hence R_f = 15.85 kΩ

The designed circuit is shown in the Fig. 5.49.



10. What is Slew rate ? List the causes of slew rate and explain its significance in applications. (10)

Slew rate is a type of **AC characteristic of OP-AMP and is** defined as the maximum rate of change of output voltage caused by a **step input voltage and is usually specified in V/µs. A slew rate of 1V/µs means the output voltage rises or falls by 1V in one microsecond. Practical IC op-amps have a slew rate between 0.1 V/µs to 1000 V/µs.**

Causes of slew rate:

Slew rate issue arises from the internal circuitry of an OP-AMP. The various causes for slew rate issues are as follows:

Frequency Compensation:

- Capacitors used within the chip for reduction of high frequency response have a marked effect on slew rate.

- Limiting the frequency response reduces the rate of change of output which in turn affects slew rate.

Output Driver Limitations:

- The low current levels in the output stage of an OP-AMP limits the rate of change of output and hence the slew rate.
- Suppose if the output stage employs a complementary amplifier , the slightly different characteristics of each half will cause a small amount on the difference between rise and fall slew rate capabilities.

High gain input stages:

- OP-AMPs have high gain differential input stages. The high gain transconductance amplifiers will start to function as a constant current source due to the saturation of input signals. When this happens , the rate of change of output is severely affected and hence the slew rate.

Significance of slew rate in applications:

Slew rates limit the response speed of all large signal waveshapes. For a sine wave input , the effect of slew rate limiting can be calculated as follows:

Consider a voltage follower

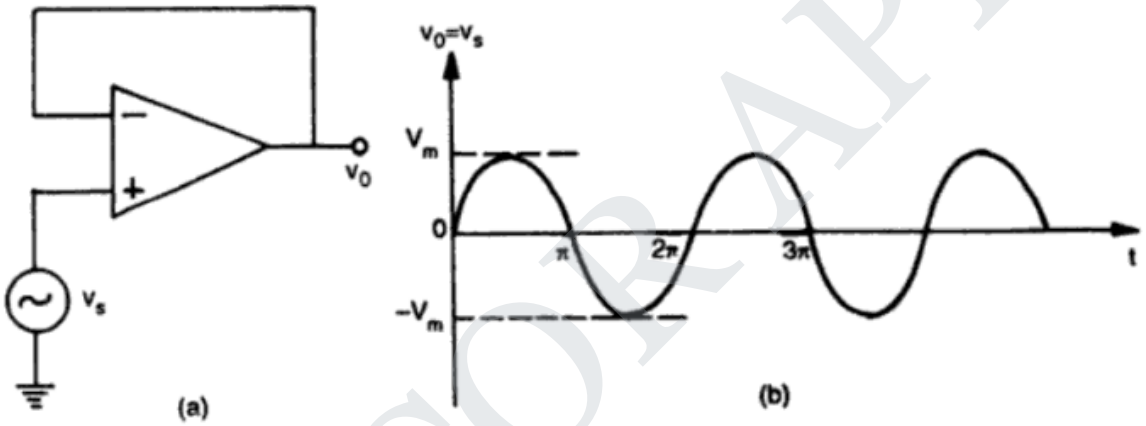


Fig. 3.12 (a) Voltage follower (b) Input/output waveform

The input is large amplitude , high frequency sine wave.

If $V_S = V_M \sin \omega t$

Then output $V_O = V_M \sin \omega t$

The rate of change of output voltage is given by

$$\frac{dV_O}{dt} = \omega V_M \cos\omega t$$

The maximum rate of change of output voltage occurs when $\cos\omega t = 1$

$$SR = \frac{dV_O}{dt}\Big|_{max} = \omega V_M$$

Therefore Slew rate = $2\pi f V_M$ volts/sec.

$$\text{or } \frac{2\pi f V_M}{10^6} \text{ V/}\mu\text{s} \quad \text{.....(B)}$$

f – Input frequency in Hz

V_M = Peak value of output voltage

If the RHS of eqn(B) is less than slew rate of the op-amp , the output will be undistorted. If the frequency or amplitude of input signal is increased to exceed slew rate of op-amp , the output will be distorted.

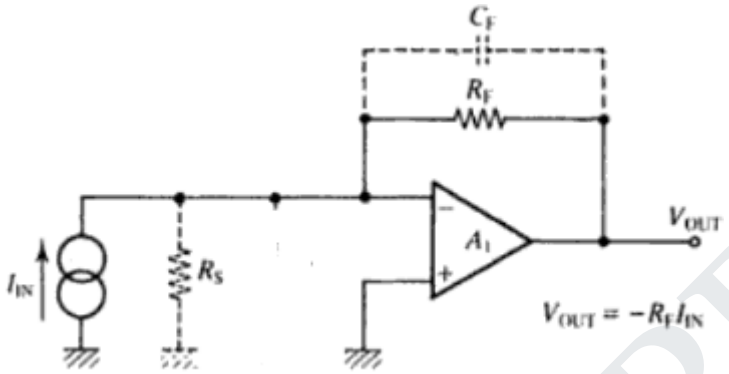
The maximum input frequency f_{MAX} at which we can obtain an undistorted output voltage of peak value V_M is given by

$$f_{MAX}\,(Hz) = \frac{Slew\ Rate}{6.28 \times V_M} \times 10^6$$

The f_{MAX} is called **full power response. It is the maximum frequency of a large amplitude sine wave with which an op-amp can have without distortion.**

11. Draw and explain the operation of current to voltage converter (8)

Current to Voltage Converter (Transresistance or Transimpedance amplifier)



Photocell , photodiode and photovoltaic cell give an output current proportional to incident radiant energy or light. The current through these devices can be converted into voltage by using **current-to-voltage converter and thereby amount of radiant energy incident on the photo-device can be measured.** Since inverting input terminal is at **virtual ground ,** no current flows through R_S and I_{IN} current flows through the feedback resistor R_F**.** Therefore the output voltage $V_{OUT} = -R_F I_{IN.}$ The lowest current that can be measured by the circuit depends on the bias current of the OP-AMP. The capacitor C_F parallel to R_F reduces high frequency noise and oscillations.

12. What are the limitations of an ordinary op-amp differentiator ? Draw the circuit of a practical differentiator that will eliminate these limitations (8)

Limitations of ideal differentiator:

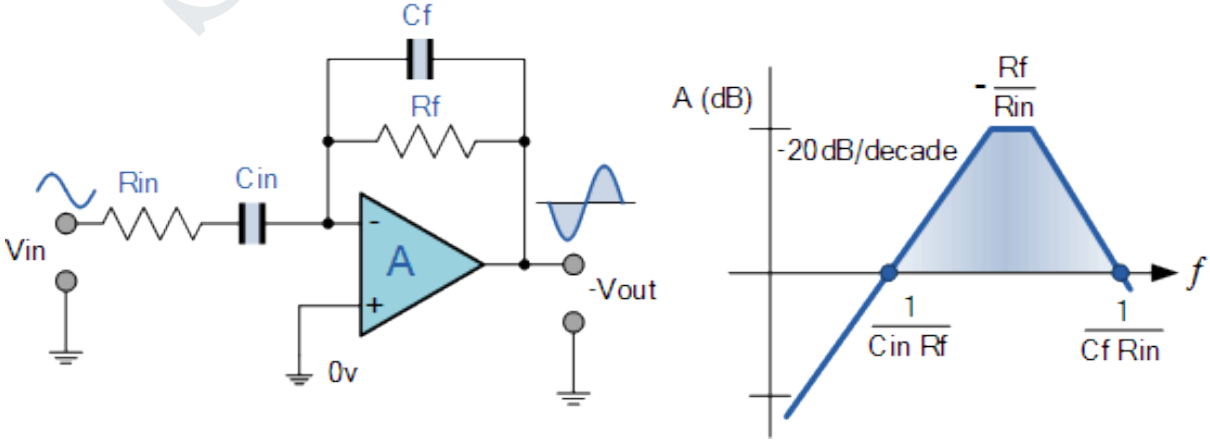
The frequency response of an ideal op-amp differentiator is given by

$$|A| = \frac{f}{f_A}$$

$$\text{Where } f_A = \frac{1}{2\pi R_F C_1}$$

At $f = f_A$, $|A|=1$ i.e. 0 dB. The gain increases at a rate of +20 dB/decade. Thus at high frequency ,a differentiator may become unstable and break into oscillations. Another limitation is that the input impedance decreases with increase in frequency , thereby making the circuit sensitive to **high frequency noise**.

To overcome these limitations of ideal differentiator , a practical differentiator is designed as follows:



The **practical op-amp differentiator eliminates the problem of instability and high frequency noise.**

The transfer function of the practical OP-AMP differentiator is given by

$$\frac{V_O(s)}{V_I(s)} = -\frac{Z_F}{Z_1} = -\frac{sR_FC_1}{(1+sR_FC_F)(1+sR_1C_1)} \quad \text{....(A)}$$

For $R_FC_F = R_1C_1$ we get

$$\frac{V_O(s)}{V_I(s)} = -\frac{Z_F}{Z_1} = -\frac{sR_FC_1}{(1+sR_1C_1)^2} = -\frac{sR_FC_1}{(1+j\frac{f}{f_b})^2}$$

$$\text{Where } f_B = \frac{1}{2\pi R_1C_1} \quad \text{.....(B)}$$

From equation (B) , it is evident that the **gain increases at a rate of +20 dB per decade for $f < f_B$ and decreases at a rate of -20 dB per decade for $f > f_B$. This 40 dB per decade change is caused by R_1C_1 and R_FC_F.**

For the ideal differentiator , the gain increases at a rate of +20 dB per decade for $f \geq f_B$, thereby causing high frequency stability problems.

The value of f_B selected in such a way $f_A < f_B < f_C$, where f_C is the unity-gain bandwidth or gain-bandwidth product of OP-AMP in open loop configuration.

For good frequency response one must ensure $T \geq R_FC_1$, where T is the time period of the input signal. When R_FC_1 very much greater than R_1C_1 or R_FC_1 , the equation (A) reduces to $V_O/V_I = -sR_FC_1$, which is the equation of **ideal differentiator**.

A compensation resistor R_{COMP} equal to the parallel combination of $R_1||R_F$ connected to the non-inverting terminal to reduce the effect of bias current.

A good differentiator may be designed as follows:

→ Choose f_A equal to the highest frequency of the input signal. Assume a practical value of C_1(< 1 μF) and then calculate R_F.

→ Choose $f_B = 10\ f_A$. Now calculate the values of R_1 and C_F so that $R_1C_1 = R_FC_F$.

13. Draw the circuits for inverting , non-inverting and difference amplifier using op-amp. Also derive the expression for their gains.

Inverting Amplifier:

This device produces an output AC signal that is 180˚ out of phase with input signal. Input voltage is applied to inverting terminal of OP-AMP ; Non-Inverting terminal is grounded.

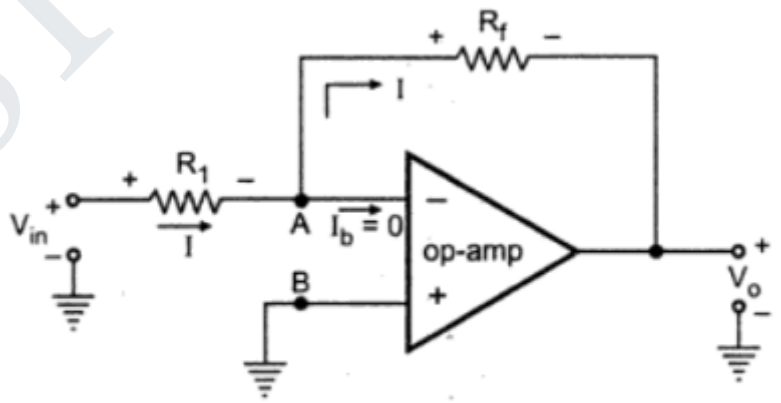


Fig. 2.44 Inverting amplifier

As node B is grounded, node A is also at ground potential, from the concept of virtual ground, so $V_A = 0$

$$\therefore \quad I = \frac{V_{in} - V_A}{R_1}$$

$$\therefore \quad I = \frac{V_{in}}{R_1} \qquad \ldots (1)$$

Now from the output side, considering the direction of current I we can write,

$$I = \frac{V_A - V_o}{R_f}$$

$$\therefore \quad I = \frac{-V_o}{R_f} \qquad \ldots (2)$$

Entire current I passes through R_f as op-amp input current is zero.

Equating (1) and (2) we get,

$$\frac{V_{in}}{R_1} = -\frac{V_o}{R_f}$$

$$\therefore \quad \frac{V_o}{V_{in}} = -\frac{R_f}{R_1} \qquad \ldots (3)$$

This gain is called gain with feedback A_{VF} or closed loop gain A_{CL} of the circuit.

$$\therefore \quad \boxed{A_{CL} = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1}}$$

Non-Inverting Amplifier:
This device produces an output signal which is having same phase as input signal. Input voltage is applied to non-inverting terminal ; Inverting terminal is grounded.

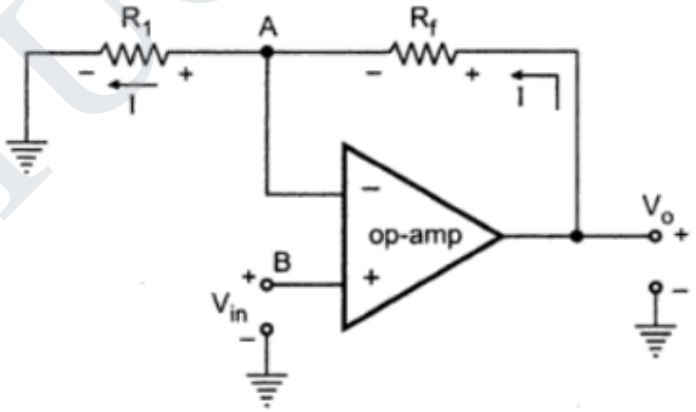


Fig. 2.49 Noninverting amplifier

The node B is at potential V_{in}, hence the potential of point A is same as B which is V_{in}.

$$\therefore \quad V_A = V_B = V_{in} \qquad \ldots (1)$$

From the output side we can write,

$$I = \frac{V_o - V_A}{R_f}$$

$$\therefore \quad I = \frac{V_o - V_{in}}{R_f} \qquad \ldots (2)$$

At the inverting terminal,

$$I = \frac{V_A - 0}{R_1}$$

$$\therefore \quad I = \frac{V_{in}}{R_1} \qquad \ldots (3)$$

Entire current passes through R_1 as input current of op-amp is zero.

Equating equations (2) and (3),

$$\therefore \quad \frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\therefore \quad \frac{V_o}{R_f} = \frac{V_{in}}{R_f} + \frac{V_{in}}{R_1}$$

$$\therefore \quad \frac{V_o}{R_f} = V_{in}\left[\frac{(R_1 + R_f)}{R_1 R_f}\right]$$

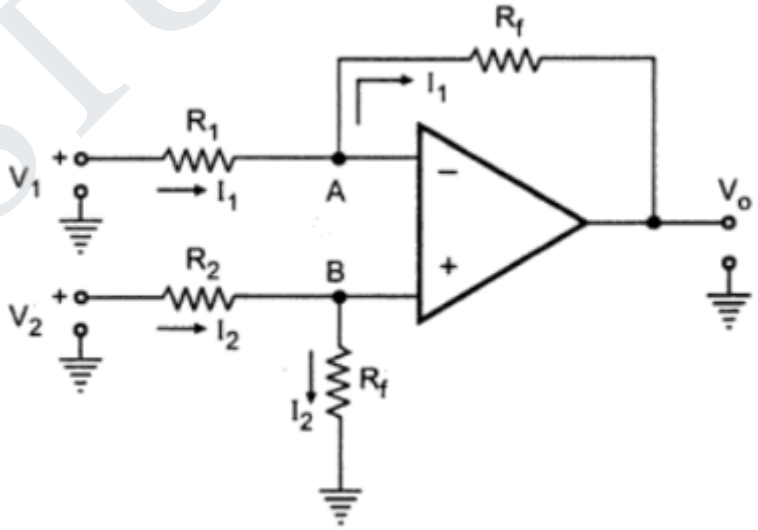
$$\therefore \quad \frac{V_o}{V_{in}} = \frac{(R_1 + R_f) R_f}{R_1 R_f} = \frac{R_1 + R_f}{R_1}$$

$$\therefore \quad \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}$$

$$\therefore \quad \boxed{A_{CL} = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}} \qquad \ldots (4)$$

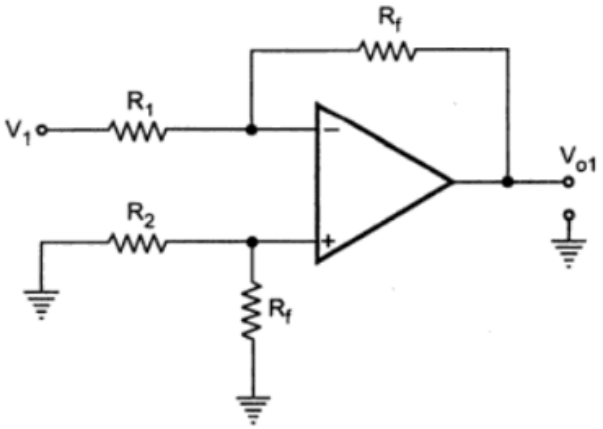
Subtractor or Difference Amplifier:

This device provides algebraic difference of input voltages as the output.



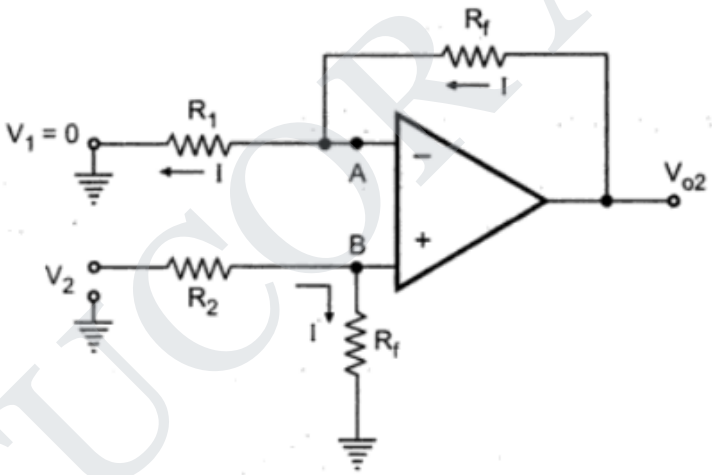
The relation between the input and output voltages found using **superposition principle.**

Case 1 : With V_2 zero, the circuit acts as an inverting amplifier, as shown in the Fig. 2.82. Hence we can write,



$$V_{o1} = -\frac{R_f}{R_1} V_1$$

Case 2 : While with V_i as zero, the circuit reduces to as shown in the Fig. 2.83.



That is the circuit acts as a NON-INVERTING AMPLIFIER.

Let potential of node B is V_B. The potential of node A is same as B i.e. $V_A = V_B$.

Applying voltage divider rule to the input V_2 loop,

$$V_B = \frac{R_f}{R_2 + R_f} V_2 \quad \ldots (2)$$

Now
$$I = \frac{V_A}{R_1} = \frac{V_B}{R_1} \quad \ldots (3)$$

And
$$I = \frac{V_{o2} - V_A}{R_f}$$

$$= \frac{V_{o2} - V_B}{R_f} \quad \ldots (4)$$

Equating the equations (3) and (4),

$$\frac{V_B}{R_1} = \frac{V_{o2} - V_B}{R_f}$$

$$\therefore \quad V_{o2} = \frac{R_1 + R_f}{R_1} V_B$$

$$\therefore \quad V_{o2} = \left[1 + \frac{R_f}{R_1}\right] V_B \quad \ldots (5)$$

Substituting V_B from (2) in (5) we get,

$$\boxed{V_{o2} = \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_f}\right] V_2} \quad \ldots(6)$$

Hence using Superposition principle,

$$V_o = V_{o1} + V_{o2}$$

$$= -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_1}\right] V_2 \quad \ldots (7)$$

Now if the resistances are selected as $R_1 = R_2$,

$$V_o = -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_1 + R_f}\right] V_2$$

$$= -\frac{R_f}{R_1} V_1 + \frac{R_f}{R_1} V_2$$

$$\therefore \quad \boxed{V_o = +\frac{R_f}{R_1}(V_2 - V_1)} \quad \ldots(8)$$

14. Explain the ideal and non-ideal DC characteristics of an op-amp (13)

Ideal DC characteristics of an OP-AMP:

Open Loop Voltage Gain or Differential Open Loop Voltage Gain or Large Signal Voltage Gain: Open Loop Voltage gain is the ratio of output voltage to input voltage of an op-amp under **open loop configuration** and **differential mode operation**. The unit of **differential open loop voltage gain is V/mV.**

$$A_{OL} = \frac{V_{out}}{V^+ - V^-},$$

$V^+ - V^-$ - Difference of input voltages.

Ideal Value : Infinity **Practical Value: 100 V/mV**

Input Impedance:
It is the opposition offered by an op-amp to the flow of current through its **inverting and non-inverting terminals.**
Ideal value : Infinity **Practical Value : 1 MΩ to 100 MΩ**

Output Impedance:
It is the opposition offered to the flow of current coming out from its output terminal. The value of the output impedance irrespective of the value of load resistance.
Ideal Value : 0 **Practical Value : 75 Ω**

Bandwidth
The range of frequency over which the amplifier performance is satisfactory is called **bandwidth.**
Ideal Value : Infinity **Practical Value : 1 MHz**

CMRR (Common Mode Rejection Ratio)
The ratio of differential mode voltage gain to common mode voltage gain is called CMRR. It is represented by **ρ.**
Ideal Value : Infinity **Practical Value : 90 dB**

Non-Ideal DC Characteristics:
Input Offset Current (I_{IOS}):
Absolute difference between the current flowing through inverting and non-inverting input terminals

$$I_{IOS} = |I_{B1} - I_{B2}|$$

I_{B1} – Current flowing into the non-inverting terminal
I_{B2} – Current flowing into the inverting terminal
Ideal Value : 0 **Practical Value : 20 nA**

Input Offset Voltage(V_{IOS}):
A small positive or negative DC voltage that has to be applied to the one of the input terminals under tezero input conditions to make the output voltage zero.

$$V_{IOS} = |V_{DC1} - V_{DC2}|$$

V_{DC1} – DC voltage applied to Non-inverting terminal
V_{DC2} = DC voltage applied to Inverting Terminal

Ideal Value: 0 **Practical Value : 2 mV**

Input bias Current : (I_B)
Absolute average of the current flowing through inverting and non-inverting input terminals.

$$I_B = \frac{|I_{B1} + I_{B2}|}{2}$$

Ideal Value : 0 **Practical Value : 80 nA**

Output Offset Voltage (V_{OOS}):
A small positive or negative DC voltage appearing at the output terminals of the op-amp due to **input offset current**.

$$V_{OOS} = V_O \text{ due to } V_{IOS} + V_O \text{ due to } I_B$$

Ideal Value : 0 **Practical Value : 2 mV**

Thermal Drift:
Thermal drift refers to variation of a parameter with respect to temperature variation. The parameters of op-amp that are affected by temperature variations are **(i) Input Bias current drift (ii) Input Offset Current Drift**

Input Bias Current Drift : The average rate of change of input bias current per unit change in temperature. The formula is as follows:

$$\frac{\Delta I_B}{\Delta T} \text{ [nA/°C or pA/°C]}$$

[nA = nano-ampere = 10^{-9} A ; pA = pico-ampere = 10^{-12} A]

Input Offset Current Drift : The average rate of change of input offset current per unit change in temperature. The formula is as follows:

$$\frac{\Delta I_{IOS}}{\Delta T} \text{ [nA/°C or pA/°C]}$$

[nA = nano-ampere = 10^{-9} A ; pA = pico-ampere = 10^{-12} A]

Input Offset Voltage Drift : The average change of input offset voltage per unit change in temperature. The formula is as follows:

$$\frac{\Delta V_{IOS}}{\Delta T} \text{ [µV/°C]}$$

[µV = micro volt = 10^{-6} V]

AC Characteristics:

Slew Rate :
Maximum rate of change of output voltage with respect to time. The formula is as follows:

$$S = \frac{I_{MAX}}{C}$$

I_{MAX} = Maximum value of charging current through the internal compensating capacitor of OP-AMP
C = Compensating capacitor in the feedback path of **Class-A Voltage Amplifier Stage of OP-AMP**

$$S = \frac{\Delta V_O}{\Delta t} \text{ [V/µs]}$$

ΔV_O = Change in output Voltage
Δt = Change in time
$S = 2\pi f_{MAX} V_{OUT(PEAK)}$
f_{MAX} = Full Power Bandwidth of the OP-AMP
$V_{OUT(PEAK)}$ = Peak value or Maximum Value or Amplitude of Output Voltage = $\frac{V_{OUT(PEAK\ to\ PEAK)}}{2}$

Ideal Value : Infinity **Practical Value : 0.5 V/µs**

PSRR(Power Supply Rejection Ratio) or PSV(Power Supply Sensitivity)
Ratio of change in input offset voltage to change in one of the supply voltage , keeping other supply voltage constant. V_{CC} is called **positive supply voltage** ; V_{EE} is called **negative supply voltage**
When V_{CC} is kept constant

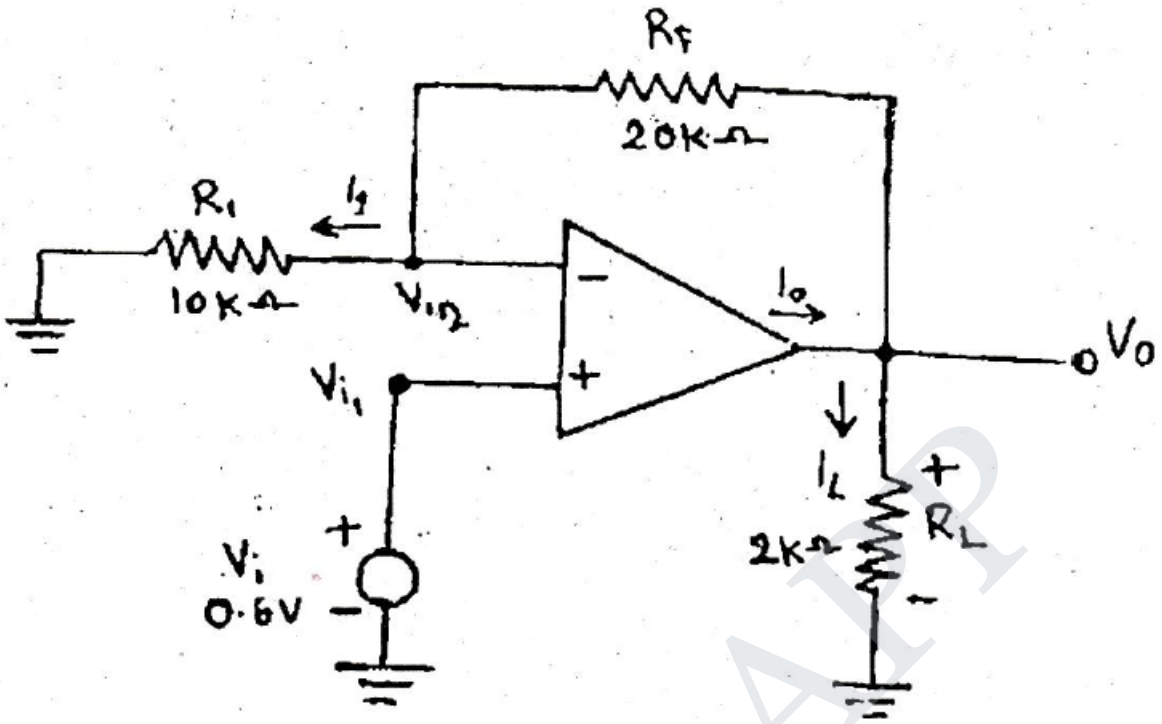
$$PSRR = \frac{\Delta V_{IOS}}{\Delta V_{EE}}$$

When V_{EE} is kept constant

$$PSRR = \frac{\Delta V_{IOS}}{\Delta V_{CC}}$$

Ideal Value : 0 **Practical Value : 30 µV/V**

15. For the given non-inverting amplifier shown in figure below , determine (i) A_V (ii) V_0 ; I_L and ; I_0



Given:
Input Resistance , R_1 = 10 kΩ
Negative Feedback Resistance , R_F = 20 kΩ
Load Resistance , R_L = 2 kΩ
V_I = Input Voltage = 0.6 V
Solution

(i) A_V = Closed Loop Voltage Gain of Non-Inverting Amplifier = $(1+\frac{R_F}{R_1})$

$$= (1+\frac{20 \times 10^3}{10 \times 10^3}) = 3 \text{ or } 20 \log_{10}(1.8) = 9.5 \text{ dB}$$

(ii) V_O = Output Voltage of Non-Inverting Amplifier = $(1+\frac{R_F}{R_1})$ V_I

$$= (1+\frac{20 \times 10^3}{10 \times 10^3}) \times 0.6 = 1.8 \text{ V}$$

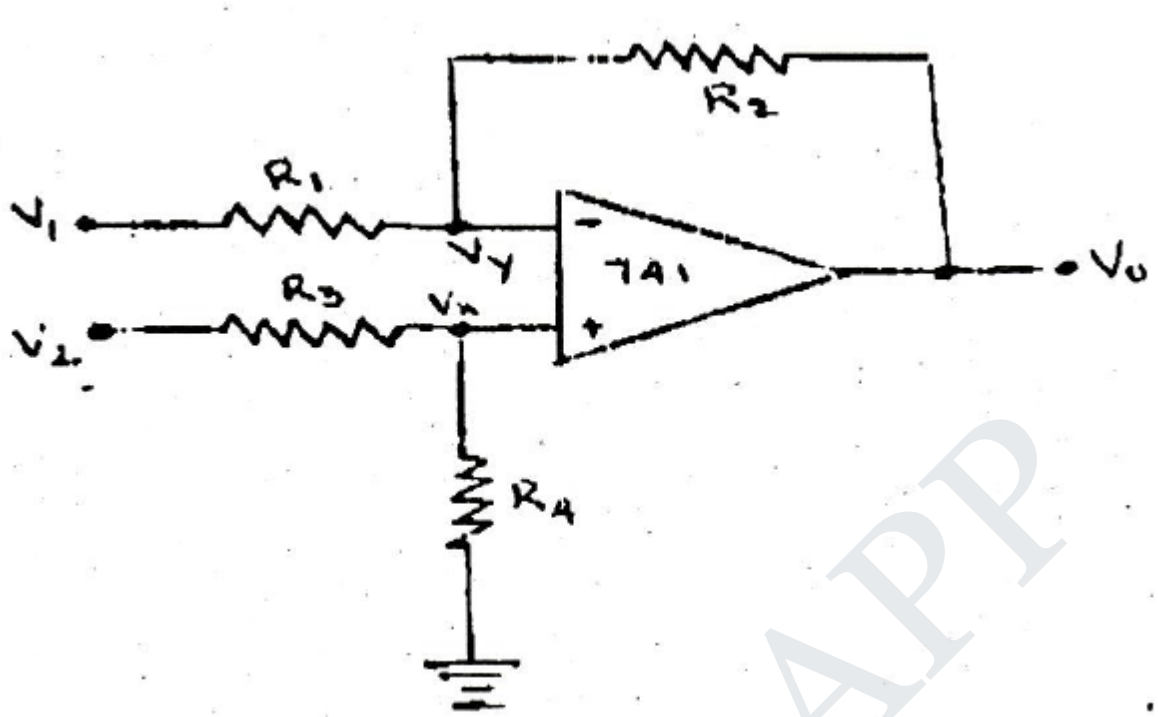
(iii) Load Current , $I_L = \frac{V_O}{R_L} = \frac{1.8}{2 \times 10^3} = 0.9$ mA

(iv) Output Current , $I_O = I_L + I_1$ (By Applying KCL at output node. $I_O - I_L - I_1 = 0$)

I_1 = Input Current $= \frac{V_O}{R_F} = \frac{1.8}{20 \times 10^3} = 0.09$ mA

Therefore $I_O = I_L + I_1 = 0.9$ mA + 0.09 mA = 0.99 mA

16. Find the following for the given Op-amp differential amplifier : (i) The gain of the amplifier (ii) The input resistance (iii) Output voltage , when the inputs are 1 sin(2000t) V and 1.2sin(2000t) and $R_1 = R_3 = 1.2$ kΩ ; and $R_2 = R_4 = 22$ kΩ (13)



Solution:

The given circuit is a subtractor or difference amplifier circuit

(i) The gain of the amplifier , $A_V = \frac{R_F}{R_1} = \frac{R_2 \text{ or } R_4}{R_1 \text{ or } R_3} = \frac{22 \times 10^3}{1.2 \times 10^3} = 18.33$

(or)

$20 \log_{10}(18.33) = 25.2$ dB

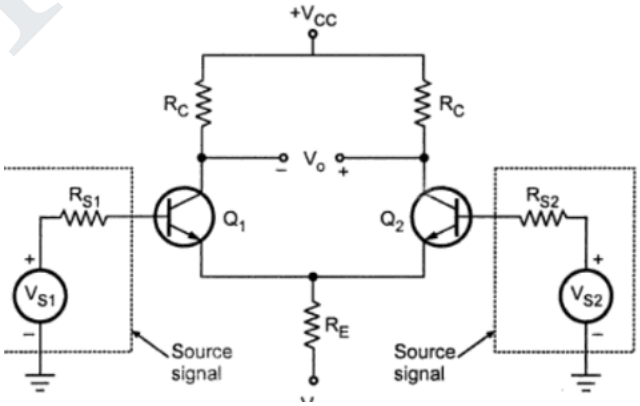
(ii) Input Resistance with V_1 acting alone , $R_1 = 1.2$ kΩ

Input Resistance with V_2 acting alone = $R_3 + R_4 = 1.2$ kΩ + 22 kΩ = 23.2 kΩ

(iii) Output Voltage , $V_O = \frac{R_F}{R_1}(V_2 - V_1) = 18.33\ (1.2 - 1) = 18.33 \times 2 = 36.66$ V

17. Draw the circuit of a symmetrical emitter coupled differential amplifier and derive for CMRR

Symmetrical Emitted Coupled Differential amplifier is also called Dual Input Balanced Output Differential Amplifier.



Derivation for Differential Gain:

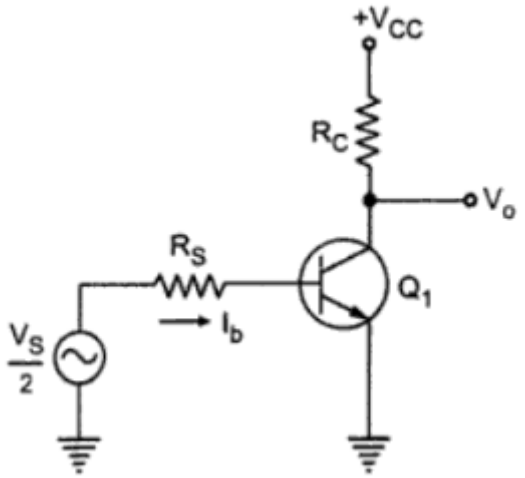


Fig. AC Equivalent Circuit for Differential Operation

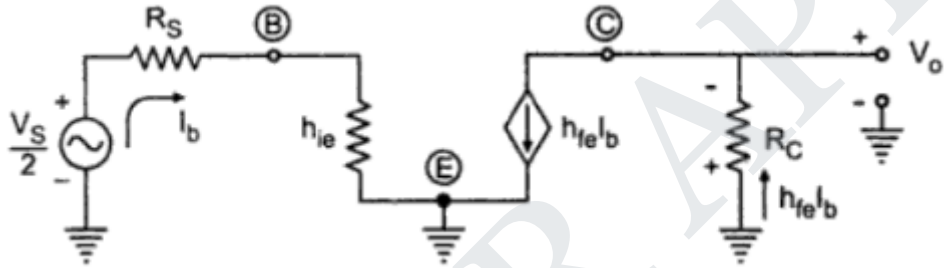


Fig. Approximate hybrid model for Differential Operation

Applying KVL to the input loop,

$$-I_b R_S - I_b h_{ie} + \frac{V_S}{2} = 0 \qquad \ldots(1.20)$$

$$\therefore \quad -I_b(R_S + h_{ie}) = -\frac{V_S}{2}$$

$$\therefore \quad I_b = \frac{V_S}{2(R_S + h_{ie})} \qquad \ldots(1.21)$$

Applying KVL to the output loop and considering directin of $h_{fe}I_b$,

$$V_o = -h_{fe} I_b R_C \qquad \ldots(1.22)$$

Substituting (1.21) in (1.22),

$$V_o = -h_{fe} R_C \frac{V_S}{2(R_S + h_{ie})}$$

$$\frac{V_o}{V_S} = \frac{-h_{fe} R_C}{2(R_S + h_{ie})} \qquad \ldots(1.23)$$

The negative sign indicates the phase difference between input and output.

Now two input signal magnitudes are $\frac{V_S}{2}$ but they are opposite in polarity, as 180° out of phase.

$$\therefore \quad V_d = V_1 - V_2$$

$$= \frac{V_S}{2} - \left(-\frac{V_S}{2}\right)$$

$$= V_S$$

$$A_d = \frac{h_{fe} R_C}{2(R_S + h_{ie})} \text{ (magnitude)}$$

Derivation of Common Mode Gain

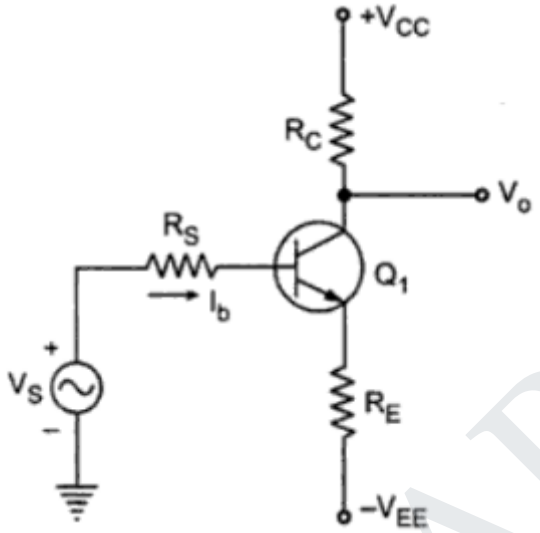


Fig. AC equivalent circuit for Common Mode Operation

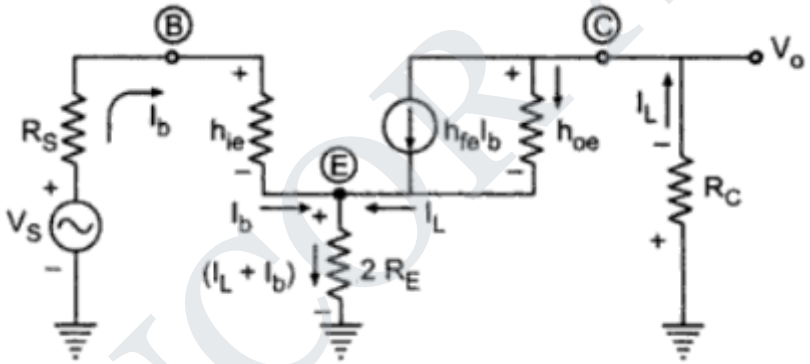


Fig. Approximate hybrid model for Common Mode Operation

current through R_C = load current I_L

effective emitter resistance = $2 R_E$

current through emitter resistance = $I_L + I_b$

current through h_{oe} = $(I_L - h_{fe} I_b)$

Applying KVL to the input side,

$$-I_b R_S - I_b h_{ie} - 2 R_E (I_L + I_b) + V_S = 0$$

$$\therefore \quad V_S = I_b (R_S + h_{ie} + 2R_E) + I_L (2 R_E) \quad \ldots(1.27\ (a))$$

While $$V_o = -I_L R_C \quad \ldots(1.28)$$

Negative sign due to the assumed direction of current. Applying KVL to the output loop

$$\frac{-(I_L - h_{fe} I_b)}{h_{oe}} - 2R_E (I_L + I_b) - I_L R_C = 0$$

$$\therefore \quad -\frac{I_L}{h_{oe}} + \frac{h_{fe}}{h_{oe}} I_b - 2R_E I_L - 2R_E I_b - I_L R_C = 0$$

$$\therefore \quad I_b \left[\frac{h_{fe}}{h_{oe}} - 2R_E\right] = I_L \left[\frac{1}{h_{oe}} + 2R_E + R_C\right]$$

$$I_b [h_{fe} - 2R_E h_{oe}] = I_L [1 + h_{oe} (2R_E + R_C)]$$

$$\therefore \quad \frac{I_L}{I_b} = \frac{[h_{fe} - 2R_E h_{oe}]}{[1 + h_{oe} (2R_E + R_C)]} \qquad \ldots (1.29)$$

Substituting value of I_b, into the equation 1.27 (a), we get

$$V_S = \frac{I_L [1 + h_{oe} (2R_E + R_C)](R_S + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + I_L (2R_E)$$

$$\therefore \quad \frac{V_S}{I_L} = \frac{[1 + h_{oe} (2R_E + R_C)](R_S + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + (2R_E)$$

Finding L.C.M. and adjusting the terms, we get

$$\therefore \frac{V_S}{I_L} = \frac{2R_E (1 + h_{fe}) + R_S (1 + 2R_E h_{oe}) + h_{ie} (1 + 2R_E h_{oe}) + h_{oe} R_C [2R_E + R_S + h_{ie}]}{[h_{fe} - 2R_E h_{oe}]}$$

$$\therefore \frac{V_S}{I_L} = \frac{2R_E (1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe}) + h_{oe} R_C [2R_E + R_S + h_{ie}]}{[h_{fe} - 2R_E h_{oe}]} \qquad \ldots (1.30)$$

Neglecting the terms of $h_{oe} R_C$ as practically $h_{oe} R_C << 1$.

$$\therefore \quad \frac{V_S}{I_L} = \frac{2R_E (1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \qquad \ldots (1.31)$$

Substituting the value of I_L, in the equation (1.28)

$$V_o = \frac{-V_S (h_{fe} - 2R_E h_{oe}) R_C}{2R_E (1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})}$$

Hence the common mode gain can be written as (absorbing negative sign),

$$A_c = \frac{V_o}{V_S} = \frac{(2R_E h_{oe} - h_{fe}) R_C}{2R_E (1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})} \qquad \ldots (1.32)$$

In practice h_{oe} is generally neglected hence the expression for A_c can be further modified as

$$A_c = \frac{-h_{fe} R_C}{R_S + h_{ie} + 2R_E (1 + h_{fe})} \qquad \ldots (1.33)$$

Therefore CMRR is

$$\text{CMRR} = \left|\frac{A_d}{A_c}\right|$$

$$\therefore \quad \text{CMRR} = \frac{R_S + h_{ie} + 2R_E (1 + h_{fe})}{(R_S + h_{ie})} \qquad \ldots (1.34)$$

18. Explain the working principle of a emitter coupled differential amplifier

Differential Mode Operation:

- Two input signals which are 180˚ out of phase with respect to each other are produced by means of connecting a AC voltage source to a **centre tap transformer**.

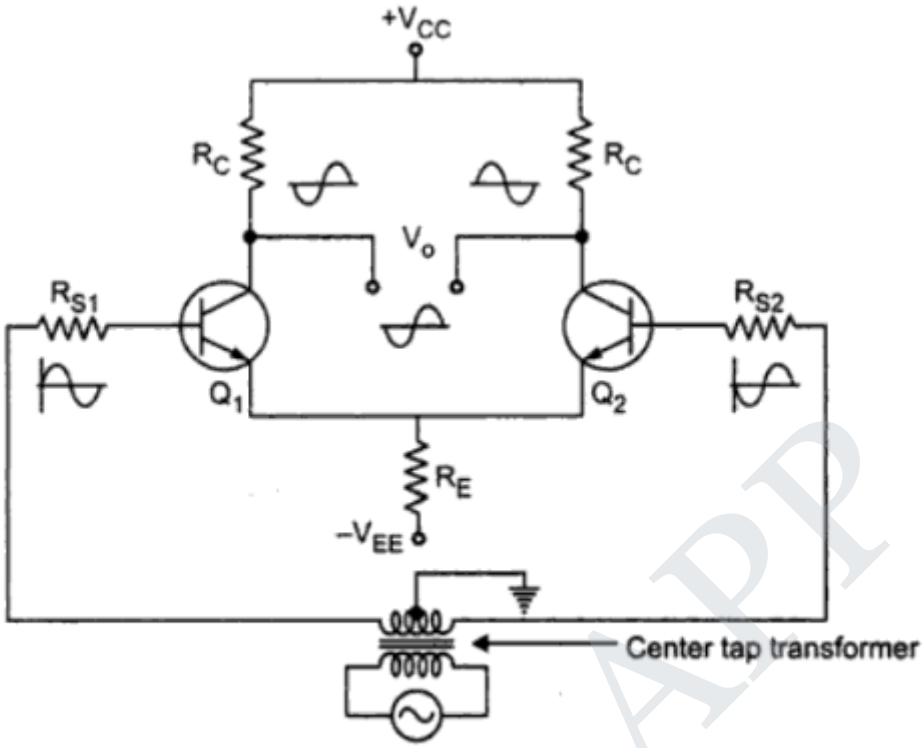


Fig. 1.8 Differential mode operation

- The signals are called **positive going signal and negative going signal.**
- Positive going signal is applied to the base of CE amplifier Q_1. Negative going signal is applied to the base of CE Q_2. [CE means Common Emitter]
- A negative going signal is developed at the collector of CE amplifier Q_1. Positive Going signal is developed at the collector of CE amplifier Q_2.
- A positive going signal due to CE amplifier Q1 and negative going signal due to CE amplifier Q_2 is developed across the emitter. Since these voltages are equal in magnitude and 180˚ out of phase , they cancel out and no AC SIGNAL CURRENT flows through R_E.
- Similarly the voltages developed at the collectors of Q_1 and Q_2 are equal in magnitude and 180˚ out of phase. The net output voltage measured between the collector terminals of Q_1 and Q_2 and is the phasor difference between the collector voltages.
- The output voltage is 2 times larger than the output voltage measured between each of the collector and ground.

Common Mode Operation:

- Two input signals of same magnitude and phase are applied to the individual base terminals of CE amplifier Q1 and Q2.
- Negative going signals are developed at the collector terminals of CE amplifiers Q1 and Q2. Since the output voltage is measured between the two collector terminals , the net output voltage = 0
- Positive going signals are developed at the emitter terminal R_E. Since they are of same magnitude and phase , they get added and cause a AC signal current to flow through R_E.

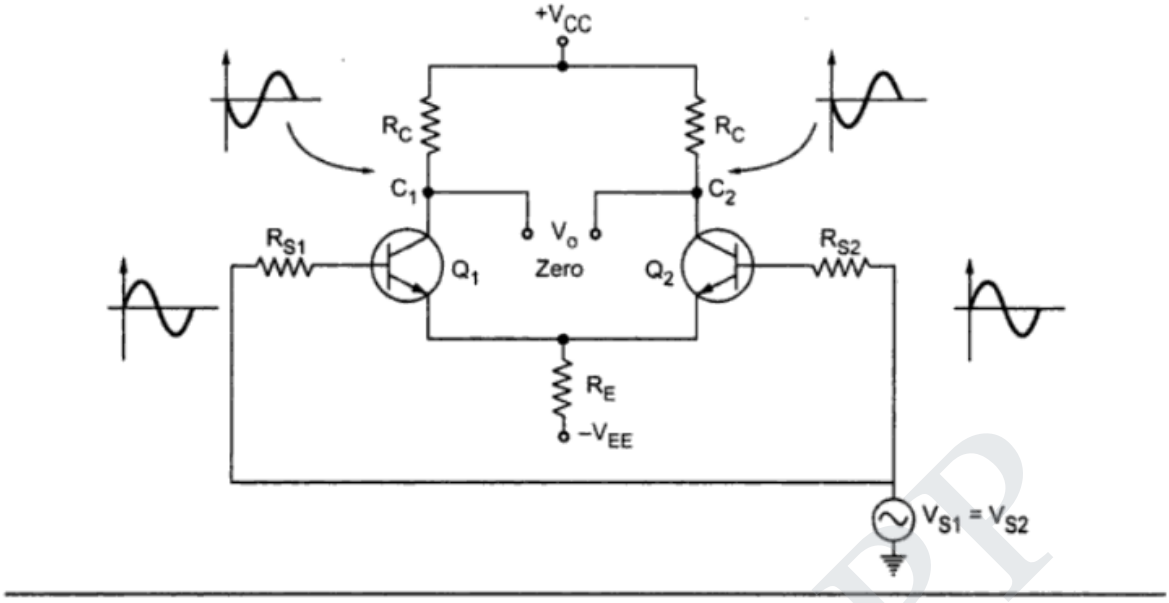


Fig. 1.9 Common mode operation

19. How common mode rejection ratio can be increased by a constant current source?

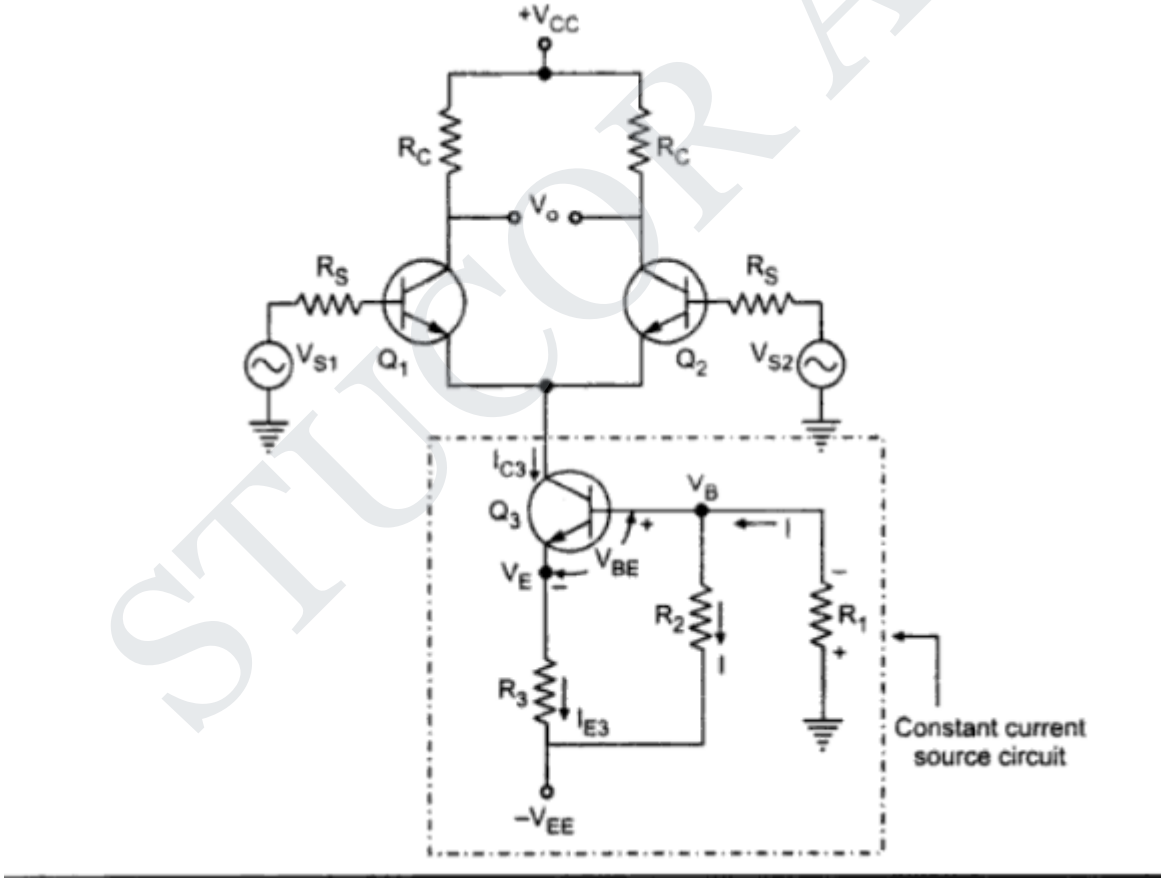


Fig. Differential Amplifier with a constant current source

To increase CMRR of a differential amplifier , the value of common mode gain A_C has to be reduced. This is possible by increasing the value of emitter resistance. For this purpose a constant current source is provided in the emitter.

The transistors Q_1 , Q_2 and Q_3 are designed to have the same operating point.

Let current through R_3 be I_{E3} while current through R_1 is I. Neglecting the base current of Q_3 which is very small due to large h_{fe}, we can assume that current through R_2 is also I.

Applying Kirchhoff's law,

$$-IR_1 - IR_2 + V_{EE} = 0$$

$$\therefore \quad I = \frac{V_{EE}}{R_1 + R_2} \qquad \ldots(1.56)$$

Now $V_B = -IR_1$

Negative sign according to the direction of current .

$$\therefore \quad V_B = -\frac{V_{EE}\, R_1}{R_1 + R_2} \qquad \ldots(1.57)$$

Now $V_E = V_B - V_{BE}$

and $$I_{E3} = \frac{V_E - (-V_{EE})}{R_3} \qquad \ldots(1.58)$$

Substituting expressions for V_B and V_E,

$$\therefore \quad I_{E3} = \frac{\frac{-V_{EE}\, R_1}{R_1 + R_2} - V_{BE} + V_{EE}}{R_3}$$

$$\therefore \quad I_{E3} = \frac{V_{EE}\left[\frac{R_2}{R_1 + R_2}\right] - V_{BE}}{R_3} \qquad \ldots(1.59)$$

Neglecting I_{B3} we can write

$$I_{C3} = I_{E3}$$

Thus as V_{EE}, R_1, R_2, R_3 and V_{BE} are constants, current I_{C3} is almost equal to I_{E3} and also constant. Thus circuit with transistor Q_3, acts as a constant current source.

20. For a non-inverting amplifier using an op-amp , assume $R_1 = 470\ \Omega$, $R_2 = 4.7\ k\Omega$. Calculate the closed loop voltage gain of the amplifier

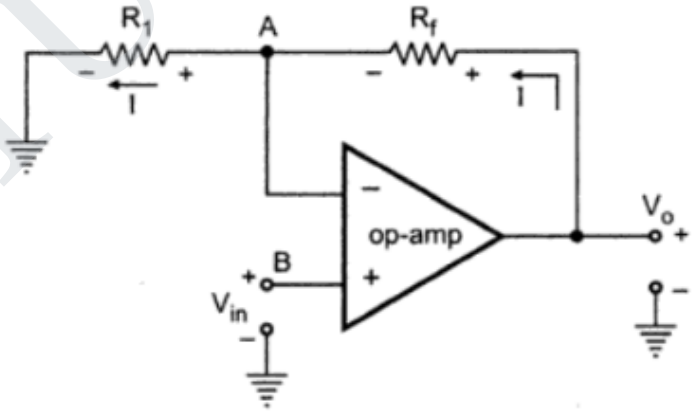


Fig. 2.49 Noninverting amplifier

Here $R_1 = 470\ \Omega$, $R_2 = R_F = 4.7\ k\Omega$.

Therefore closed loop voltage gain of non-inverting amplifier , $A_V = 1 + \frac{R_2}{R_1}$

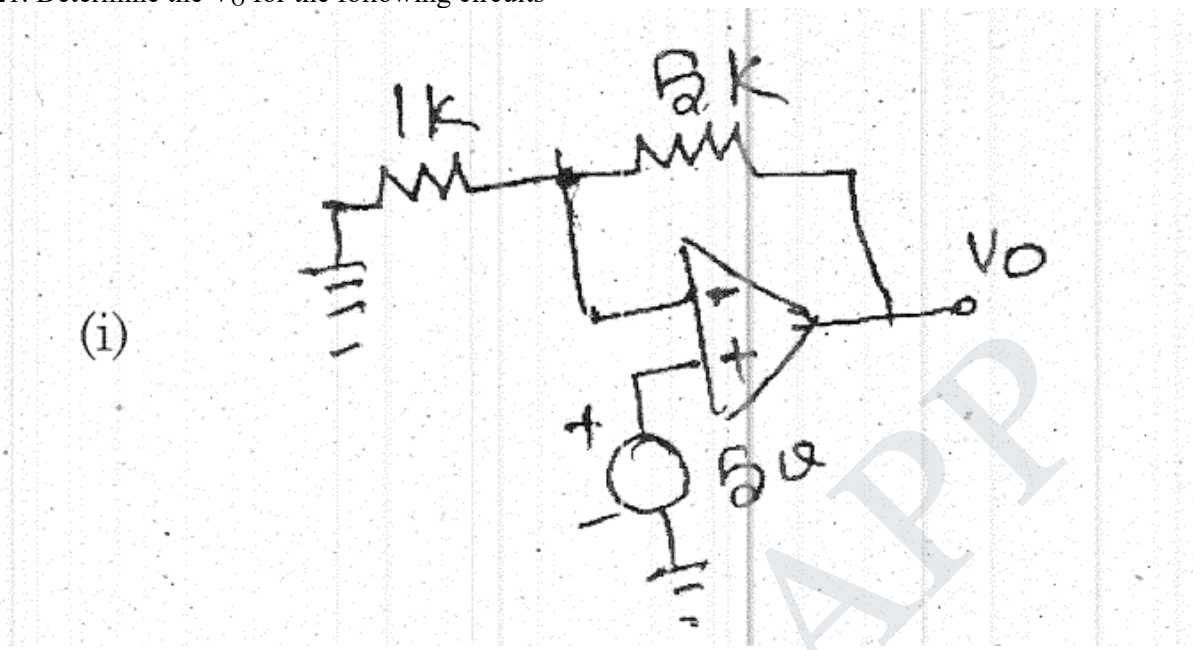
$$= 1 + \left(\frac{4.7 \times 10^3}{470}\right)$$

$= 11$

In terms of decibel , $A_V = 20 \log_{10} A_V = 20 \log_{10} 11 = 20.83$ dB

21. Determine the V_O for the following circuits

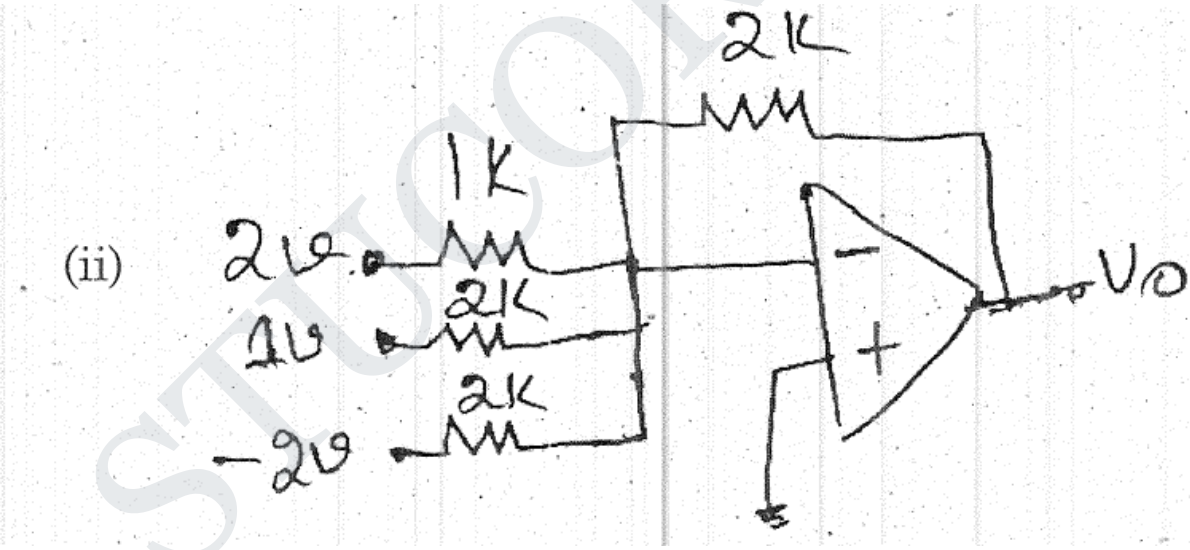
(i)



The given circuit is a non-inverting amplifier

$$V_O = (1+\frac{R_F}{R_1})\, V_I = (1+\frac{5 \times 10^3}{1 \times 10^3}) \times 5 = 30 \text{ V}$$

(ii)



The given circuit is a Inverting Summing Amplifier

$$V_O = -(\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3) = -(\frac{2 \times 10^3}{1 \times 10^3} \times 2 + \frac{2 \times 10^3}{2 \times 10^3} \times 1 + \frac{2 \times 10^3}{2 \times 10^3} \times -2)$$

$$= -(4 + 1\text{-}2) = -3 \text{ V}$$

22. Explain the application of OP-AMP as differentiator

The circuit which produces **first order time derivative of the input signal as the output is called differentiator. An OP-AMP based differentiator is also called active differentiator.**

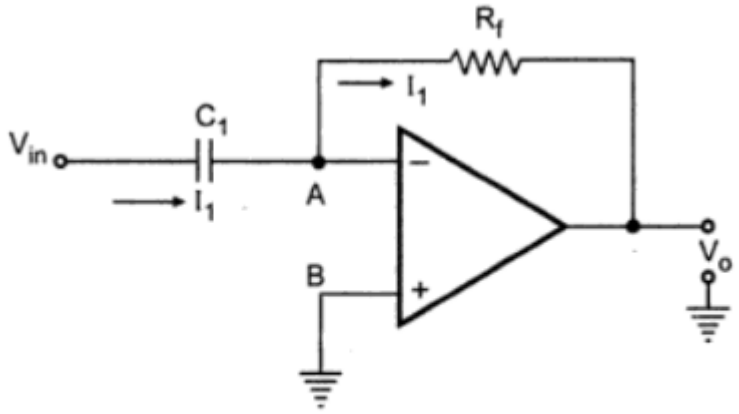


Fig. 2.103 Op-amp differentiator

The node B is grounded. The node A is also at the ground potential hence $V_A = 0$.

As input current of op-amp is zero, entire current I_1 flows through the resistance R_f.

From the input side we can write,

$$I_1 = C_1 \frac{d(V_{in} - V_A)}{dt} = C_1 \frac{dV_{in}}{dt} \quad \ldots (1)$$

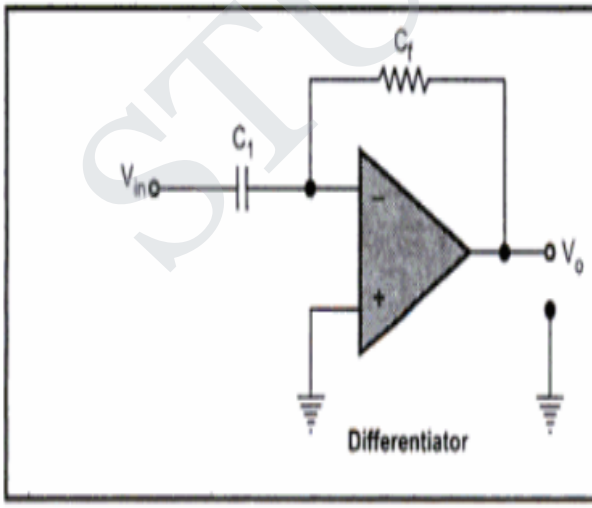
From the output side we can write,

$$I = \frac{(V_A - V_o)}{R_f} = -\frac{V_o}{R_f} \quad \ldots (2)$$

Equating the two equations,

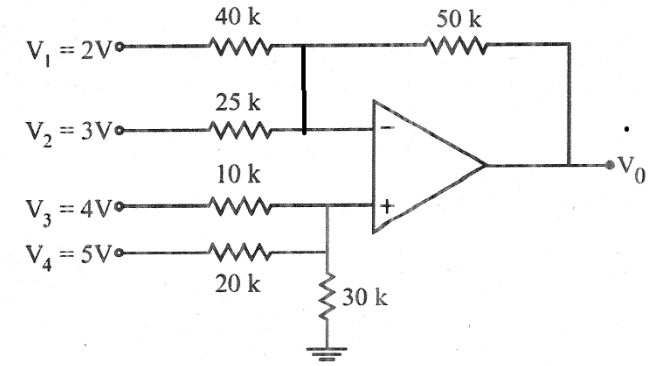
$$C_1 \frac{dV_{in}}{dt} = -\frac{V_o}{R_f} \quad \ldots (3)$$

$$\boxed{V_o = -C_1 R_f \frac{dV_{in}}{dt}} \quad \ldots (4)$$



$V_{in}(t)$	$V_0(t)$
Step	Ramp
Square wave	Train of impulses
Sine wave	Negative cosine wave

23. Find V_O for the given circuit



The given circuit is a OP-AMP based **subtractor or Difference amplifier circuit**

Case 1:

Assume V_1 and V_2 acting alone [$V_3 = V_4 = 0$ V]

The circuit works as a **inverting summing amplifier**

$$V_{O1} = -\left(\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2\right) = -\left(\frac{50 \times 10^3}{40 \times 10^3} \times 2 + \frac{50 \times 10^3}{25 \times 10^3} \times 3\right)$$

$$= -(2.5\text{ V} + 6\text{ V}) = -8.5\text{ V}$$

Case 2:

Assume V_3 acting alone [$V_1 = V_3 = V_4 = 0$ V]

The circuit works as a **non-inverting amplifier**

$$V_{O2} = \left(1+\frac{R_F}{R_1}\right)V_B = \left(1+\frac{R_F}{R_1}\right)\left(V_3 \times \frac{R_3}{R_2 + R_3}\right)$$

$$= \left(1+\frac{50 \times 10^3}{15.38 \times 10^3}\right)\left(4 \times \frac{12 \times 10^3}{(10+12) \times 10^3}\right) = 9.27\text{ V}$$

$R_3 = 20\ k\Omega \parallel 30\ k\Omega = 12\ k\Omega$

$R_1 = 40\ k\Omega \parallel 25\ k\Omega = 15.38\ k\Omega$

Case 3:

Assume V_4 acting alone[$V_1 = V_3 = V_3 = 0$ V]

The circuit acts as a **non-inverting amplifier**

$$V_{O3} = \left(1+\frac{R_F}{R_1}\right)V_B = \left(1+\frac{R_F}{R_1}\right)\left(V_4 \times \frac{R_3}{R_2 + R_3}\right)$$

$$= \left(1+\frac{50 \times 10^3}{15.38 \times 10^3}\right)\left(5 \times \frac{7.5 \times 10^3}{(20+7.5) \times 10^3}\right) = 5.79\text{ V}$$

$R_3 = 10\ k\Omega \parallel 30\ k\Omega = 7.5\ k\Omega$

$R_1 = 40\ k\Omega \parallel 25\ k\Omega = 15.38\ k\Omega$

Therefore total output voltage of the circuit $V_O = V_{O1} + V_{O2} + V_{O3} = -8.5 + 9.27 + 5.79$

$= 6.57$ V

UNIT III APPLICATIONS OF OPAMP **9**

Instrumentation amplifier and its applications for transducer Bridge, Log and Antilog Amplifiers- Analog multiplier & Divider, first and second order active filters, comparators, multivibrators, waveform generators, clippers, clampers, peak detector, S/H circuit, D/A converter (R- 2R ladder and weighted resistor types), A/D converters using opamps.

Part-A

1. Draw the fundamental sample and hold circuit ? What is the purpose of S/H in data convertors?

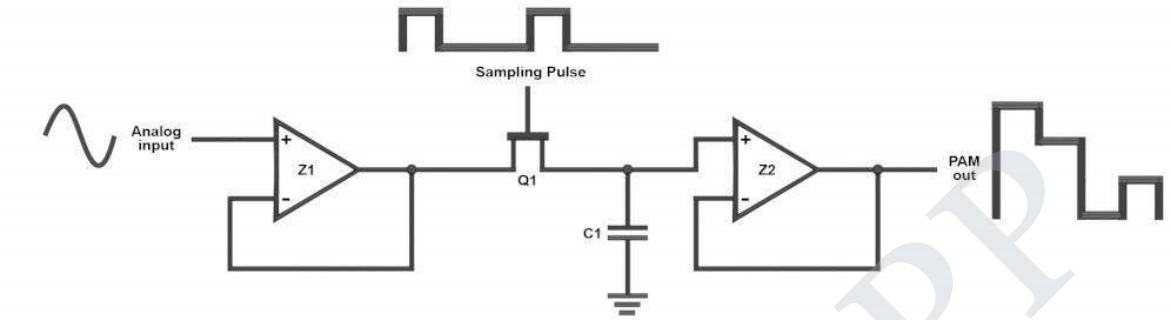


Fig.a. Sample and Hold Circuit

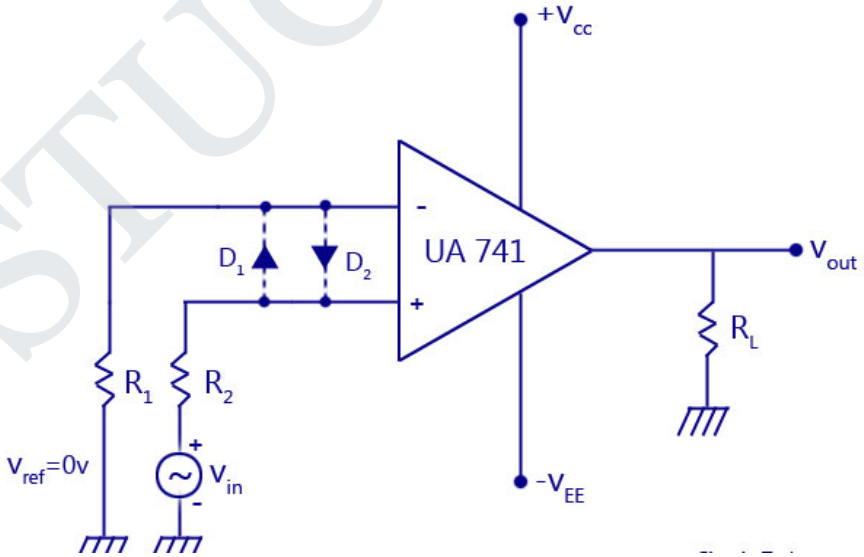
The purpose of sample and hold circuit is to create samples of voltage given to it as input and hold these sample for certain length of time for subsequent processing.

2. How many comparators are required to design a 10-bit flash ADC?

Number of comparators required for n-bit ADC = 2^n-1 ; Therefore for 10-bit ADC , the number of comparators required is 2^{10} -1 = 1024 – 1 = 1023.

3. What is a zero crossing detector?

Zero Crossing Detector or Sine to Square Wave Converter is a voltage comparator circuit that changes the output between $+V_{SAT}$ and $-V_{SAT}$, whenever the input voltage crosses its zero point.



4. Calculate the number of comparators required for realizing an 8-bit flash A/D converter?

Number of comparators required for a N-bit flash or parallel ADC is 2^N-1.

Given N = 8. Therefore number of comparators required is 2^8 – 1 = 255

5. Draw the circuit of a log amplifier using two op-amps

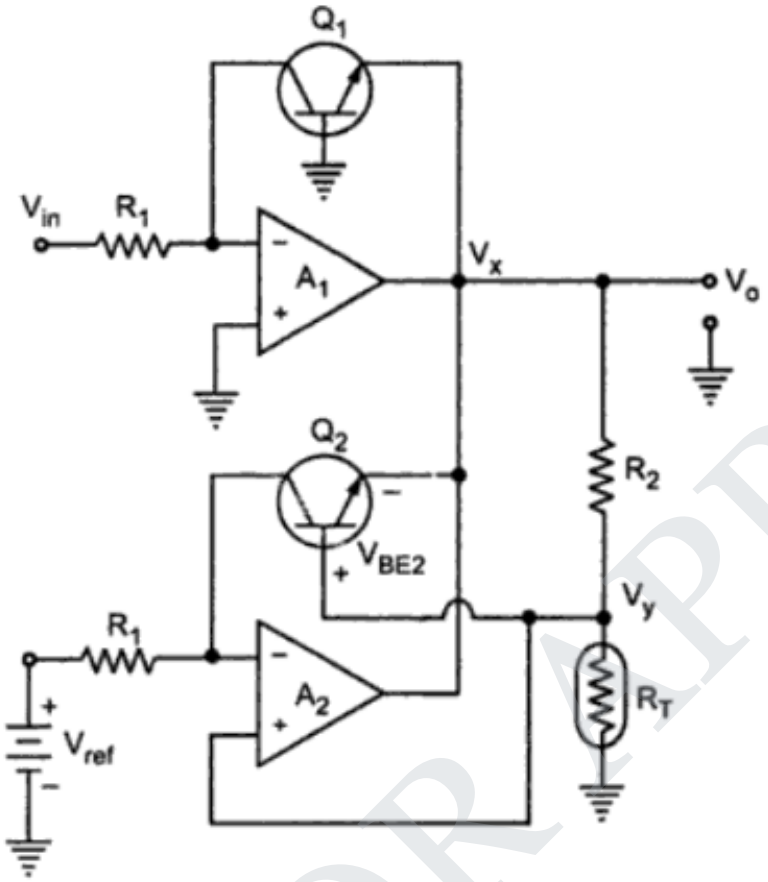


Fig. Temperature Compensated Log Amplifier

7. Calculate the value of LSB, MSB and full-scale output for an 8-bit DAC for the 0V to 12 V. (**Example 10.2 Pg. 357 D.Roy Choudhury)**
Solution :

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

$$\text{For a 12 V range , LSB} = 12 \times \frac{1}{2^8} = 12 \times \frac{1}{256} = 46.87 \text{ mV}$$

$$\text{MSB} = 0.5 \times \text{Full Scale Voltage Value} = 0.5 \times 12 = 6 \text{ V}$$

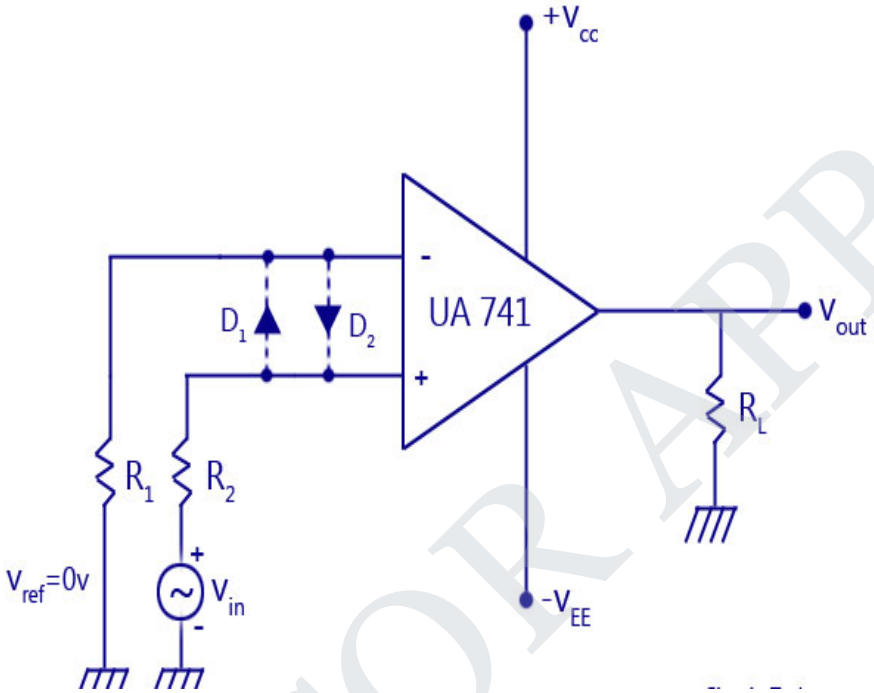
$$\text{Full Scale Output Voltage} = (\text{Full Scale Voltage} - 1 \text{ LSB})$$
$$= 12 \text{ V} - 0.04687 = 11.95 \text{ V}$$

8. What is sample and hold circuit ? Where it is used?
A **sample and hold circuit** samples an input signal and holds on to its last sampled value until the input is sampled again. **This type of circuit is used in DIGITAL INTERFACING , ADC and Pulse Code Modulation(PCM) systems.**

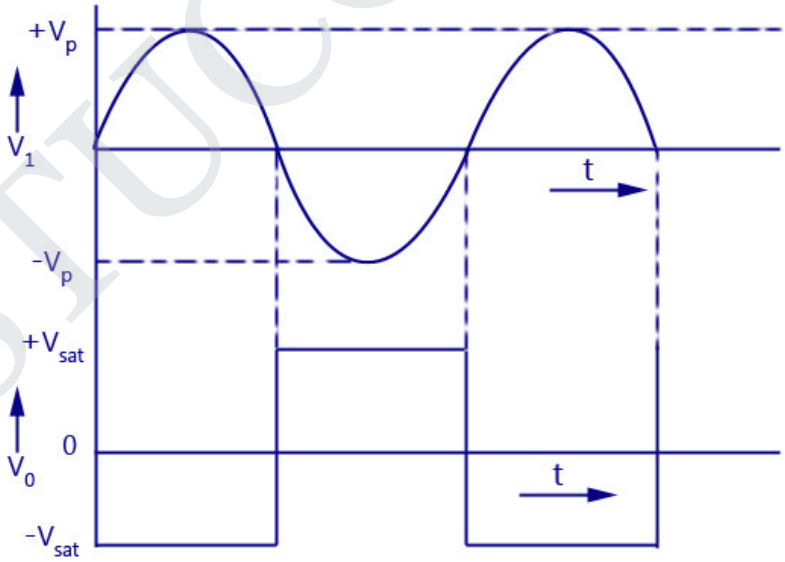
9. What is the advantage of using active clipper over passive clipper?
In **passive clipper ,** the diode cannot work as an ideal diode due to **voltage drop across it**. But in **active clipper** , the voltage drop across the diode gets divided by the open-loop gain of the op-amp **which is very high**. Hence **diode turns on instantaneously and behaves as an ideal diode. This causes a precise clipping action**.
10. Write the difference between active clipper and passive clipper circuit.

S.No	Active Clipper	Passive Clipper
1.	Consist of OP-AMP in series with diode	Consist of resistor in series with diode
2.	Diode behaves as lossless diode	Diode behaves as a lossy diode
3.	More efficient	Less efficient

11. Draw the circuit diagram of zero-cross detector with input and output waveforms



Waveforms:



12. Which is the fastest ADC ? State reason.

Flash type ADC is the fastest ADC because the conversion is performed simultaneously by a set of comparators. Typical conversion time is ≤ 100 ns.

13. Write any two applications of clipper and clamper

Clipper Applications:

- Separating Synchronising signal from composite video signal
- Excessive noise spikes above a certain level can be clipped in FM transmitter

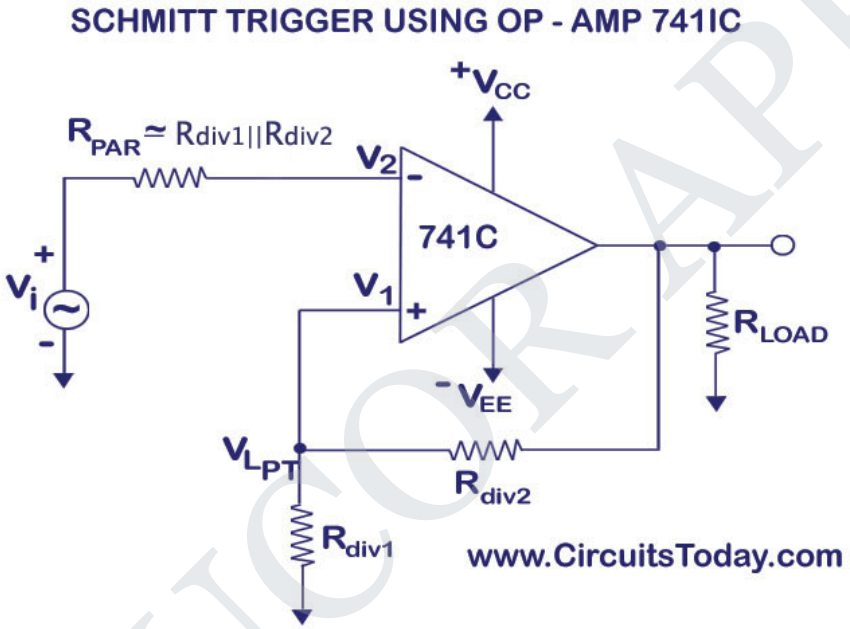
- Protection of transistors from transients.

Clamper Applications:

- In test equipment , sonar and radar systems
- Removing distortions
- Protection of amplifiers
- As Voltage Multiplier

14. Enlist the applications of comparators
    - Threshold Detector
    - Zero Crossing Detector
    - Schmitt trigger
    - Relaxation Oscillator

15. How does Schmitt trigger acts as a regenerative comparator?



A **Schmitt Trigger is also called REGENERATIVE COMPARATOR , SQUARING CIRCUIT etc.**

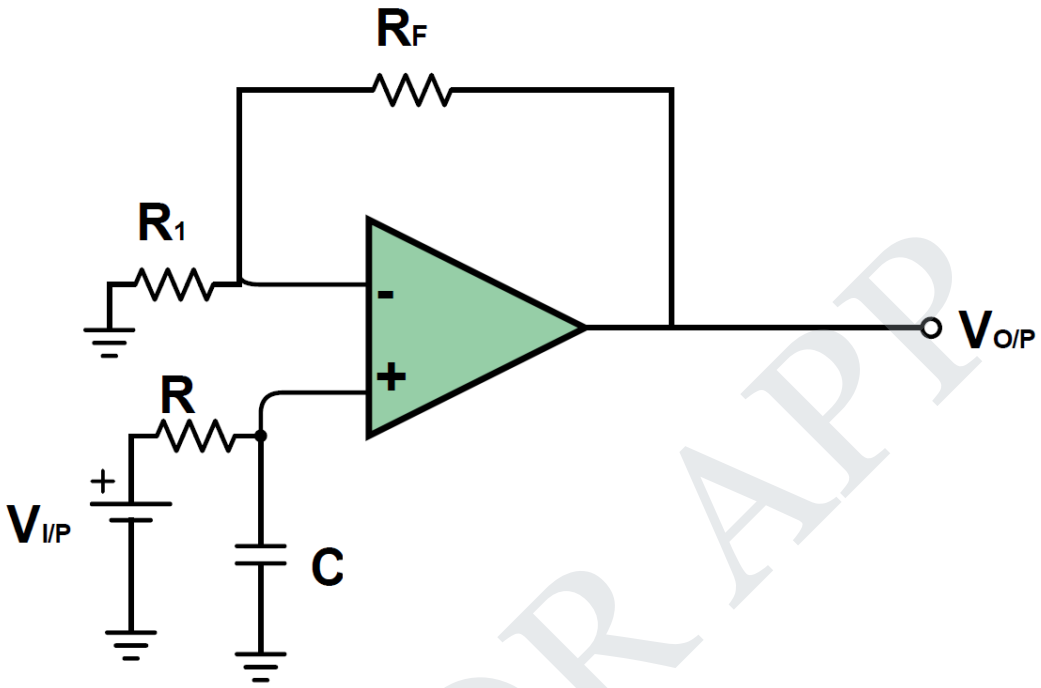
Assume a small positive voltage is applied to the inverting terminal. As a result a negative output voltage is developed. This voltage applied to the **non-inverting terminal as feedback**. Now the value of **negative voltage applied to the non-inverting terminal keeps on increasing till the circuit is driven into negative saturation ($-V_{SAT}$).** Assume a small negative voltage is applied to the inverting terminal. As a result a positive output voltage is developed. This voltage applied to the **non-inverting terminal as feedback**. Now the value of **positive voltage applied to the non-inverting terminal keeps on increasing till the circuit is driven into negative saturation ($+V_{SAT}$). This is why Schmitt trigger circuit is called REGENERATIVE COMPARATOR**.

16. Mention the drawback of binary weighted resistor DAC
    - When the number of bits increase , it is difficult to maintain the resistance ratio.
    - Very different range of resistor values are required.
    - Different current flows through different resistors. So their wattage ratings also different
    - Accuracy and stability of conversion depends on the absolute accuracy of resistors.

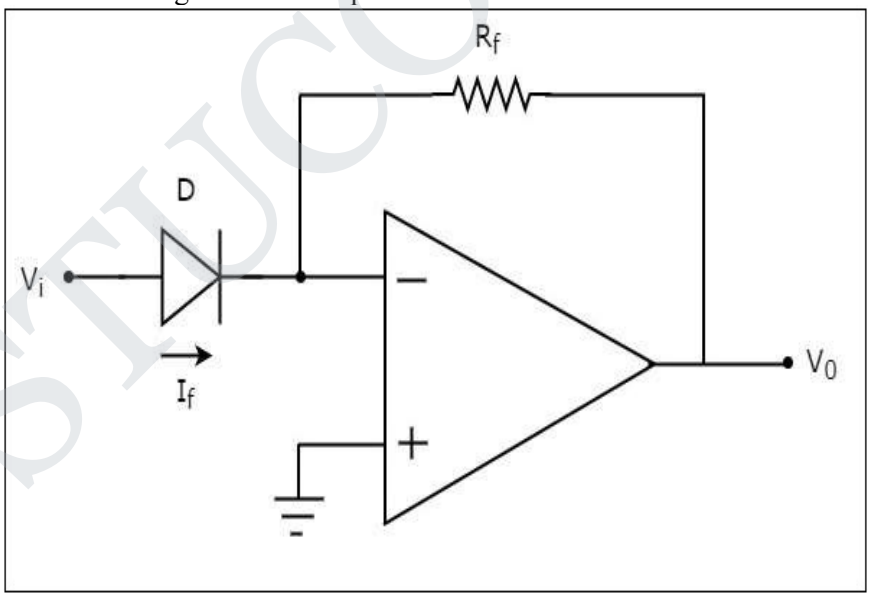
17. List the four requirements of an Instrumentation amplifier
    - High Gain Accuracy
    - High CMRR

- High Gain Stability with low temperature coefficient
- Low DC Offset
- Low Output Impedance

18. Give the circuit using Op-amp for a first order low pass filter with variable gain



19. Draw the circuit of antilog OP-AMP amplifier



Part-B

1 . A dual-slope ADC uses 16-bit counter and 4 MHz clock rate. The maximum input voltage is +10 V. The maximum integrator output voltage should be -8V when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1µF. Find the value of the resistor R of the integrator.

Solution:

V_{OI} = Maximum Integrator Output Voltage = - 8 V

$$C_1 = 0.1\ \mu F$$

$$t = \frac{2^N \times 1}{4 \times 10^6} = 16.384 \times 10^{-3}$$

Output voltage of the integrator , $V_{OI} = \frac{-V_I \times t}{R_1 C_1}$

$$R_1 = \frac{-V_I \times t}{V_{OI} C_1}$$

$$= \frac{-10 \times 16.384 \times 10^{-3}}{-8 \times 0.1 \times 10^{-6}} = 204.8\ k\Omega$$

2. Derive the expression for the log and antilog amplifiers with necessary diagrams (10)

Log Amplifier

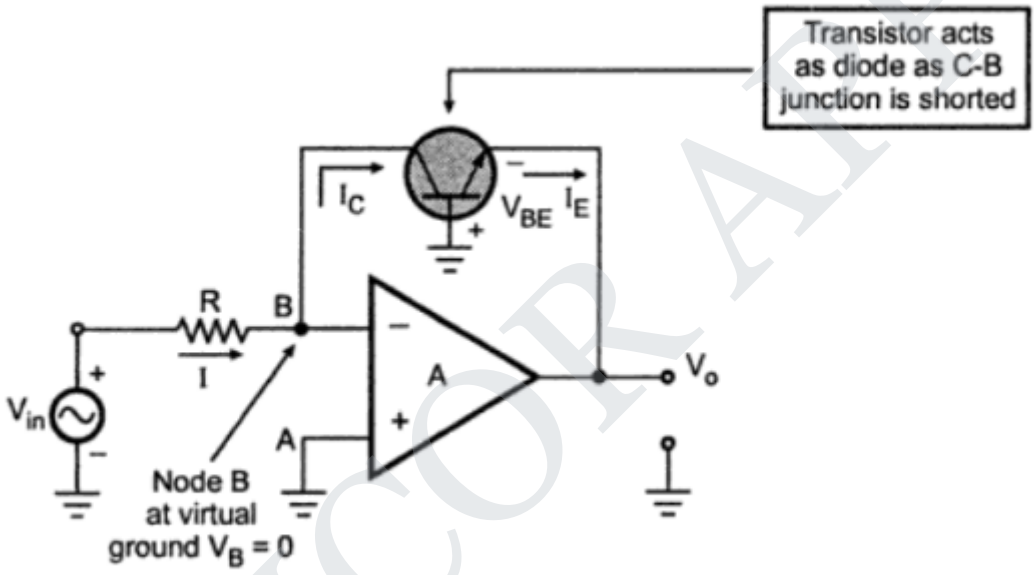


Fig. 4.83 Basic log amplifier

Derivation:

The node B is at virtual ground . Hence $V_B = 0$.

$$\text{Therefore } I = \frac{V_{IN} - V_B}{R} = \frac{V_{IN}}{R}$$

As the op-amp input current is zero

$I = I_C$ = Collector Current

The voltage $V_{CB} = 0$ as the collector is at virtual ground and base is grounded. Hence we can write the equation of I_C as

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \quad \text{.....(A)}$$

Applying KVL to the output side

$$V_O + V_{BE} = 0$$

$$\text{Therefore } V_{BE} = -V_O$$

$$\text{And } I_C = I = \frac{V_{IN}}{R}$$

Substituting value of I_C and V_{BE} in equation(A)

$$-V_O = V_T \ln \frac{V_{IN}}{R \times I_S}$$

$$\text{Let } V_{REF} = R \times I_S$$

Therefore

$$-V_O = V_T \ln \frac{V_{IN}}{V_{REF}}$$

$$V_O = -V_T \ln \frac{V_{IN}}{V_{REF}}$$

A log amplifier circuit produces an output voltage V_O which is natural logarithm of input voltage.

Antilog Amplifier:

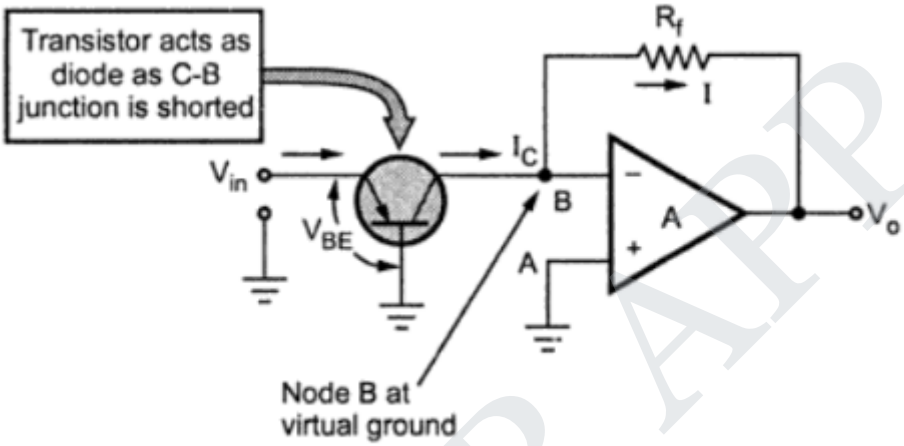


Fig. 4.89 Basic antilog amplifier

Derivation:

The node B is at virtual ground . Hence $V_B = 0$. Thus both collector and base of the transistor are at ground potential and $V_{CB} = 0$. Hence the voltage across the transistor is V_{BE} and the collector current I_C is given by

$$I_C = I_S e^{\frac{V_{IN}}{V_T}}$$

$I_C = I$ (As OP-AMP input current is zero)

$$\text{Therefore } I_C = I = \frac{V_B - V_O}{R_F} = \frac{-V_o}{R_F}$$

$$\text{Therefore } \frac{-V_o}{R_F} = I_S e^{\frac{V_{IN}}{V_T}}$$

$$V_O = -R_F I_S e^{\frac{V_{IN}}{V_T}}$$

$$\text{Let } V_{REF} = R \times I_S$$

$$\text{Therefore } V_O = -V_{REF} e^{\frac{V_{IN}}{V_T}}$$

An anti-log amplifier produces an output voltage that is exponential (anti-log) of input voltage.

(Or)

3. In a triangular wave generator given $R_2 = 1.2$ kΩ , $R_3 = 6.8$ kΩ , $R_1 = 120$ kΩ , $C_1 = 0.01$ μF . Determine the peak to peak output amplitude of triangular wave and frequency of the triangular wave. **(Pg. No. 221 , Pg. No. 22 Roy Choudhury)**

Solution:

$$\text{Peak to Peak amplitude of triangular Wave} = 2\frac{R_2}{R_3} V_{SAT}$$

$$= 2\frac{1.2 \times 10^3}{6.8 \times 10^3} \times V_{SAT}$$

$$= 1.412\ V_{SAT}$$

Frequency of the triangular wave

$$f = \frac{1}{T} = \frac{R_3}{4 \times R_1 \times C_1 \times R_2} = \frac{6.8 \times 10^3}{4 \times 120 \times 10^3 \times 0.01 \times 10^{-6} \times 1.2 \times 10^3} = 1.18\ \text{kHz}$$

4. Design a RC phase shift oscillator for a frequency of 1 kHz

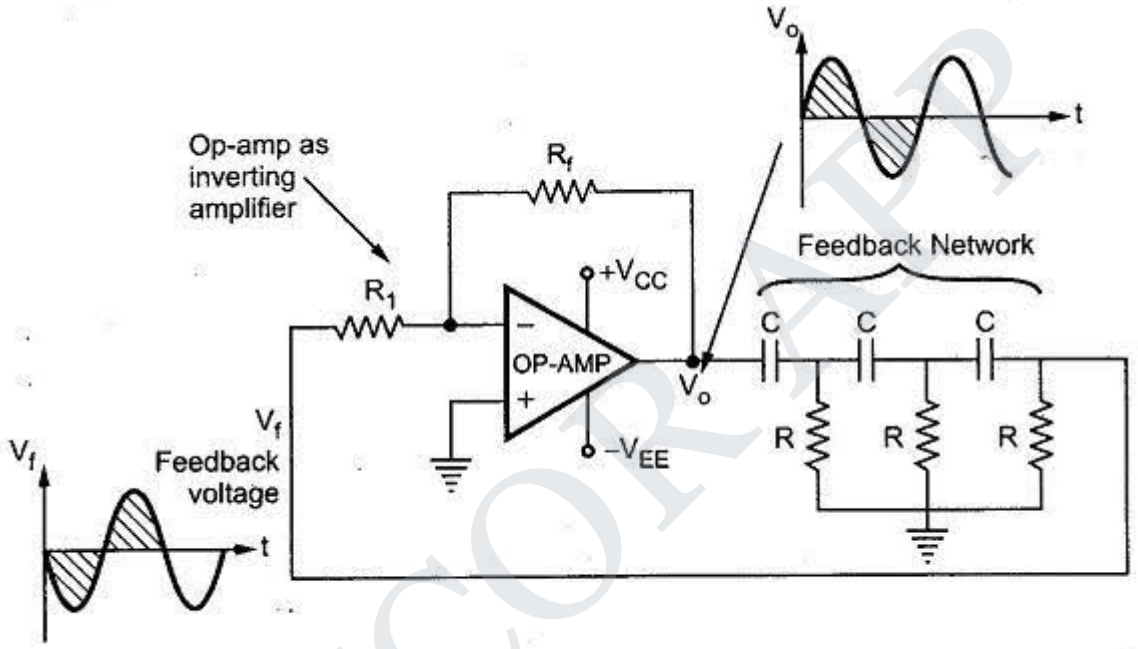


Fig. 2.92 R-C Phase shift oscillator using op-amp

Solution:

Let C = 0.1 µF

$$R = \frac{1}{2\pi f C \sqrt{6}}$$

$$= \frac{1}{2\pi \times 1 \times 10^3 \times 0.1 \times 10^{-6} \times \sqrt{6}} = 1.59\ \text{k}\Omega$$

To prevent loading of the amplifier network , $R_1 \leq 10\ R$

Therefore let $R_1 = 10\ R = 15.9\ \text{k}\Omega$

Since $R_F = 29\ R_1$

$R_F = 29 \times 15.9\ \text{k}\Omega = 461\ \text{k}\Omega$

5. Discuss the second order high pass filter with its frequency response and design the circuit with a cut-off frequency of 5 kHz (8)

Second Order High Pass Butterworth Filter:

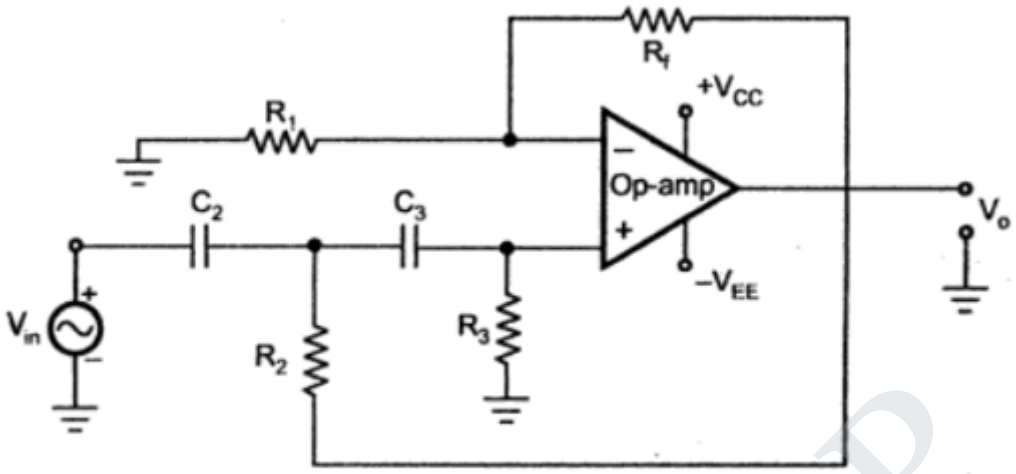


Fig. 5.22 Second order high pass Butterworth filter

- The second order high pass butterworth filter has gain roll-off[lower down] at the rate of +40 dB per decade in the stop band.
- The second order high pass butterworth filter can also be realized by interchanging the positions of resistors and capacitors in a second order low pass filter.

Expression for cut-off frequency:

The input RC network in Laplace domain

$$I_1 = I_2 + I_3 \quad \ldots\ldots(A)$$

$$\frac{V_{in} - V_1}{R_2} = \frac{V_1 - V_o}{\left(\frac{1}{sC_2}\right)} + \frac{V_1 - V_A}{R_3} \quad \ldots\ldots(B)$$

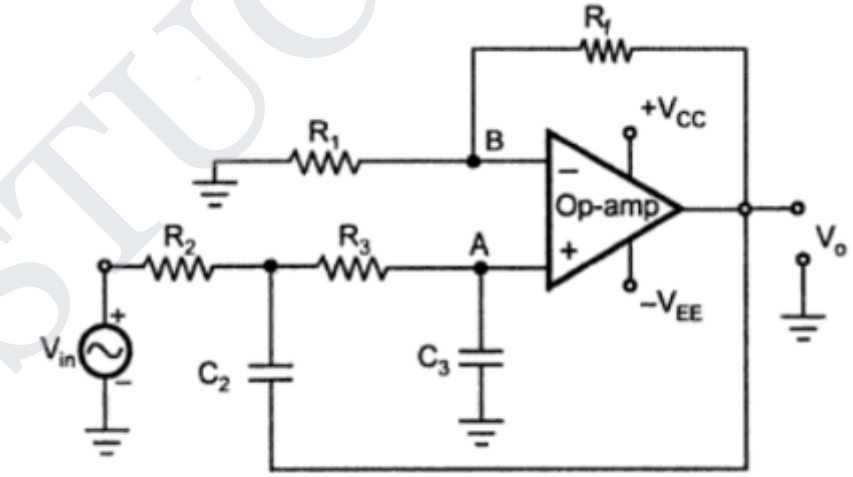


Fig. 9.20 Second order low pass Butterworth filter

Using potential divider rule we can write

$$V_A = V_1 \left[\frac{\frac{1}{sC_3}}{R_3 + \frac{1}{sC_3}} \right] \quad \ldots (3)$$

$$V_A = \frac{V_1}{1 + sR_3 C_3} \quad \ldots (4)$$

$$V_1 = V_A (1 + s R_3 C_3)$$

$$\frac{V_{in} - V_A (1+sR_3 C_3)}{R_2} = \frac{V_A (1+s R_3 C_3) - V_o}{\left(\frac{1}{sC_2}\right)} + \frac{V_A (1+s R_3 C_3) - V_A}{R_3}$$

$$\frac{V_{in}}{R_2} + V_o (s C_2) = V_A \left[\frac{(1+s R_3 C_3)}{R_2} + s C_2 (1+s R_3 C_3) + \frac{(1+s R_3 C_3)}{R_3} - \frac{1}{R_3} \right]$$

$$\therefore \frac{V_{in}}{R_2} + V_o (s C_2) = V_A \left[\frac{R_3 (1+s R_3 C_3) + R_2 R_3 s C_2 (1+s R_3 C_3) + R_2 (1+s R_3 C_3) - R_2}{R_2 R_3} \right]$$

$$\therefore (R_3 V_{in} + V_o s R_2 R_3 C_2) = V_A [(1 + s R_3 C_3) (R_3 + R_2 R_3 s C_2 + R_2) - R_2]$$

$$V_A = \frac{R_3 V_{in} + V_o s R_2 R_3 C_2}{[(1+s R_3 C_3)(R_3 + R_2 R_3 C_2 s + R_2) - R_2]} \quad \ldots (5)$$

For non-inverting op-amp

$$V_o = A_F V_A$$

where $A_F = 1 + \frac{R_f}{R_1}$

and V_A = the voltage at the noninverting terminal

$$\therefore V_o = A_F \left[\frac{R_3 V_{in} + V_o s R_2 R_3 C_2}{(1+s R_3 C_3)(R_3 + R_2 R_3 C_2 s + R_2) - R_2} \right]$$

$$\therefore \frac{A_F R_3 V_{in}}{(1+s R_3 C_3)(R_3 + R_2 R_3 C_2 s + R_2) - R_2} = V_o \left[1 - \frac{s R_2 R_3 C_2}{(1+s R_3 C_3)(R_3 + R_3 R_2 C_2 s + R_2) - R_2} \right]$$

$$\therefore A_F R_3 V_{in} = V_o [(1 + s R_3 C_3) (R_3 + R_3 R_2 C_2 s + R_2) - R_2 - s R_2 R_3 C_2]$$

$$\therefore \frac{V_o}{V_{in}} = \frac{A_F}{s^2 + \frac{(R_3 C_3 + R_2 C_3 + R_2 C_2 - A_F R_2 C_2) s}{R_2 R_3 C_2 C_3} + \frac{1}{R_2 R_3 C_2 C_3}} \quad \ldots (7)$$

As the highest degree of the polynomial in the denominator is 2 , the given filter is a **second order filter**

The standard form of transfer function of second order system

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad \text{.....(8)}$$

A = overall gain

ξ – Damping ratio

ω_N – natural frequency or resonant frequency of oscillations

$$\omega_n^2 = \frac{1}{R_2 R_3 C_2 C_3} \quad \text{....(9)}$$

$$\therefore \quad \omega_H^2 = \frac{1}{R_2 R_3 C_2 C_3} \quad \text{.....(10)}$$

$$\therefore \quad (2\pi f_H)^2 = \frac{1}{R_2 R_3 C_2 C_3}$$

$$\therefore \quad f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

Since the positions of R and C in this high pass filter are the interchanged ones than those existing in low pass filter , f_H becomes f_L.

f_L is the **lower cut-off frequency**

Replacing s by jω, the transfer function can be written in the frequency domain and hence, finally, can be expressed in the polar form as

$$\frac{V_o}{V_{in}} = \left|\frac{V_o}{V_{in}}\right| \angle \phi$$

Where $\left|\frac{V_O}{V_{IN}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$

A_F = Passband gain = 1.586 to ensure second order butterworth response

$R_F = 0.586\ R_1$

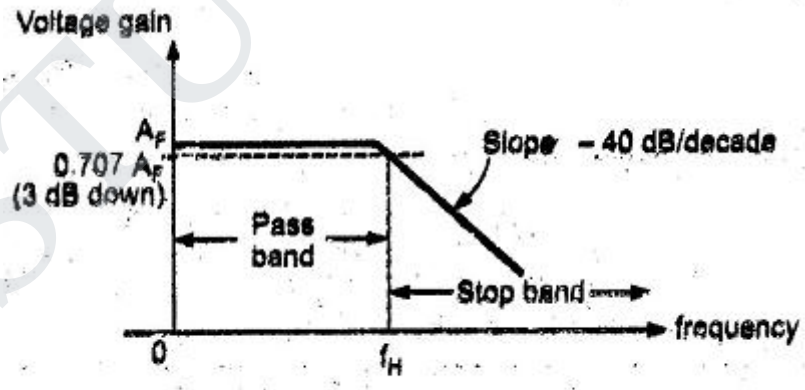


Fig. 2.78 Frequency response

Design a second order highpass butterworth filter with a cut-off frequency 5 kHz:

Solution : i) A second order Butterworth active high pas filter for a cut-off frequency of 5 kHz : The cut-cíf frequency is $f_o = 5$ kHz

$$\text{Choose } R = 10\,k\Omega$$

$$\therefore \quad f_0 = \frac{1}{2\pi RC}$$

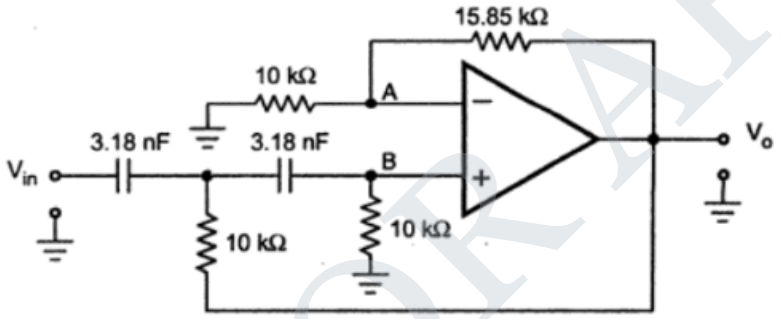
$$\text{i.e.} \quad C = \frac{1}{2\pi \times 10 \times 10^3 \times 5 \times 10^3} = 3.18\ nF$$

For second order Butterworth filter,

$$\frac{R_f}{R_1} = 1.585$$

Choose R = 10 kΩ hence R_f = 15.85 kΩ

The designed circuit is shown in the Fig. 5.49.



6. With a neat circuit diagram , explain the working of Schmitt trigger using op-amp

A Schmitt trigger is also called REGENERATIVE COMPARATOR or SINE-TO-SQUARE WAVE CONVERTER.

Inverting Schmitt trigger

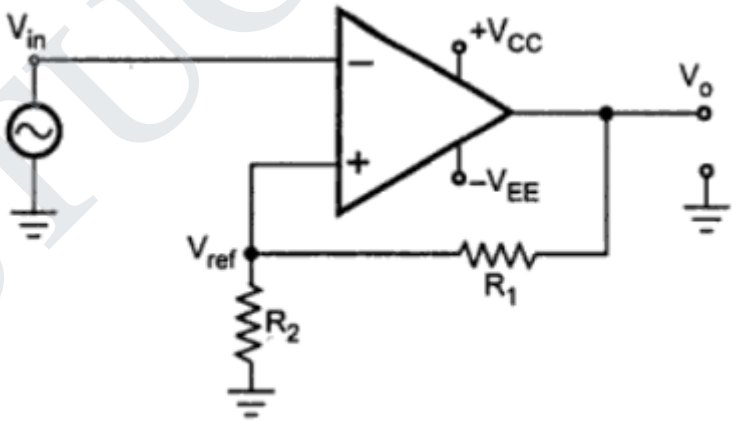


Fig. 5.33 Inverting Schmitt trigger

- Input voltage signal is applied to the inverting input terminal. The inverting mode produces an output voltage that is 180˚ out of phase with input voltage. This voltage is applied to the **non-inverting terminal**
- When $V_{IN} > V_{UT}$, the output gets saturated at $-V_{SAT}$
- When $V_{IN} < V_{LT}$, the output gets saturated at $+ V_{SAT}$.
- The voltage at which output changes from $+V_{SAT}$ to $-V_{SAT}$ is controlled by the potential dividers R_1 and R_2.

$$+V_{ref} = \frac{V_o}{R_1+R_2} \times R_2 = \frac{+V_{sat}}{R_1+R_2} \times R_2 \quad \text{.... positive saturation}$$

$$-V_{ref} = \frac{V_o}{R_1+R_2} \times R_2 = \frac{-V_{sat}}{R_1+R_2} \times R_2 \quad \text{.... negative saturation}$$

$+V_{REF}$ is also called **UPPER THRESHOLD VOLTAGE(V_{UT})**. $-V_{REF}$ is also called **LOWER THRESHOLD VOLTAGE(V_{LT})**.

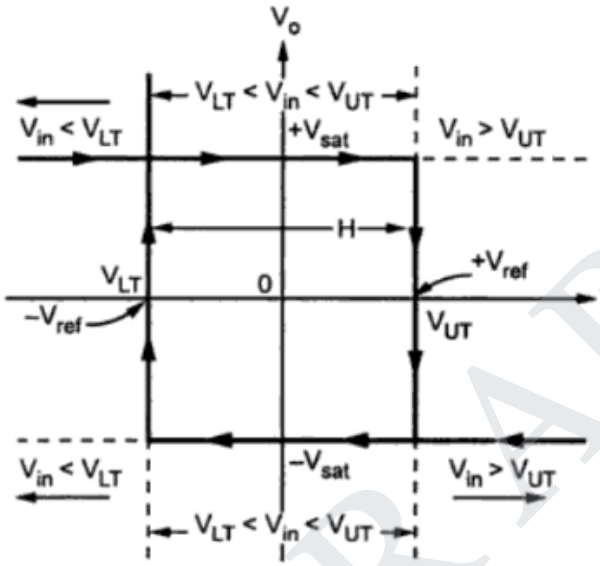


Fig. Hysterisis Curve of Inverting Schmitt Trigger

- The hysteresis curve indicates that once the output changes its state from $+V_{SAT}$ to $-V_{SAT}$ or vice-versa , it remains there indefinitely till the input voltage exceeds the threshold voltage levels. This is called **hysteresis or dead band or dead zone of Inverting Schmitt Trigger.**
- The difference between V_{UT} and V_{LT} is called **width of hysteresis**

$$H = V_{UT} - V_{LT} = \frac{+V_{sat}\ R_2}{R_1+R_2} - \left[\frac{-V_{sat}\ R_2}{R_1+R_2}\right]$$

$$\boxed{H = \frac{2\ V_{sat}\ R_2}{R_1+R_2}}$$

Schmitt trigger converts sine wave into a square wave

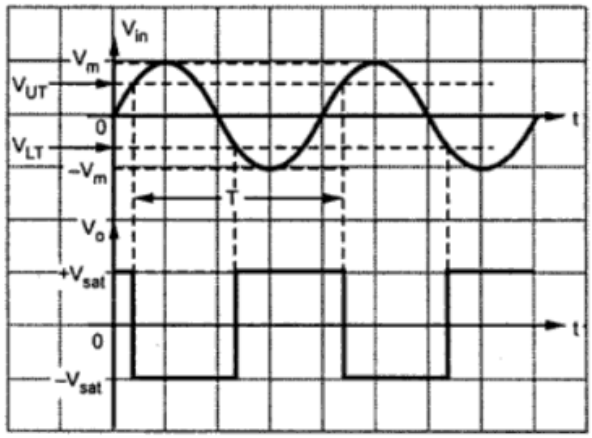


Fig. 5.35 Input and output waveforms of inverting Schmitt trigger

Non-Inverting Schmitt Trigger:

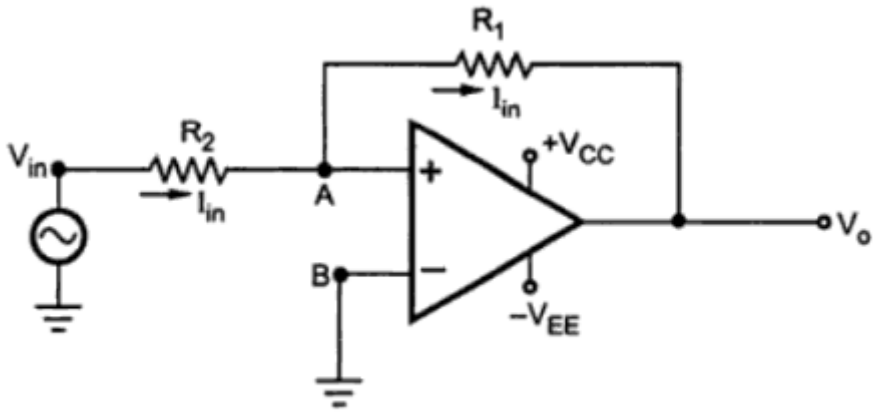


Fig. 5.37 Noninverting schmitt trigger

- Assume the output is at $+V_{SAT}$. This is applied as feedback through R_1 to **non-inverting terminal**.
- Now though V_{IN} is decreased , the output remains in its positive saturation level till the input becomes more negative than V_{LT}. Once the input exceeds V_{LT} , the output changes its state from $+V_{SAT}$ to $-V_{SAT}$. The circuit remains in $-V_{SAT}$, till the input becomes more positive than V_{UT}.

Now V_A = voltage at point A $= I_{in} R_2$

$= V_{UT}$

As op-amp input current is zero, I_{in} entirely passes through R_1.

$$\therefore \quad I_{in} = \frac{V_o}{R_1} = \frac{+V_{sat}}{R_1}$$

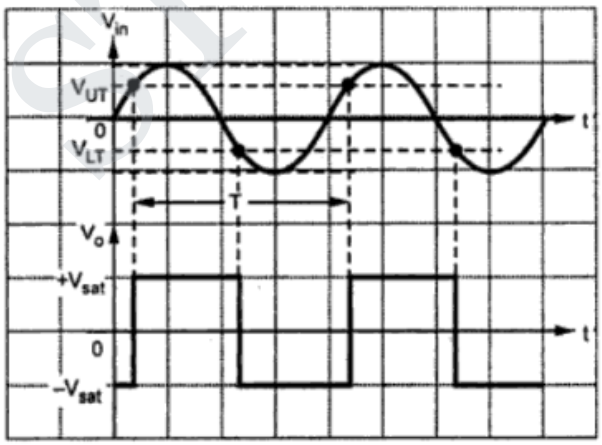
$$\therefore \quad \boxed{V_{UT} = I_{in} R_2 = \frac{R_2}{R_1}(+V_{sat}) = V_{sat}\frac{R_2}{R_1}}$$

and

$$\boxed{V_{LT} = \frac{R_2}{R_1}(-V_{sat}) = -V_{sat}\frac{R_2}{R_1}}$$

and

$$\boxed{H = V_{UT} - V_{LT} = 2\,V_{sat}\frac{R_2}{R_1}}$$



$V_{in} > V_{UT}$
V_o changes from
$-V_{sat}$ to $+V_{sat}$

$V_{in} < V_{LT}$
V_o changes from
$+V_{sat}$ to $-V_{sat}$

Fig. 5.39 Input and output waveforms

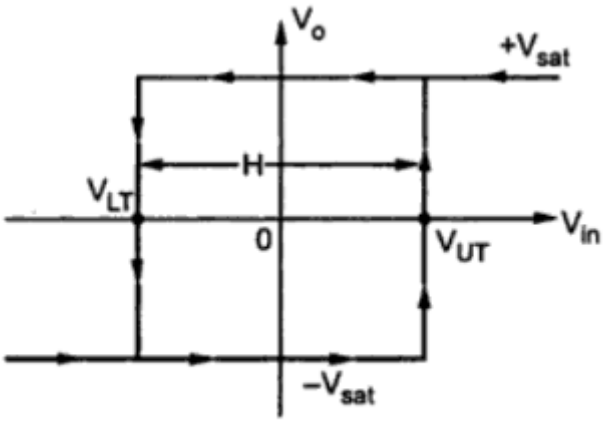


Fig. 5.38 Transfer characteristics showing Hysteresis

(Or)

7. Explain the working of instrumentation amplifier (8)

(ii) With a neat circuit diagram, explain the working of R/2R DAC. (8)

Two types R/2R ladder DAC:

- Current Mode R/2R DAC or Inverted R/2R ladder DAC.
- Voltage Mode R/2R DAC or R/2R ladder DAC.

Current Mode R/2R DAC or Inverted R/2R ladder DAC:

- The inverting ladder R/2R DAC works on the principle of summing currents and is also said to operate in **current steering mode**.
- All ladder node voltages remain constant with changing input codes thereby avoiding any shutdown effects by stray capacitances.
- Each bit of the binary word connects the corresponding switch to either ground or the inverting terminal of op-amp. The inverting input terminal of op-amp is at virtual ground.
- Since both the positions of the switches are at ground potential , the current flowing through the resistances is constant and independent of switch position. These constant currents are given by
- This type of DAC uses **voltage scaling and identical resistors to achieve its operation**.

$$I_1 = \frac{V_R}{2R}$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

$$I_n = \frac{\frac{V_R}{2^n - 1}}{2R} = \frac{I_1}{2^n - 1}$$

We know that, V_o is given as

$$V_o = -I_T R_f$$

$$V_o = -R_f (I_1 + I_2 + I_3 + \cdots + I_n)$$

$$= -R_f \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \cdots + b_n \frac{V_R}{2^n R} \right)$$

$$= \frac{-V_R R_f}{R} \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right) \quad \ldots (9)$$

When $R_f = R$, V_o is given as

$$\boxed{V_o = -V_R \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right)} \quad \ldots (10)$$

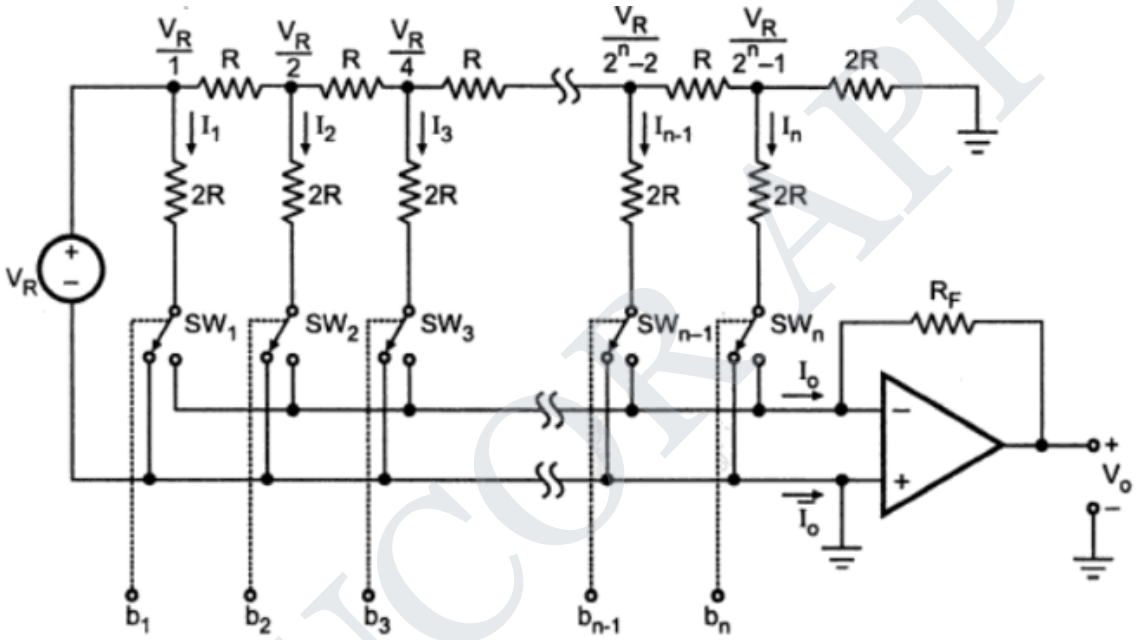


Fig. 13.4 Inverted R/2R ladder DAC

Voltage mode R/2R ladder or R/2R ladder DAC:

- In this type , reference voltage is applied to one of switch positions and other switch position is connected to ground.

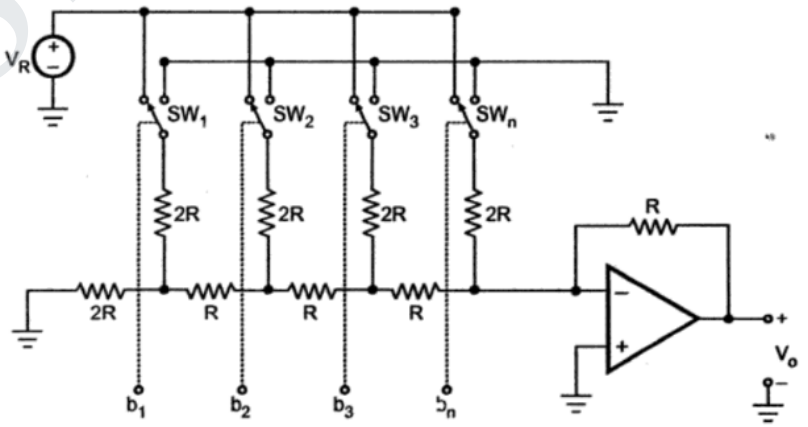


Fig. 13.6 R/2R Ladder D/A converter

Let us consider 3-bit R/2R ladder DAC with binary input 001, as shown in the Fig. 13.7.

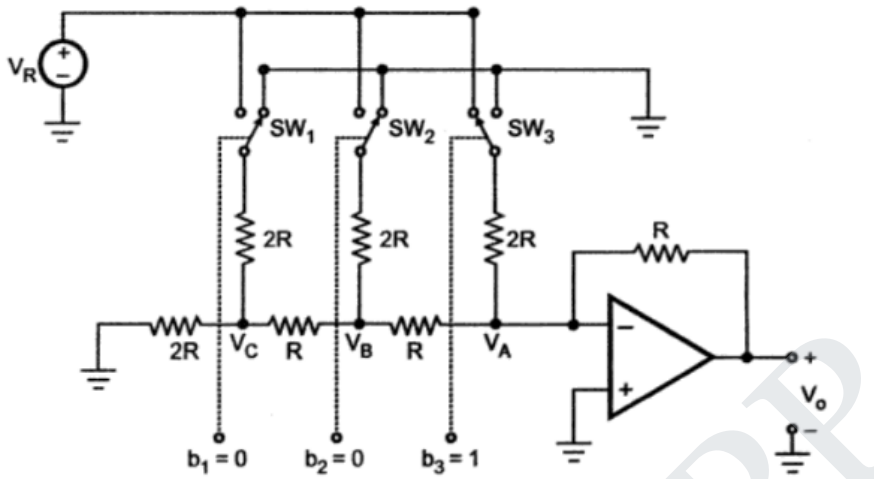


Fig. 13.7 3-bit R/2R ladder DAC

Reducing above network to the left by Thevenin's theorem we get,

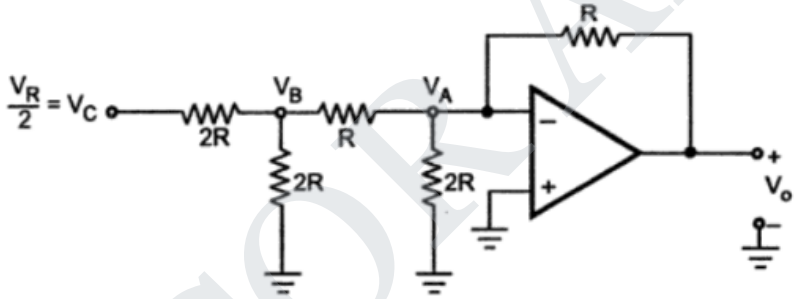


Fig. 13.8 (a)

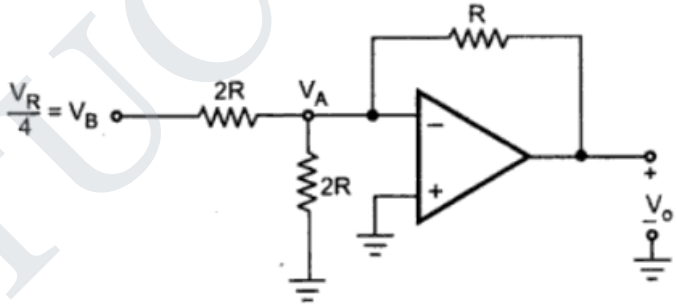
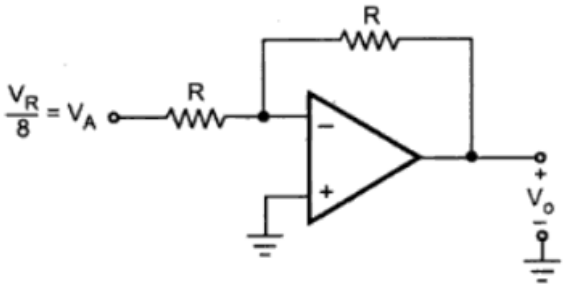


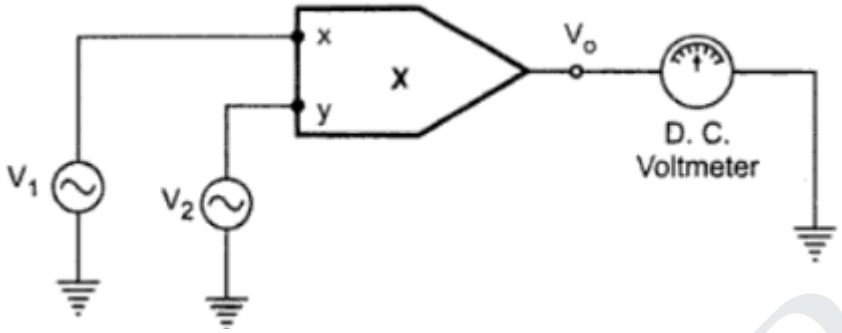
Fig. 7.10 (b)



Therefore, the output voltage is $V_R/8$ which is equivalent to binary input 001.

8. Explain how do you measure phase difference between two signals.

The frequency doubler circuit designed using **analog multiplier having two input signals with same frequency but different amplitudes and phases can be used for phase angle detection.(Phase angle – Phase difference between two signals)**



the output of the multiplier is

$$V_o = \frac{K V_{1m} V_{2m} \cos\theta}{2} - \frac{K V_{1m} V_{2m}}{2} \cos(2\omega t - \theta)$$

This is because, circuit acts as a frequency doubler. Now the D.C. voltmeter is connected at the output. The voltmeter will not respond to a.c. component present in the output, while the d.c. component can be easily measured on the voltmeter.

Now for $\theta = 0°$, voltmeter reading $= \frac{K V_{1m} V_{2m}}{2}$

for $\theta = 45°$, voltmeter reading $= \frac{K V_{1m} V_{2m}}{\sqrt{2}}$

for $\theta = 90°$, voltmeter reading $= 0$

So calibrating the d.c. voltmeter as a phase angle meter, the phase angle between the two inputs can be measured.

9. Draw a sample and hold circuit and explain its operation

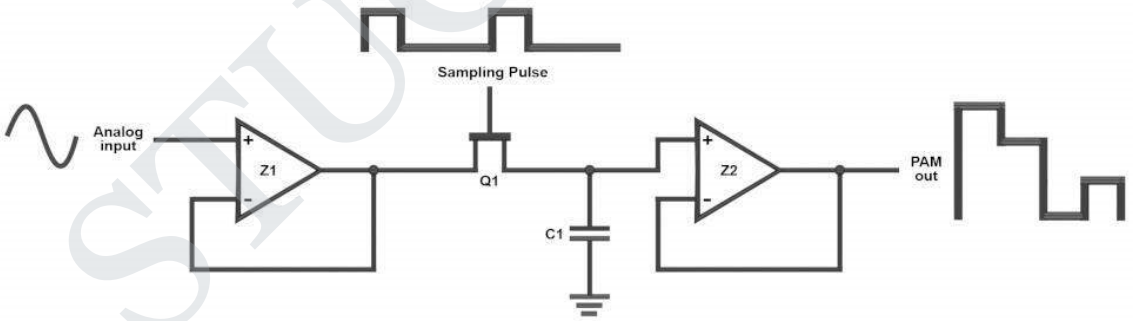
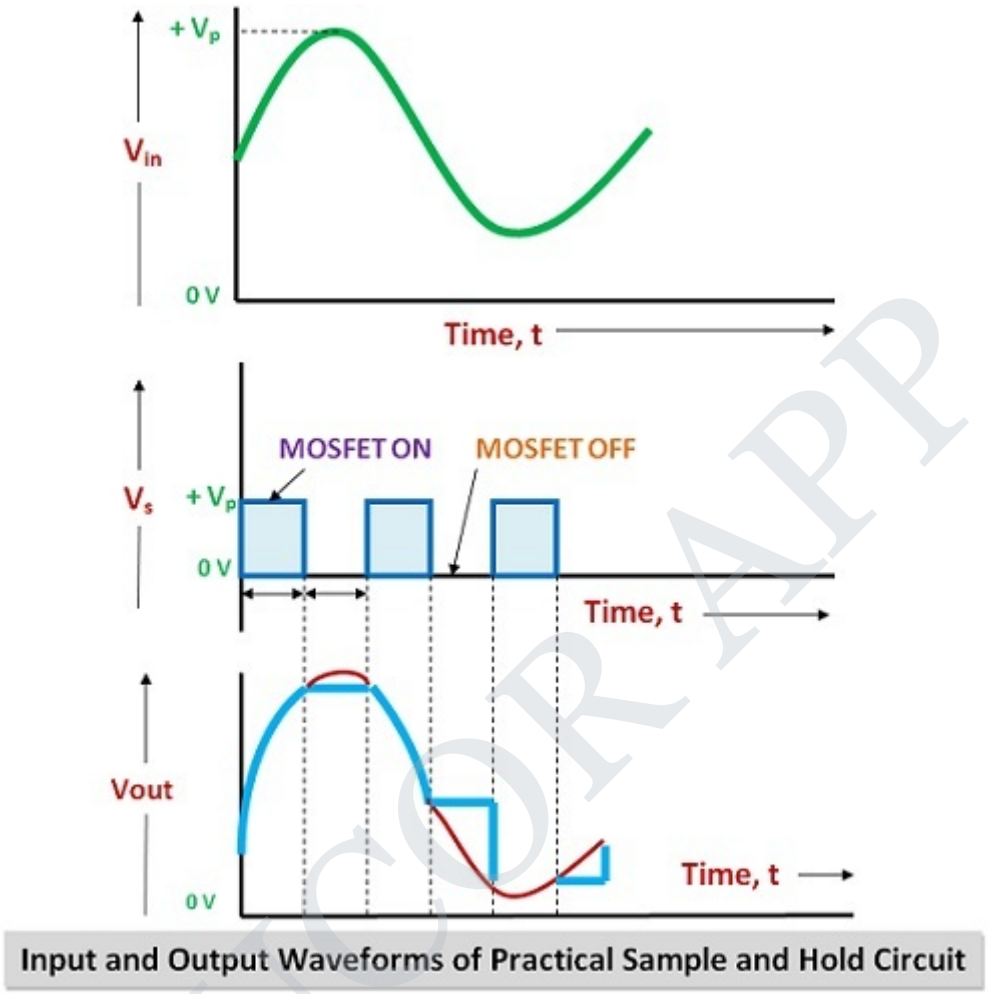


Fig. **Open Loop Type S/H[Sample and Hold] circuit**

- A sample and hold circuit samples[measures] an analog input voltage based on a sampling command in the range of 1 µs to 10 µs and holds the sampled voltage level from few milliseconds and several seconds.
- During the sampling time , JFET[Q_1] is switched ON and holding capacitor[C_1] charges to the level of analog input voltage.
- At the end of sampling period , JFET switch is turned OFF. This isolates the holding capacitor from analog input signal.
- Now the output voltage and capacitor voltage will be at the analog input voltage level.
- During the holding period , the capacitor charge leaks slightly. To avoid this , input and output voltage followers or buffers are used.

- Open loop S/H circuits are faster than their closed loop counterparts ; Closed loop S/H circuits have high dc accuracy than open loop S/H circuits.

Input and Output Waveforms:



Input and Output Waveforms of Practical Sample and Hold Circuit

Electronics Coach

Parameters of S/H circuit:

Acquisition Time: Time taken for the holding capacitor to charge to the analog input voltage ; The acquisition time must be generally low ; The acquisition time is affected by the following:
(i) RC time constant (R – ON resistance of JFET ; C – Holding Capacitor)
(ii) Maximum output current that can be source or sunk by OP-AMP
(iii) Slew Rate of OP-AMP

Aperture Time : Time taken by the capacitor to remain in charging even after getting sampling time is over. This is due to propagation delay of the JFET switch

Voltage Droop : Voltage drop in the capacitor due to charge leakage.

Hold Mode Settling Time: The time taken for charges to settle in the capacitor after hold command is given.

Advantages:

Advantages of S/H circuits:

- Hold sampled analog input voltage constant during conversion time of ADC.
- In case of multichannel ADC, synchronisation can be achieved by simultaneous sampling of all signals.

- Reduces cross-talk in MUX

Applications:

- Digital Interfacing
- ADC
- Pulse Modulation Systems

10. Design circuit of a clipper which will clip the input signal below a reference voltage.

Negative Clipper Circuit:

A negative clipper is an OP-AMP based circuit that removes input signal below the reference voltage.

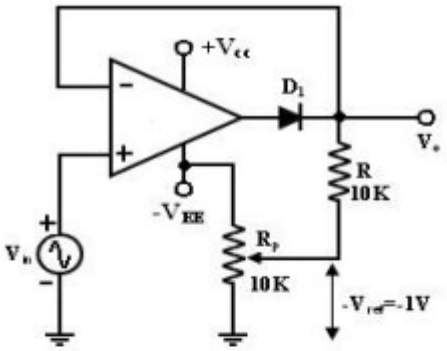


Fig.2.46 Negative clipper

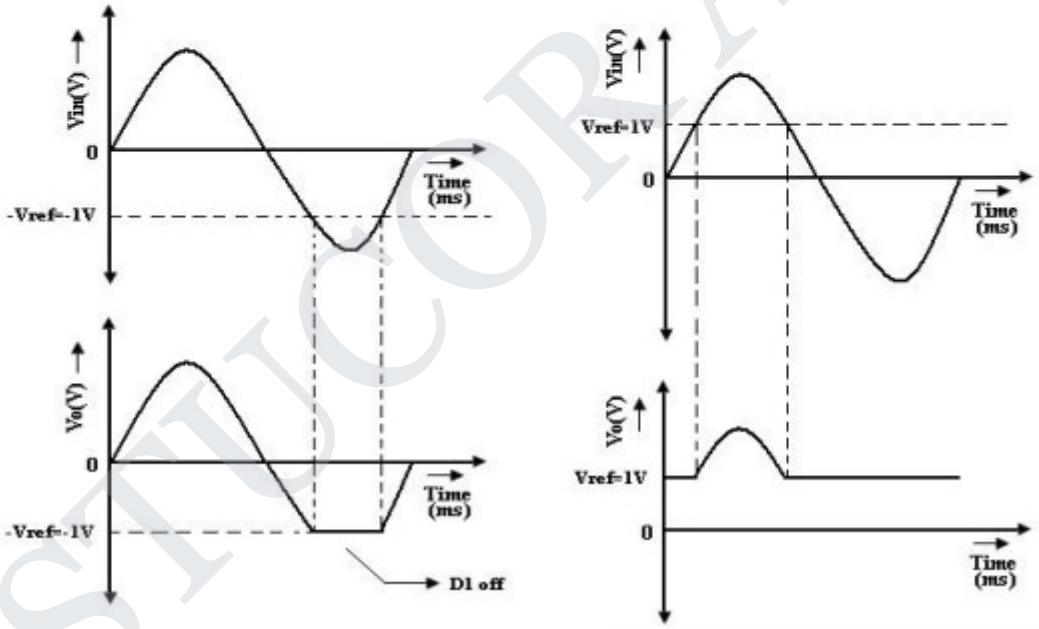


Fig. 2.47 Input output waveforms

Operation :

When $V_{IN} > -V_{EE}$ [i.e. $-V_{REF}$] , the diode D_1 gets forward biased and the OP-AMP functions as a **voltage follower i.e. Output voltage = Input Voltage**

When $V_{IN} < -V_{EE}[-V_{REF}]$, the diode D_1 gets reverse biased and output voltage below $-V_{EE}$ is removed.

When the potentiometer R_P (10K potentiometer) is connected to $+V_{CC}$, for $V_{IN} < +V_{CC}$, the diode D_1 gets reverse biased and output voltage below $+V_{CC}$ is removed.

11. Design second order Butterworth low pass filter having upper cut-off frequency of 1 kHz

Solution :

The cut-off frequency , f_H = 1 kHz

Choose $C_2 = C_3 = C = 0.01$ µF

From the formula for f_H, determine the value of $R=R_2 = R_3$

$$f_H = \frac{1}{2\pi RC}$$

Therefore R = 15.915 kΩ

For Butterworth response

$R_F = 0.586\ R_1$

Choose R_1 = 10 kΩ

Therefore R_F = 5.86 kΩ

Use a 10 kΩ potentiometer for precise adjustment of R_F

12. Explain the first order low pass Butterworth filter with a neat diagram. Derive its frequency response and plot the same.

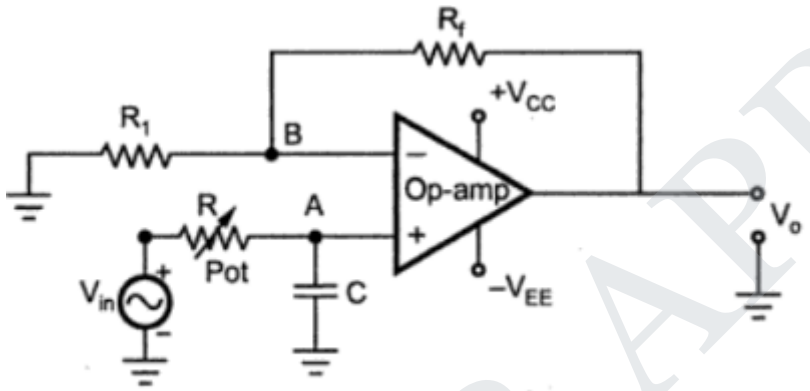


Fig. 9.17 First order low pass Butterworth filter

A non-inverting amplifier with a RC circuit at its non-inverting terminal will function as a **low pass Butterworth Filter**

The device is also called ONE POLE LOW PASS BUTTERWORTH FILTER

The resistances R_1 and R_F decide the gain of the filter in passband.[Passband is the set of frequencies allowed to flow through it without attenuation]

Analysis of filter circuit:

The impedance of the capacitor C is $-jX_C$ where X_C is the capacitive reactance given by $X_C = \frac{1}{2\pi fC}$.

By the potential divider rule, the voltage at the non-inverting input terminal A which is the voltage across capacitor C is given by,

$$V_A = \frac{-jX_C}{R - jX_C} \cdot V_{in} \qquad \ldots (1)$$

$$\therefore \quad V_A = \frac{-j\left(\frac{1}{2\pi fC}\right)}{R - j\left(\frac{1}{2\pi fC}\right)} \cdot V_{in} = \frac{-j}{2\pi fRC - j} \cdot V_{in}$$

$$= \frac{V_{in}}{1 - \frac{2\pi fRC}{j}}$$

but $-j = \frac{1}{j}$ and $-\frac{1}{j} = j$

$$\therefore \quad V_A = \frac{V_{in}}{1 + j\,2\pi f R C} \qquad \ldots (2)$$

As the op-amp is in the non-inverting configuration,

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_A \qquad \ldots (3)$$

$$\therefore \quad V_o = \left(1 + \frac{R_f}{R_1}\right) \frac{V_{in}}{(1 + j\,2\pi f R C)}$$

i.e. $$\frac{V_o}{V_{in}} = \frac{A_F}{1 + j\left(\frac{f}{f_H}\right)} \qquad \ldots (4)$$

where $$A_F = \left(1 + \frac{R_f}{R_1}\right) = \text{Gain of filter in pass band} \qquad \ldots (5)$$

and $$f_H = \frac{1}{2\pi R C} = \text{High cut-off frequency of filter} \qquad \ldots (6)$$

and f = operating frequency

The $\frac{V_o}{V_{in}}$ is the transfer function of the filter and can be expressed in the polar form as,

$$\frac{V_o}{V_{in}} = \left|\frac{V_o}{V_{in}}\right| \angle \phi$$

where $$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} \qquad \ldots (7)$$

and $$\phi = -\tan^{-1}\left(\frac{f}{f_H}\right) \qquad \ldots (8)$$

The phase angle ϕ is in degrees.

The equation (7) describes the behaviour of the low pass filter.

1. At very low frequencies, $f < f_H$

$$\left|\frac{V_o}{V_{in}}\right| \cong A_F \text{ i.e. constant}$$

2. At $f = f_H$,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{2}} = 0.707\, A_F \quad \text{i.e. 3 dB down to the level of } A_F.$$

3. At $f > f_H$

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

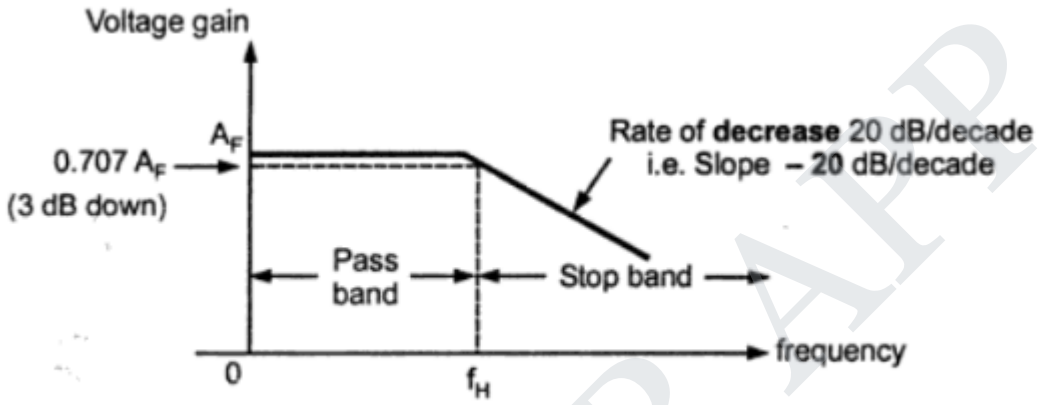


Fig. 6.65 Frequency response

For frequency range within the cut-off frequency (f_H) , the gain is constant equal to A_F. At f= f_H , the gain reduces to 0.707 A_F [or 20 $\log_{10}$ 0.707 A_F = - 3 dB].
As the frequency increases beyond f_H , for every 10 times increase in frequency , the gain reduces by 20 dB.
f_H is called **cut-off frequency or break frequency or -3 dB frequency or corner frequency**.

13. Draw the instrumentation amplifier using 3 op-amp and derive its output voltage equation

A **difference amplifier having two non-inverting amplifiers at its input is called instrumentation amplifier**

The input impedance of difference amplifier is low. It is increased by adding a **non-inverting voltage buffer**.

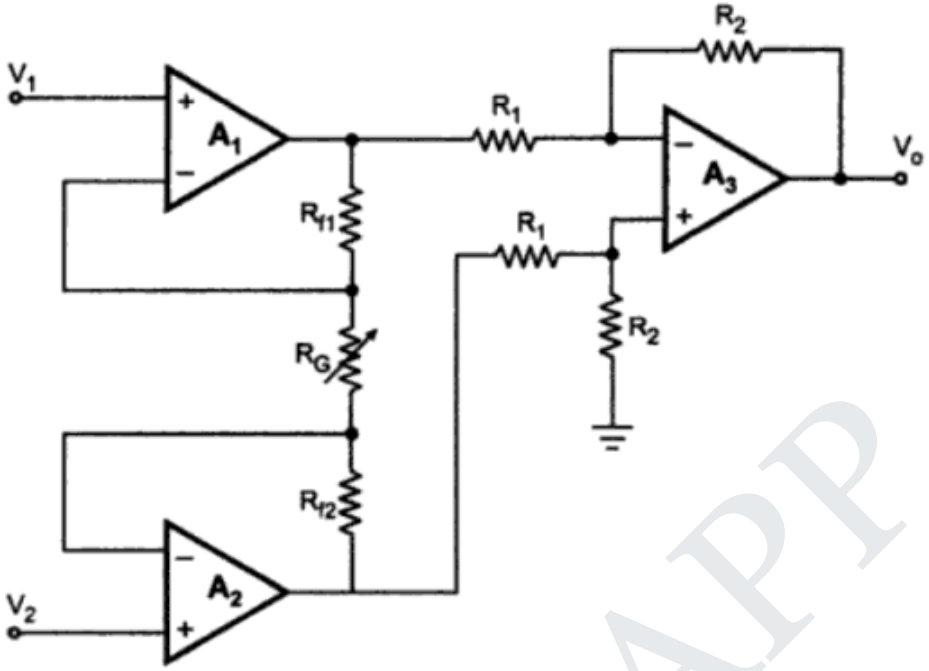
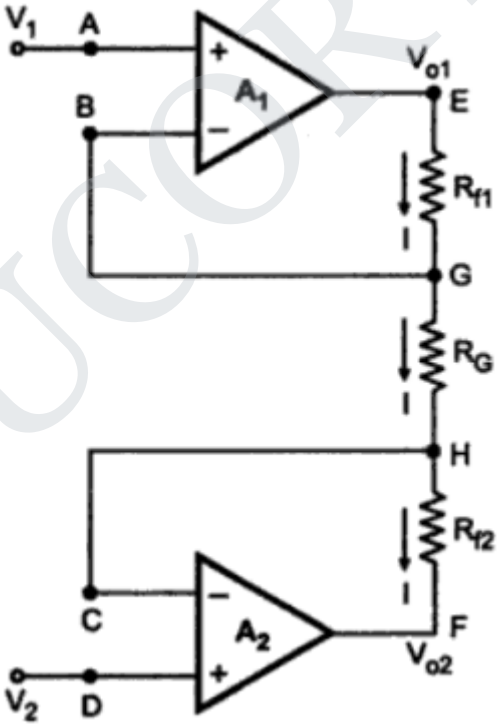


Fig. 2.44 Three op-amp instrumentation amplifier

Analysis of 3-stage op-amp instrumentation amplifier:



Output of the op-amp A_1 is V_{O1} ; Output of the op-amp A_2 is V_{O2};
By vitual ground concept , $V_G = V_B = V_A = V_1$; $V_H = V_C = V_D = V_2$

Applying Ohm's law between the nodes E and F we get,

$$I = \frac{V_{o1} - V_{o2}}{R_{f1} + R_G + R_{f2}} \quad \text{... (2)}$$

Let $R_{f1} = R_{f2} = R_f$ ... (3)

$$\therefore \quad I = \frac{V_{o1} - V_{o2}}{2R_f + R_G} \quad \text{... (4)}$$

Now from the observation of nodes G and H,

$$I = \frac{V_G - V_H}{R_G} = \frac{V_1 - V_2}{R_G} \quad \text{... (5)}$$

Equating (4) and (5)

$$\frac{V_{o1} - V_{o2}}{2R_f + R_G} = \frac{V_2 - V_1}{R_G} \quad \text{... (6)}$$

$$\therefore \quad \frac{V_{o2} - V_{o1}}{2R_f + R_G} = \frac{V_1 - V_2}{R_G} \quad \text{... (7)}$$

$$\therefore \quad V_{o2} - V_{o1} = \frac{(2R_f + R_G)(V_2 - V_1)}{R_G} \quad \text{... (8)}$$

Substituting the $V_{o2} - V_{o1}$, in the equation (1),

$$V_o = \frac{R_2}{R_1} \cdot \left[\frac{2R_f + R_G}{R_G}\right](V_2 - V_1) \quad \text{... (9)}$$

$$\therefore \quad V_o = \frac{R_2}{R_1} \cdot \left(1 + \frac{2R_f}{R_G}\right)(V_2 - V_1) \quad \text{... (10)}$$

This is the overall gain of the circuit.

Advantages:

- With the help of R_G , the gain can be easily varied
- By selecting high quality resistances , gain can be adjusted accurately
- High input impedance
- Low output impedance
- Very High CMRR

14. a. With a neat diagram explain the following applications of op-amp (13)
(i) Clippers and clampers
(ii) Triangular waveform generator

Clipper : [DC Limiter]

A clipper is an op-amp based device that is used to remove a DC level from the AC output voltage above or below the reference voltage. The op-amp is made to function as a NON-INVERTING VOLTAGE FOLLOWER.

Positive Clipper:

A positive clipper is a circuit that clips a positive portion of a signal above a reference voltage

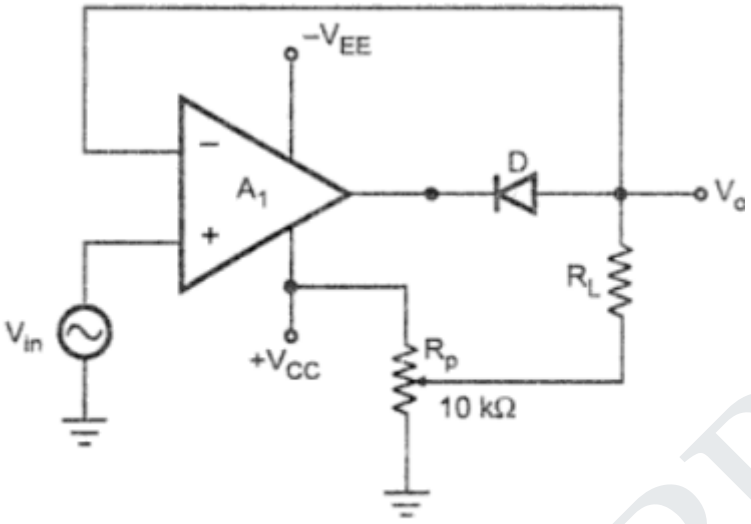


Fig. 4.154 Positive clipper circuit

A sinusoidal voltage is applied to the non-inverting terminal of OP-AMP. The value of V_{REF} is determined by connecting a 10 kΩ potentiometer to either $+V_{CC}$ or $-V_{EE}$.

When $V_{IN} \geq +V_{REF}$ $(+V_{CC})$, the diode D is reverse biased. Now the OP-AMP operates in open loop mode. The OP-AMP gets driven towards positive saturation value $+V_{CC}$. Hence all the portions of the waveform above $+V_{CC}$ gets removed. When $V_{IN} < +V_{REF}(+V_{CC})$, the diode D is forward biased. Now the OP-AMP operates in closed loop mode as **voltage follower**.

If $+V_{CC}$ is replaced with $-V_{EE}$, when the diode is reverse biased , all the portions of the waveform above $-V_{EE}$ gets removed.

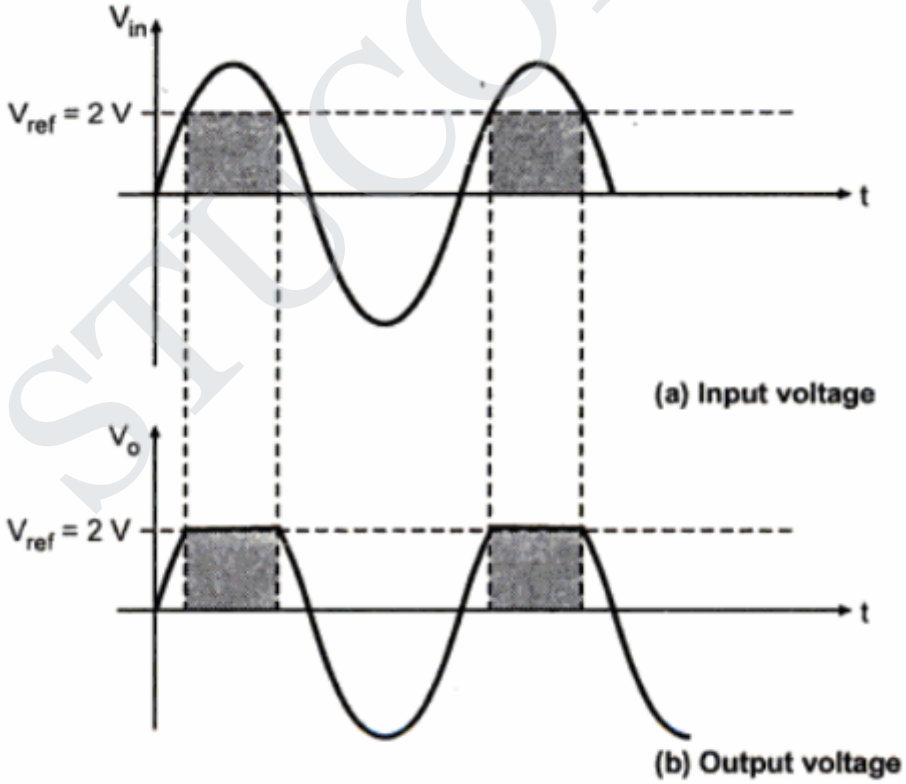


Fig. Waveforms of positive Clipper with $+V_{REF}$ $(+V_{CC})$

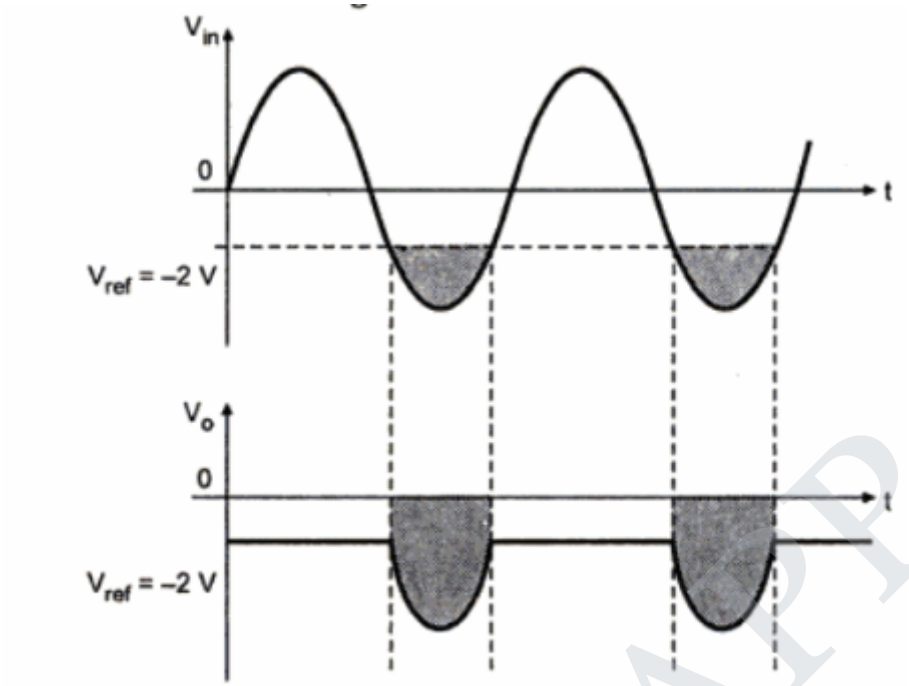


Fig. 4.156 Waveforms with negative V_{ref}

Fig. Waveforms of negative clipper with $-V_{REF}$ ($-V_{EE}$)

Negative Clipper:

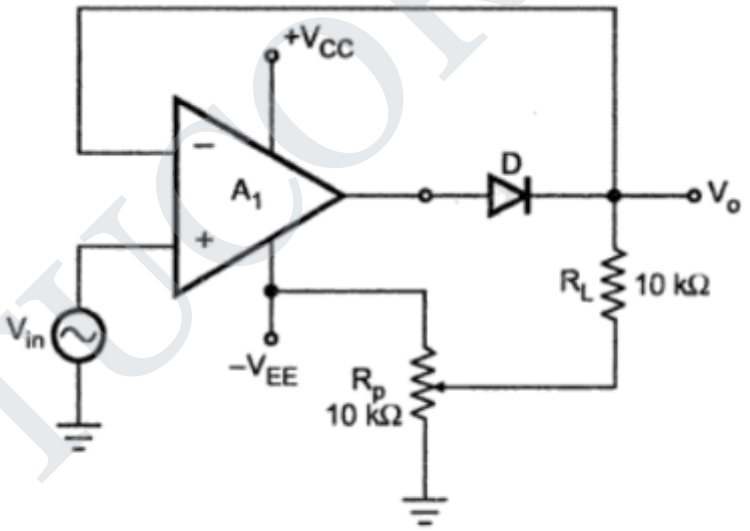


Fig. 4.157 Negative clipper circuit

A negative clipper is a device which is used to remove the portion of the output waveform below a reference voltage.

A sinusoidal voltage is applied to the non-inverting terminal of OP-AMP. The value of V_{REF} is determined by connecting a 10 kΩ potentiometer to either $+V_{CC}$ or $-V_{EE}$.

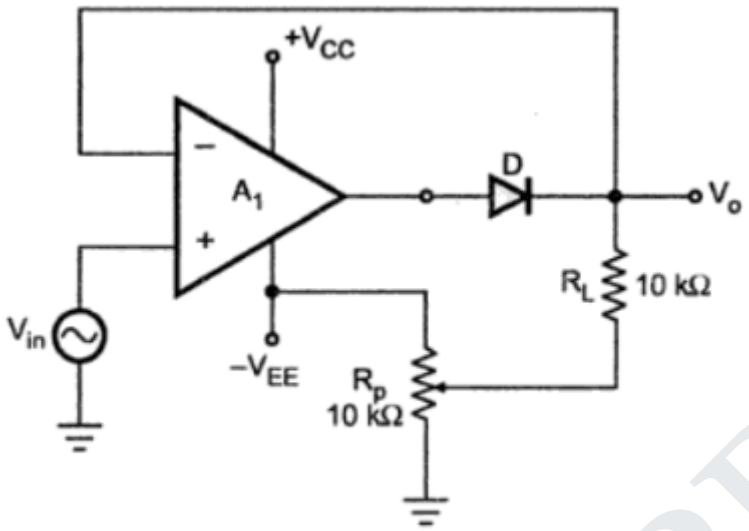


Fig. 4.157 Negative clipper circuit

When $V_{IN} \geq -V_{EE}$, the diode D is forward biased and the op-amp functions as a closed loop voltage follower.

When $V_{IN} < -V_{EE}$, the diode D is reverse biased and op-amp functions in open loop mode. The OP-AMP gets driven towards positive saturation value $-V_{EE}$. Hence all the portions of the waveform below $-V_{EE}$ gets removed.

If $-V_{EE}$ is replaced with $+V_{CC}$, when the diode is reverse biased , all the portions of the waveform below $+V_{CC}$ gets removed.

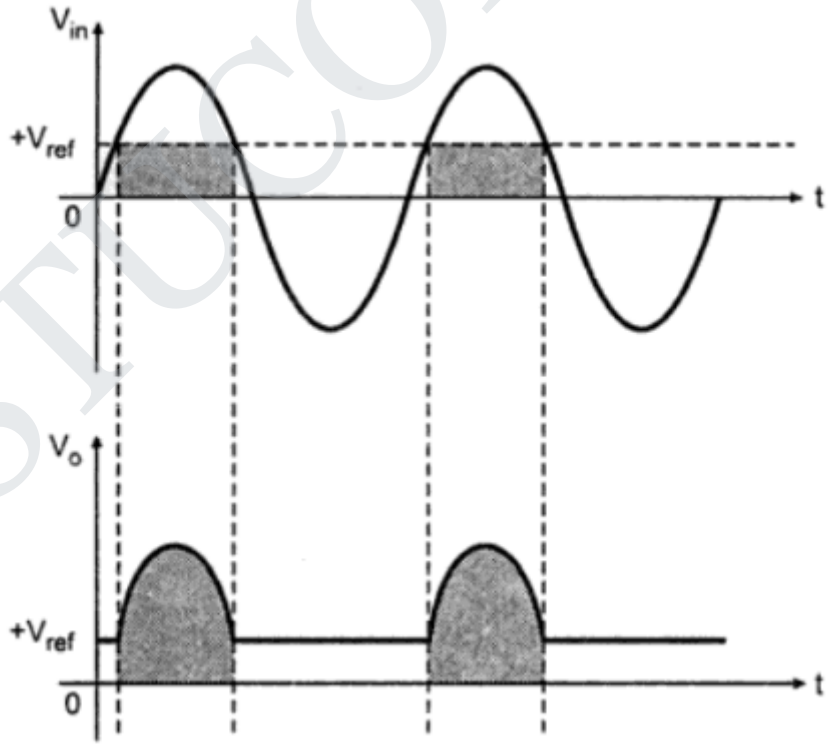


Fig. Waveforms with $-V_{REF}$ ($-V_{EE}$)

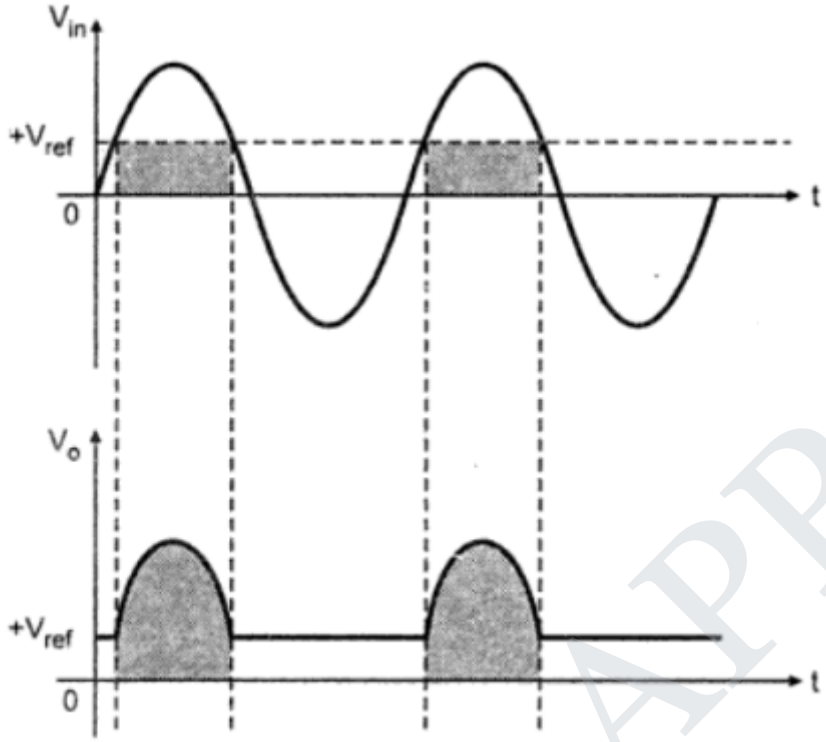


Fig. 4.159 Waveforms with positive V_{ref}

Clamper[DC restorer]

A clamper is a device which is used to a positive or negative DC level to the AC output waveform. It is the reciprocal of **clipper**. The OP-AMP is made to function as a **INVERTING VOLTAGE FOLLOWER**.

Positive Clamper:

A positive clamper is an op-amp based device that is used to a **add a positive DC level** to the AC output voltage.

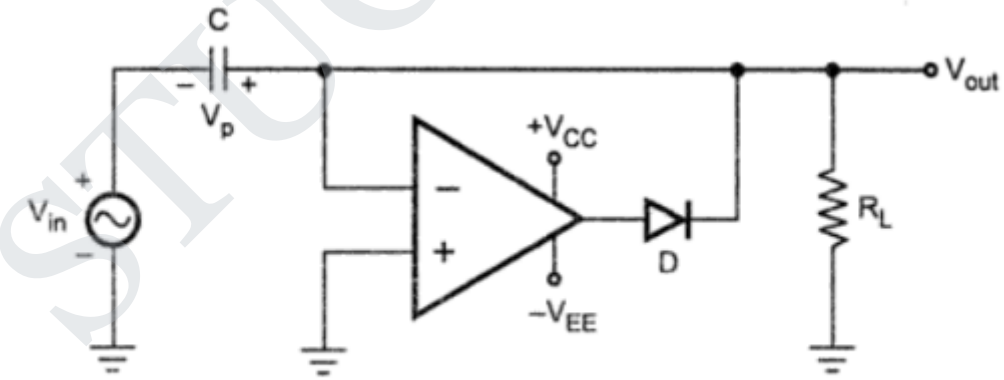


Fig. 4.160 Positive clamper circuit

The input voltage is applied to the **inverting terminal of op-amp**. During negative half cycle of the input signal , a positive going voltage is developed at the output of the OP-AMP. This forward biases the diode and capacitor C charges to the negative peak of input signal.

When the input waveform starts to rise towards positive half cycle , a negative going voltage is developed at the output of the OP-AMP. This reverse biases the diode. Hence the output voltage is the sum of input voltage and capacitor voltage.

$$V_{OUT} = V_{IN} + V_P$$

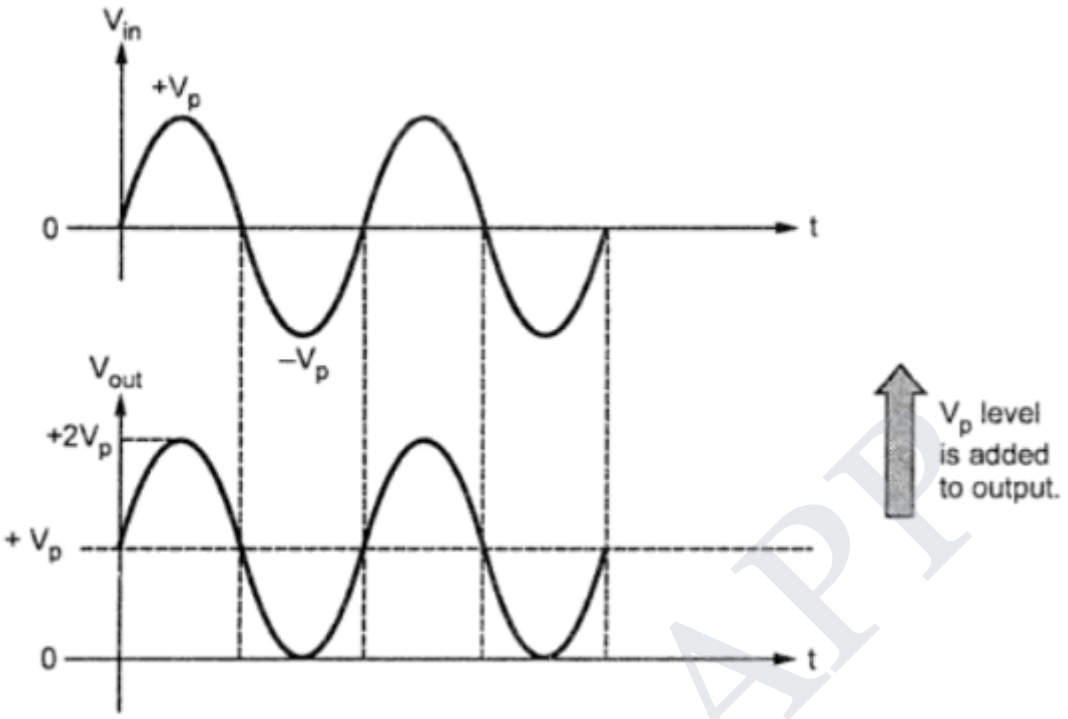


Fig. 4.161 Waveforms of positive clamper circuit

By adding a potentiometer at the non-inverting terminal , the waveform can rest on **non-zero DC level determined by $+V_{REF}$.**

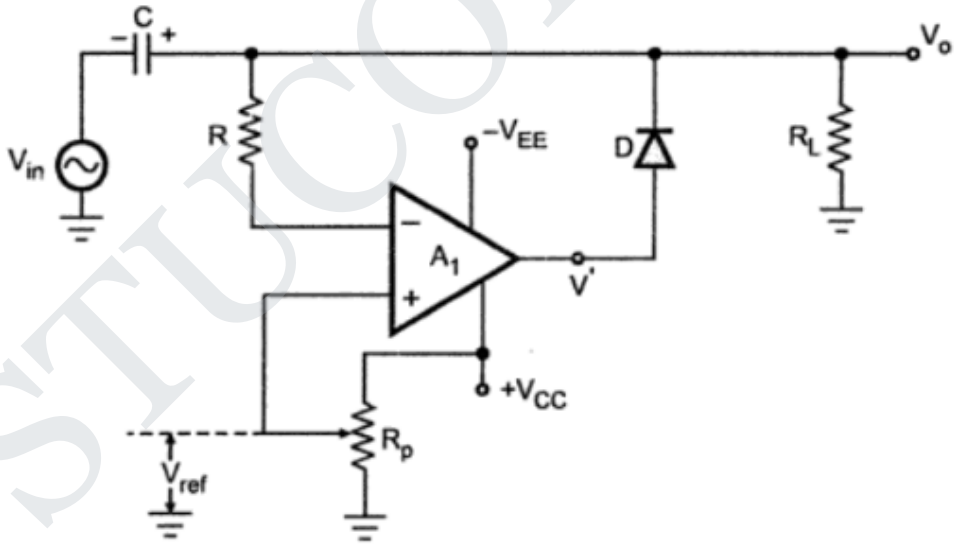


Fig. 4.162 Positive clamper circuit

As the circuit clamps the peak of the input waveform to the output waveform , the circuit is also called POSITIVE PEAK CLAMPER CIRCUIT.

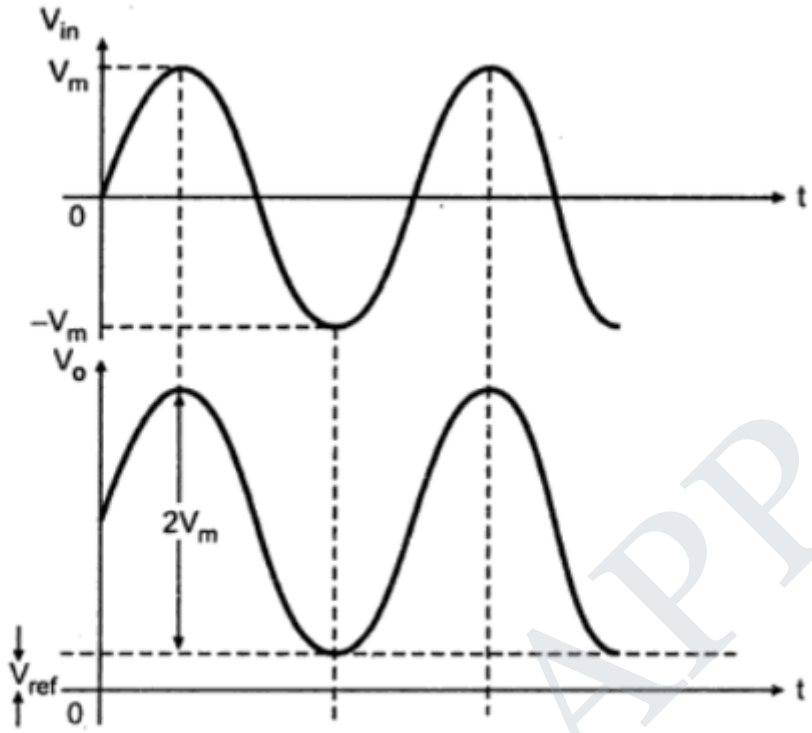


Fig. 4.163 Waveforms for positive clamper circuit

Negative Clamper Circuit:

A negative clamper is an op-amp based device that is used to a **add a negative DC level** to the AC output voltage

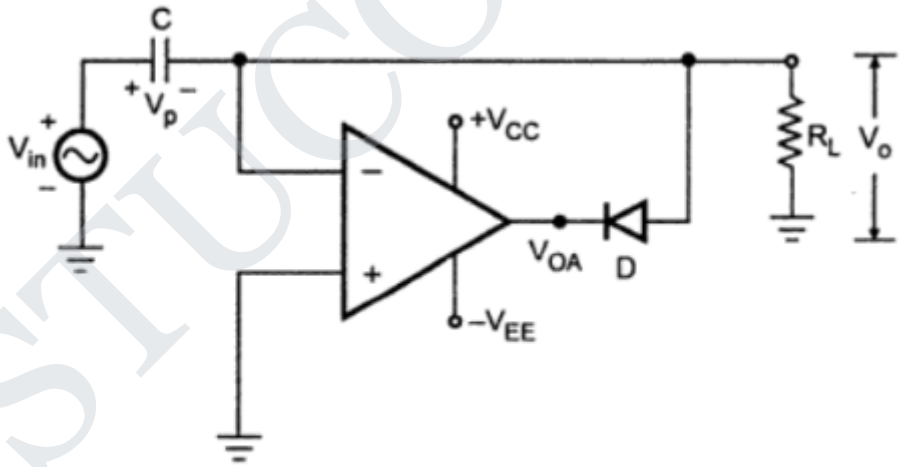


Fig. 4.164 Negative clamper circuit

The input voltage is applied to the **inverting terminal of op-amp**. During positive half cycle of the input signal , a negative going voltage is developed at the output of the OP-AMP. This forward biases the diode and capacitor C charges to the positive peak of input signal.

When the input waveform starts to fall towards negative half cycle , a positive going voltage is developed at the output of the OP-AMP. This reverse biases the diode. Hence the output voltage is the sum of input voltage and capacitor voltage.

$$V_{OUT} = V_{IN} - V_P$$

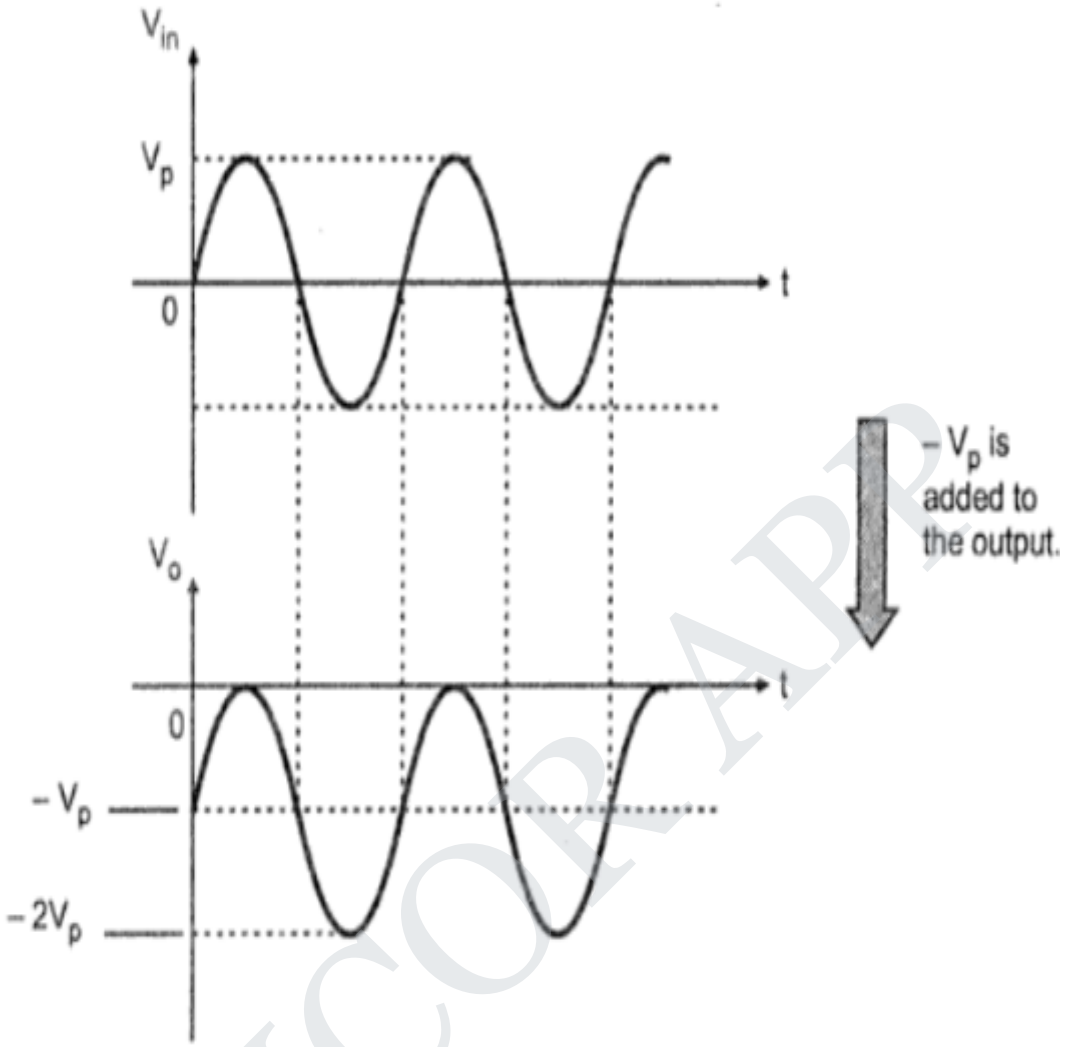


Fig. Waveforms for negative clamper circuit

Similar to a positive clamper , by adding a potentiometer at the non-inverting terminal , the waveform can rest on **non-zero DC level determined by -V_{REF}.**

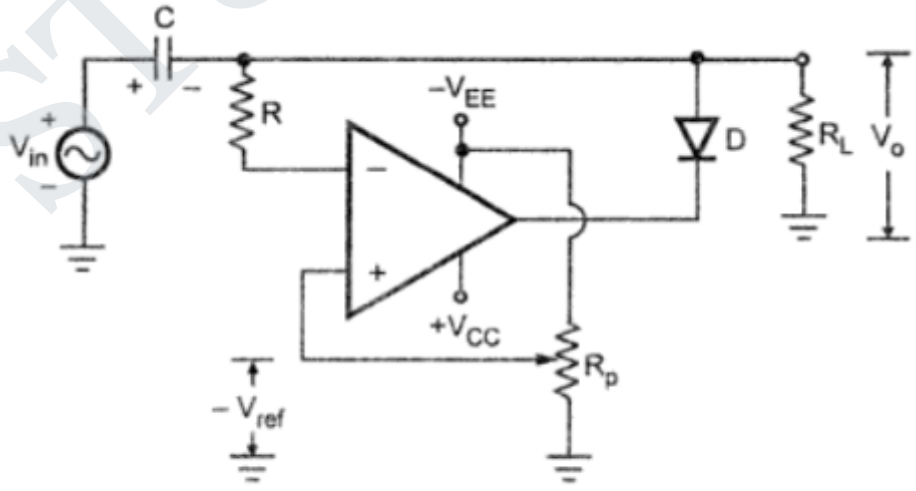


Fig. 4.166 Negative clamper circuit

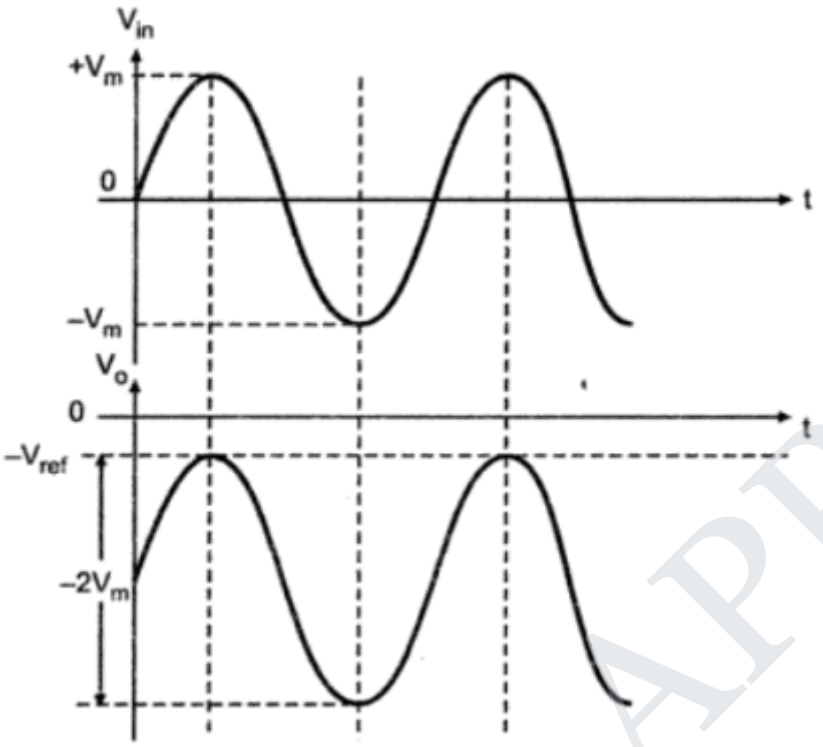
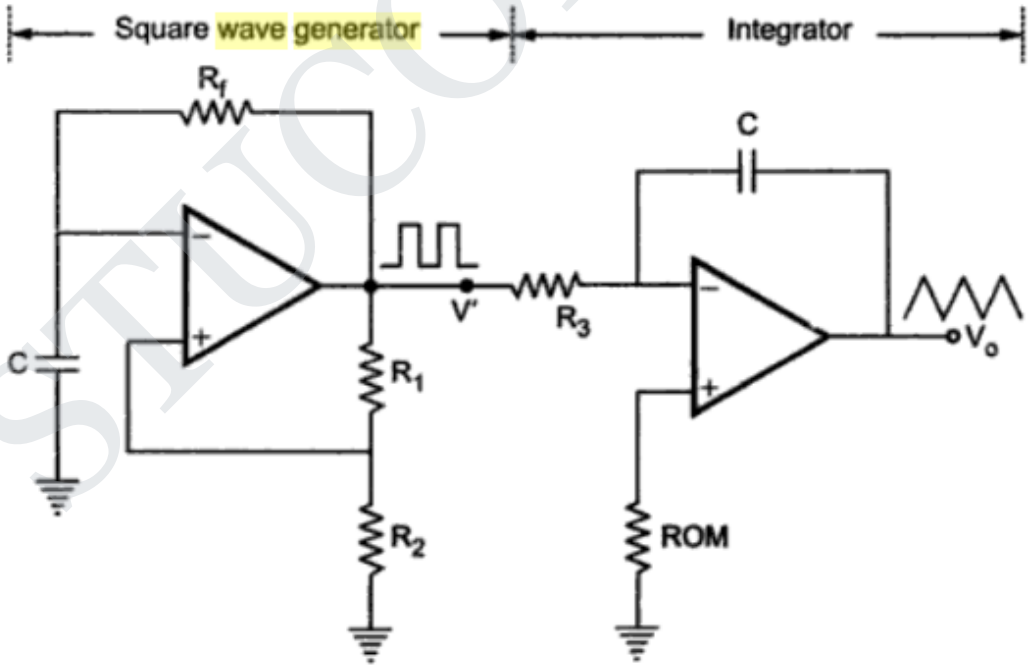


Fig. 4.167 Waveforms for negative clamper circuit

Triangular Waveform Generator:



A square wave generator having an integrator at its output is called **triangular wave generator.**

The triangular wave is generated by constantly charging and discharging of the capacitance of integrator.

Assume the output of square wave generator , V' = $+V_{SAT}$. This forces a constant current ($+V_{SAT}/R_3$) through the feedback capacitor [from left to right]of integrator causing a **negative ramp at the output**. When V' = $-V_{SAT}$, it forces a constant current ($-V_{SAT}/R_3$) through feedback capacitor[from right to left] of integrator causing a **positive ramp at the output**.

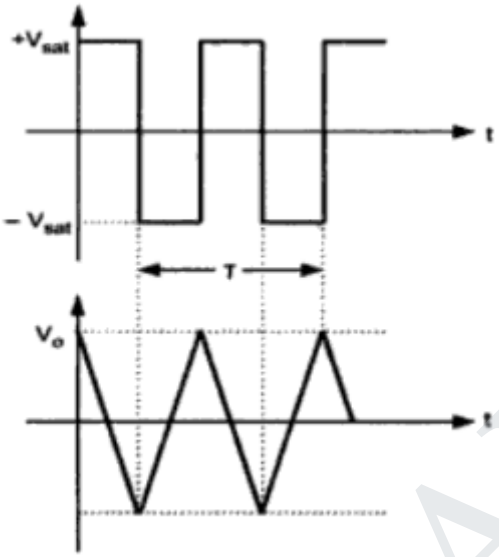


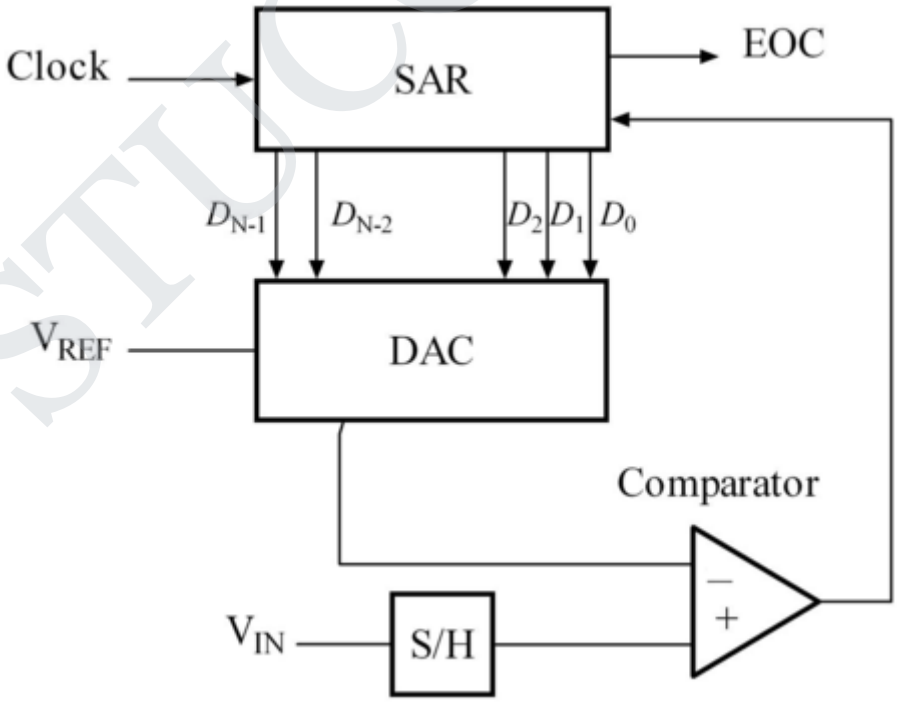
Fig. Waveforms of Triangular Wave Generator

A resistance R_4 connected across the feedback capacitance C of the integrator reduces saturation problem at low frequencies.

To obtain stable triangular wave at the output , $5R_3C_2$ [C_2 is the feedback capacitance of integrator] must be greater than T/2 [T – Time period of square wave]

15. Explain the working of SAR type and Flash type A/D converter

SAR[Successive Approximation Register] Type ADC:



A SAR ADC converts a analog signal into a equivalent binary value by means of **binary search algorithm**.

The ADC consist of four sub-circuits namely:

→ Sample and Hold Circuit to acquire the input voltage V_{IN}.

→ Analog voltage comparator that converts V_{IN} with the output of DAC.
→ A successive approximation register to hold the digital code.
→ An internal DAC to convert the digital code of SAR into an equivalent analog voltage

Working:
The MSB(Most Significant Bit) of the SAR is set to 1. This code is supplied to DAC which converts into a analog value equal to $V_{REF}/2$. The input analog voltage and $V_{REF}/2$ is fed into a analog comparator . If $V_{REF}/2 > V_{IN}$, then MSB is reset to 0 and the next LSB(Least Significant Bit) is set to 1. If $V_{REF}/2 < V_{IN}$, the MSB is left as 1 and the next LSB(Least Significant Bit) is set to 1. This test of **binary search is done** repeatedly till all the bits of SAR is tested. Once all the bits of SAR is tested , the final code held by the SAR is the equivalent digital value of V_{IN}.

The conversion time of SAR type ADC is given by $T_C = T(n+1)$
T- Clock Period n – Number of bits in SAR

Flash Type ADC (or Direct Conversion ADC or Parallel Comparator ADC)

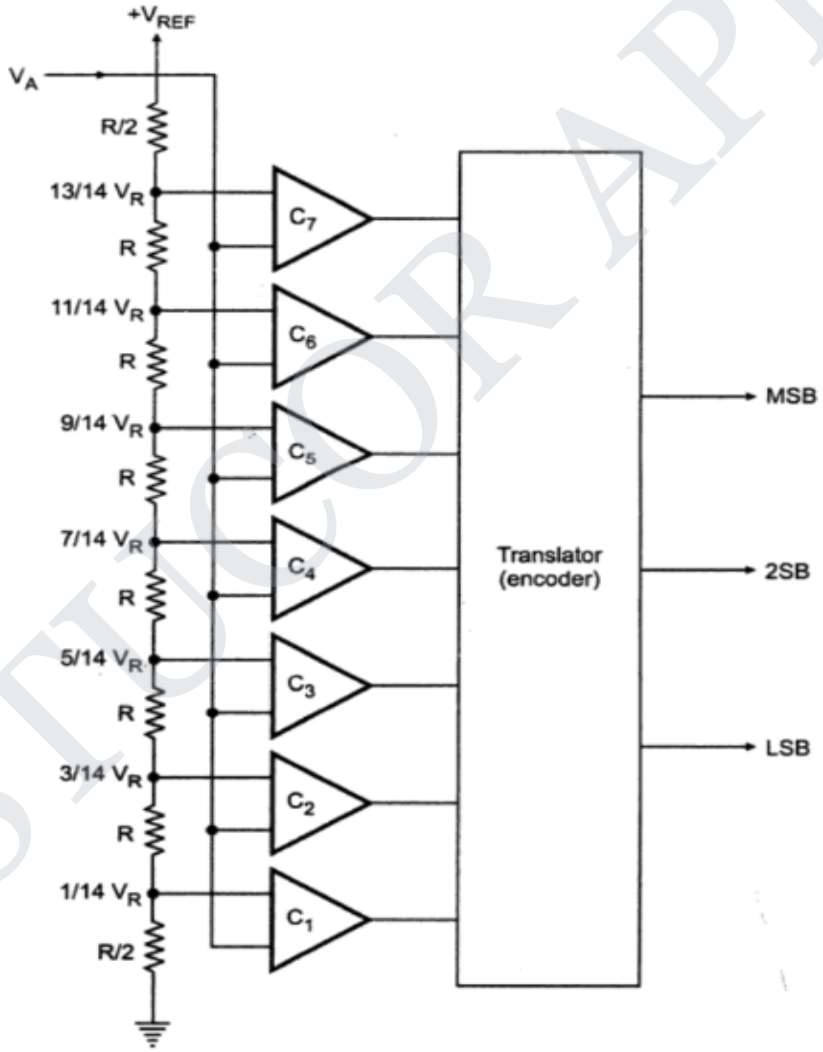


Fig. 3-bit Flash Type ADC

- Their conversion speed is very high
- Number of comparators required = 2^n-1 ; n – Number of bits
- One input of each comparator connected to input signal and another input of each comparator connected to reference voltage [Generated by voltage dividing resistors]
- The reference voltage is equal to full scale input voltage.

- The comparators provide an output of "0" when their input voltage is greater than reference voltage ; The comparators provide an output of "1" when their input voltage is lesser than or equal to the reference voltage.
- The code resulting from the comparator is converted into a binary code by encoder
- The conversion time, $T_C = \frac{1}{2\pi f_{max} 2^n}$;

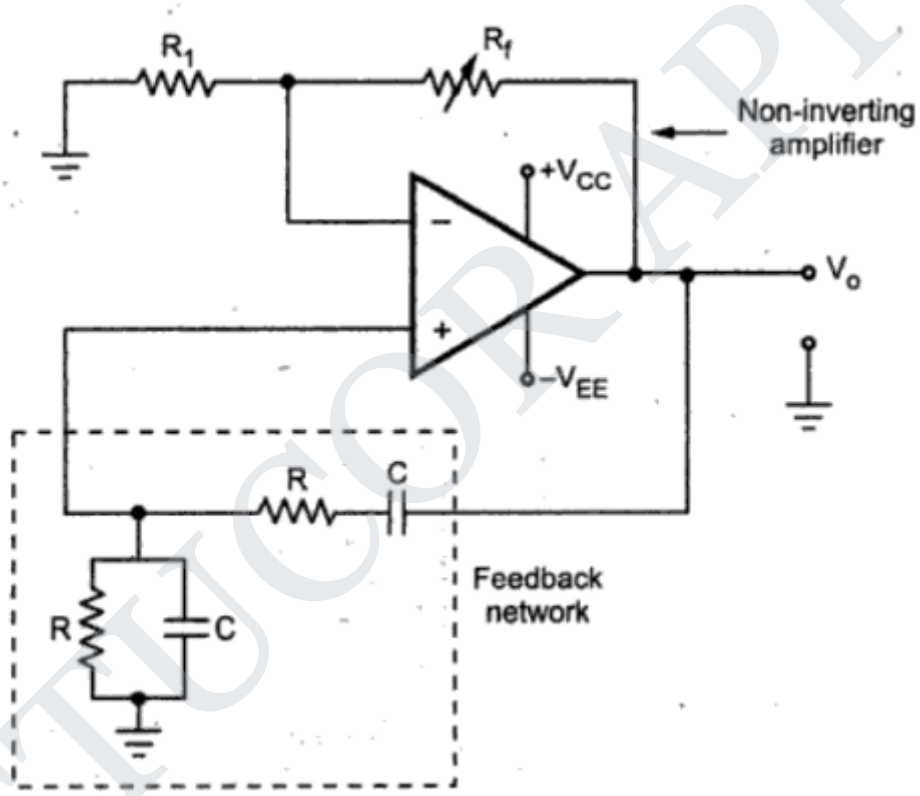
f_{MAX} = Maximum Value of Input Signal Frequency

n = Number of bits

16. Design a Wein Bridge oscillator for a frequency of 5 kHz. Assume C = 0.01 μF.

$$R = \frac{1}{2\pi f C}$$

$$R = \frac{1}{2\pi \times 5 \times 10^3 \times 0.01 \times 10^{-6}} = 6.4\ k\Omega$$



$R_F = 2R_1$

Choose $R_1 = 1\ k\Omega$

Therefore $R_F = 2\ k\Omega$

17. With circuit diagram , discuss the operation of peak detector?

A **peak detector** is an op-amp based device which notes and remember the peak positive or negative value of an input signal for an infinite period of time.

The peak detector stores the amplitude of input voltage in a capacitor. If a peak higher than stored peak value occurs , the capacitor stores the new peak value of input voltage.

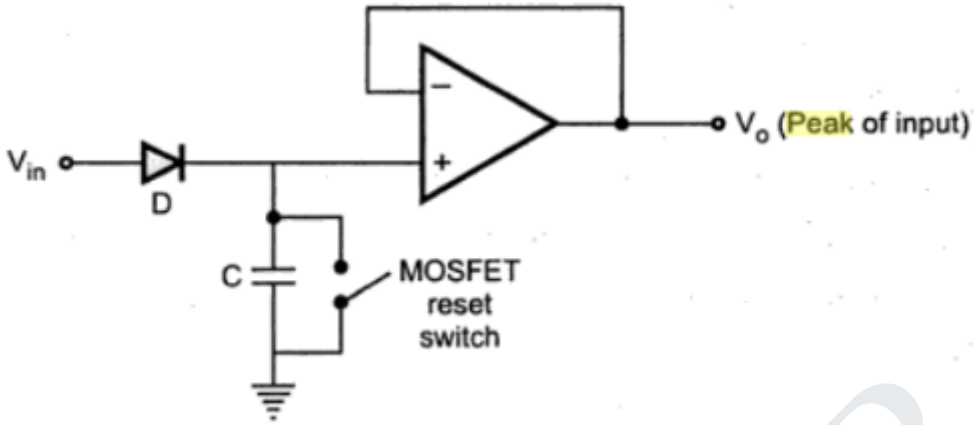


Fig. Basic Positive Peak Detector

- For positive value of input voltage ,the capacitor C gets charged to the highest value of input voltage through the diode D.
- The capacitor remains in the charged value till it is discharged by means of MOSFET reset switch connected parallel to it.
- The op-amp acts as a non-inverting voltage follower. Its output will be equal to the voltage held by the capacitor.
- For negative value of input voltage , the diode gets reverse biased and the capacitor retains its voltage.

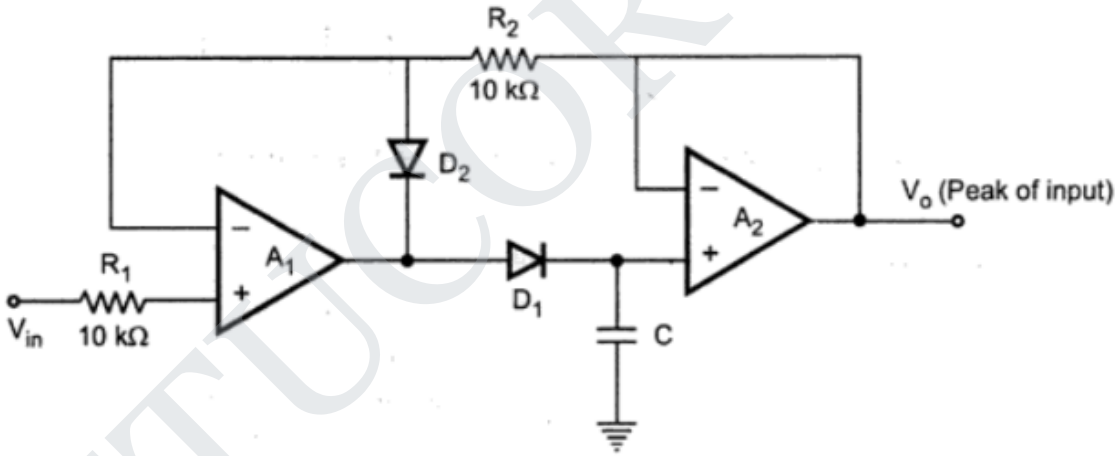
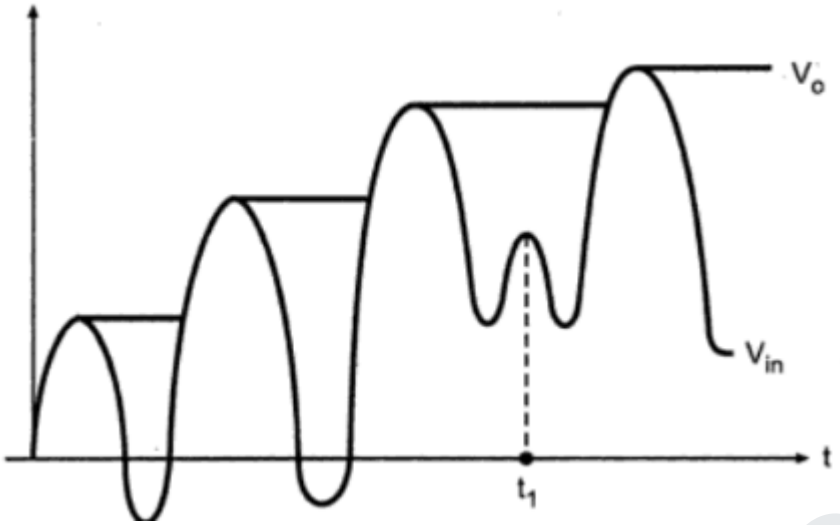


Fig. 3.111 Improved peak detector

- The op-amp A_1 acts as a high input impedance non-inverting amplifier. The op-amp A_2 acts as a non-inverting voltage follower between capacitor and load.
- When the input level gets dropped , the capacitor holds the peak value of input voltage because the diode D_1 gets reverse biased and D_1 prevents the output of A_2 from attaining negative saturation value.
- Resistance R_2 provides input bias current path for A_1 ; $R_1 = R_2$ in order to minimize the effect of offset voltage ; A_1 is made stable against oscillations by providing required frequency compensation.
- Peak detectors are used in amplitude modulation in communication and in test and measurement instrument applications.



18. With a neat figures explain the design of a circuit for performing (i) Square Wave Generation (ii) Sweep Signal Generation (iii) Clamped Signal Output (15)

Square Wave Generation: [Schmitt Trigger]

A Schmitt trigger is also called REGENERATIVE COMPARATOR or SINE-TO-SQUARE WAVE CONVERTER.

Inverting Schmitt trigger

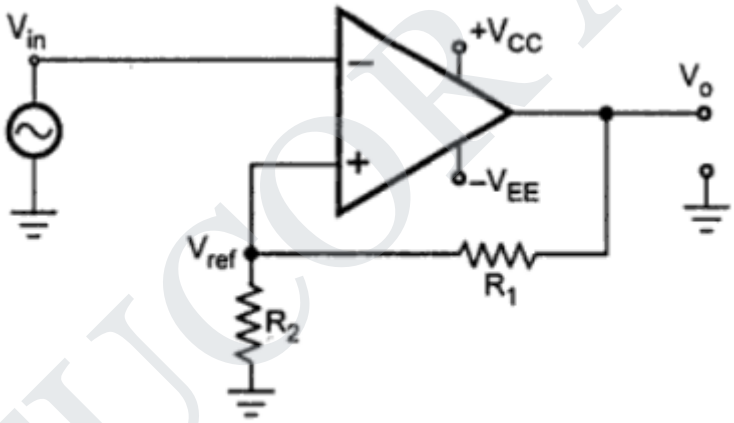


Fig. 5.33 Inverting Schmitt trigger

- Input voltage signal is applied to the inverting input terminal. The inverting mode produces an output voltage that is 180˚ out of phase with input voltage. This voltage is applied to the **non-inverting terminal**
- When $V_{IN} > V_{UT}$, the output gets saturated at $-V_{SAT}$
- When $V_{IN} < V_{LT}$, the output gets saturated at $+ V_{SAT}$.
- The voltage at which output changes from $+V_{SAT}$ to $-V_{SAT}$ is controlled by the potential dividers R_1 and R_2.

$$+V_{ref} = \frac{V_o}{R_1 + R_2} \times R_2 = \frac{+ V_{sat}}{R_1 + R_2} \times R_2 \quad \text{.... positive saturation}$$

$$-V_{ref} = \frac{V_o}{R_1 + R_2} \times R_2 = \frac{- V_{sat}}{R_1 + R_2} \times R_2 \quad \text{.... negative saturation}$$

$+V_{REF}$ is also called **UPPER THRESHOLD VOLTAGE(V_{UT})**. $-V_{REF}$ is also called **LOWER THRESHOLD VOLTAGE(V_{LT})**.

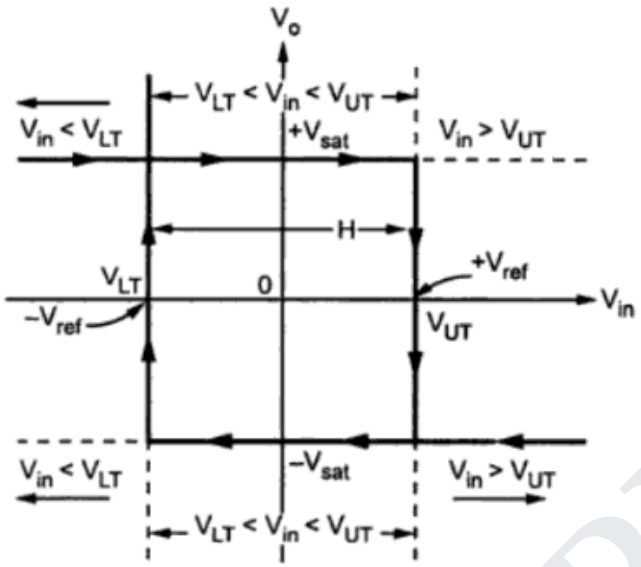


Fig. Hysterisis Curve of Inverting Schmitt Trigger

- The hysteresis curve indicates that once the output changes its state from $+V_{SAT}$ to $-V_{SAT}$ or vice-versa , it remains there indefinitely till the input voltage exceeds the threshold voltage levels. This is called **hysteresis or dead band or dead zone of Inverting Schmitt Trigger.**
- The difference between V_{UT} and V_{LT} is called **width of hysteresis**

$$H = V_{UT} - V_{LT} = \frac{+V_{sat}\ R_2}{R_1 + R_2} - \left[\frac{-V_{sat}\ R_2}{R_1 + R_2}\right]$$

$$\boxed{H = \frac{2\ V_{sat}\ R_2}{R_1 + R_2}}$$

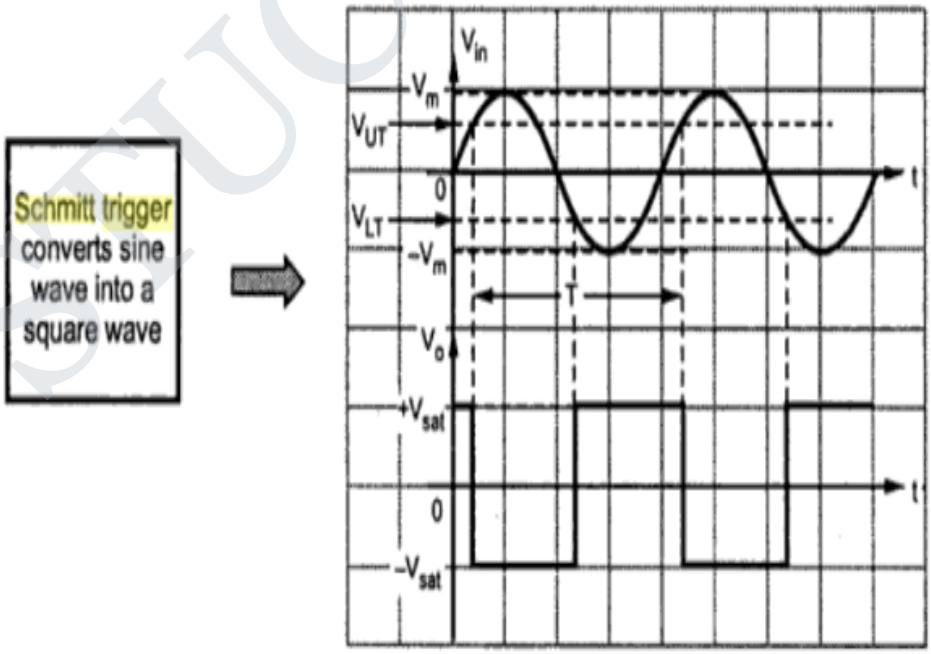


Fig. 5.35 Input and output waveforms of inverting Schmitt trigger

Non-Inverting Schmitt Trigger:

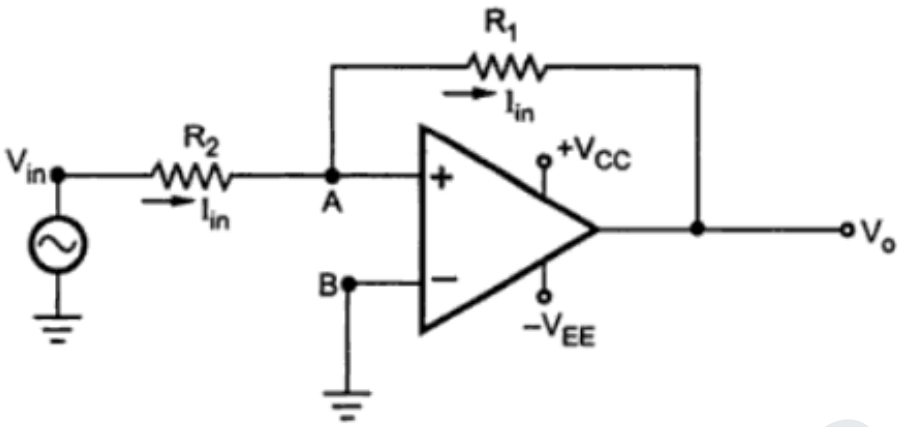


Fig. 5.37 Noninverting schmitt trigger

- Assume the output is at $+V_{SAT}$. This is applied as feedback through R_1 to **non-inverting terminal**.
- Now though V_{IN} is decreased , the output remains in its positive saturation level till the input becomes more negative than V_{LT}. Once the input exceeds V_{LT} , the output changes its state from $+V_{SAT}$ to $-V_{SAT}$. The circuit remains in $-V_{SAT}$, till the input becomes more positive than V_{UT}.

Now V_A = voltage at point A = $I_{in} R_2$

$= V_{UT}$

As op-amp input current is zero, I_{in} entirely passes through R_1.

$$\therefore \quad I_{in} = \frac{V_o}{R_1} = \frac{+V_{sat}}{R_1}$$

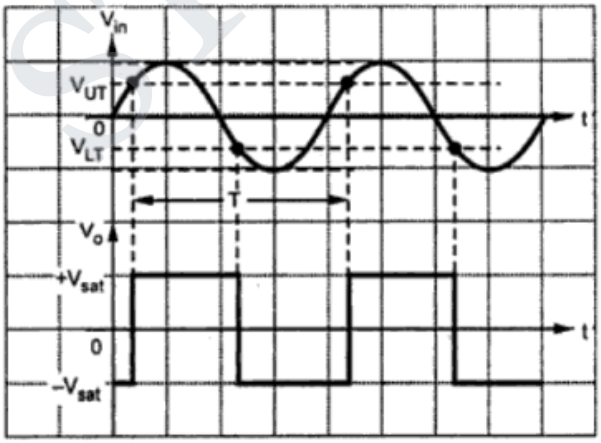
$$\therefore \quad \boxed{V_{UT} = I_{in} R_2 = \frac{R_2}{R_1}(+V_{sat}) = V_{sat}\frac{R_2}{R_1}}$$

and

$$\boxed{V_{LT} = \frac{R_2}{R_1}(-V_{sat}) = -V_{sat}\frac{R_2}{R_1}}$$

and

$$\boxed{H = V_{UT} - V_{LT} = 2\,V_{sat}\frac{R_2}{R_1}}$$



$V_{in} > V_{UT}$
V_o changes from
$-V_{sat}$ to $+V_{sat}$

$V_{in} < V_{LT}$
V_o changes from
$+V_{sat}$ to $-V_{sat}$

Fig. 5.39 Input and output waveforms

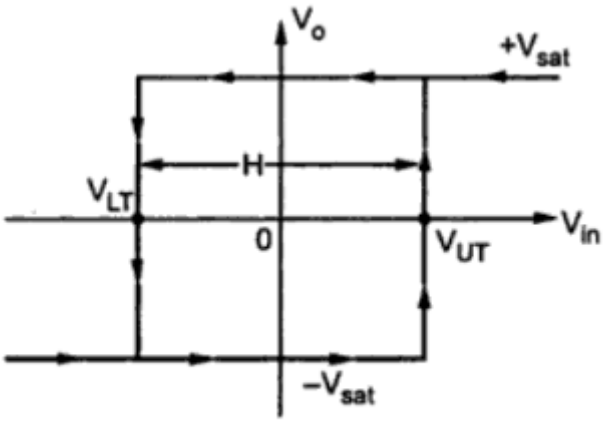
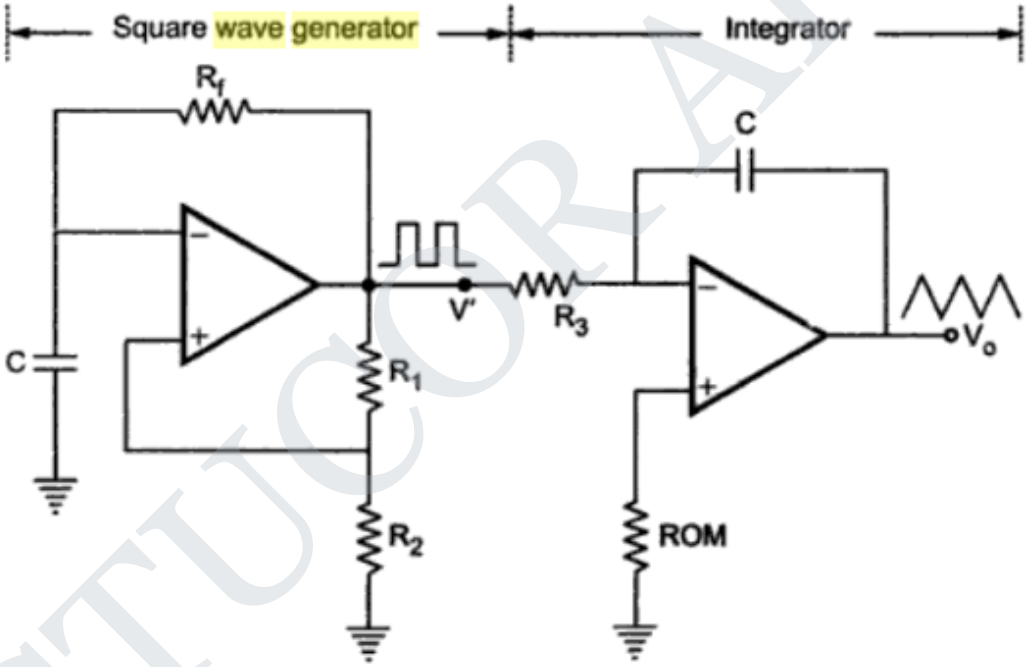


Fig. 5.38 Transfer characteristics showing Hysteresis

(ii) Sweep Signal Generation (Triangular Waveform Generator)
Triangular Waveform Generator:



A square wave generator having an integrator at its output is called **triangular wave generator.**

The triangular wave is generated by constantly charging and discharging of the capacitance of integrator.

Assume the output of square wave generator , V' = $+V_{SAT}$. This forces a constant current ($+V_{SAT}/R_3$) through the feedback capacitor [from left to right]of integrator causing a **negative ramp at the output**. When V' = $-V_{SAT}$, it forces a constant current ($-V_{SAT}/R_3$) through feedback capacitor[from right to left] of integrator causing a **positive ramp at the output**.

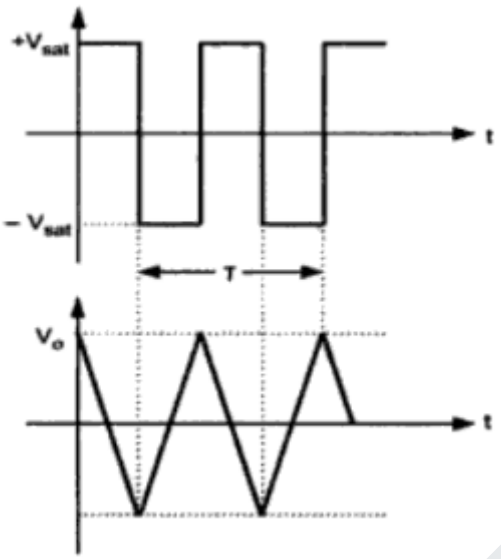


Fig. Waveforms of Triangular Wave Generator

A resistance R_4 connected across the feedback capacitance C of the integrator reduces saturation problem at low frequencies.

To obtain stable triangular wave at the output , $5R_3C_2$ [C_2 is the feedback capacitance of integrator] must be greater than T/2 [T – Time period of square wave]

(iii) Clamped Signal Output

Clamper[DC restorer]

A clamper is a device which is used to a positive or negative DC level to the AC output waveform. It is the reciprocal of **clipper**. The OP-AMP is made to function as a **INVERTING VOLTAGE FOLLOWER**.

Positive Clamper:

A positive clamper is an op-amp based device that is used to a **add a positive DC level** to the AC output voltage.

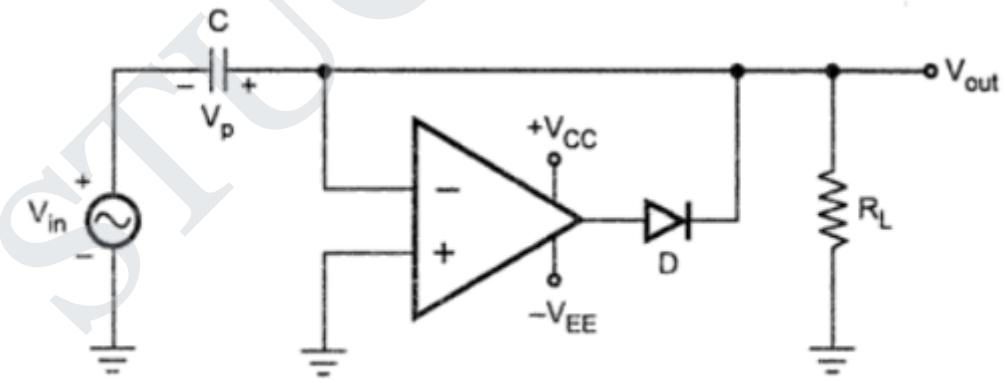


Fig. 4.160 Positive clamper circuit

The input voltage is applied to the **inverting terminal of op-amp**. During negative half cycle of the input signal , a positive going voltage is developed at the output of the OP-AMP. This forward biases the diode and capacitor C charges to the negative peak of input signal.

When the input waveform starts to rise towards positive half cycle , a negative going voltage is developed at the output of the OP-AMP. This reverse biases the diode. Hence the output voltage is the sum of input voltage and capacitor voltage.

$$V_{OUT} = V_{IN} + V_P$$

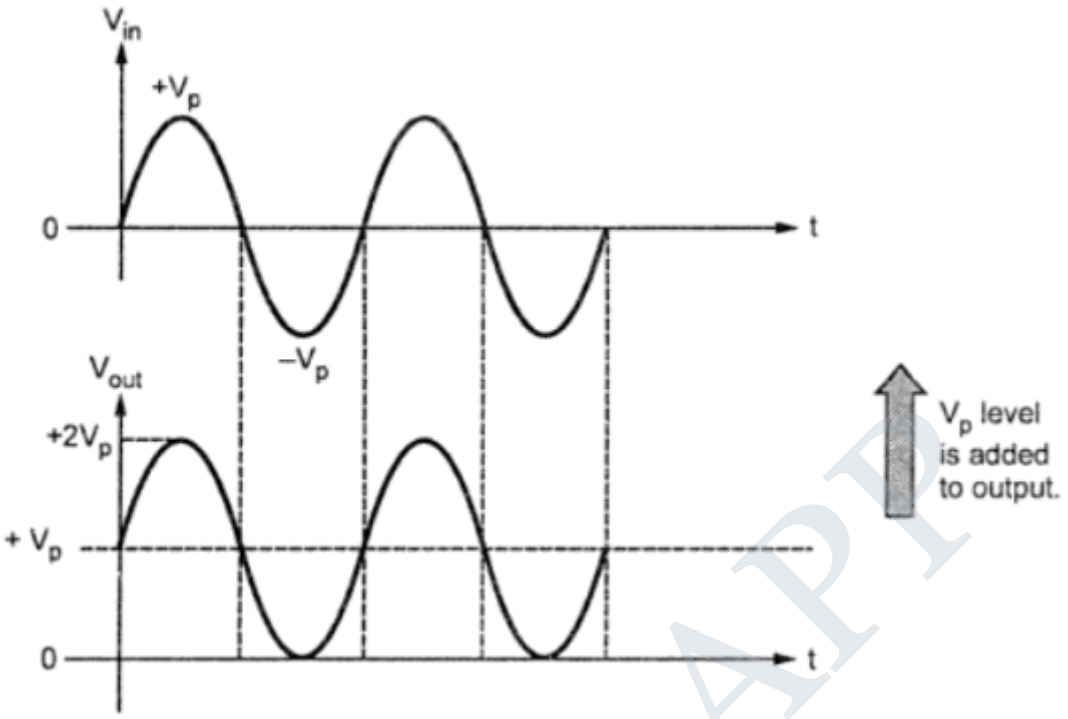


Fig. 4.161 Waveforms of positive clamper circuit

By adding a potentiometer at the non-inverting terminal , the waveform can rest on **non-zero DC level determined by $+V_{REF}$.**

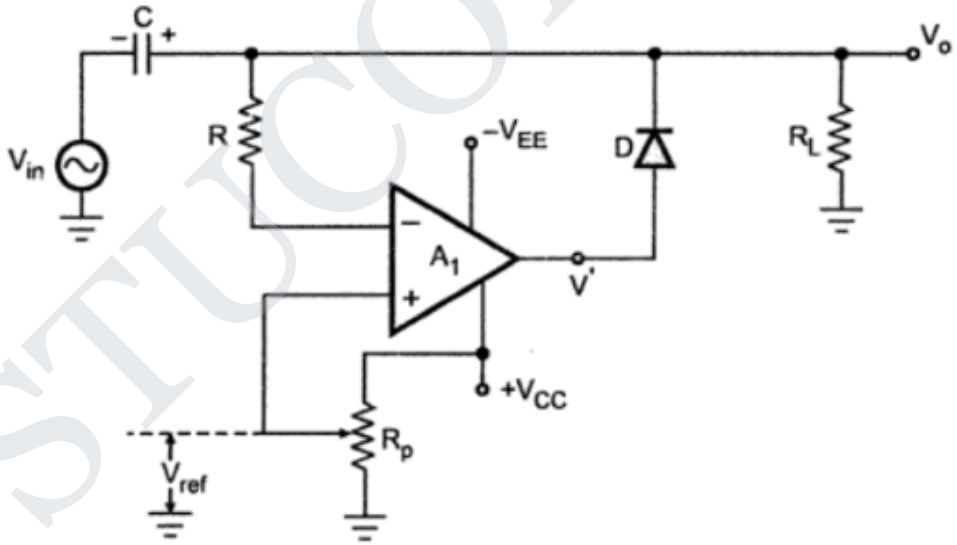


Fig. 4.162 Positive clamper circuit

As the circuit clamps the peak of the input waveform to the output waveform , the circuit is also called POSITIVE PEAK CLAMPER CIRCUIT.

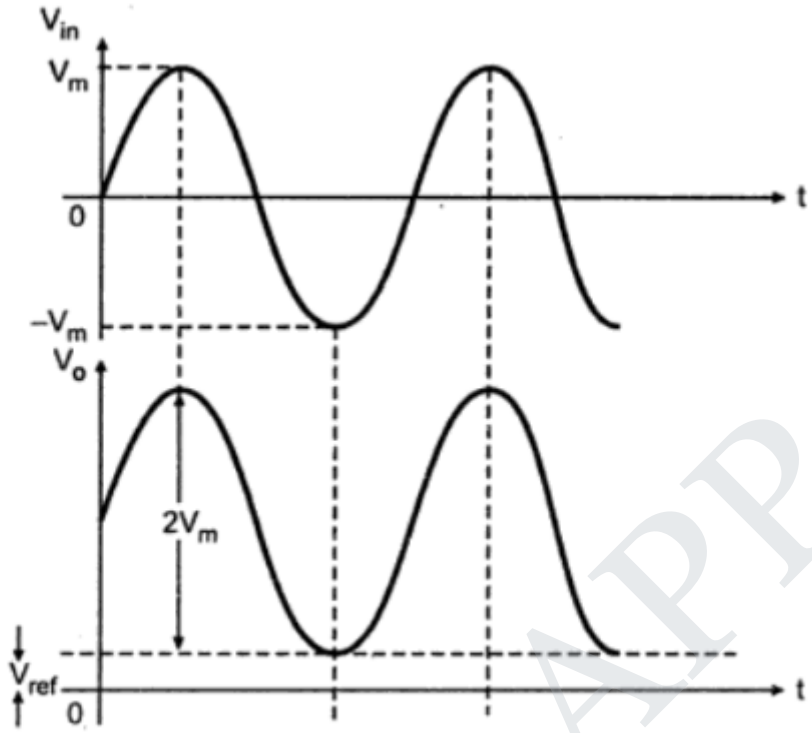


Fig. 4.163 Waveforms for positive clamper circuit

Negative Clamper Circuit:

A negative clamper is an op-amp based device that is used to a **add a negative DC level** to the AC output voltage

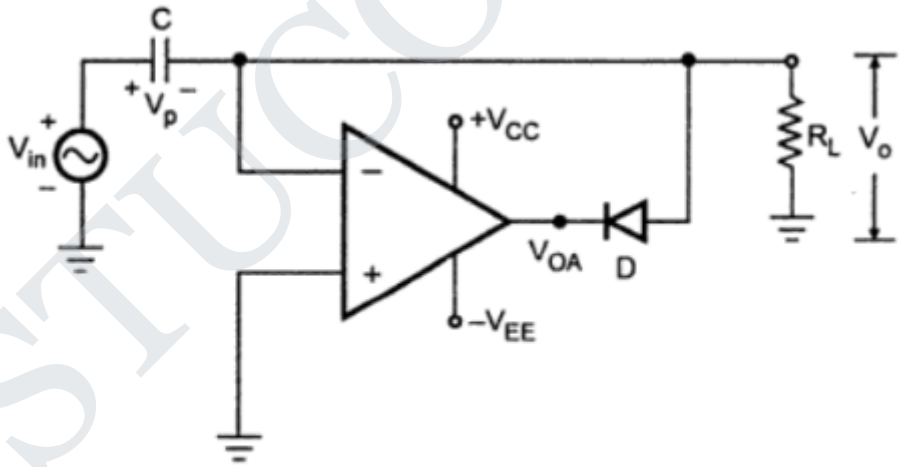


Fig. 4.164 Negative clamper circuit

The input voltage is applied to the **inverting terminal of op-amp**. During positive half cycle of the input signal , a negative going voltage is developed at the output of the OP-AMP. This forward biases the diode and capacitor C charges to the positive peak of input signal.

When the input waveform starts to fall towards negative half cycle , a positive going voltage is developed at the output of the OP-AMP. This reverse biases the diode. Hence the output voltage is the sum of input voltage and capacitor voltage.

$$V_{OUT} = V_{IN} - V_P$$

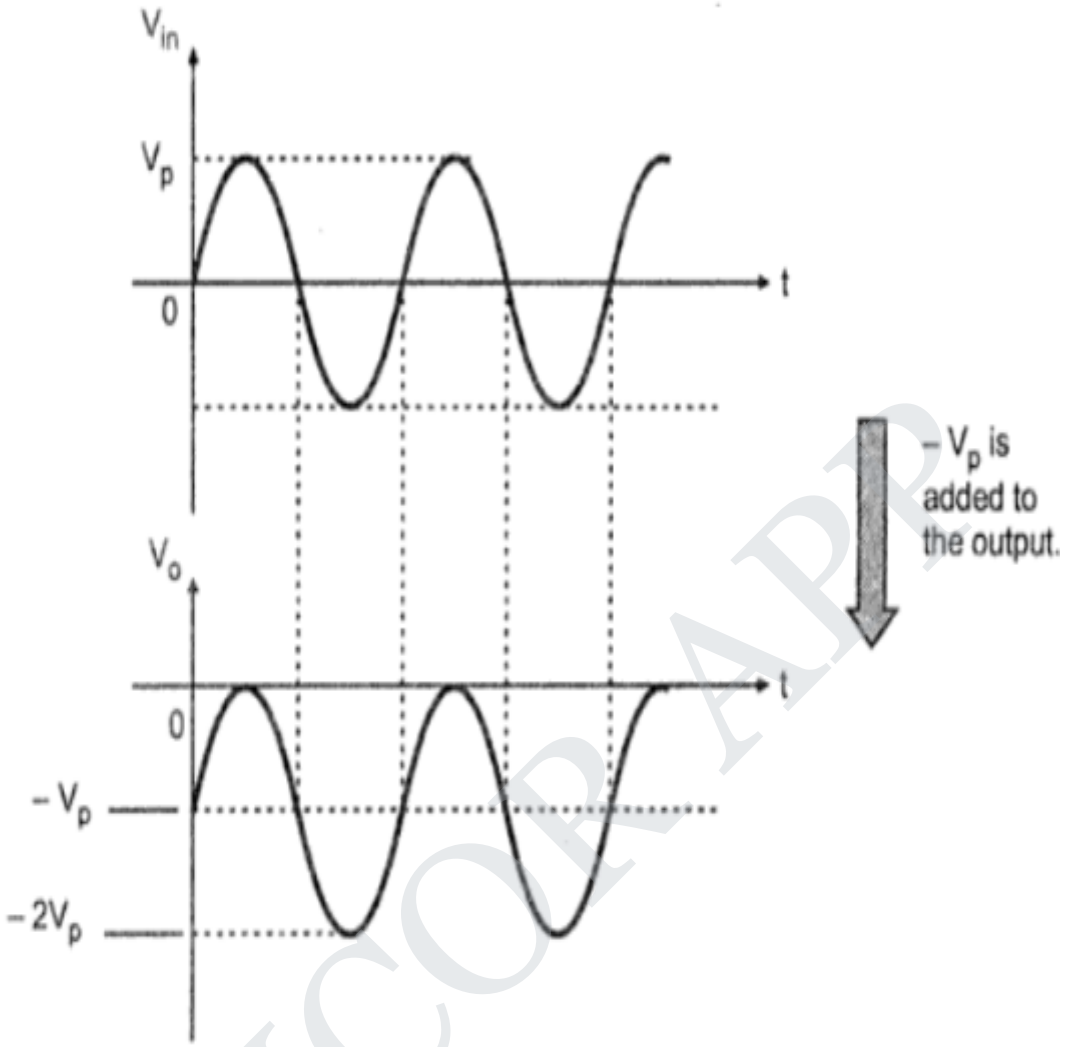


Fig. Waveforms for negative clamper circuit

Similar to a positive clamper , by adding a potentiometer at the non-inverting terminal , the waveform can rest on **non-zero DC level determined by -V_{REF}.**

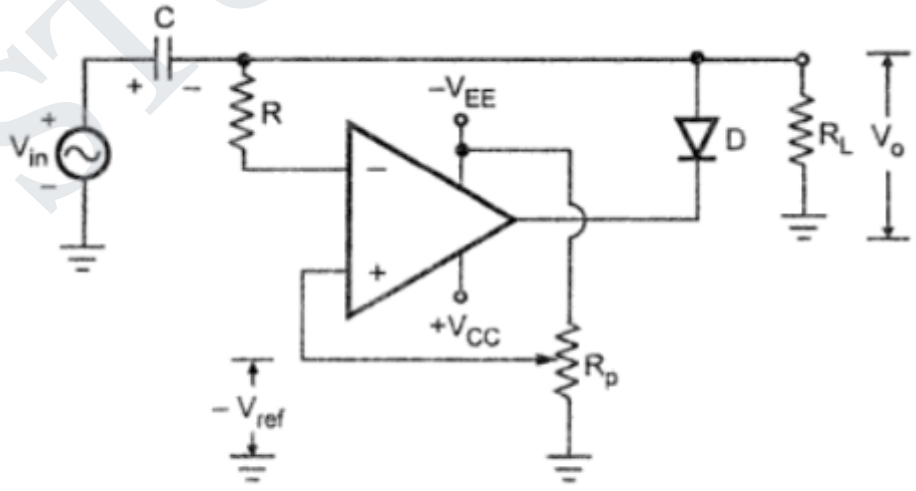


Fig. 4.166 Negative clamper circuit

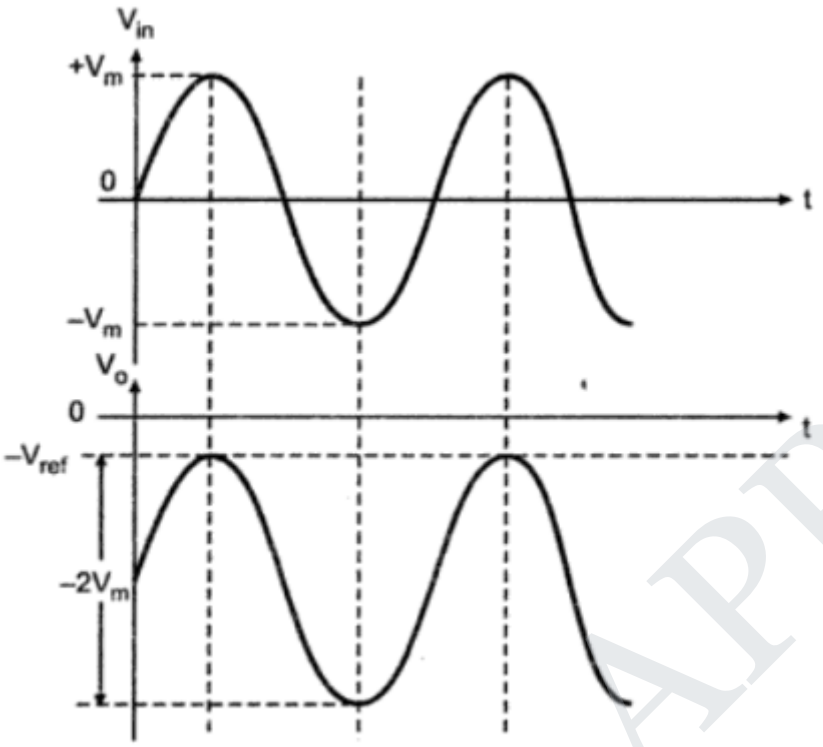


Fig. 4.167 Waveforms for negative clamper circuit

UNIT IV SPECIAL ICs **9**

Functional block, characteristics of 555 Timer and its PWM application - IC-566 voltage controlled oscillator IC; 565-phase locked loop IC, AD633 Analog multiplier ICs.

Part-A(10×2 = 20 marks)

1. A PLL frequency multiplier has an input frequency "f" and a decade counter is included in the loop? What will be the frequency of PLL output?

The divide-by-10 or decade counter when inserted between VCO(Voltage Controlled Oscillator) and the phase detector , produces an output $f_O = 10 \times f$, at the output of PLL.

2 . What are the advantages of variable transconductance technique?

→ Good accuracy
→ Economical
→ Simple to integrate
→ Higher bandwidth

3. Define duty cycle in astable multivibrator using IC555.

Duty cycle D of the astable multivibrator circuit is the ratio of ON time of the circuit to the total time period of the circuit.

$$D = \frac{t_{ON}}{T} \times 100 = \frac{t_{ON}}{t_{ON} + t_{OFF}} \times 100 = \frac{R_B}{R_A + 2R_B} \times 100$$

Where $t_{ON} = 0.69\ R_B C$

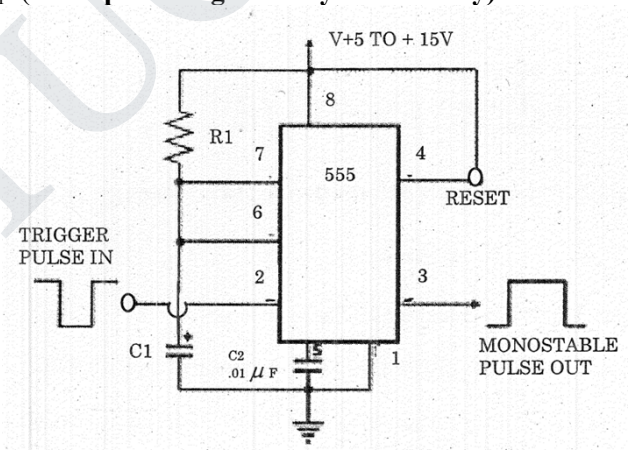
$t_{OFF} = 0.69(R_A + R_B)C$

$T = t_{ON} + t_{OFF}$

4. List the applications of PLL.

- Frequency Multiplication and Division
- Frequency Translation
- AM Detection
- FM Demodulation
- FSK(Frequency Shift Keying) Demodulator

5. In the Monostable multivibrator of below figure circuit , $R_1 = 100\ k\Omega$ and the time delay T = 100 ms. Calculate the value of C_1. **(Example 8.1 Pg 315 Roy Choudhury)**



Solution:

$$C = \frac{T}{1.1 \times R} = \frac{100 \times 10^{-3}}{1.1 \times 100 \times 10^{3}} = 0.9\ \mu F.$$

8. Define capture range , lock-in range and pull-in time.

Capture Range : Range of frequencies over which a PLL(Phase Locked Loop) can **acquire lock with an input signal**; This parameter is usually expressed as percentage of the VCO(Voltage Controlled Oscillator) frequency f_O.

Lock Range : Range of frequencies over which a PLL(Phase Locked Loop) can **maintain an acquired lock with an input signal**; This parameter is usually expressed as percentage of the VCO(Voltage Controlled Oscillator) frequency f_O.

Pull-in Time: Total time taken by PLL to establish a lock ; It depends on

(i) Initial Phase Difference between two signals

(ii) Initial Frequency difference between two signals

(iii) Overall Loop Gain

(iv) Loop Filter Characteristics

9. What is analog multiplier IC ? Where it is used?

Analog multiplier ICs such as AD533 , AD534 , AD633 takes two input voltages namely V_X and V_Y and provides an output as the ratio of product of inputs to the reference voltage V_{REF}.

$$V_O = \frac{V_x V_Y}{V_{REF}}$$

Analog multipliers are used in following applications:

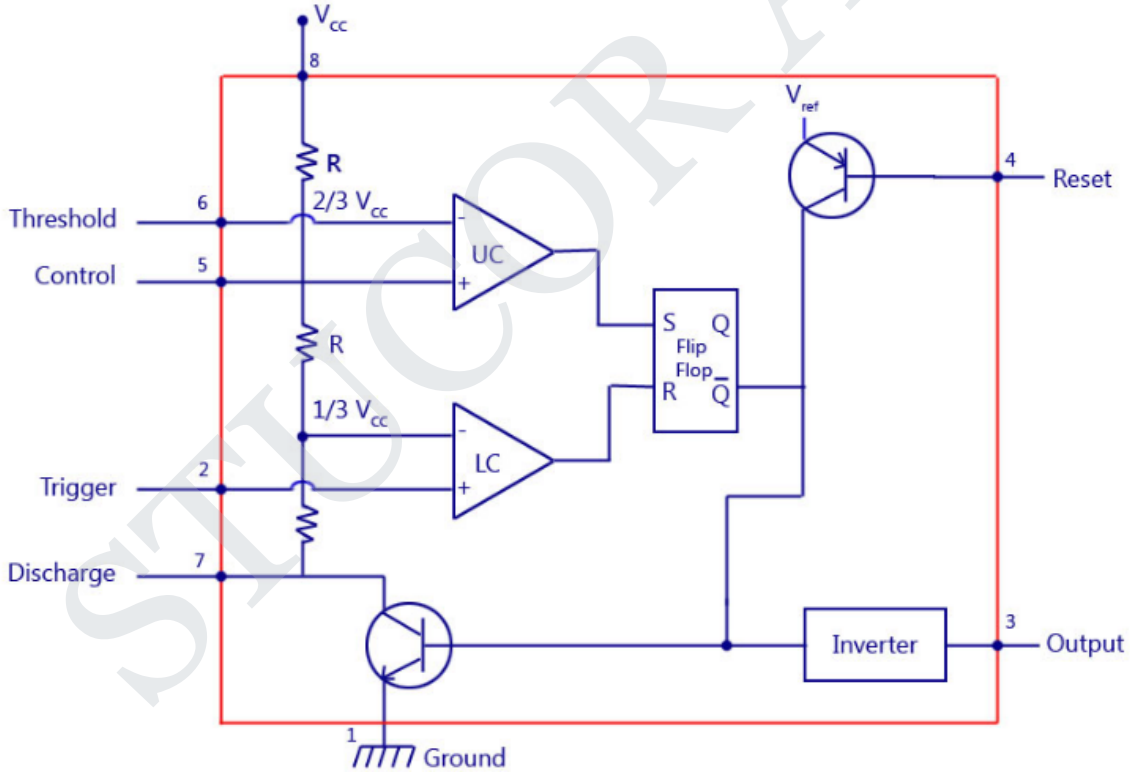
→ **Frequency Doubling**

→ **Real Power Measurement**

→ **Detecting Phase Angle difference between two signals of equal frequency**

→ **Multiplying two signals**

10 . Draw the functional block diagram of 555 Timer IC.

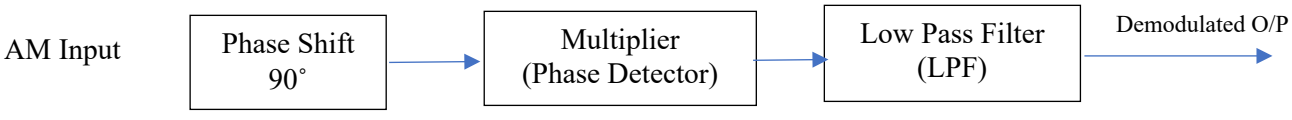


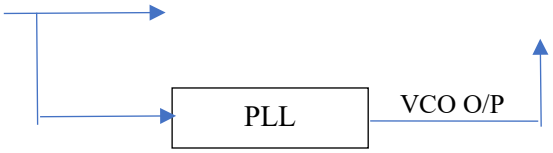
11. Define PLL

PLL(Phase Locked Loop) is an electronic circuit with a voltage oscillator or voltage controlled oscillator to match the phase and frequency of an input signal. They are frequently used for phase modulation , frequency modulation.

12. Draw the circuit diagram of a PLL circuit used as an AM modulator.

PLL circuit is used as an AM Demodulator and not as AM modulator.





13. What are the features of VCO.

- Maximum operating voltage 10 V to 24 V
- High temperature stability
- Excellent power supply rejection
- Operating temperature 0˚C to 70˚C.

14. . Determine the frequency of oscillations , if the duty cycle D = 20% and the ON period T_{ON} = 2 ms.

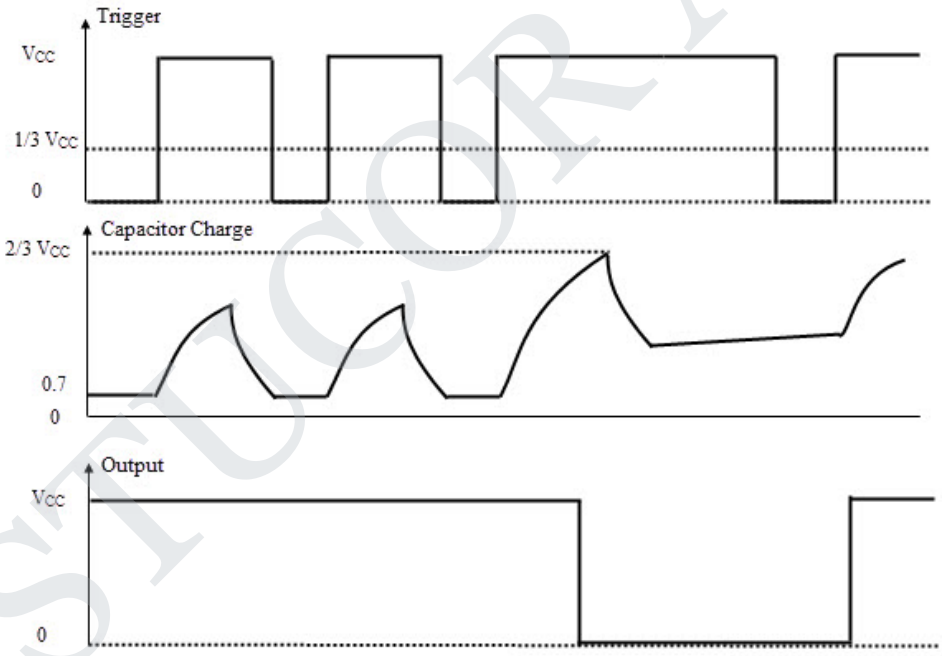
$$\textbf{\% Duty Cycle} = \frac{T_{ON}}{T} \times 100$$

$$20 = \frac{2 \times 10^{-3}}{T} \times 100$$

$$T = \frac{1}{f} = \frac{2 \times 10^{-3} \times 100}{20} = 0.01 \text{ s}$$

$$\text{Therefore } f = \frac{1}{T} = \frac{1}{0.01} = 100 \text{ Hz}$$

15. Draw the output of a missing pulse detector



16. Define duty cycle in astable multivibrator using IC 555.

Duty cycle D of the astable multivibrator circuit is the ratio of ON time of the circuit to the total time period of the circuit.

$$D = \frac{t_{ON}}{T} \times 100 = \frac{t_{ON}}{t_{ON} + t_{OFF}} \times 100 = \frac{R_B}{R_A + 2R_B} \times 100$$

Where $t_{ON} = 0.69\ R_B C$

$t_{OFF} = 0.69(R_A + R_B)C$

$T = t_{ON} + t_{OFF}$

17. What is Astable Multivibrator ?

Astable Multivibrator or Relaxation Oscillator is a circuit in which the output is neither stable in 0-state nor in 1-state.

18. In a Monostable multivibrator using 555 timer , the component values are R_A = 5.6 Ω and C = 0.068 µF. Find the pulse width period T.

Pulse Width Period , T = 1.1 RC

= 1.1 × 5.6 × 0.068 × 10^{-6}

= 419 ns

Part-B

1. For the VCO circuit , assume R_2 = 2.2 kΩ , R_1 = R_3 = 15 kΩ and C_1 = 0.001 µF. Assume V_{CC} = 12 V. Determine the output frequency , the change in output frequency if modulating input V_C is varied from 7 V to 8 V. **(Example 3.3 Linear Integrated Circuits by S Salivahanan , V S Kanchana Bhaskaran)** (8)

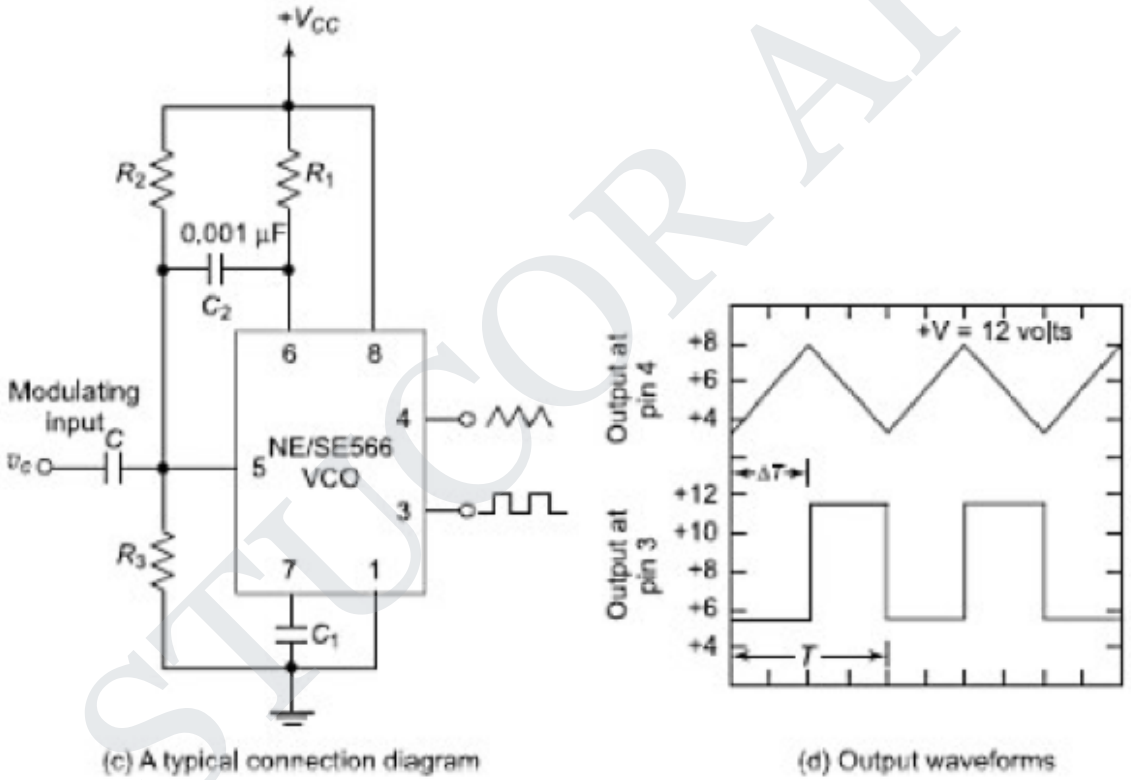
Solution:

The resistors R_2 and R_3 form a potential divider

Therefore $V_C = \frac{V_{CC} \times R_3}{R_2 + R_3} = \frac{12 \times 15 \times 10^3}{2.2 \times 10^3 + 15 \times 10^3}$ = 10.47 V

Therefore the output frequency is $f_{OP} = \frac{2(V_{CC} - V_C)}{R_1 \times C_1 \times V_{CC}} = \frac{2(12 - 10.47)}{15 \times 10^3 \times 0.001 \times 10^{-6} \times 12}$ =

= 17 kHz



(c) A typical connection diagram (d) Output waveforms

(i) For V_C = 7 V

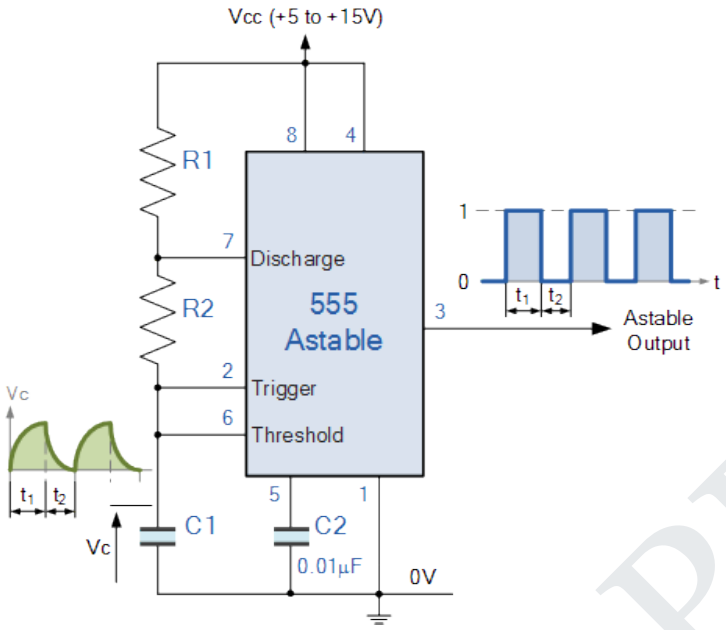
output frequency is $f_{OP} = \frac{2(V_{CC} - V_C)}{R_1 \times C_1 \times V_{CC}} = \frac{2(12 - 7)}{15 \times 10^3 \times 0.001 \times 10^{-6} \times 12}$ = 55.55 kHz

(i) For V_C = 8 V

output frequency is $f_{OP} = \frac{2(V_{CC} - V_C)}{R_1 \times C_1 \times V_{CC}} = \frac{2(12 - 8)}{15 \times 10^3 \times 0.001 \times 10^{-6} \times 12}$ = 44.44 kHz

Hence the change in the output frequency is = 55.55 kHz - 44.44 kHz = 11.11 kHz

2. For a 555 astable circuit , determine the high state time interval , low state time interval , period , frequency and duty cycle. (8)



Derivation:

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{CC} volts is given by

$$V_C = V_{CC}(1-e^{\frac{-t}{RC}})$$

The time t_1 taken by the circuit to charge from 0 to $\frac{2}{3}V_{CC}$ is

$$\left(\frac{2}{3}V_{CC} = V_{CC}(1-e^{\frac{-t_1}{RC}}\right)$$

or $t_1 = 1.09\ RC$

The time t_2 taken by the circuit to charge from 0 to $\frac{1}{3}V_{CC}$ is

$$\frac{1}{3}V_{CC} = V_{CC}(1-e^{\frac{-t_2}{RC}})$$

or $t_2 = 0.405\ RC$

Therefore the time taken by the circuit to charge from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$ is

$$\mathbf{t_{HIGH} = t_1 - t_2}$$
$$\mathbf{= 1.09\ RC - 0.405\ RC = 0.69\ RC}$$
So for the given circuit
$$\mathbf{t_{HIGH} = 0.69(R_1 + R_2)\ C_1 \ldots..(A)\ [High\ Time]}$$

The output is low while the capacitor discharges from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$

$$\frac{1}{3}V_{CC} = \frac{2}{3}V_{CC}(1-e^{\frac{-t}{RC}})$$

Solving we get $t = 0.69\ RC$

So for the given circuit , $\mathbf{t_{LOW} = 0.69\ R_2C_1 \ldots..(B)[Low\ Time]}$

R_1 and R_2 exist in the charging path , R_2 alone exist in the discharge path

Total time , $T = t_{HIGH} + t_{LOW}$

$$\mathbf{= 0.69(R_A + 2\ R_B)\ C \ldots.(C)\ [\ Time\ Period]}$$

$$\mathbf{Frequency\ ,\ f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \ldots.(D)[Frequency]}$$

$$\% \text{ Duty Cycle} = \frac{t_{ON}}{T} \times 100 = \frac{t_{LOW}}{T} \times 100 = \frac{R_B}{R_A + 2R_B} \quad \text{....(E) [Duty Cycle]}$$

(Or)

3. With neat diagram , explain the operation of four quadrant variable transconductance multiplier circuit. (16)

Derivation for Linear Two Quadrant Multiplier:

- The four quadrant variable transconductance multiplier consist of combination of **linearized two quadrant multiplier circuit** and **differential V/I converter.**
- Q_3-Q_4 forms a differential pair to provide variable transconductance and the diode pair Q_1-Q_2 drive the base of the differential pair Q_3-Q_4 in Fig. a and b.
- The diode pair Q_1-Q_2 are matched transistors.
- Apply KVL to **linear two quadrant multiplier circuit**

$$V_{BE1} + V_{BE4} - V_{BE2} - V_{BE3} = 0$$

$$\text{Therefore } V_{BE1} - V_{BE2} = V_{BE3} - V_{BE4}$$

- For the matched transistors Q_1-Q_2 , change in V_{BE} is proportional to the log ratio of their currents.

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \quad \alpha \ln \frac{I_1}{I_2} \text{ for } Q_1\text{-}Q_2 \text{ .....(A)}$$

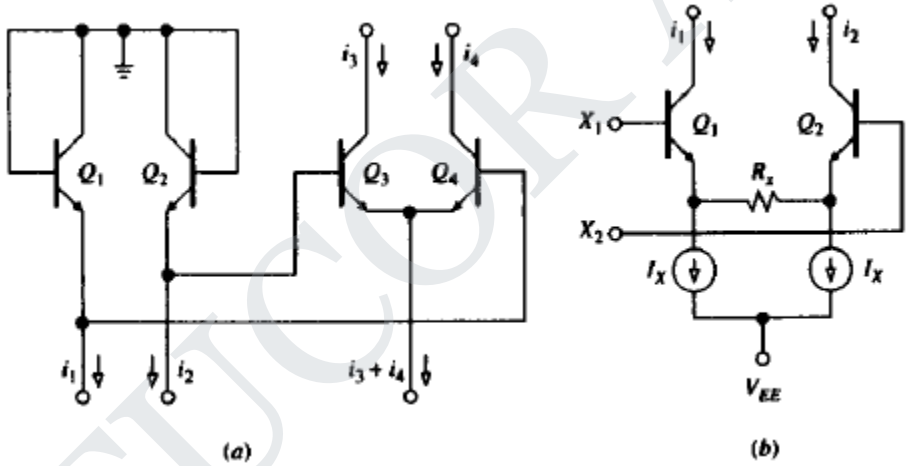


Fig.a **Linear Two Quadrant Multiplier** Fig.b **Differential V/I Converter**

$$\Delta V_{BE} = V_{BE3} - V_{BE4} \quad \alpha \ln \frac{I_3}{I_4} \quad \text{for } Q_3 - Q_4 \text{.....(B)}$$

Equating (A) and (B) we get , $\ln \frac{I_3}{I_4} = \ln \frac{I_1}{I_2}$

$$\text{Therefore } \frac{I_3}{I_4} = \frac{I_1}{I_2}$$

Mathematically it can be written as

$$\frac{I_3 - I_4}{I_3 + I_4} = \frac{I_1 - I_2}{I_1 + I_2}$$

$$\text{Therefore } I_3 - I_4 = \frac{I_1 - I_2}{I_1 + I_2} \times (I_3 + I_4) \text{ .....(B1)}$$

To convert V_1 into $(I_1 + I_2)$ and V_2 into $(I_3 + I_4)$ two separate V/I converters are required.
To convert $(I_3 - I_4)$ into V_O , one I/V converter is required.

Derivation for differential V/I Converter:

Ignoring base currents of $Q_1 – Q_2$ and applying KCL we get,

$$I_1 = I_X + I_{RX} \ldots.(C)$$

$$I_2 = I_X - I_{RX} \ldots.(D)$$

Subtracting (C) and (D) we get

$$I_1 – I_2 = 2\ I_{RX} \ldots.(E)$$

Let V_{E1} and V_{E2} be the emitter voltages of transistors Q1 and Q2.

$$I_{RX} = \frac{V_{E1} - V_{E2}}{R_X} \ldots..(F)$$

Substituting (F) in (E) we get

$$I_1 – I_2 = 2\left(\frac{V_{E1} - V_{E2}}{R_X}\right) \ldots(G)$$

By applying KVL to the differential VI converter Q1-Q2 we get

$$V_{E1} = V_1 – V_{BE1}$$

$$V_{E2} = V_2 – V_{BE2}$$

$$V_{E1} – V_{E2} = (V_1 – V_2) – (V_{BE1} – V_{BE2}) \ldots.(H)$$

$$\text{As } \Delta V_{BE} = \mathbf{V_{BE1} – V_{BE2}} \ \alpha \ln \frac{I_1}{I_2}$$

$$\text{Therefore } V_{E1} – V_{E2} = (V_1 – V_2) - V_T \ln \frac{I_1}{I_2} \ldots(I)$$

Substituting (I) in (G)

$$I_1 – I_2 = 2\frac{(V_1 - V_2)}{R_X} - \frac{2V_T}{R_x}\ln \frac{I_1}{I_2} \ldots..(J)$$

The term of $\frac{2V_T}{R_x}\ln \frac{I_1}{I_2}$ is negligibly small in well designed multiplier and hence neglected.

$$\text{Therefore } I_1 – I_2 = 2\frac{(V_1 - V_2)}{R_X} \ldots.(K)$$

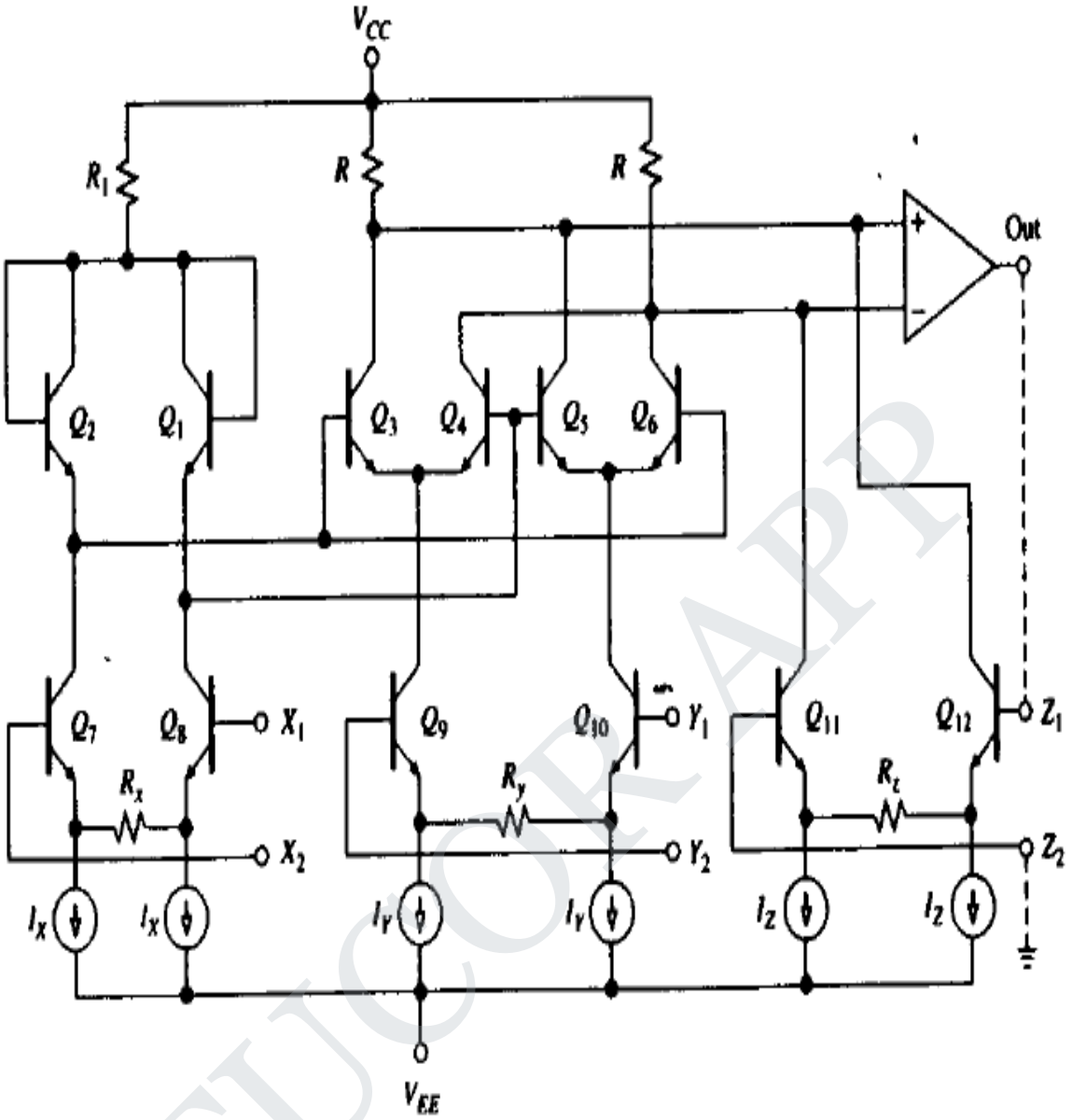


Fig.c Four Quadrant Variable Transconductance Multiplier Circuit

Derivation of Four Quadrant Variable Transconductance Multiplier Circuit:

Substituting (K) in (B1) we get

$$I_3 - I_4 = \frac{2(X_1 - X_2)}{R_X(I_1 + I_2)} \times (I_3 + I_4) \ldots\ldots.(L)$$

From (C) and (D) we get , $I_1 + I_2 = 2I_X$ …….(M)

From Fig.c $I_3 + I_4 = I_9$ (By applying KCL) ….(N)

Substituting (M) and (N) in (L)

$$\frac{2(X_1 - X_2)}{2\,R_X\,I_X} \times (I_9)$$

$$I_3 - I_4 = \frac{(X_1 - X_2)}{R_X\,I_X} \times (I_9) \ldots\ldots(O)$$

From fig. d $I_5 + I_6 = I_{10}$

Similar to (O) $I_6 - I_5 = \frac{I_{10}(X_1 - X_2)}{I_x R_x}$ …. (P)

Subtracting (O) from (P)

$$(I_4 + I_6) - (I_3 + I_5) = \frac{(I_{10} - I_9)\,(X_1 - X_2)}{I_x R_x} \quad \text{.....(Q)}$$

The transistors $Q_9 - Q_{10}$ form another V/I converter

$$I_{10} - I_9 = 2\frac{(Y_1 - Y_2)}{R_Y} \quad \text{.....(R)}$$

Substituting (R) in (Q)

$$(I_4 + I_6) - (I_3 + I_5) = \frac{2(Y_1 - Y_2)\,(X_1 - X_2)}{I_x R_x R_y}$$

The transistor Q_{11}-Q_{12} in the feedback path of OP-AMP form another V/I converter.

$$I_{12} - I_{11} = 2\frac{(Z_1 - Z_2)}{R_Z} \quad \text{.....(S)}$$

When combined with OP-AMP it forms a I/V converter.

Applying KVL we can write

$V_B = V_{CC} - R_L\,(I_3 + I_5 + I_{12})$ ……(T)

$V_A = V_{CC} - R_L\,(I_4 + I_6 + I_{11})$ ……(U)

V_A and V_B are the potentials at the input terminals of OP-AMP. For an OP-AMP , the two input terminals are at same potential due to **virtual ground**.

Therefore $V_{CC} - R_L\,(I_3 + I_5 + I_{12}) = V_{CC} - R_L\,(I_4 + I_6 + I_{11})$

$I_3 + I_5 + I_{12} = I_4 + I_6 + I_{11}$

$(I_4 + I_6) - (I_3 + I_5) = I_{12} - I_{11}$

$$\frac{2(Y_1 - Y_2)\,(X_1 - X_2)}{I_x R_x R_y} = 2\frac{(Z_1 - Z_2)}{R_Z}$$

Therefore $K\,(X_1 - X_2)\,(Y_1 - Y_2) = Z_1 - Z_2$

Where $K = \frac{R_Z}{I_x R_x R_y}$

General value of K = 0.1

Let $(X_1 - X_2) = V_1$

$(Y_1 - Y_2) = V_2$

$(Z_1 - Z_2) = V_O$

Then $V_O = K\,V_1\,V_2$

4. With the help of neat internal functional diagram explain the working of IC 555 as astable multivibrator. (10)

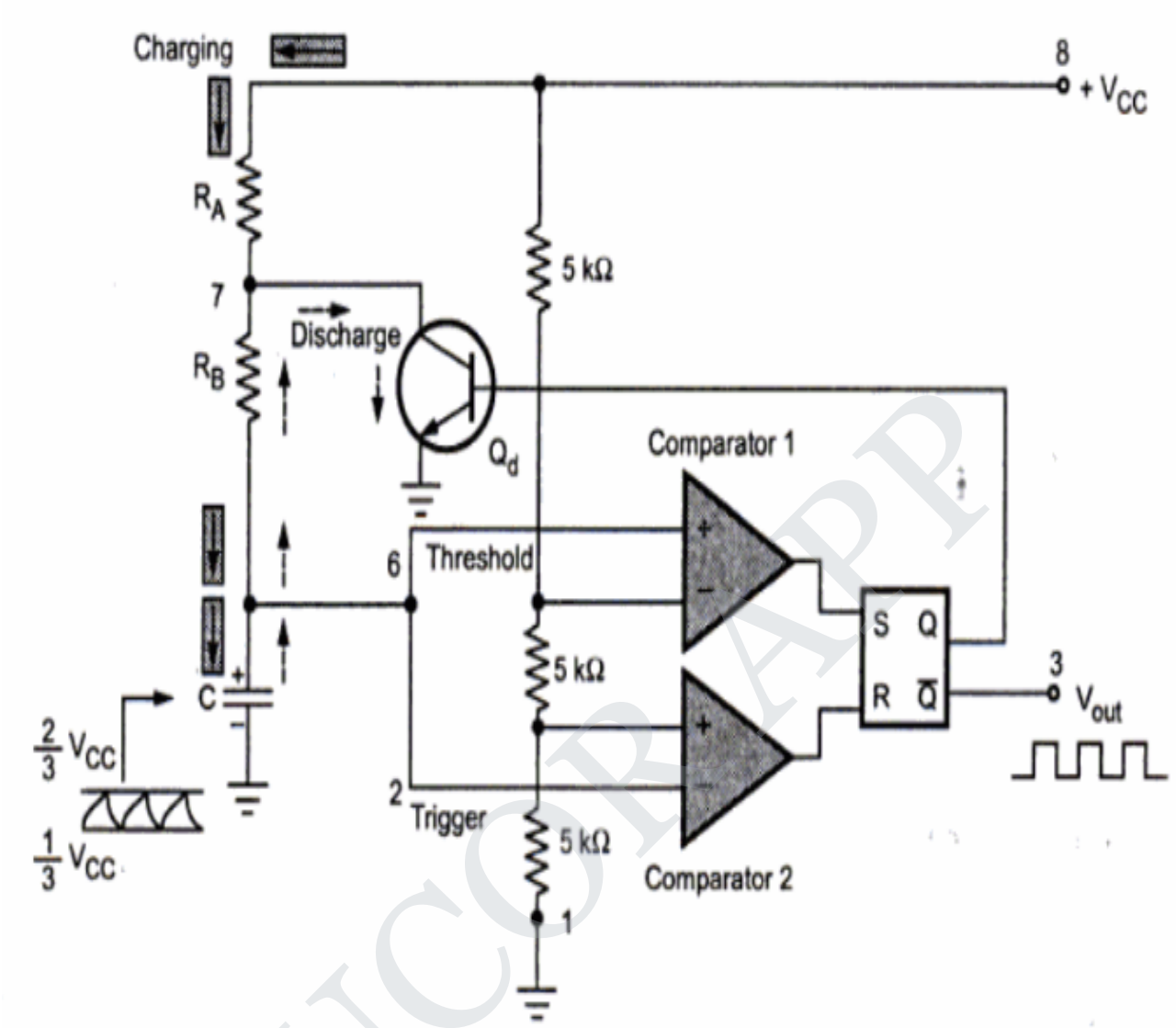


Fig. IC 555 Timer as **Astable Multivibrator**

- **Astable Multivibrator is also called FREE RUNNING NON-SINUSOIDAL OSCILLATOR**.
- **No stable state exist for the circuit**. State of the circuit alternates repeatedly.

Operation:

- The voltage across the capacitor is called **trigger voltage**.
- Q output of SR flip-flop = 1 during set operation. Transistor Q_D driven into saturation and capacitor C gets discharged through Q_D and R_B.
- While discharging when voltage across capacitor = $V_{CC}/3$, comparator 2 output becomes high. As a result SR flip is reset (i.e. Q output of SR flip-flop =0). Transistor Q_D is driven into cut-off.
- As a result , the capacitor starts charging to V_{CC} through R_A , R_B. Now the voltage across the capacitor is called **threshold voltage.** If the threshold voltage exceeds $2V_{CC}/3$, comparator 1 output goes high which sets the Q output of SR flip-flop = 1.
- Charging time constant = $(R_A + R_B)$ C ; Discharging time constant = R_B C.
- Therefore when the capacitor is charging **output is high while when the capacitor is discharging output is low generating a RECTANGULAR WAVE.**

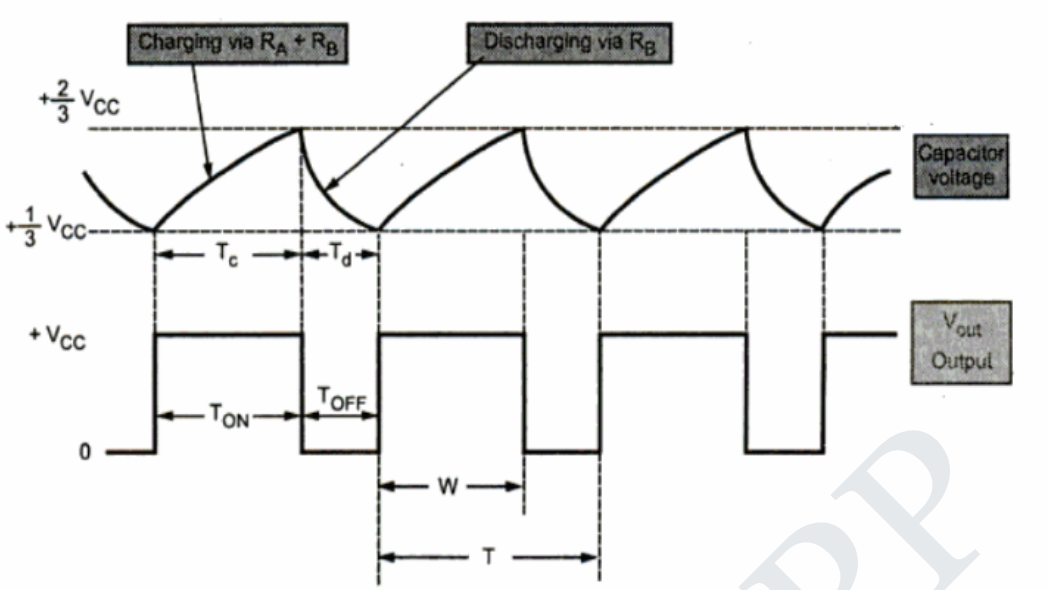


Fig. 4.24 Waveforms of astable operation

5. In the astable multivibrator using IC 555 timer , $R_A = 2.2\ k\Omega$, $R_B = 6.8\ k\Omega$,and C= 0.01 µF. Calculate t_{HIGH} , t_{LOW} , free running frequency and Duty cycle. (6)

Solution:

$$t_{HIGH} = 0.692(R_A + R_B)\ C = 0.693 \times 9 \times 10^3 \times 0.01 \times 10^{-6} = \mathbf{62.37\ \mu s}$$

$$t_{LOW} = 0.692\ R_B\ C = 0.693 \times 6.8 \times 10^3 \times 0.01 \times 10^{-6} = \mathbf{47.124\ \mu s}$$

$$T = t_{HIGH} + t_{LOW} = \mathbf{109.494\ \mu s}$$

$$f = 1/T = \mathbf{9.133\ kHz}$$

$$\%\ D = \frac{t_{HIGH}}{T} \times 100 = \frac{62.37 \times 10^{-6}}{109.494 \times 10^{-6}} = \mathbf{56.962\%}$$

6. Explain the working of voltage controlled oscillator and derive its output frequency

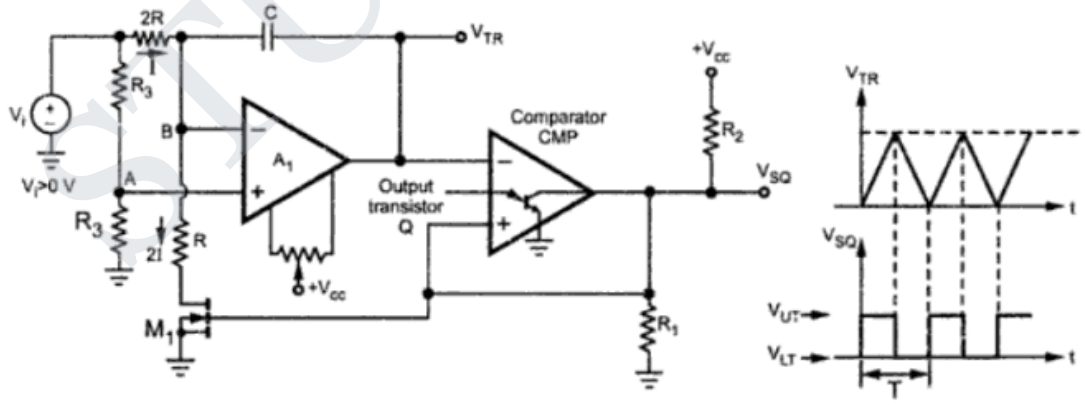


Fig. 5.8 Voltage controlled oscillator circuit

Operation:

- A VCO**(Voltage Controlled Oscillator)** is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage.
- Applied voltage is called **control voltage**. In VCO , frequency of generated oscillations controlled by control voltage. Hence VCO is also called **V/F (Voltage-to-Frequency) Converter**.

- Generally VCO generates **square and triangular waves**.
- The OP-AMP A_1 acts as a **V/I(Voltage to Current) Converter circuit i.e. Current through capacitor C is proportional to input voltage V_I** . The charging and discharging of the capacitor generates **square and triangular waveforms. For this current direction through capacitor is controlled by NMOS switch** M_1.
- The NMOS switch is controlled by a **Schmitt Trigger Comparator.** The square wave is obtained at the terminal V_{SQ} and triangular wave is obtained at the terminal V_{TR}.
- V_{SQ} connected to the **non-inverting terminal of comparator** determines the **upper(V_{UT}) and lower threshold(V_{LT}) levels of the comparator**.
- When V_{SQ} is low , the NMOS switch is OFF and the resistor R is floating. Therefore the entire current $I = V_I / 4R$, has to pass through the capacitor and the voltage V_{TR} starts to ramp down.
- When V_{TR} becomes zero , the comparator changes its state and output V_{SQ} becomes high. Due to this NMOS switch turns ON and the resistor R is grounded. The current through R now is 2I. Out of 2I , I is supplied by 2R and remaining I is supplied by capacitor C. Thus the direction of current through capacitor reverses. Therefore V_{TR} starts tor ramp up.
- Thus the ramp-up and ramp down cycles of triangular waveform continues.

The period of oscillation is determined by equating the charge expressions,

$$C\Delta V = I\Delta t$$

During any half cycle,

$$\Delta V = V_{UT} - V_{LT}$$

$$I = \frac{V_i}{4R}$$

and $$\Delta t = \frac{T}{2}$$

$$\therefore \quad C(V_{UT} - V_{LT}) = \frac{V_i}{4R} \times \frac{T}{2}$$

$$\therefore \quad T = \frac{4RC \times 2[V_{UT} - V_{LT}]}{V_i}$$

$$\therefore \quad f = \frac{1}{T} = K_v V_i \qquad \text{... (5)}$$

where $$\boxed{K_v = \frac{1}{8RC[V_{UT} - V_{LT}]}} \qquad \text{.. (6)}$$

7. Explain how frequency multiplication done using PLL

(Or)

Briefly explain the functional block diagram of NE-565 PLL IC to operate as a frequency divider

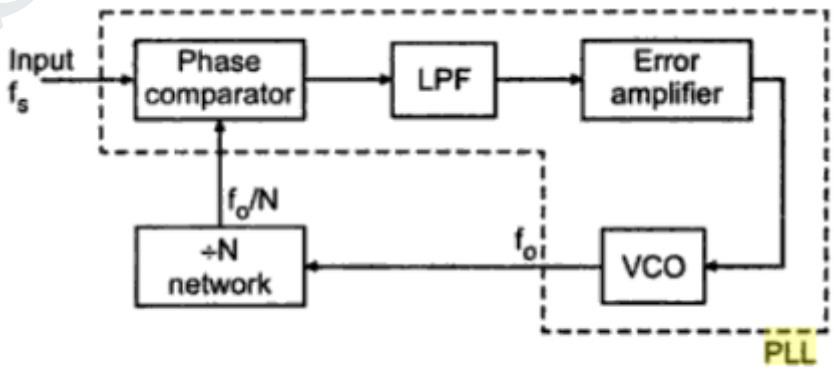


Fig. 5.24 Block diagram of frequency multiplier

- A frequency multiplier is a circuit which provides an output signal whose frequency depends on input signal frequency.
- A divide by N network (COUNTER) is inserted between VCO output and Phase comparator input.
- The output of the divide by N network is locked to the input frequency.
- Therefore in locked state , the VCO output frequency , $f_O = N f_I$
- By selecting proper divide-by-N network , we can obtain desired frequency multiplication.

8. Discuss the operation of a FSK generator using 555 timer (6)

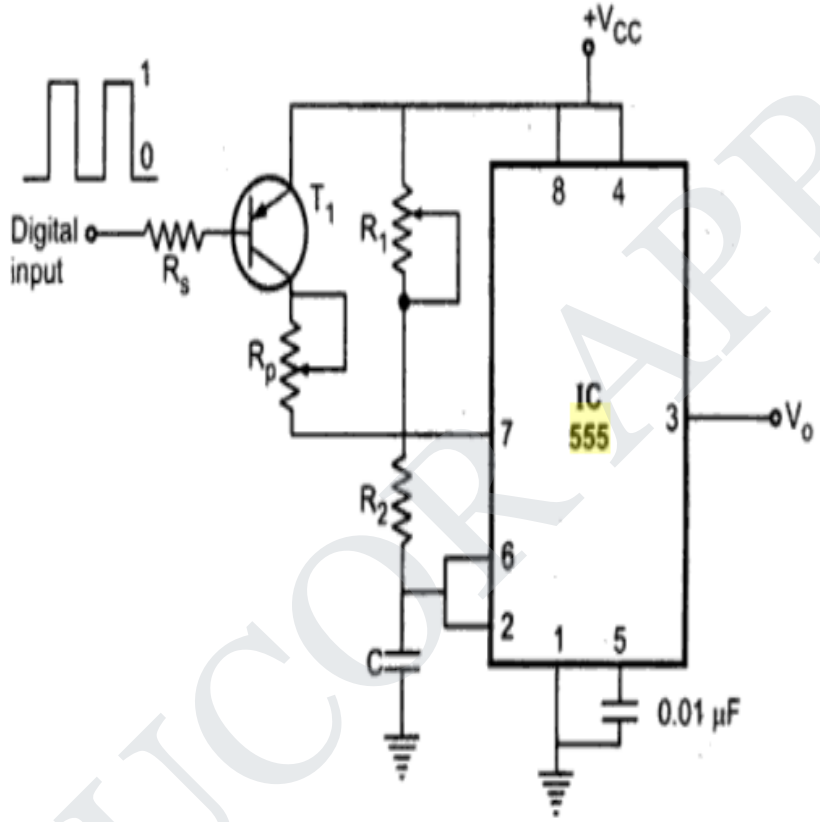


Fig. 7.30 FSK generator

- Two separate carrier frequencies used : One for logic '1' and another for logic '0' for transmitting and receiving binary data. This is called **Frequency Shift Keying.**
- At the receiving end the carrier frequencies are converted into 0s and 1s to get the original binary data.
- When digital input is HIGH(logic 1) , transistor T1 is OFF and 555 timer works in **normal astable mode.**The frequency of the output waveform is given by

$$f_o = \frac{1.45}{(R_1 + 2R_2)\,C}$$

- When digital input is LOW(logic 0) , transistor T1 is ON and connects the resistance R_P parallel to R_1. The frequency of the output waveform is given by

$$f_o = \frac{1.45}{[(R_1 \parallel R_p) + 2R_2]\,C}$$

10. Briefly explain the difference between two operating modes of 555 timer

Astable Multivibrator Mode

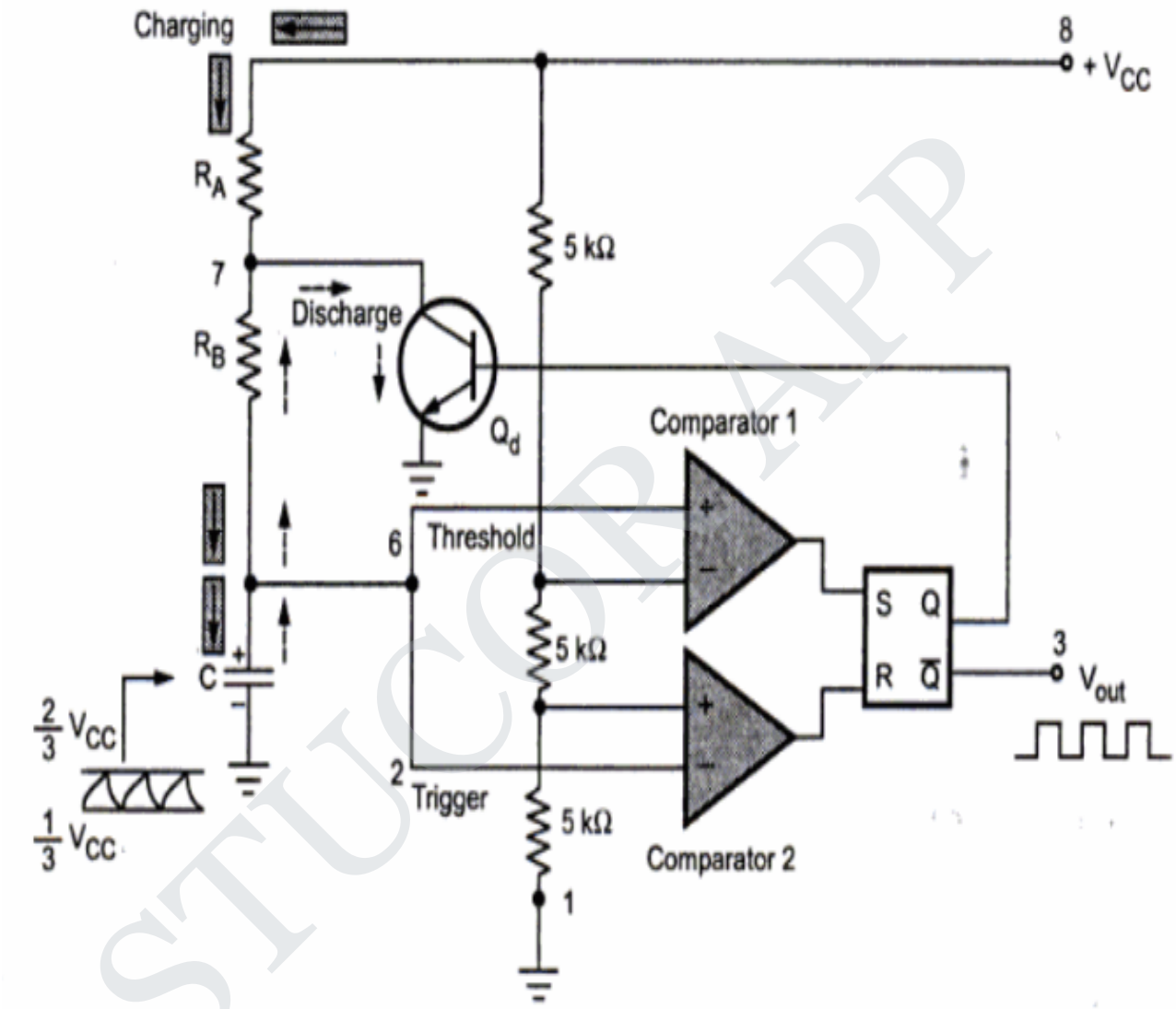


Fig. IC 555 Timer as **Astable Multivibrator**

- **Astable Multivibrator is also called FREE RUNNING NON-SINUSOIDAL OSCILLATOR**.
- **No stable state exist for the circuit**. State of the circuit alternates repeatedly.

Operation:

- The voltage across the capacitor is called **trigger voltage**.
- Q output of SR flip-flop = 1 during set operation. Transistor Q_D driven into saturation and capacitor C gets discharged through Q_D and R_B.
- While discharging when voltage across capacitor = $V_{CC}/3$, comparator 2 output becomes high. As a result SR flip is reset (i.e. Q output of SR flip-flop =0). Transistor Q_D is driven into cut-off.

- As a result , the capacitor starts charging to V_{CC} through R_A , R_B. Now the voltage across the capacitor is called **threshold voltage.** If the threshold voltage exceeds $2V_{CC}/3$, comparator 1 output goes high which sets the Q output of SR flip-flop = 1.
- Charging time constant = $(R_A + R_B)$ C ; Discharging time constant = R_B C.
- Therefore when the capacitor is charging **output is high while when the capacitor is discharging output is low generating a RECTANGULAR WAVE.**

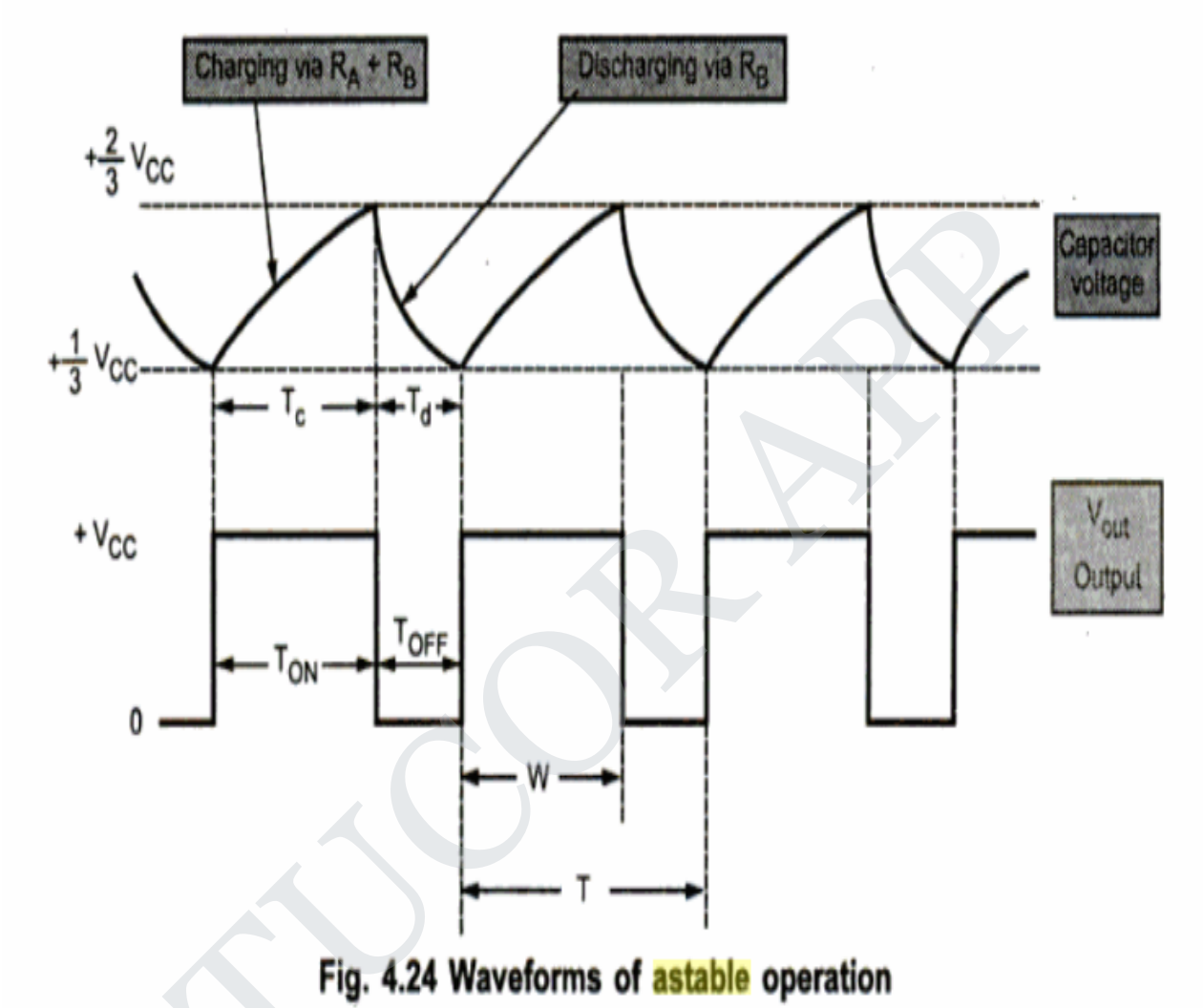


Fig. 4.24 Waveforms of astable operation

Monostable Multivibrator Mode

- **Monostable Multivibrator is also called ONE SHOT MULTIVIBRATOR.**
- **Only one stable state exist for the circuit.** When the trigger is applied , it produces a pulse at the output and returns back to its stable state.

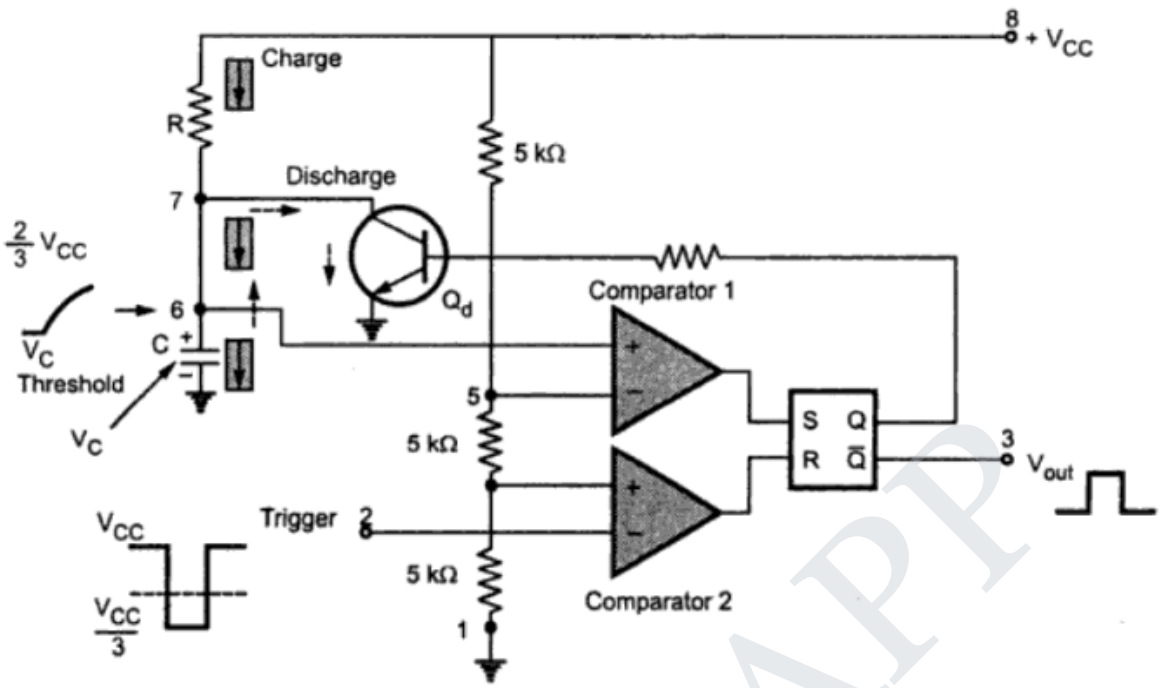


Fig. 4.11 Monostable operation of 555

Operation:

- When trigger voltage is less than $V_{CC}/3$, the comparator 2 output goes high. As a result SR flip-flop is reset (i.e. Q output of SR flip-flop =0). Transistor Q_D is driven into cut-off. The capacitor starts charging through R.
- When threshold voltage is greater than $2V_{CC}/3$, the comparator 1 output goes high. As a result SR-flip-flop is set (i.e. Q output of SR flip-flop =1). Transistor Q_D is driven into saturation. The capacitor starts discharging through R.
- Charging time constant = RC.
- Therefore when the capacitor is charging the **output is high while when capacitor is discharging the output is low , generating rectangular waveform.**

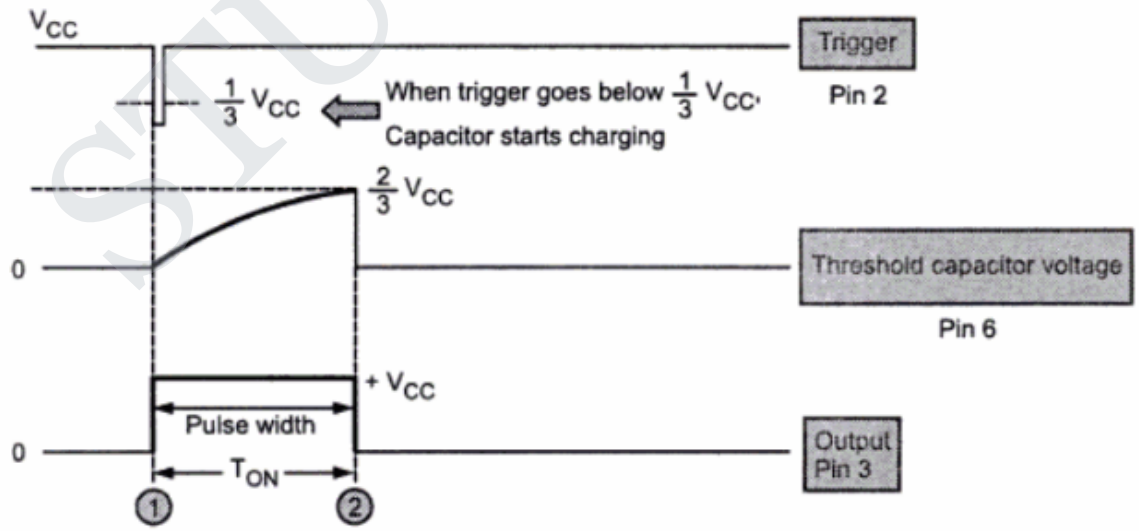


Fig. 12.11 Waveforms of monostable operation

12.6.2 Derivation of Pulse Width

The voltage across capacitor increases exponentially and is given by

$$V_C = V\,(1 - e^{-t/CR})$$

If $V_C = 2/3\ V_{CC}$

then $$\frac{2}{3} V_{CC} = V_{CC}\,(1 - e^{-t/CR})$$

$$\frac{2}{3} - 1 = -e^{-t/CR}$$

$$\frac{1}{3} = e^{-t/CR}$$

$$\therefore \quad -\frac{t}{CR} = -1.0986$$

$$\therefore \quad t = +1.0986\ CR$$

$$\therefore \quad t \approx 1.1\ CR$$

where C in farads, R in ohms, t in seconds.

Thus, we can say that voltage across capacitor will reach 2/3 V_{CC} in approximately 1.1 times, time constant i.e. 1.1 RC

Thus the pulse width denoted as W is given by,

$$W = 1.1\ RC$$

11. List the important features of 555 Timer (6)
    - Wide operating voltage + 5 V to +18 V
    - Sinks or sources 200 mA load current
    - By proper selection of external components , timing interval of the order of minutes and frequencies exceeding several 100 kHz can be achieved.
    - Duty cycle of timer is adjustable.
    - Maximum power dissipation is 600 mW.
    - Temperature stability is 50 ppm/°C.
12. Narrate the process of FSK demodulation using PLL

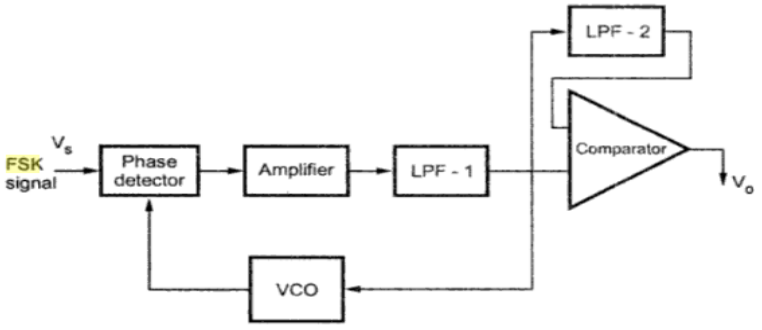


Fig. 5.28 Frequency shift keying demodulator

- Two separate carrier frequencies used : One for logic '1' and another for logic '0' for transmitting and receiving binary data. This is called **Frequency Shift Keying.**
- At the receiving end the carrier frequencies are converted into 0s and 1s to get the original binary data.
- Let the carrier frequency f1 be assigned to '0' and carrier frequency f2 be assigned to '1'. If the PLL is locked into the FSK signal at f1 and f2 , the VCO control voltages are given as follows:

$$V_{C1} = (f_1 - f_o) / K_v$$

$$V_{C2} = (f_2 - f_o) / K_v$$

K_V – Voltage to frequency transfer coefficient of VCO.

The difference between two control voltage levels are given as follows

$$\Delta V_C = (f_2 - f_1) / K_v$$

The reference voltage for the comparator is adjusted between V_{C1} and V_{C2} . For V_{C1} , the comparator gives an output of '0' ; For V_{C2} , the comparator gives an output of '1'.

13. Explain the operation of astable multivibrator using op-amp

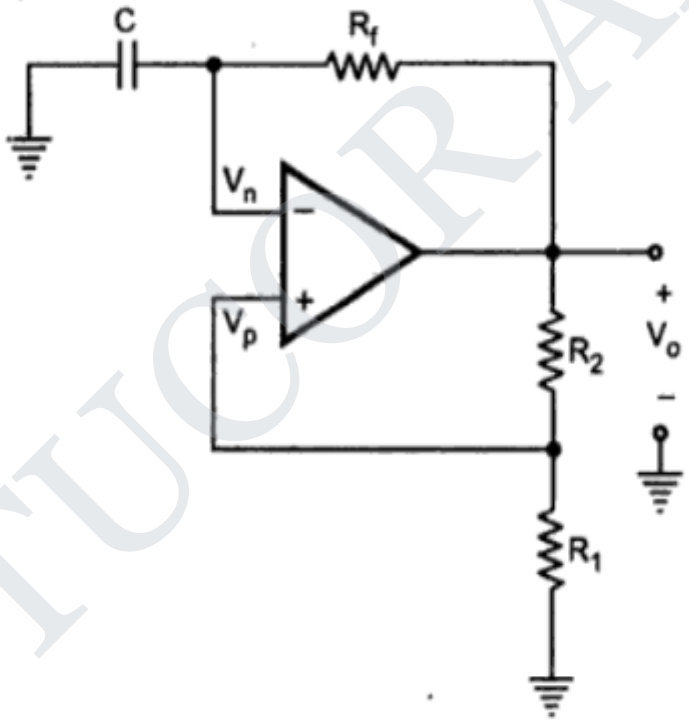


Fig. 3.70 Astable multivibrator using op-amp

The comparator and resistors R_1 and R_2 form a **inverting Schmitt Trigger**

When power is turned ON , the output voltage swings between $+V_{SAT}$ and $-V_{SAT}$. When $V_O = +V_{SAT}$, $V_P = V_{UT}$ and capacitor starts charging to $+V_{SAT}$ through feedback resistor R_F.

$$V_{UT} = \frac{R_1 \cdot (+V_{sat})}{R_1 + R_2}$$

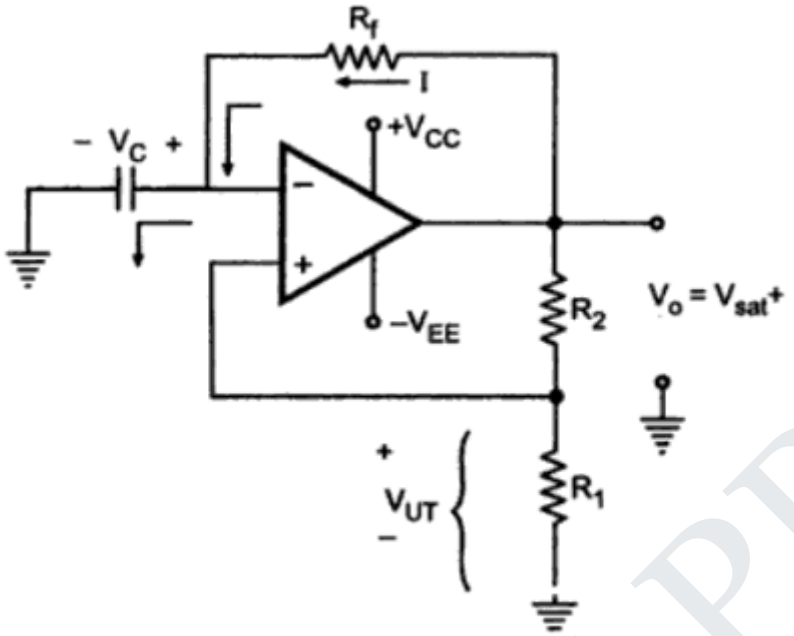


Fig. 3.71 (a) When $V_o = +V_{sat}$, capacitor charges towards V_{UT}

As $V_C > V_{UT}$, the output voltage V_O switches from $+V_{SAT}$ to $-V_{SAT}$ and $V_P = V_{LT}$. The capacitor starts discharging through R_F . When V_C is more negative than V_{LT} , the output voltage V_O switches from $-V_{SAT}$ to $+V_{SAT}$.

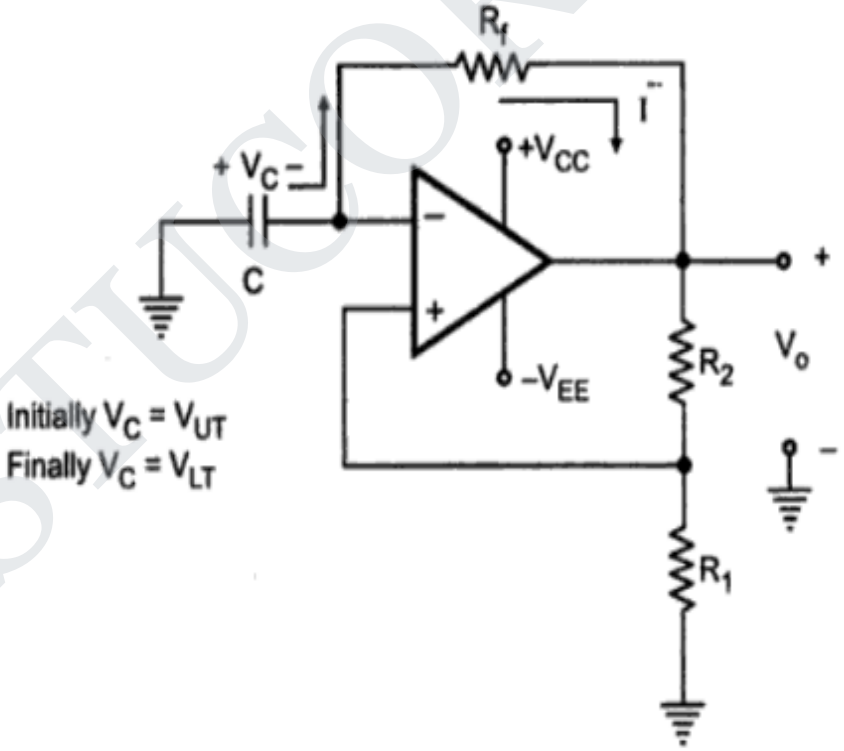


Fig. 3.71 (b) When $V_o = -V_{sat}$, capacitor charges towards V_{LT}

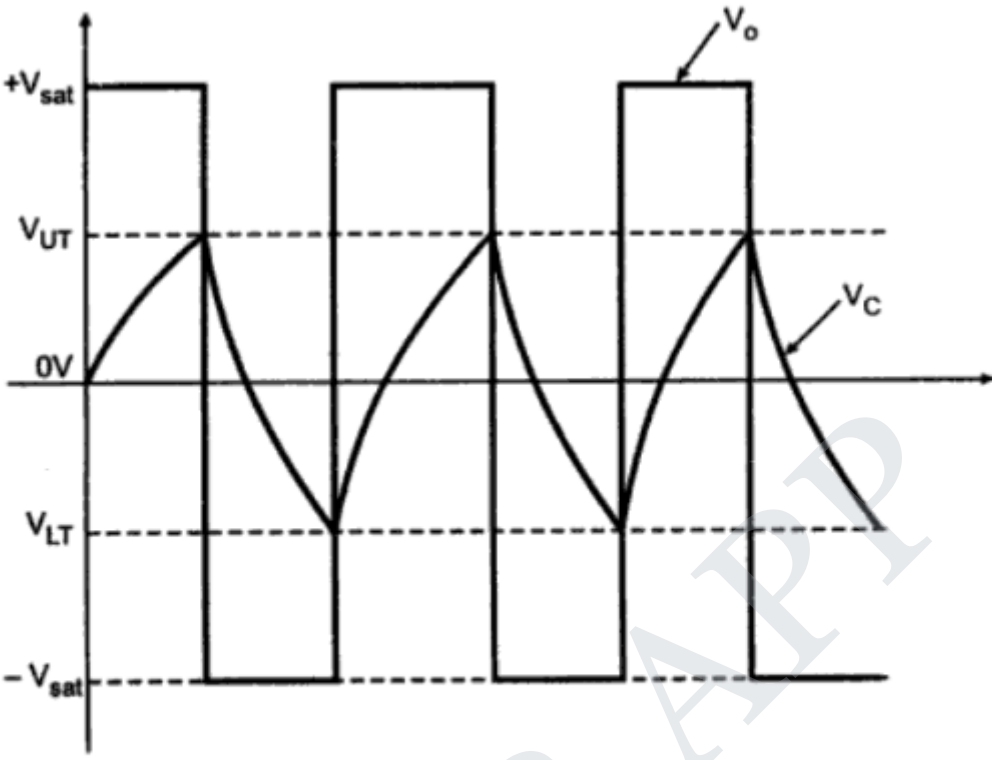


Fig. 3.71 (c) Waveforms

UNIT V APPLICATION ICs **9**

AD623 Instrumentation Amplifier and its application as load cell weight measurement - IC voltage regulators –LM78XX, LM79XX; Fixed voltage regulators its application as Linear power supply - LM317, 723 Variability voltage regulators, switching regulator- SMPS - ICL 8038 function generator IC.

Part-A (10 × 2 = 20 marks)

1. What is meant by thermal shutdown as applied to voltage regulators?

The purpose of thermal shutdown circuit is to sense whether the voltage regulator chip temperature exceeds the design limit or not. If it exceeds , the circuit acts to shutdown the current flowing through pass transistor.

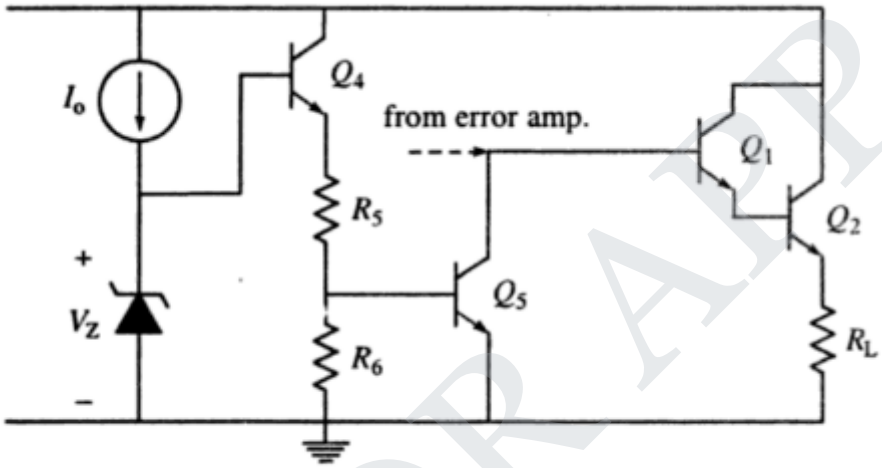
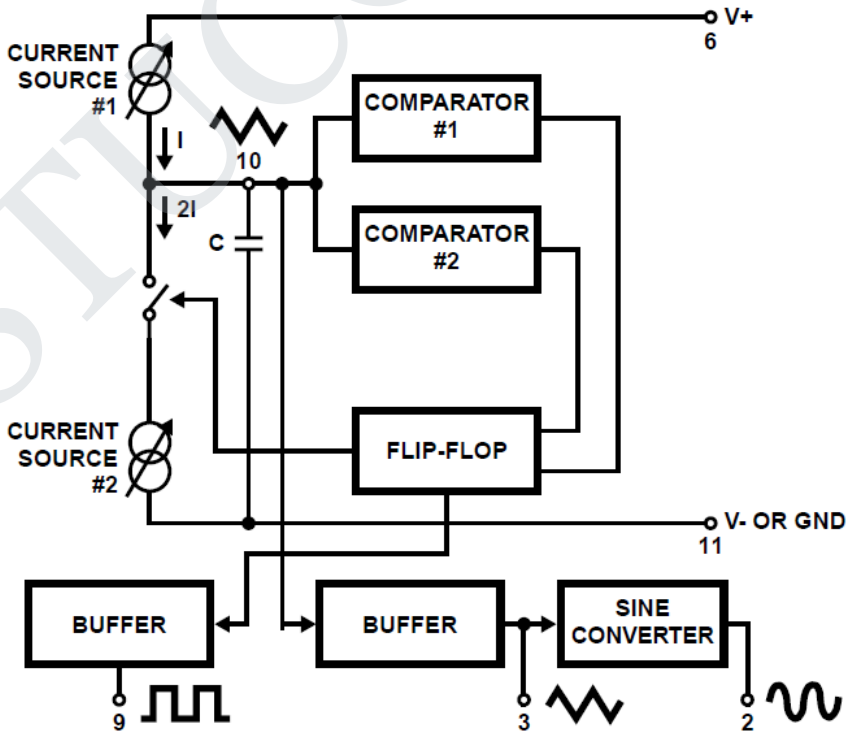


Fig. 7.10 Thermal shutdown circuit.

2. Draw the internal block diagram of function generator IC.



3. What are the limitations of three terminal regulator ?

- Low efficiency if the difference between input and output voltage is large

- Large heat dissipation
- Limited Current Range
- Need external bypass capacitors for stabilization

4. How current boosting is achieved in a 723 IC?
The maximum current that can be provided by IC 723 is 140 mA. For many applications this is not sufficient. The current output from IC 723 can be boosted by adding a BJT pass transistor between the unregulated DC supply , IC 723 and load.

5. Define Line regulation and Load regulation.
Line or Input Regulation is the **percentage change in the output voltage for a given change in the input voltage. It is usually expressed in millivolts or as a percentage of the output voltage. Typical Line regulation IC 7805 is 3 mV.**

Load or Output Regulation is the **percentage change in the output voltage for a given change in the load current. It is usually expressed in millivolts or as a percentage of the output voltage. Typical Line regulation IC 7805 is 15 mV for load current variation between 5 mA to 1.5 A.**

6. What is the purpose of using an external pass transistor with an IC voltage regulator.
The main purpose of the external pass transistor is to **boost the output current of the IC voltage regulator.**

7. Why do switching regulators have better efficiency than the series regulators?
Switching regulator operates the **power series pass transistor** as a **high frequency ON/OFF switch , so that the power transistor does not conduct current continuously. This gives improved efficiency over series or linear regulators.**

8. Give some examples of monolithic IC voltage regulators.
78XX[XX = 5,6,8,12,15,18,24], , 79XX [XX = -5.2,-2,5,6,8,12,15,18,24], 723 are examples of general purpose monolithic voltage regulators. 78XX is **three terminal positive fixed output voltage regulator**. 79XX is a **three terminal negative fixed output voltage regulator**. 723 provides both positive and negative output voltages.

9. What is SMPS?
SMPS(Switched Mode Power Supply) is a power supply that uses a switching regulator to control and stabilize the output voltage by switching on and off the load current.

10. What are the applications of fixed voltage regulator?
- Fixed output regulator
- Adjustable output regulator
- Regulated Dual Supply
- Output Polarity Reversal Protection Circuit

11. Give one comparison for switching regulator and variable voltage regulator.
The main difference between switching regulator provides a constant output voltage whereas the variable voltage regulator provides a adjustable range of output voltage

12. How are frequency of triangular waveform , obtained using ICL 8038 function generator

$$\text{Frequency of triangular waveform of ICL 8038 function generator , } f = \frac{0.33}{RC}$$

13 . What is an isolation amplifier?
Isolation amplifier is a form of differential amplifier that allows measurement of small signals in the presence of high common mode voltage by providing electrical isolation and electrical safety barrier.

14. List the characteristics of opto-coupler

Opto-coupler or opto-isolator has the **following four characteristics:**

- **CTR(Current Transfer Ratio)**
- **Isolation Voltage**
- **Response Time**
- **CMR (Common Mode Rejection)**

15. List the features of opto-coupler ICs

- High collector to emitter voltage
- High isolation voltage between input and output
- Interfaces with common logic families
- Input-output coupling capacitance < 0.5 pF

16. What is a series voltage regulator.

Series voltage regulator or Linear voltage regulator uses a power transistor (called as pass transistor) between the unregulated DC Input voltage and load. The output voltage is controlled by the continuous voltage drop taking place across the pass transistor. The transistor operates as an **amplifier (Linear region or active region).**

17. What is a Load cell?

A load cell is a type of **force transducer** that **converts tension , compression , pressure or torque into a proportional electrical signal that can be measured and standardized.**

18. Give the seven output voltage options available in fixed voltage series regulator.

78XX[XX = 5,6,8,12,15,18,24], , 79XX [XX = -5.2,-2,5,6,8,12,15,18,24]. 78XX is **three terminal positive fixed output voltage regulator**. 79XX is a **three terminal negative fixed output voltage regulator**.

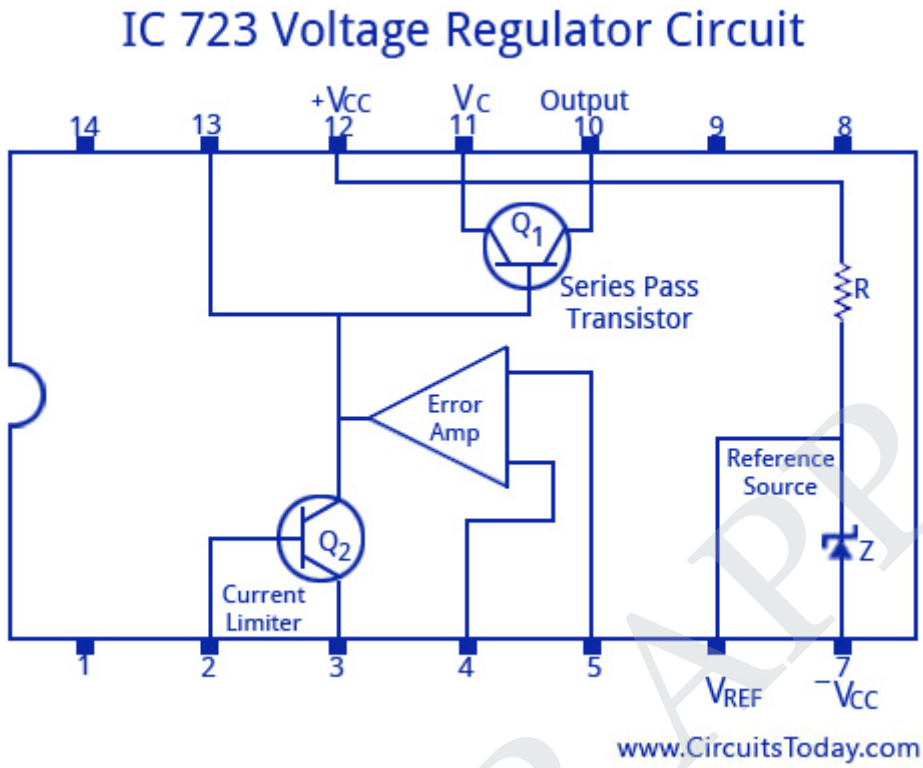
19. What is SMPS?

SMPS(Switched Mode Power Supply) is a power supply that uses a switching regulator to control and stabilize the output voltage by switching on and off the load current.

20. Name the important performance parameters of 3 terminal IC regulators.

- Line/Input Regulation
- Load/Output Regulation
- Ripple Rejection
- Overcurrent Protection
- Thermal Overload Protection

21. Draw the pin diagram of IC 723 regulator.



22. In a linear voltage regulator , the input voltage is 20 V and output voltage is 15 V. For a load current of 1 A , calculate the power dissipated in the series pass element.

Ans.

$V_{IN} = 20$ V ; $V_O = 15$ V , $I_L = 1$ A

Power dissipated in series pass element = $(V_O - V_{IN}) \times I_L$ = Dropout voltage × I_L

$= (20 - 15) \times 1 = 5$ W.

23. State the need for protection diodes in voltage regulators based on LM 317 regulator.

To avoid discharging of capacitors through low current points into the regulator.

Part-B

1. State the advantages of IC voltage regulator. Explain the features and internal structure of general purpose linear IC 723 regulator. Design a regulator using IC 723 to meet the following specifications : $V_0 = 5V$, $I_0 = 100$ mA , $V_{IN} = 15$ V $\pm$ 20% , $I_{SC} = 150$ mA , $V_{SENSE} = 0.7$ V (8)

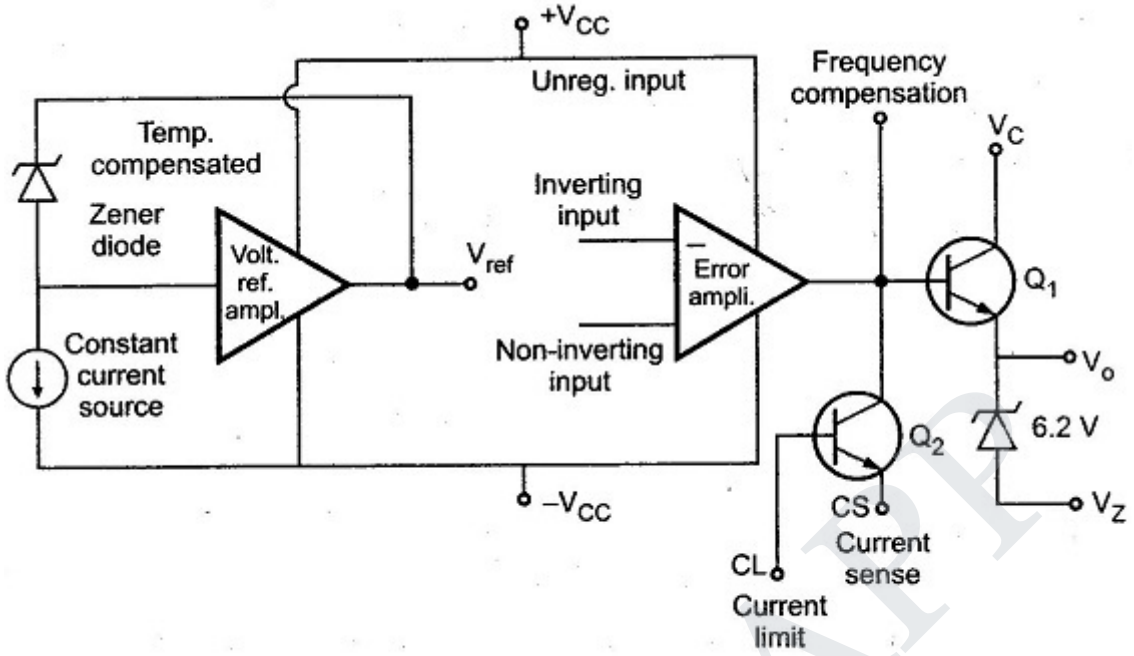
Advantages of IC Voltage Regulator

- Easy to use.
- Greatly simplifies power supply design
- Low cost
- Versatile

Features of IC 723 Variable Voltage Regulator:

- Operates as a voltage regulator between 2 V to 37 V at a load current of 150 mA.
- Can be used at load currents greater than 150 mA using suitable NPN or PNP external pass transistor.
- Good line and load regulation
- Low standby current drain.

Internal Structure of IC 723 Variable Voltage Regulator:



- Temperature compensated Zener diode + Constant Current Source + Reference Amplifier = Reference Source. Value of the reference source is 7.15 V. The reference voltage is connected to **non-inverting terminal of error amplifier**.
- The error amplifier is a **high gain differential amplifier whose inverting terminal connected to the regulated output voltage.**
- The series pass BJT acts as a **variable resistor and has a power dissipation of 800 mW.** The **unregulated power supply input (less than 36 V DC)** is connected to collector of series pass transistor.
- The BJT Q_2 acts as current limiter in case of short circuit condition. The frequency compensation terminal controls the frequency response of error amplifier.
- Since **internal reference voltage is 7 V , two different circuits are required : One for getting regulated output voltage less than 7 V and another for getting regulated output voltage greater than 7 V.**

Problem:

Given:

$V_O = 5$ V , $I_O = 100$ mA , $V_{IN} = 15$ V ± 20% , $I_{SC} = 150$ mA , $V_{SENSE} = 0.7$ V

Solution:

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}} = \frac{0.7}{150 \times 10^{-3}} = 4.67\ \Omega$$

Neglecting input bias current of error amplifier

$$R_1 = \frac{V_{REF} - V_O}{I_D} = \frac{7.15 - 5}{1 \times 10^{-3}} = 2.15\ k\Omega$$ [$V_{REF} = 7.15$ V for IC 723 ; $I_D = 1$ mA]

Therefore $R_1 = 2.2\ k\Omega$ [Standard Resistance or Resistance available commercially]

Now $V_O = V_{REF} \cdot \frac{R_2}{R_1 + R_2}$ i.e. $5 = 7.15 \times \frac{R_2}{2.2\ k\Omega + R_2} \rightarrow R_2 = 5.11\ k\Omega$

Therefore $R_1 = 5.1\ k\Omega$ [Standard Resistance or Resistance available commercially]

$$R_3 = R_1 \parallel R_2 = \frac{2.2\ k\Omega \times 5.1\ k\Omega}{2.2\ k\Omega + 5.1\ k\Omega} = 1.536\ k\Omega$$

Therefore $R_3 = 1.5\ k\Omega$ [Standard Resistance or Resistance available commercially]

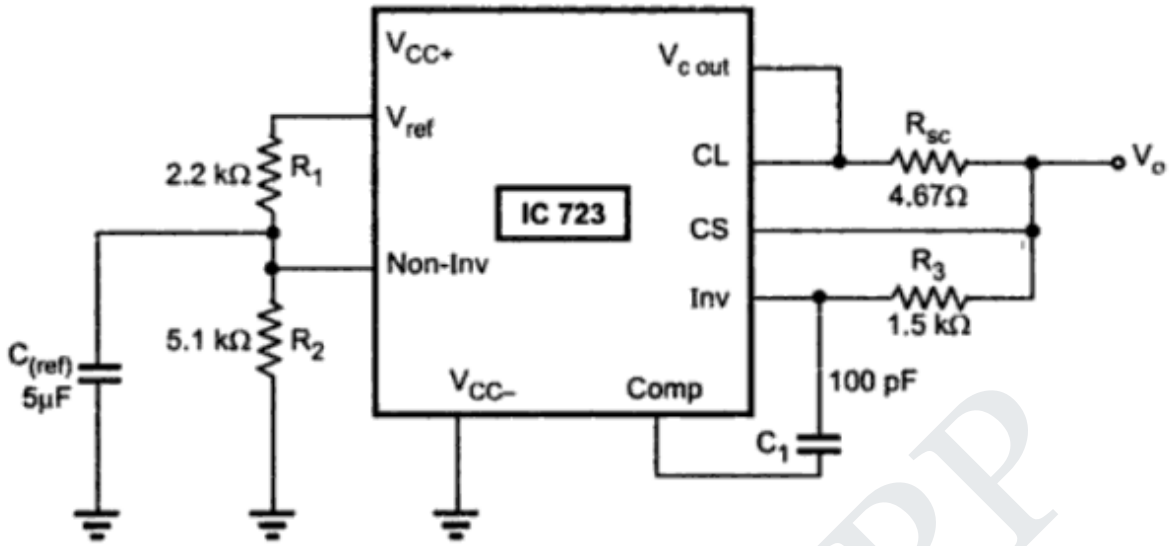


Fig. 7.51

2. With a neat diagram, explain the working of step- down switching regulator

Step down switching regulator (or Buck Type switching regulator or Buck Type SMPS[Switched Mode Power Supply])

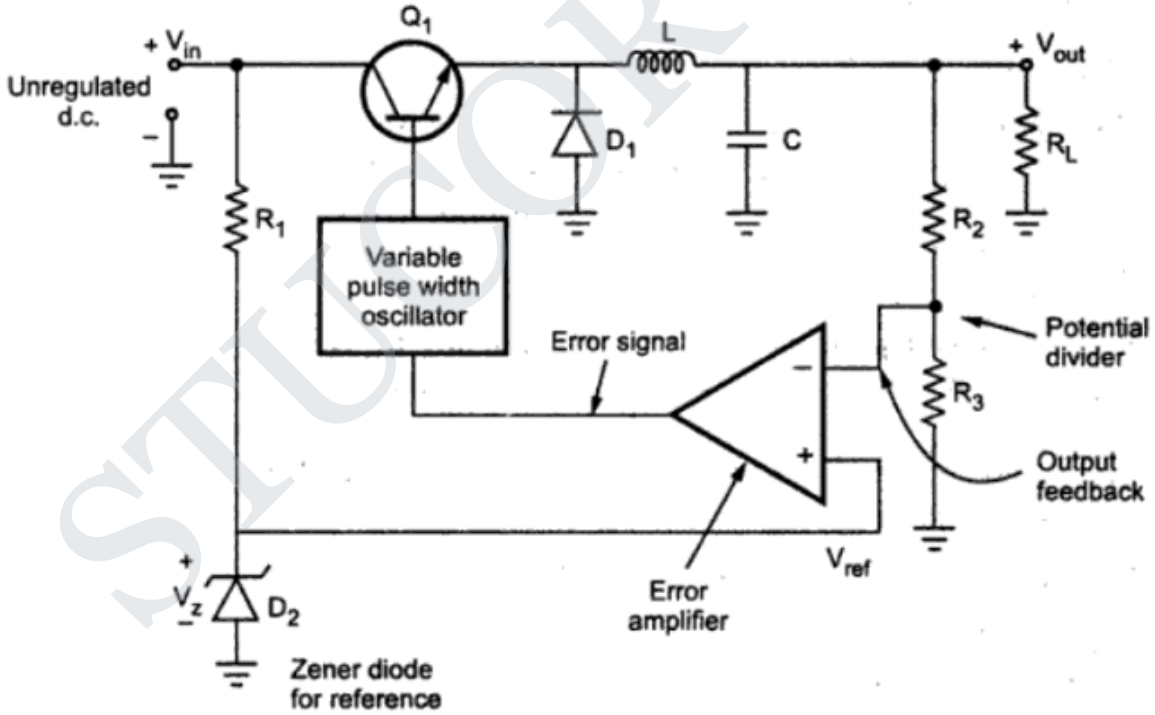


Fig. 7.77 Step down switching regulator

- The Zener diode generates reference voltage for the error amplifier. Output of the error amplifier fedback to it through a **potential divider(R_2 R_3)**.
- The **variable pulse width oscillator turns ON or OFF the series pass transistor Q_1** based on load requirements.
- The L-C filter averages **switched voltage (Voltage from the series pass transistor Q_1)**.
- When ON time of Q_1 is greater than its OFF time , the capacitor charges more increasing the output voltage. As a result , the voltage across R_3 increases. Since the reference voltage is fixed

, the error input fedback at the input of error amplifier decreases. As a result , the pulse width generates a pulse of smaller width which reduces ON time of Q_1. As a result , the capacitor discharges more reducing the output voltage.

- When ON time of Q_1 is lesser than its OFF time , the capacitor discharges more decreasing the output voltage. As a result , the voltage across R_3 decreases. Since the reference voltage is fixed , the error input fedback at the input of error amplifier increases. As a result , the pulse width generates a pulse of larger width which reduces OFF time of Q_1. As a result , the capacitor charges more increasing the output voltage.

3. Explain the operation of SMPS with neat diagrams

(Or)

What is the principle of switched mode power supplies. Discuss its advantages and disadvantages

(Or)

Explain the operation of switching regulator. Give its advantages.

(Or)

With necessary diagram and waveforms explain the working principle of switched mode power supply

(Or)

Write a detailed note on switching regulators

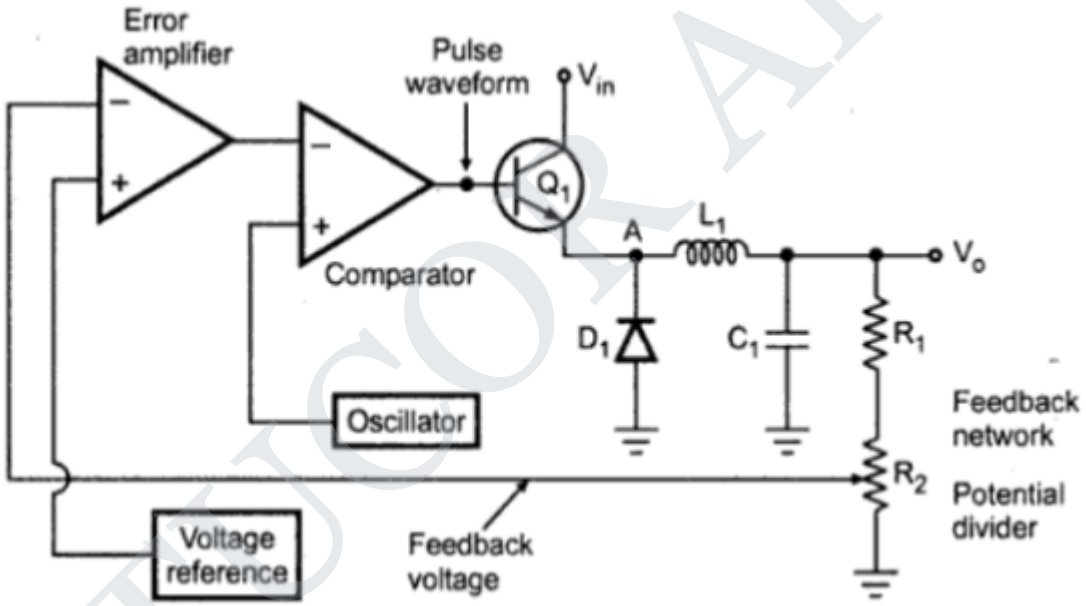


Fig. 10.52 Functional block diagram of switching regulator

The basic **switching regulator consist of four main components:**

(i) Voltage Source (V_{IN}) (iii) Pulse Generator[Comparator]

(ii) Switching Transistor (Q_1) (iv) Filter F_1

The voltage source is a DC supply either regulated or unregulated. The voltage source has to satisfy the following requirements:

- Supply Power and losses associated with the regulator
- Must be high to satisfy minimum requirements of the regulator
- Must be large to supply sufficient dynamic range of line and load changes.

The RLC filter(F_1) is used for converting pulse from the comparator into DC voltage.

Operation of Switching Regulator or SMPS(Switched Mode Power Supply) :

- The voltage across the potential divider or feedback network formed by R_1 and R_2 is applied to one of the inputs of the error amplifier.
- The error amplifier compares the reference voltage with the error voltage and generates an output voltage that drives the comparator.

- One of the input terminals of the comparator fed by **fixed frequency triangular waveform**. When the amplitude of the triangular waveform greater than the error amplifier output , the **output of the comparator becomes high**.
- The time period of the pulse waveform generated by the comparator is same as that of triangular waveform. **The duty cycle , $\delta = T_{ON}/T$** is controlled by the error amplifier output.
- When Q1 is ON(SATURATION) , the $V_{CE(SAT)}$ is zero. Hence the entire input voltage V_{IN} appears at A. Thus the current flows through inductor L1.
- When Q1 is OFF(CUT-OFF) , L1 continues to supply current to the load. The diode D1 acts as freewheeling diode(diode in the return path of a current).
- The capacitor C1 acts as a filter to provide a pure DC output voltage. The output voltage of the SMPS is given by

$$V_{OUT} = V_{IN} \times \delta$$

- SMPS involves both PWM(Pulse Width Modulation) and FM (Frequency Modulation). In PWM , the ON period of the pulse is variable whereas total time period of the pulse is fixed. In FM , the ON period of the pulse is fixed whereas total time period of the pulse is variable. Among the both PWM is the most commonly used technique because of high currents involved
- The operating frequency of SMPS is between 10 kHz and 50 kHz.

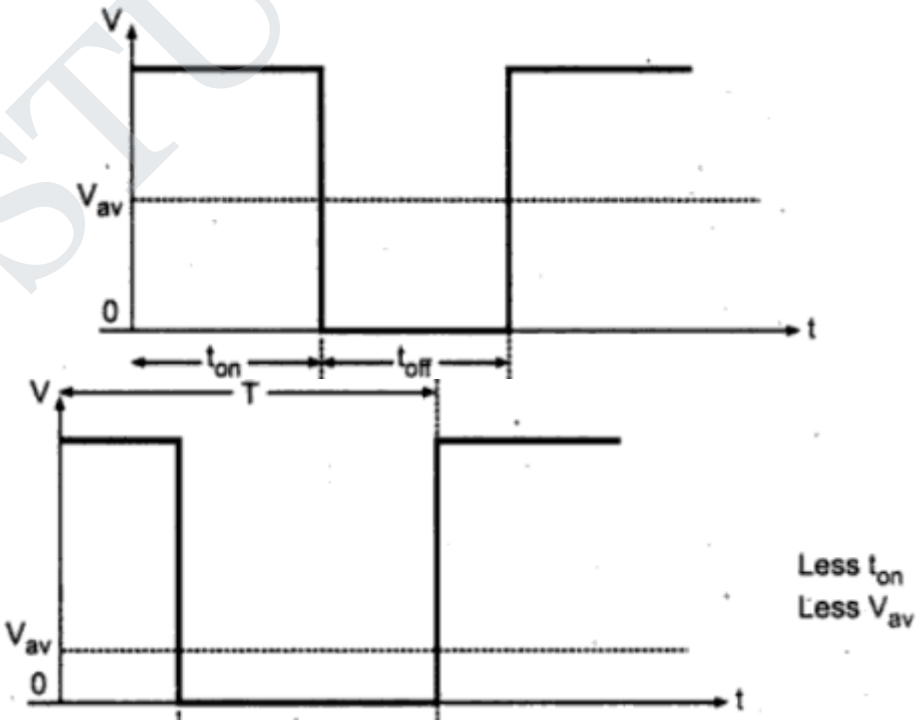
Advantages of SMPS:

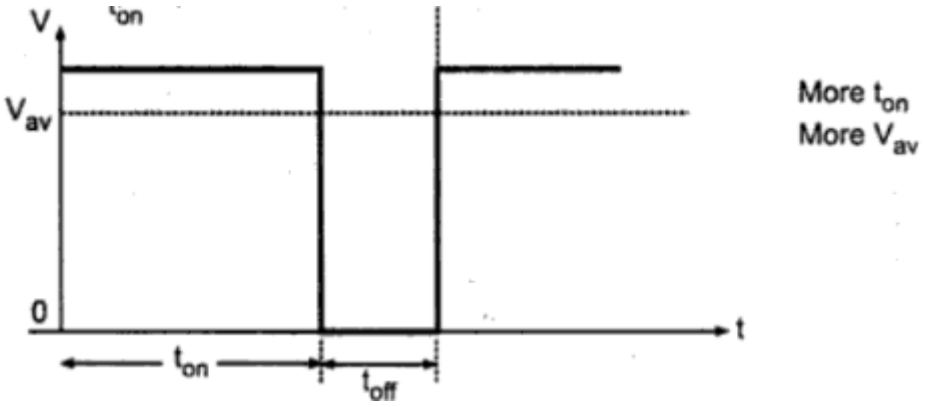
- Smaller in size
- Light Weight
- High power efficiency(60% to 70%)
- Low heat generation
- Strong Anti-Interference

Disadvantages of SMPS:

- High output ripple
- Worse Voltage Regulation
- Causes Harmonic Distortion
- Can be mainly used in buck mode [**Step Down Switching Regulator**]

Waveforms:





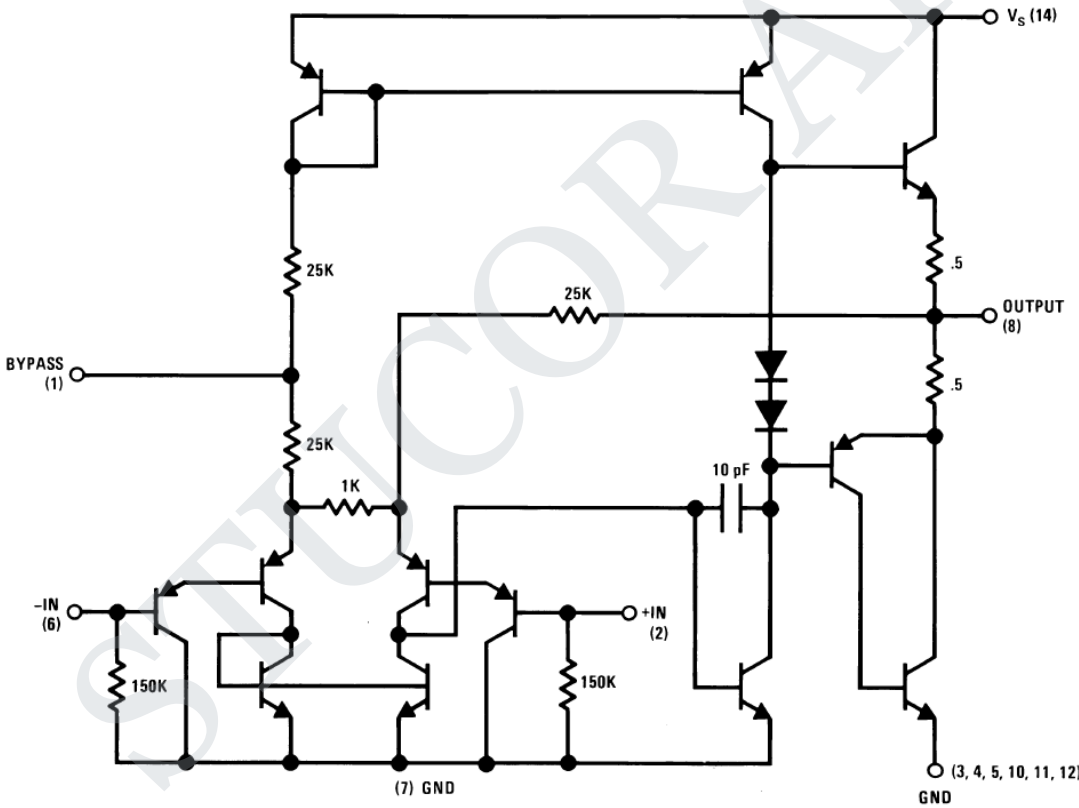
4. With a neat diagram, explain the operation of LM380 power amplifier?

(Or)

Explain the operation of a **monolithic IC Class-A Audio Power Amplifier**

(Or)

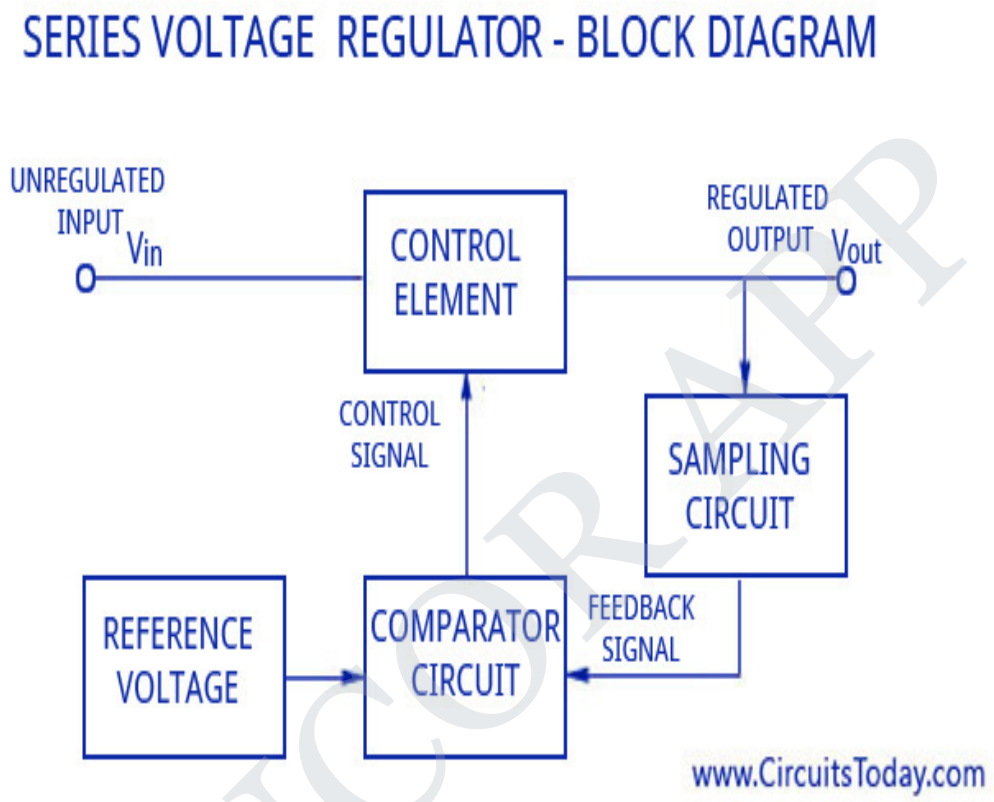
Draw the circuit diagram of LM380 Audio amplifier and explain its operation



- The PNP transistors Q1 and Q2 form an **emitter follower input stage.** Base of Q1 is the **inverting input terminal and** base of Q2 is the **non-inverting input terminal**. The resistances R_1 and R_2 provide DC return path for the input bias current so that the emitter follower stage can operate with either of the input terminals open. To decouple the input stage from $+V_{CC}$, a bypass capacitor is connected between **bypass terminal** and ground.
- This input stage drives the **differential amplifier Q3-Q4**. **The differential amplifier is biased by R_3.**
- The current in the differential pair **Q3-Q4** decided by Q7 , R3 and $+V_{CC}$. The **current mirror** Q7-Q8 and associated resistors establish collector current of Q9. The transistor Q9 with diodes **D1 and D2** form the **common emitter voltage gain stage**.

- The transistors Q5-Q6 acts as **the active load of Q3-Q4**. The diodes D1 and D2 develop a **small pre-bias voltage across the base emitter junctions of Q10-Q11 to reduce cross-over distortion**.
- The NPN transistors Q10-Q12 form a **quasi-complementary pair emitter follower**. The resistors R3 and R5 set the **quiescent voltage level of the Q10-Q12** at half the supply voltage. This allows **maximum peak-peak output voltage swing**.

5. Explain the working of series voltage regulator



- In a series voltage regulator , the control element is connected in series with the load.
- The unregulated DC voltage is the input to the circuit. The control element controls the amount of input voltage that gets to the output.
- The sampling circuit provides the necessary feedback signal.
- The comparator circuit compares the feedback signal with reference signal and generates an appropriate control signal.
- Whenever the load voltage increases , the comparator generates a control signal to reduce it.
- Whenever the load voltage decreases , the comparator generates a control signal to increase it.

6. Explain the working principle of IC 8038 function generator

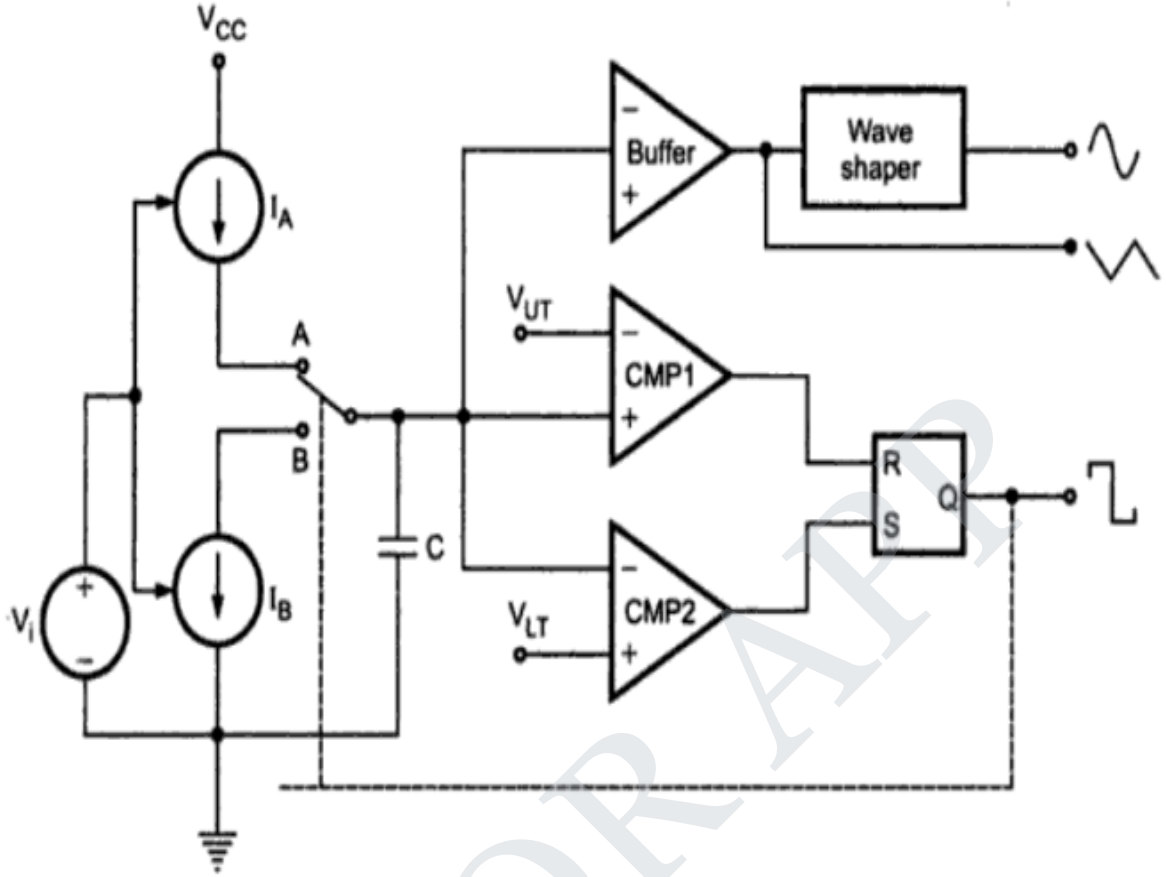


Fig. 3.205 Simplified block diagram of ICL 8038 function generator

- The **operation of the ICL 8038 precision function generator** is based on controlled charging and discharging of a **grounded capacitor** through a **programmable current generators I_A and I_B.**
- When switch is at position A , the capacitor C charges at a rate determined by the current source I_A . Once the capacitor voltage reaches V_{UT} , the upper comparator CMP 1 triggers and resets the flip-flop output. This causes the switch position to change from position A to position B.
- As a result , the capacitor starts discharging at a rate determined by current source I_B . Once the capacitor voltage reaches V_{LT} , the lower comparator CMP 2 triggers and sets the flip-flop output. This causes the switch position to change from position B to position A. This set and reset cycle continuously repeats generating a **square wave** at the output of the flip-flop , **triangular wave across capacitor** and a **sine wave** across the wave-shaper circuit. The wave shaper circuit is nothing but **Schmitt Trigger circuit**.
- The current sources I_A and I_B are **made programmable through an external control voltage V_I.**
- **When magnitudes of I_A and I_B are equal , the waveforms are SYMMETRICAL** and when they are different , the **waveforms are ASYMMETRICAL**.
- **By making one of the currents larger than the other , SAWTOOTH waveform is generated across the capacitor and RECTANGULAR WAVEFORM is generated across the SCHMITT TRIGGER**.

7. Explain foldback characteristics of IC 723 regulator

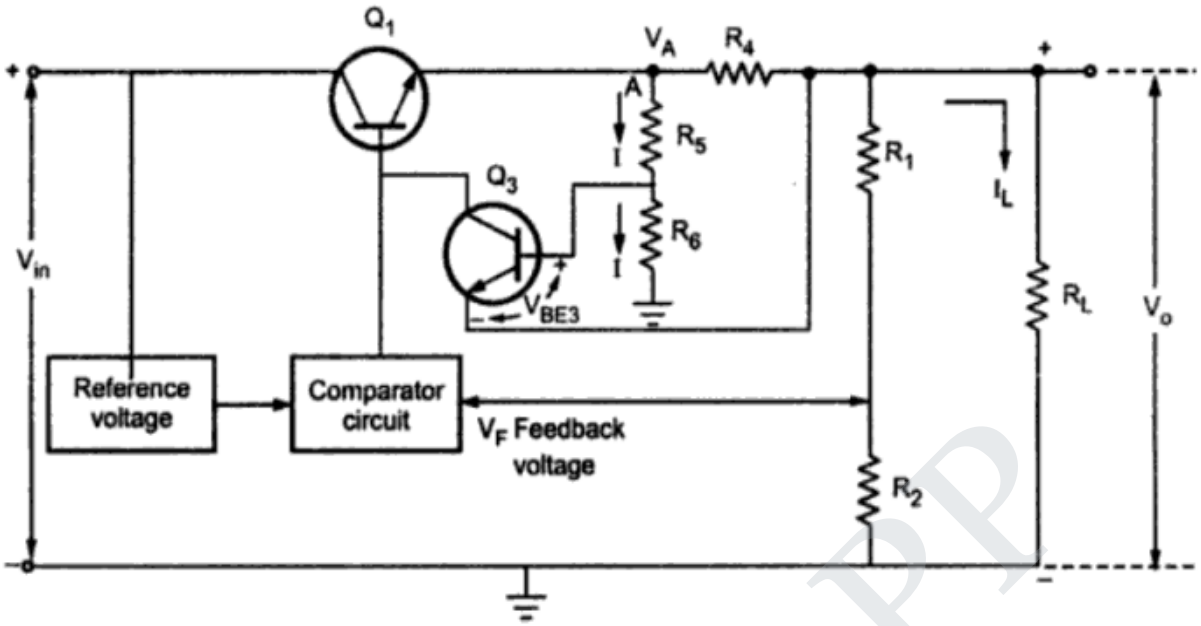


Fig. 7.55 Foldback current limiting

- Foldback current limiting circuit makes 723 regulator to provide rated load current at rated voltage at reduced short circuit current.

All the voltages are measured with respect to a common point.

Let the voltage at point A be V_A and the current flowing through R_4 is almost I_L.

$$\therefore \quad V_A = I_L R_4 + V_o \qquad \ldots (4)$$

Neglecting the base current of Q_3, the current flowing through R_5 and R_6 is same as I.

$$\therefore \quad I = \frac{V_A}{R_5 + R_6} \qquad \ldots (5)$$

Hence the voltage at the base of Q_3 is the voltage across R_6.

$$\therefore \quad V_{B3} = \frac{V_A}{R_5 + R_6} \cdot R_6$$

$$= (I_L R_4 + V_o) \left(\frac{R_6}{R_5 + R_6} \right) \qquad \ldots (6)$$

Let $\boxed{k = \frac{R_6}{R_5 + R_6}}$

$$\therefore \quad V_{B3} = k (I_L R_4 + V_o) \qquad \ldots (7)$$

The voltage at the emitter of Q_3 is

$$V_{E3} = V_o \qquad \ldots (8)$$

$$\therefore \quad V_{BE3} = V_{B3} - V_{E3} = k (I_L R_4 + V_o) - V_o$$

$$\therefore \quad V_{BE3} = k I_L R_4 + (k - 1) V_o$$

$$\therefore \quad k I_L R_4 = V_{BE3} - (k - 1) V_o$$

$$\therefore \quad I_L = \frac{V_{BE3} + (1-k)\,V_o}{k\,R_4} \qquad \ldots (9)$$

Thus if the output terminals are shorted, the output voltage V_o reduces to zero. Hence we get from the equation (9),

$$I_{SC} = I_L = \frac{V_{BE3}}{k\,R_4} \qquad \ldots (10)$$

The rated current can be written as,

$$I_L = I_{SC} + \frac{(1-k)\,V_o}{k\,R_4} \qquad \ldots (11)$$

where I_L = Rated load current

I_{SC} = Short circuit current

The rated load current I_L is also called I_{knee} known as knee current.

From equation(11) it is found that **rated load current greater than short circuit load current.**

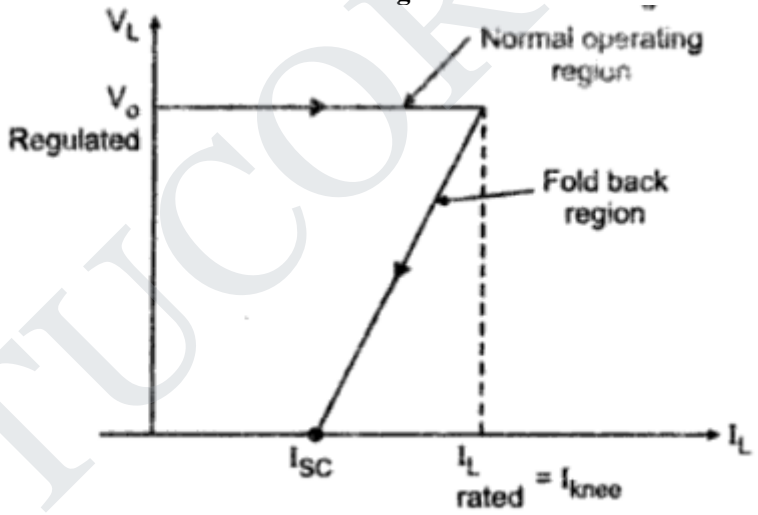


Fig. 7.56 Foldback characteristics

Value of **k** is selected in such a way the rated load current is **2 to 3 times** greater than **short circuit load current**.

From the foldback characteristics , it is found that when the load current exceeds beyond its rated value , the **load voltage foldsback and finally becomes zero at I_{SC}.**

8. What are the applications of LM380 Audio Power Amplifier

Applications of LM 380 Audio Power Amplifier:

LM380 AUDIO AMPLIFIER:

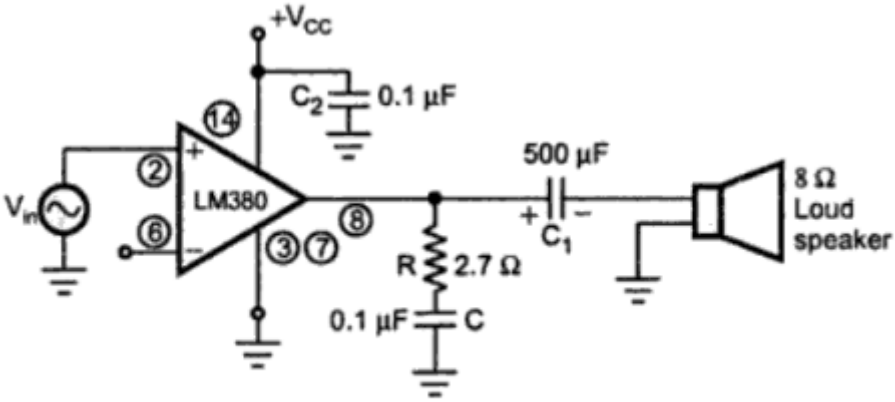


Fig. 4.94 LM 380 as audio amplifier

- The LM 380 can be used either in inverting or non-inverting configuration
- When used in non-inverting mode , inverting terminal either directly grounded or grounded through resistor or capacitor.
- When used in inverting mode , non-inverting terminal either directly grounded or grounded through resistor or capacitor.
- In inverting or non-inverting configurations ,supply voltage is decoupled by connecting a capacitor between $+V_{CC}$ and ground.
- Lag RC network (R = 2.7 Ω , C = 0.1 µF) connected between output terminal and ground to eliminate 5 MHz to 10 MHz oscillations.

Intercom System using LM380 Audio Amplifier:

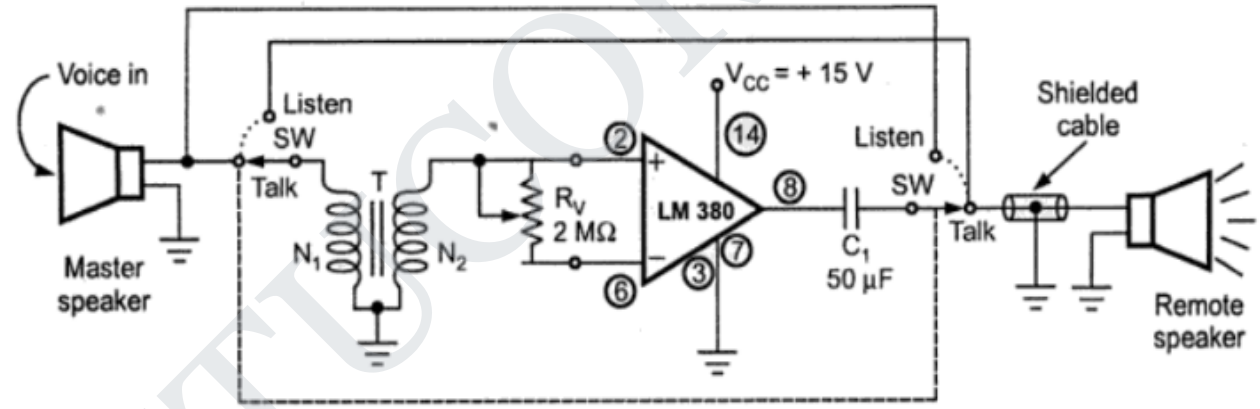


Fig. 10.116 (a) Intercom system in talk mode

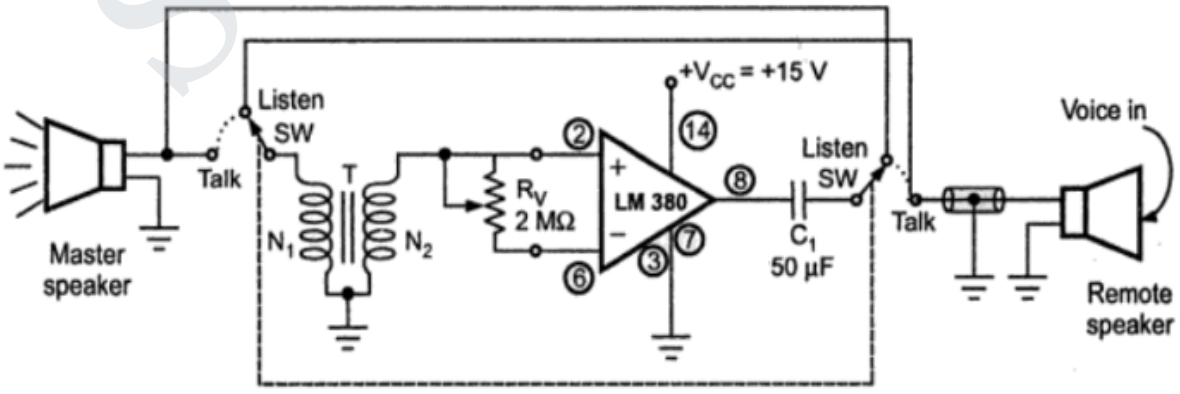


Fig. 10.116 (b) Intercom system is listen mode

- Speakers also act as microphone.
- Intercom system operated in talk mode or listen mode.
- When switch SW in talk mode, **master speaker acts as microphone accepting voice through STEP-UP TRANSFORMER T.** Overall gain of the circuit depends upon **turns ration of transformer and internal gain of LM380.**
- **Internal gain of LM380 controlled by pot R_V.**
- **When the switch SW in listen mode , the remote speaker acts as microphone.**

Phono-Amplifier using LM380 Audio Amplifier:

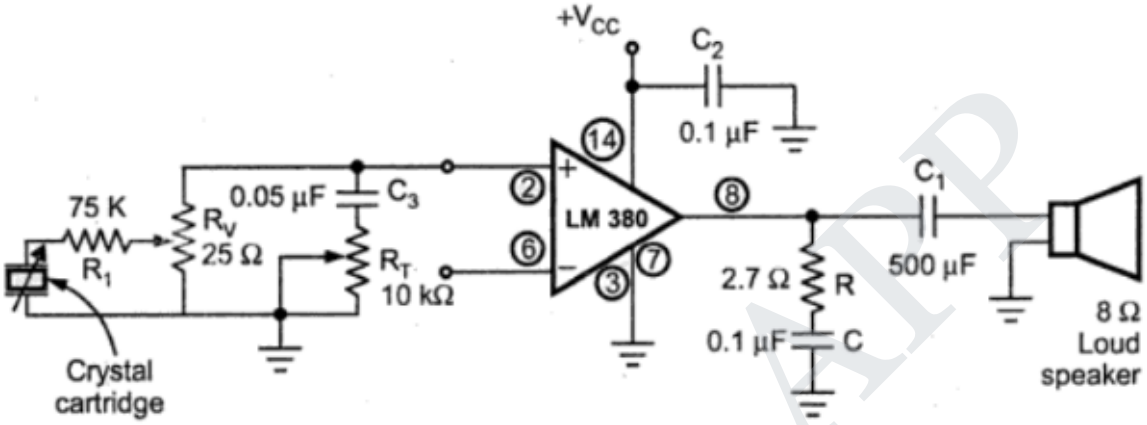


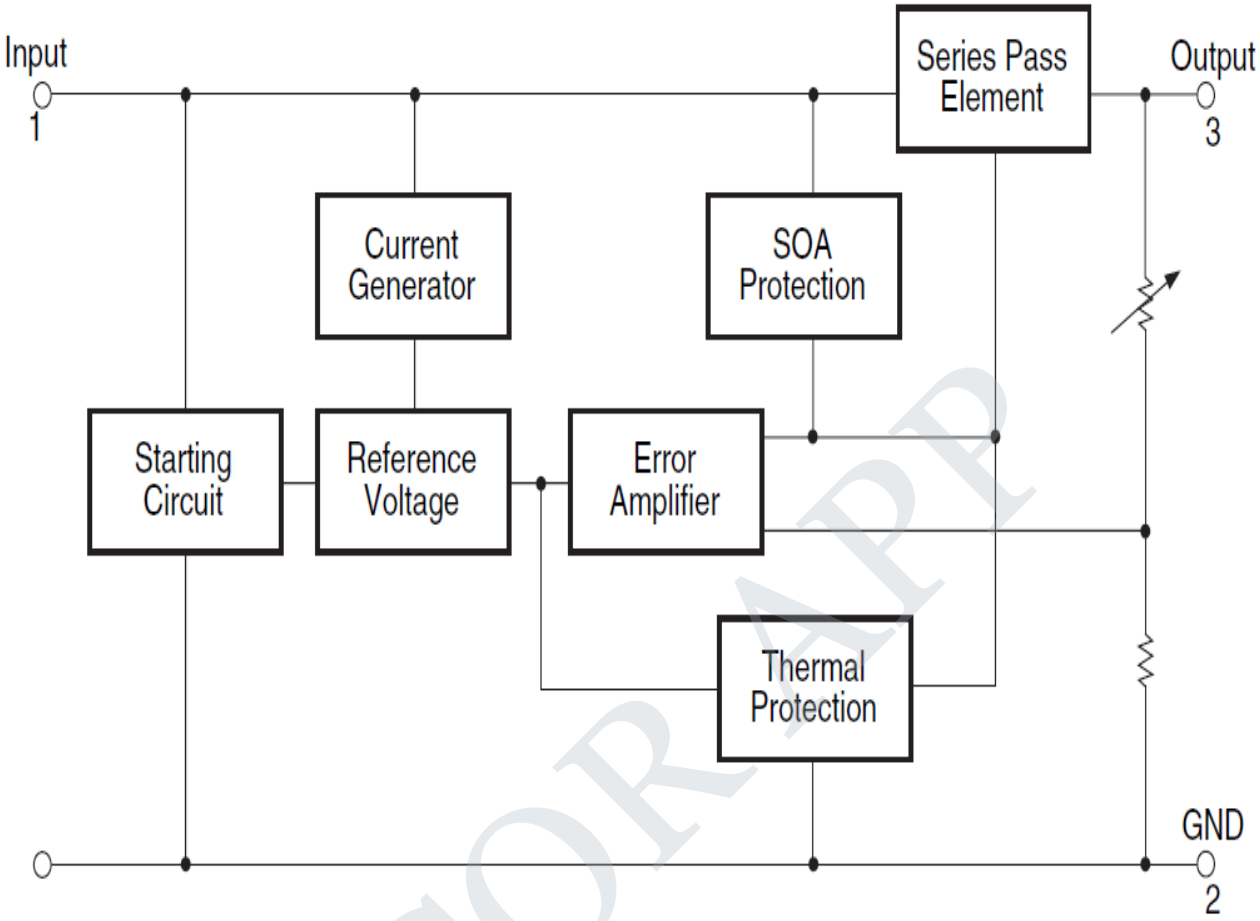
Fig. 10.115 LM 380 as a phonoamplifier

- Phono-amplifier with volume and tone control constructed using LM380 audio amplifier.
- Output is taken out from 8 Ω loud speaker. Lag RC network (R = 2.7 Ω , C = 0.1 µF) connected between output terminal and ground to eliminate 5 MHz to 10 MHz oscillations.
- Pot R_V used for volume control and pot R_T used for tune control.

9. What do you mean by fixed voltage and variable voltage regulator . List its various applications.

Fixed Voltage Regulator:

- A fixed voltage regulator is a device that provides a **constant positive or negative output voltage.**
- All the ICs belonging to 78XX series are fixed positive voltage regulator. All the ICs belonging to 79XX series are fixed negative voltage regulator. **XX** refers to the output voltages they generate.
- XX can be either 05 , 06 , 09 etc.
- Both positive and negative fixed voltage regulator are three terminal voltage regulators.



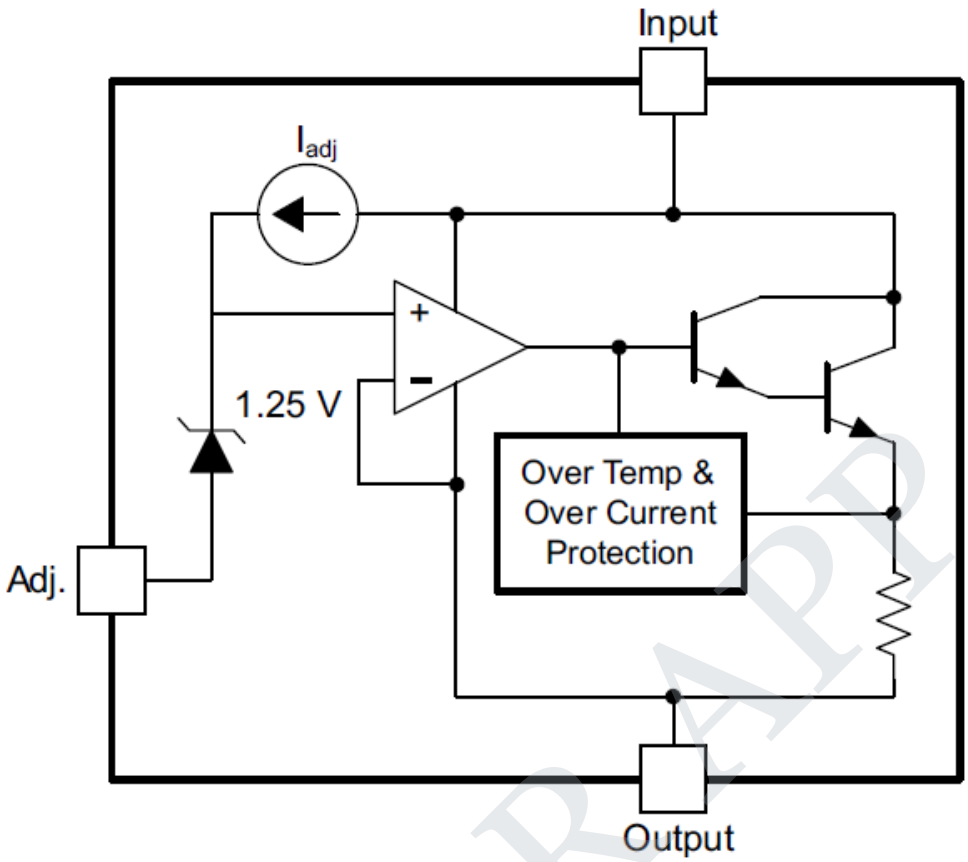
Features of Fixed Voltage Regulators:

- Has internal thermal overload protection.
- Has high power dissipation capability
- Has internal short-circuit current limiting capabilities
- Has output transistor SOA(Safe Operating Area) Compensation.
- High ripple rejection
- By means of pots[variable resistor] at the output , the fixed voltage regulator can be made to function as **adjustable voltage regulator**.
- Are generally **series voltage regulators**.
- Maximum output current is 1 A.

Applications of fixed voltage regulators:

- **Constant Current Regulator**
- **Adjustable Voltage Regulator**
- **Tracking Voltage Regulator**
- **Split Power Supply**

Adjustable Voltage Regulator:



- An adjustable voltage regulator is a device that provides **a variable positive or negative voltages**.
- LM317 is an example of **adjustable positive voltage regulator**. LM337 is an example of **adjustable negative voltage regulator**.
- **Similar to fixed voltage regulators , variable voltage regulators are also three terminal regulators**.

Features of Adjustable Voltage Regulators:

- Adjustable voltage range between 1.25 V to 37 V.
- Requires only two external resistors to set the output voltage
- Requires one external capacitor for frequency compensation
- Has internal thermal overload protection
- Has internal short-circuit current limiting capabilities
- Has output transistor SOA(Safe Operating Area) Compensation.
- Maximum output current is 1.5 A

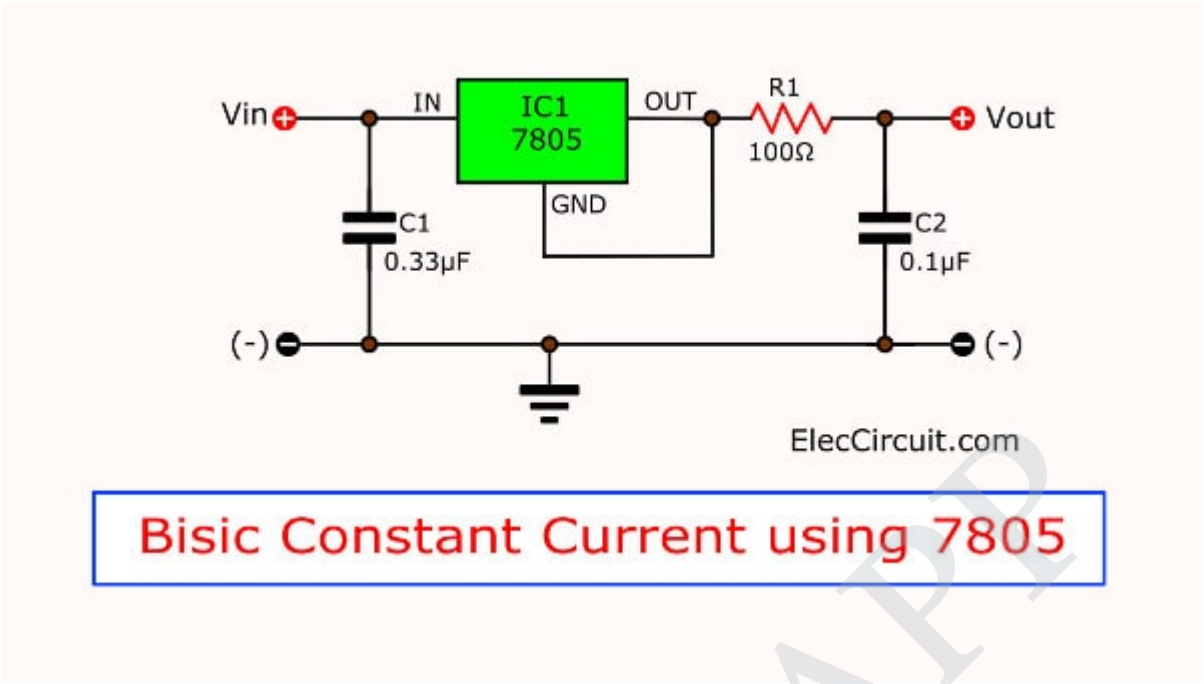
Applications:

- **ATCA(Advanced Telecommunication Computer Applications)**
- **Hyperspectral imaging**
- **ECG(Electro Cardio Gram)**
- **PBX(Private Branch Exchange).**

10. Discuss with neat diagram , the working of IC 7805 regulator as

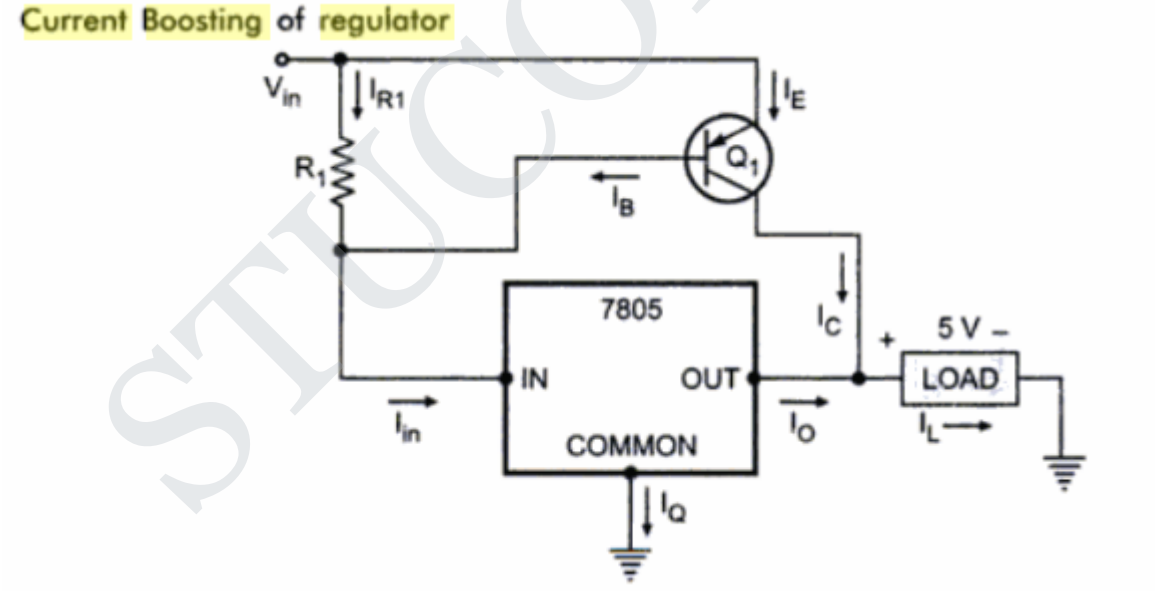
(i) Current Source

The 7805 voltage regulator can function as constant current source by connecting a constant resistor at its output terminal.



(ii) Boosting regulator output current.

- The maximum output current of LM7805 is 1A. It can be boosted to 10 A by connecting a BJT[$\mathbf{Q_1}$] in parallel to its output.
- For low load currents (I_L) [i.e. < 100 mA], the voltage drop across R_1 is insufficient to turn on the BJT. Hence the voltage regulator supplies the entire current.
- For large load currents(I_L)[ie. > 100 mA] , the voltage drop across R_1 is sufficient to turn on the BJT. The excess current required by the regulator is provided by Q_1.



$$I_L = I_C + I_o = \beta I_B + I_o$$

But $$I_B = I_{in} - I_{R1}$$

Neglecting I_Q, $I_{in} = I_o$ hence we get,

$$I_B = I_o - I_{R1}$$

But $$I_{R1} = \frac{V_{BE}}{R_1}$$

11. Elaborate with neat diagram , the working of IC723 as low voltage and high voltage regulators.

Low Voltage Low Current Regulator: (or Basic Low Voltage Regulator)

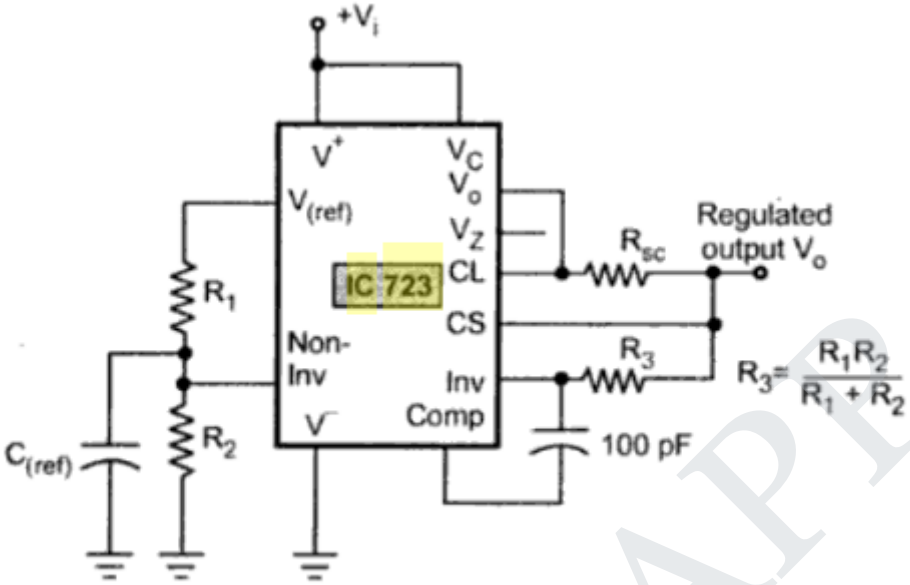


Fig. 10.33 Basic low voltage regulator

- The value of the output voltage varies between 2 V to 7 V. Value of output current is less than 150 mA.
- The short circuit load current limiting resistance R_{SC} is connected between CS and CL pins.
- The current limiting transistor remains OFF unless voltage drop across R_{SC} is less than 0.6 V.
- The value of R_{SC} can be found from the following:

$$R_{SC} = \frac{0.6}{I_{LIMIT}}$$

- I_{LIMIT} is selected 1.2 to 1.5 times the maximum load current. Potential divider made up of R_1 and R_2 connected between V_{REF} and non-inverting terminals. The voltage

$$V_{\text{non-inverting}} = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

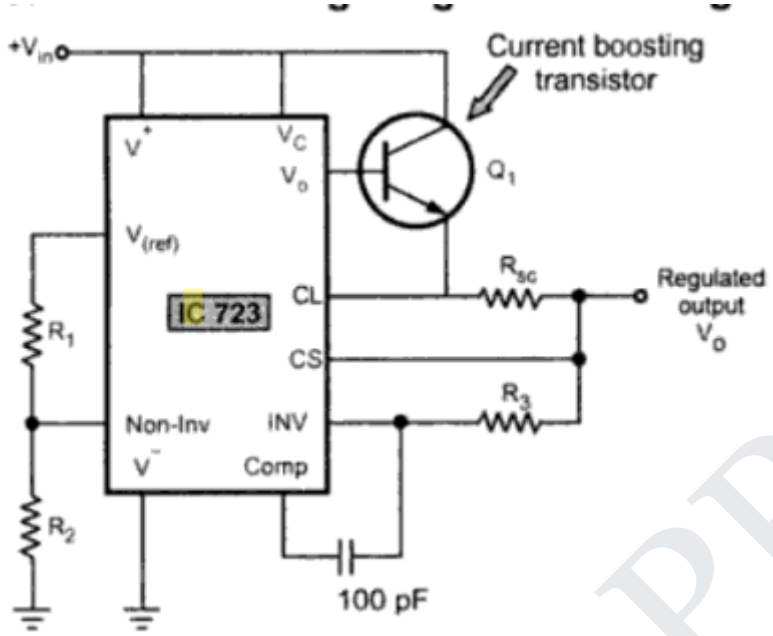
As the series pass transistor connected between V_C and ground is working as a **emitter follower** , the output voltage is same as the voltage at the **non-inverting terminal**.

$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

R_1 and R_2 can be between 1 kΩ to 10 kΩ.

$$R_3 = R_1 \parallel R_2 \quad \therefore R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

Low Voltage High Current Regulator:



- Value of output voltage varies between 2 V to 7 V. Value of output current is ≥ 150 mA.
- To increase the output current , a BJT[Q1] is connected between output terminal and CL pin.

$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

$$R_{sc} = \frac{0.6}{I_{limit}}$$

Power dissipation of transistor = $[V_{i(max)} - V_{o(min)}] \times I_{L(max)}$

Power dissipation of IC = $[V_{i(max)} - V_{o(min)}] \times \frac{I_{L(max)}}{h_{fe\,(min)\ of\ Q_1}}$

High Voltage Low Current Regulator: (**or Basic High Voltage Regulator)**

- Value of output voltage varies between 7 V to 37 V. Value of output current is less than 150 mA.
- For this purpose , the non-inverting terminal is connected to V_{REF} through resistance R_3.
- The error amplifier in IC 723 acts as **non-inverting amplifier**.

The gain, $$A = 1 + \frac{R_1}{R_2}$$

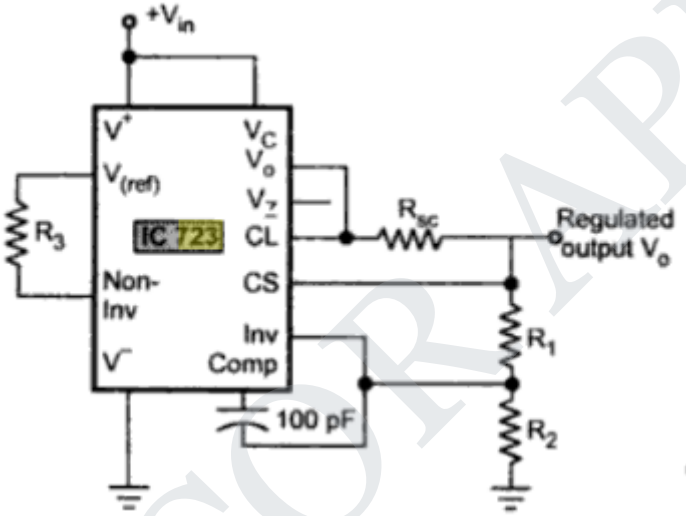
…. Gain of Error or Non-inverting amplifier

The output voltage is,

$$V_o = V_{ref}\left(1 + \frac{R_1}{R_2}\right) = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right) \quad \ldots (6)$$

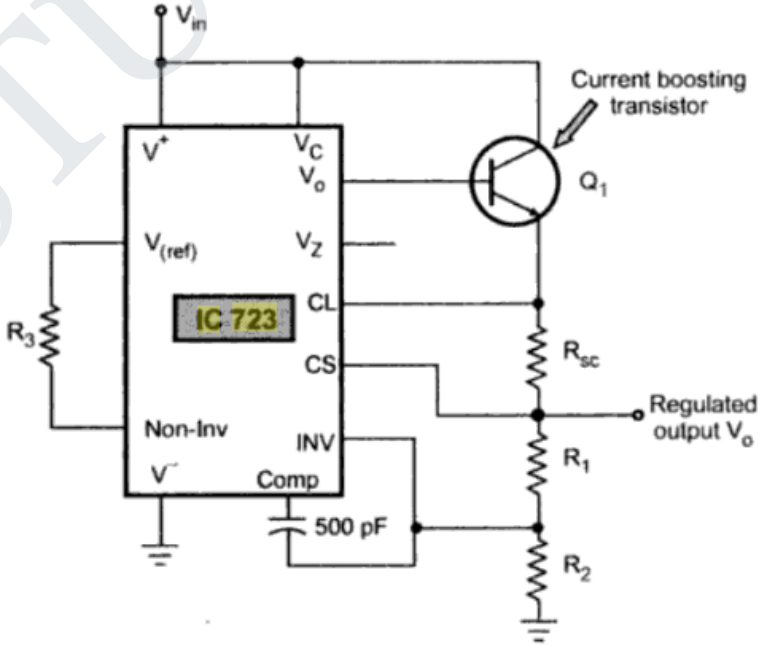
$$R_{sc} = \frac{0.6}{I_{limit}} = \frac{V_{sense}}{I_{sc}} \quad \ldots (7)$$

$$R_3 = R_1 \parallel R_2 = \left(\frac{R_1 R_2}{R_1 + R_2}\right) \quad \ldots (8)$$



High Voltage High Current Regulator:

- Value of output voltage varies between 7 V to 37 V. Value of output current is ≥ 150 mA.
- For this purpose , BJT connected between output terminal and CL pin and potential divider provided between CS pin and ground.



$$V_o = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right)$$

$$R_{sc} = \frac{0.6}{I_{limit}} = \frac{V_{sense}}{I_{sc}}, \quad R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

12. Explain the fixed voltage regulator and its applications.

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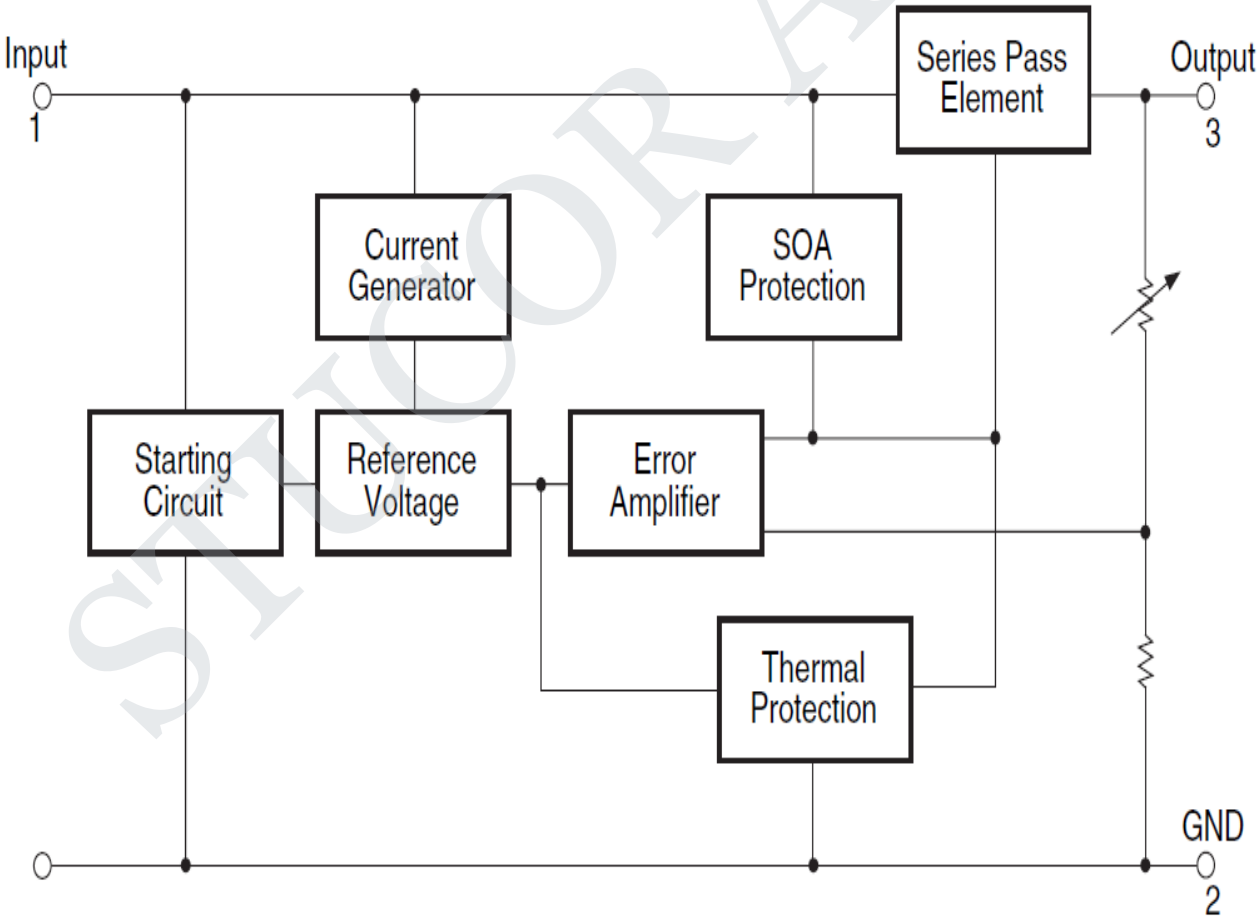

Features of Fixed Voltage Regulators:

- Has internal thermal overload protection.
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- Has internal short-circuit current limiting capabilities
- Has output transistor SOA(Safe Operating Area) Compensation.
- High ripple rejection

- By means of pots[variable resistor] at the output , the fixed voltage regulator can be made to function as **adjustable voltage regulator**.
- Are generally **series voltage regulators**.
- Maximum output current is 1 A.

Applications of fixed voltage regulators:

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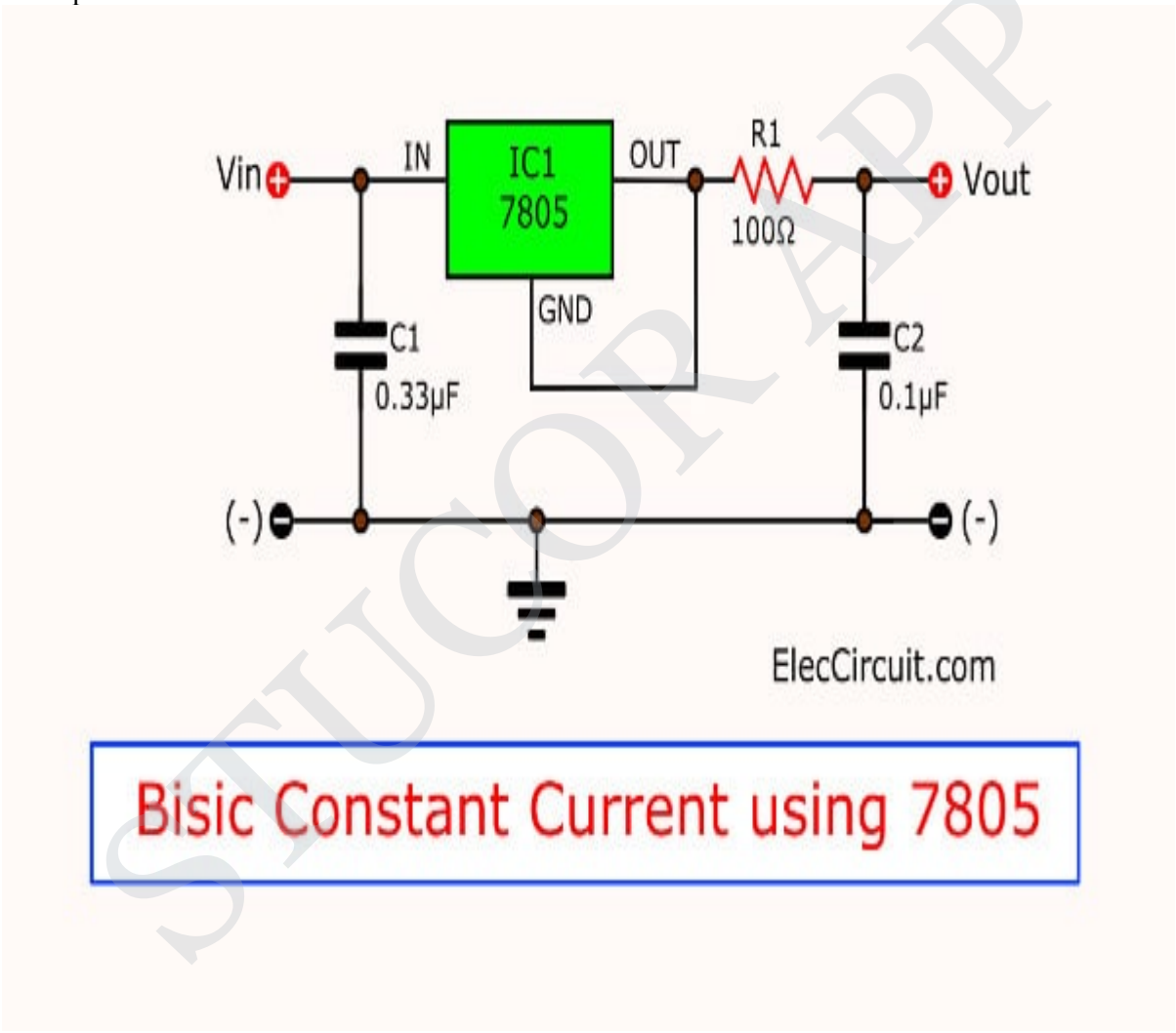

(ii) Boosting regulator output current.

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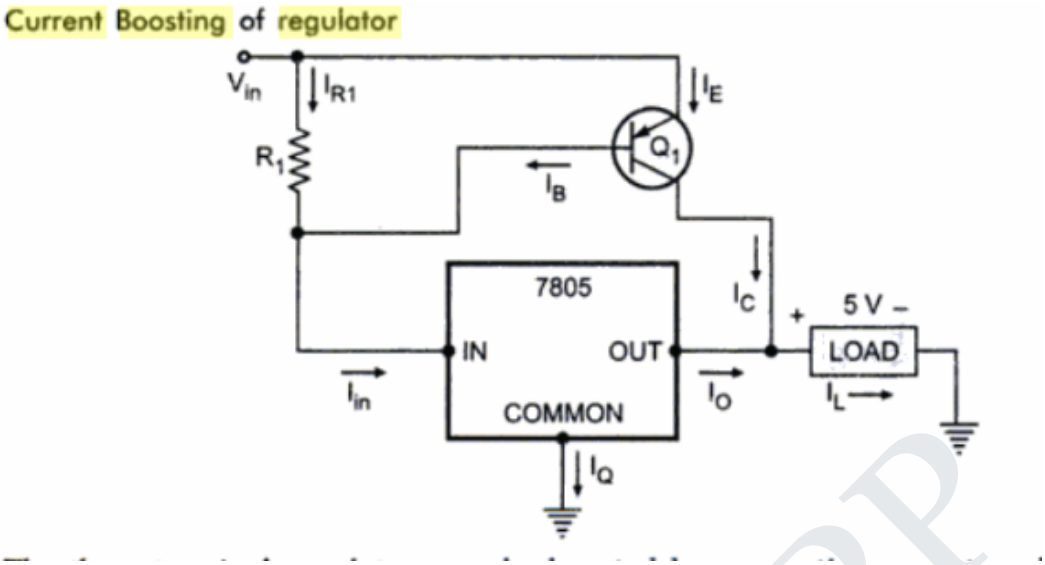
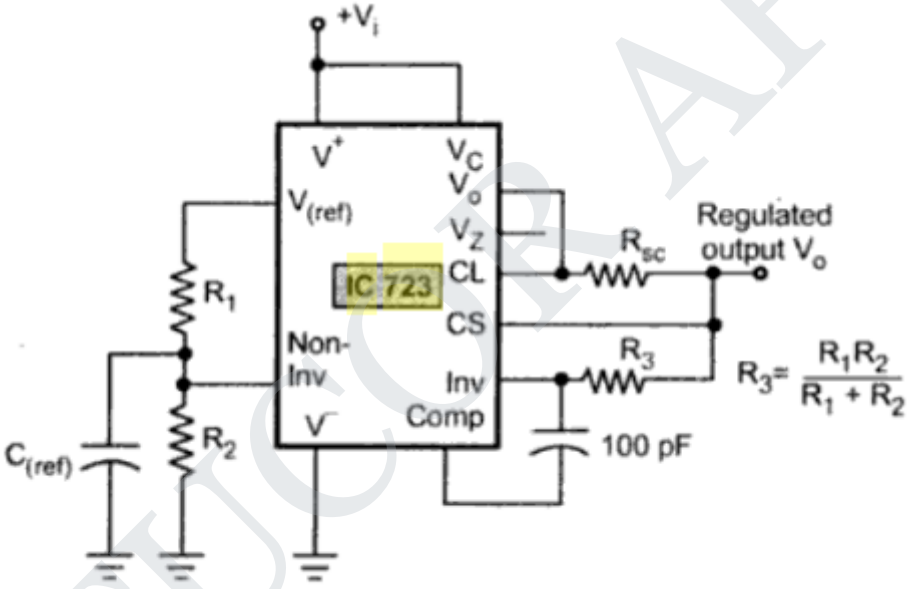


Low Voltage Low Current Regulator: (or Basic Low Voltage Regulator)



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$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

R_1 and R_2 can be between 1 kΩ to 10 kΩ.

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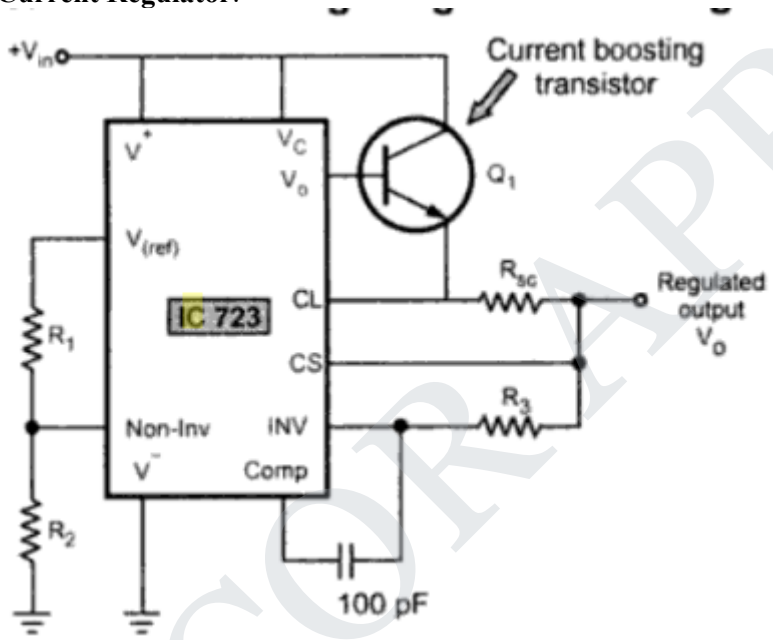
Low Voltage High Current Regulator:



- Value of output voltage varies between 2 V to 7 V. Value of output current is ≥ 150 mA.
- To increase the output current , a BJT[Q1] is connected between output terminal and CL pin.

$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

$$R_{sc} = \frac{0.6}{I_{limit}}$$

$$\text{Power dissipation of transistor} = [V_{i(max)} - V_{o(min)}] \times I_{L(max)}$$

$$\text{Power dissipation of IC} = [V_{i(max)} - V_{o(min)}] \times \frac{I_{L(max)}}{h_{fe\,(min)\ of\ Q_1}}$$

High Voltage Low Current Regulator: (**or Basic High Voltage Regulator)**

- Value of output voltage varies between 7 V to 37 V. Value of output current is less than 150 mA.
- For this purpose , the non-inverting terminal is connected to V_{REF} through resistance R_3.
- The error amplifier in IC 723 acts as **non-inverting amplifier**.

The gain, $$A = 1 + \frac{R_1}{R_2}$$

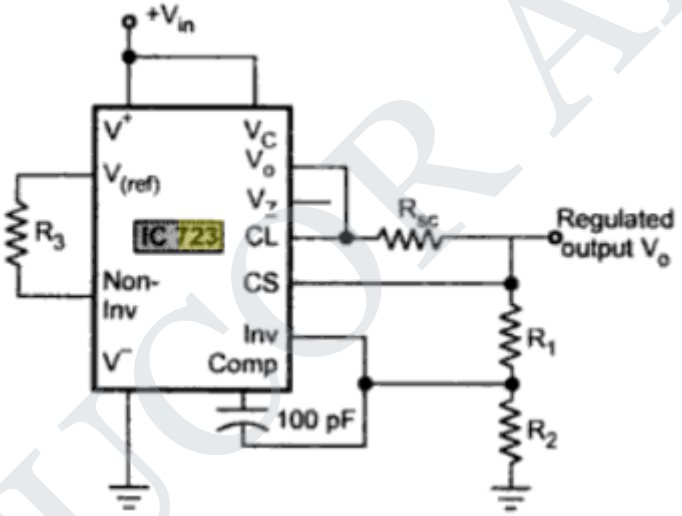
…. Gain of Error or Non-inverting amplifier

The output voltage is,

$$V_o = V_{ref}\left(1 + \frac{R_1}{R_2}\right) = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right) \quad \ldots (6)$$

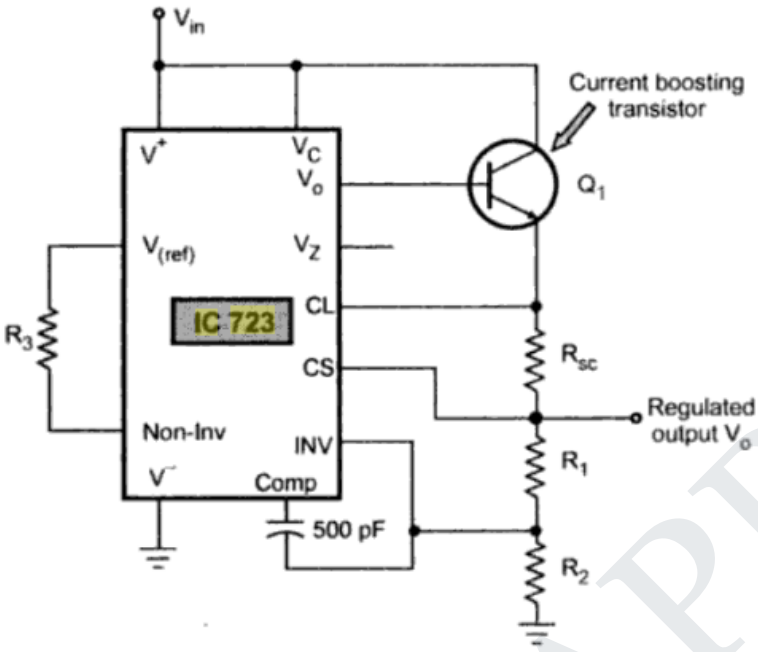
$$R_{sc} = \frac{0.6}{I_{limit}} = \frac{V_{sense}}{I_{sc}} \quad \ldots (7)$$

$$R_3 = R_1 \parallel R_2 = \left(\frac{R_1 R_2}{R_1 + R_2}\right) \quad \ldots (8)$$



High Voltage High Current Regulator:

- Value of output voltage varies between 7 V to 37 V. Value of output current is ≥ 150 mA.
- For this purpose , BJT connected between output terminal and CL pin and potential divider provided between CS pin and ground.



$$V_o = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right)$$

$$R_{sc} = \frac{0.6}{I_{limit}} = \frac{V_{sense}}{I_{sc}}, \quad R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

$$I_L = I_C + I_o = \beta I_B + I_o$$

But $$I_B = I_{in} - I_{R1}$$

Neglecting I_Q, $I_{in} = I_o$ hence we get,

$$I_B = I_o - I_{R1}$$

But $$I_{R1} = \frac{V_{BE}}{R_1}$$

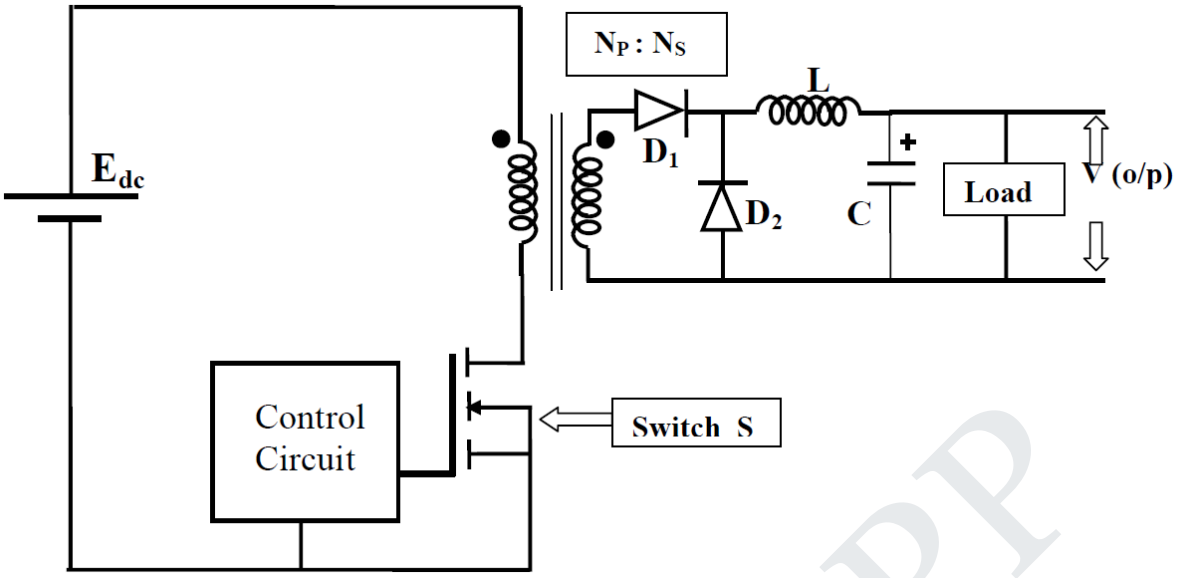
13. Explain with a neat block diagram and switching power supply waveforms for the following types of SMPS

(i) Forward Converter

(ii) Flyback Converter

(i) Forward Converter SMPS:

- **Forward Converter SMPS** is the most commonly used SMPS for **high power applications (100 W to 200 W)**.
- Overall circuit topology is bit complex than **flyback converter SMPS.**
- The circuit can offer single or multiple isolated output voltages and operate over a wide range of input voltage variations.
- The operating frequency of the forward converter is ≥ 100 kHz.
- The device is called **forward converter because it uses forward transformer**.
- A forward transformer has primary winding , secondary winding and no air-gap as the core.
- The most commonly used switch is a **enhancement mode N-channel MOSFET**.
- The DC voltage is usually **switched DC (DC voltage from a rectifier)**.



Mode 1: (Powering Mode)

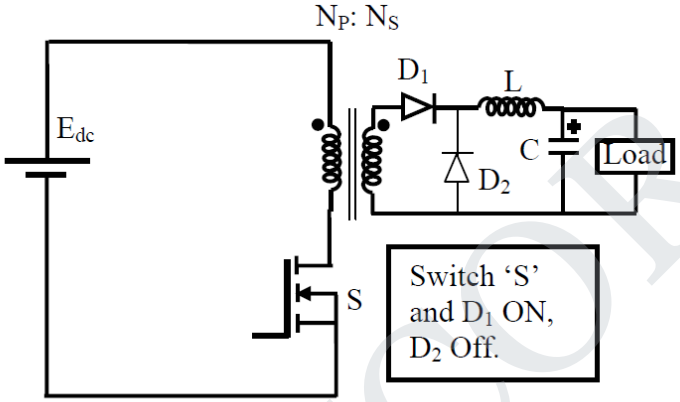


Fig. 23.2(a): Current path during Mode-1

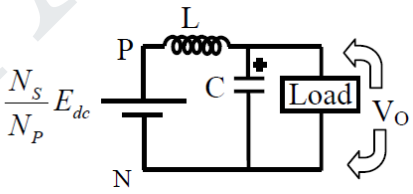


Fig.23.2(b): Equivalent circuit in Mode-1

- When the MOSFET switch is turned on by applying a gate signal , dotted end of the primary winding gets connected to positive terminal of battery and undotted end of primary winding gets connected to negative terminal of battery.
- Current entering the dotted ends of a winding (primary or secondary) produces positive MMF and current entering the undotted ends of a winding(primary or secondary) produces negative MMF.
- Positive MMF produces positive EMF ; Negative MMF produces negative EMF. Therefore positive EMFs are created in the primary and secondary. The dotted end of the secondary winding is connected to anode of D_1 and undotted end is connected to anode of D_2.
- Since the dotted end of the secondary winding is at higher potential than undotted end , the diode D1 turns ON and diode D2 turns OFF.
- As a result the LC filter and load receives secondary voltage through D1. The value of the secondary voltage is as follows:

$$\frac{N_S}{N_P} E_{dc}$$

Mode 2 : (Freewheeling Mode)

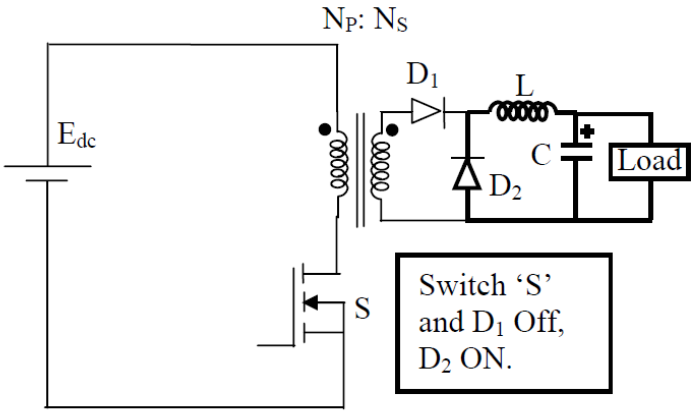


Fig. 23.3(a): Current path during Mode-2

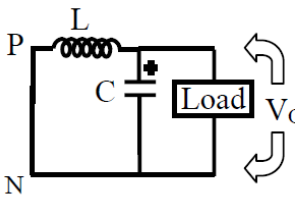


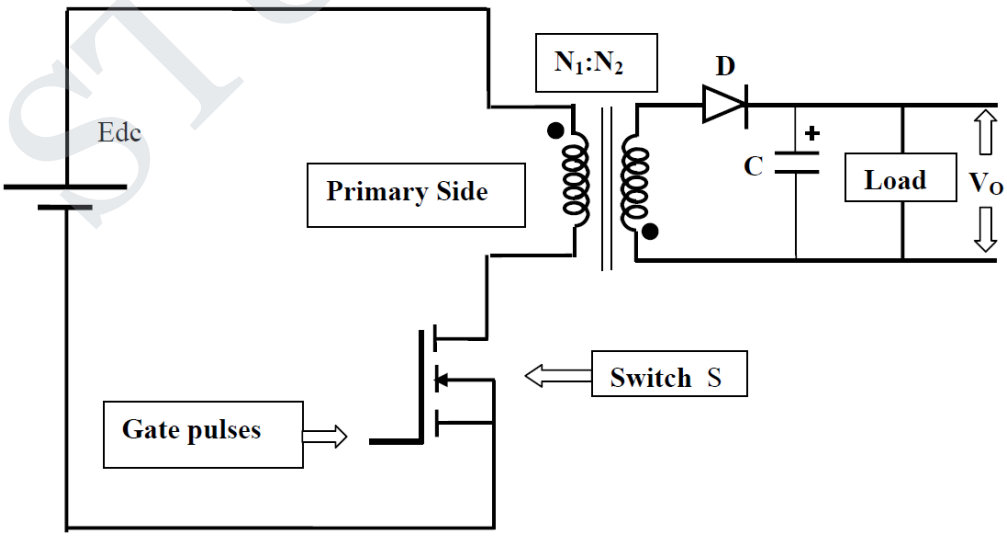
Fig.23.2(b): Equivalent circuit in Mode-2

When the MOSFET switch is turned OFF , the primary and secondary MMFs and EMFs become zero.

- Now due to collapse of the magnetic field , the diode D2 turns ON and diode D1 turns OFF. The inductor in LC filter maintains current through the load through the freewheeling diode D2.
- Since there is no input power in mode-2 , the stored energy in LC filter will slowly start to dissipate. In order to maintain the load voltage within the tolerance band , the circuit is switched back to **mode-1**

(ii) Flyback Converter SMPS:

- **Flyback Converter SMPS** is the most commonly used SMPS for **low power applications(0.1 W to 100 W)**.
- Overall circuit topology simpler than other SMPS circuits.
- The circuit can offer single or multiple isolated output voltages and operate over a wide range of input voltage variations.
- The operating frequency of the flyback SMPS is 100 kHz.
- The device is called flyback converter because it employs **flyback transformer**. A **flyback transformer** or **line output transformer** or **coupled inductors** has primary winding , secondary winding and air gap as the core.
- The most commonly used switch is a **enhancement mode N-channel MOSFET**.
- The DC voltage is usually **switched DC (DC voltage from a rectifier)**.



Operation:

Mode 1: (Freewheeling Mode)

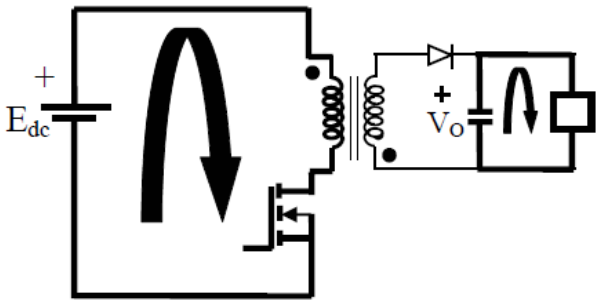


Fig.22.2(a): Current path during Mode-1 of circuit operation

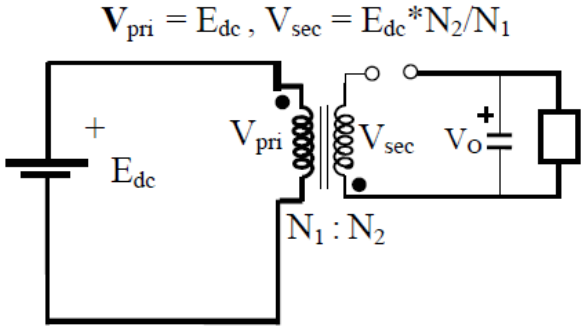


Fig.22.2(b): Equivalent circuit in Mode-1

- When the switch (MOSFET) is turned ON by applying gate signal , the dotted end of the primary winding of the transformer gets connected to the positive terminal of battery. The undotted end of the primary winding gets connected through the MOSFET to the negative terminal of the battery.
- The current flow in the primary induces a current into the dotted end of the secondary. As a result , the dotted end of the secondary is at higher potential than the undotted end. Since the anode of the diode is connected to the undotted end of the secondary and cathode of the diode is connected to the dotted end of the secondary , the diode gets reverse biased.
- At the end of mode 1 , the load receives uninterrupted current from the capacitor that was pre-charged.
- The voltage across the diode is given as follows:

$$(V_{diode} = V_O + E_{DC} \times N_2 / N_1).$$

- During mode-1 , the current through the primary winding **ramps up(linearly rises)** to $0.5\times L_{PR} \times I_{PR}^2$, where L_{PR} is the self-inductance of primary winding and I_{PR} is the DC current flowing through primary winding.

Mode 2: (Powering Mode)

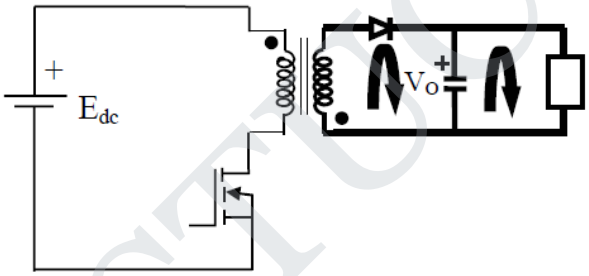


Fig:22.3(a) : Current path during Mode-2 of circuit operation

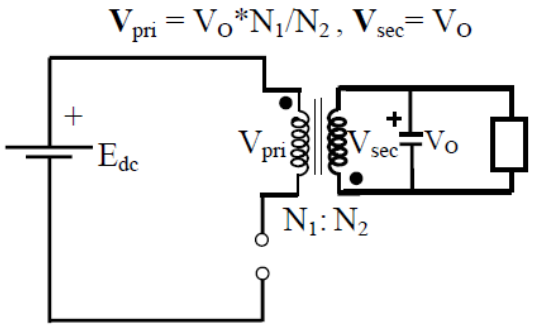


Fig.22.3(b): Equivalent circuit in Mode-2

- When the switch S is turned OFF , according to laws to electromagnetic induction , the polarity of the primary winding gets reversed. That is the dotted end is at lower potential and undotted end is at higher potential. As a result , the dotted end of the secondary winding is at lower potential and undotted end is at higher potential . As a result , the diode gets forward biased and capacitor C gets charged.
- At the close of the switch , the secondary current is at its peak value and **ramps down(linearly falls)** discharging stored energy to the load.
- Current entering the dotted ends of a winding (primary or secondary) produces positive MMF and current entering the undotted ends of a winding(primary or secondary) produces negative MMF.
- Positive MMF produces positive EMF ; Negative MMF produces negative EMF.

If the OFF period of the switch is large , MODE 2 is called **CONTINUOUS FLUX MODE**; If the OFF period of the switch is small , MODE 2 is called **DISCONTINUOUS FLUX MODE**.

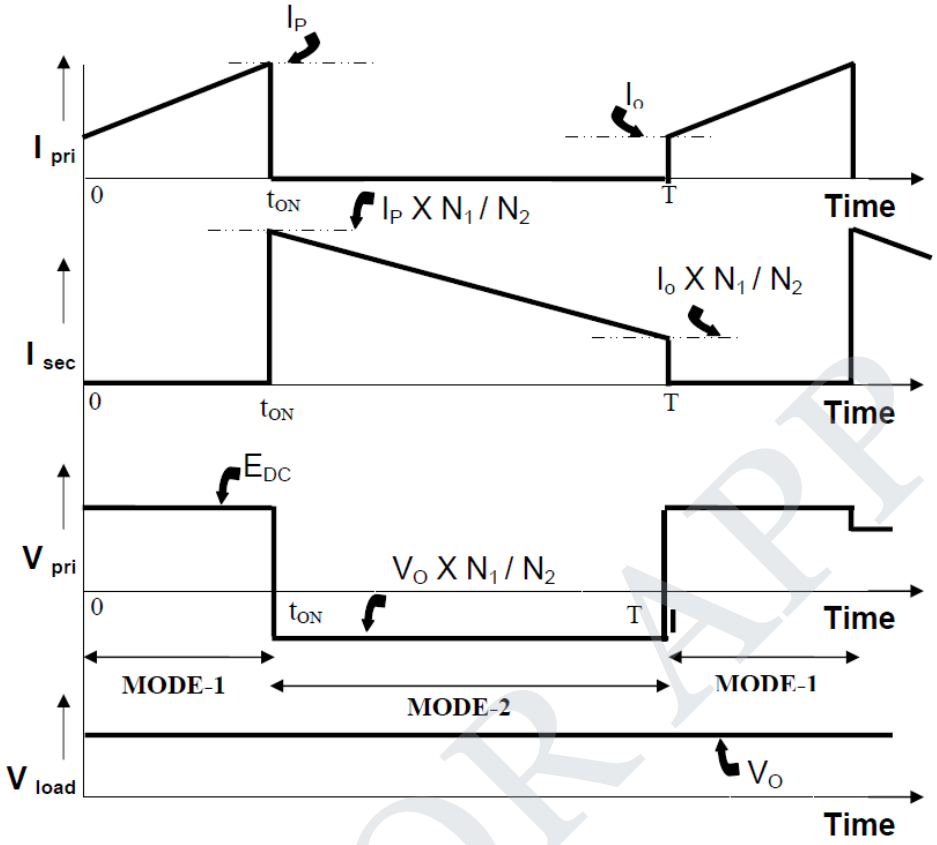
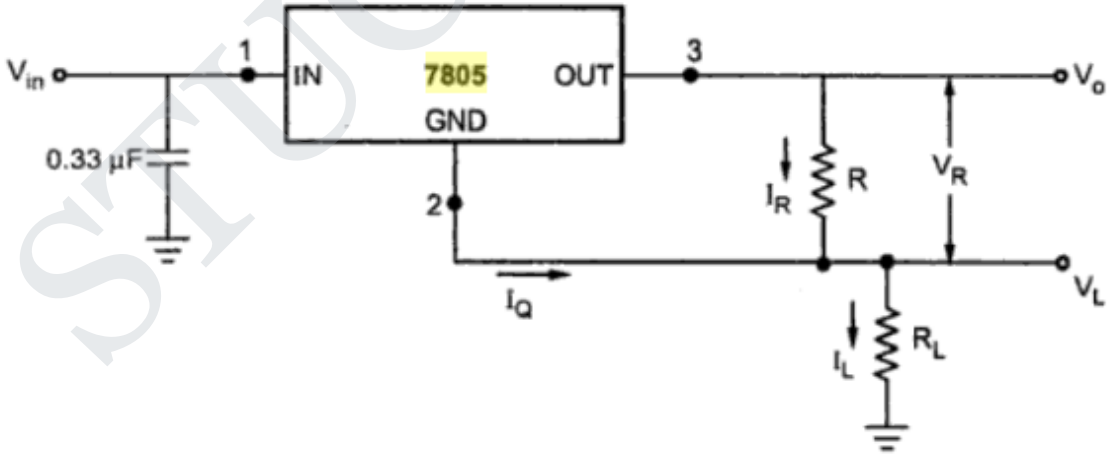


Fig.22.5(a): Fly-back circuit waveforms under continuous magnetic flux

14. Using 7805 design a current source to deliver a 0.2 A current to a 22 Ω 10 W load.(15)



Current through load resistance R_L

$$I_L = I_R + I_Q = \frac{V_R}{R} + I_Q$$

I_Q = 4.2 mA[Quiescent Current of IC 7805]
V_R = 5 V
I_L = 0.2 A , R_L = 22 Ω , Dropout Voltage = 2 V
Therefore 0.2 = (5/R) + 4.2× 10^{-3}

Therefore R = 25.536 Ω

$V_O = V_R + V_L = 5 + I_L R_L = 5 + (0.2 \times 22) = 9.4$ V

$V_{IN} = V_O$ + Dropout Voltage = 9.4 + 2 = 11.4 V