UNIT –I IC FABRICATION

Integrated Circuits:

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

Advantages of integrated circuits:

Miniaturization and hence increased equipment density.
Cost reduction due to batch processing.
Increased system reliability due to the elimination of soldered joints.
Improved functional performance.
Matched devices.
Increased operating speeds.
Reduction in power consumption

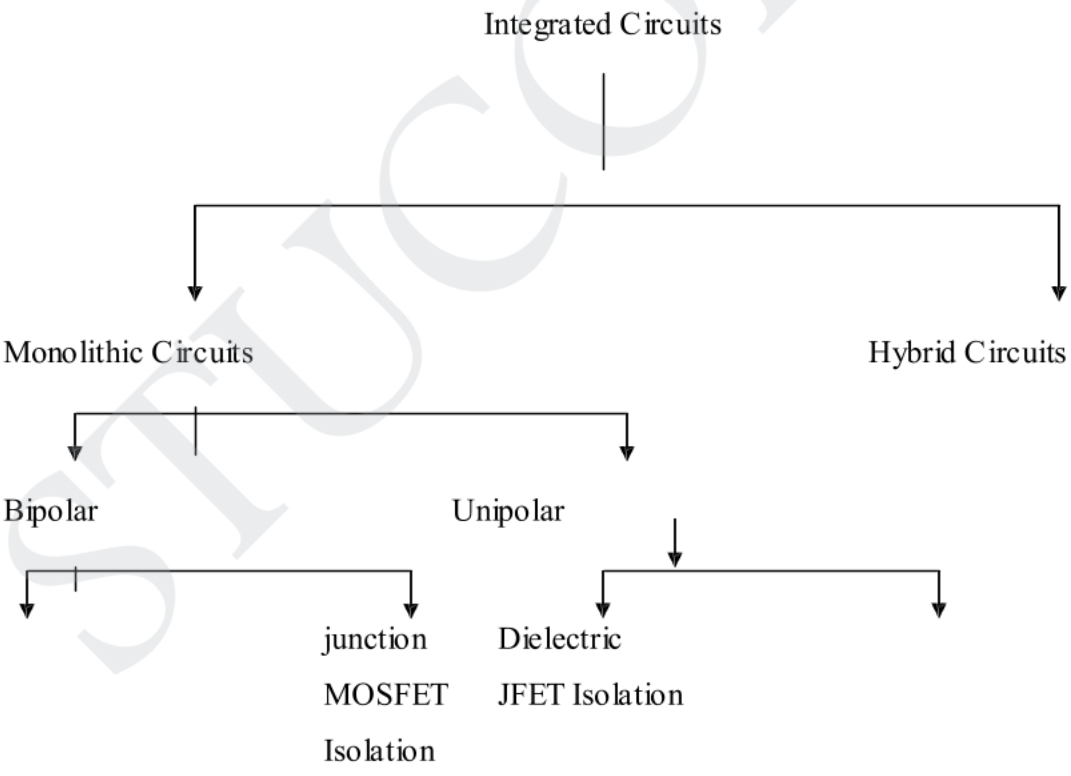
Classification:

Integrated circuits can be classified into analog, digital and mixed signal (both analog and digital on the same chip). Based upon above requirement two different IC technology namely Monolithic Technology and Hybrid Technology have been developed. In monolithic IC ,all circuit components ,both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bounds.

Digital integrated circuits can contain anything from one to millions of logic gates, flip-flops, multiplexers, and other circuits in a few square millimeters. The small size of these circuits allows high speed, low power dissipation, and reduced manufacturing cost compared with board-level integration. These digital ICs, typically microprocessors, DSPs, and micro controllers work using binary mathematics to process "one" and "zero" signals.

Analog ICs, such as sensors, power management circuits, and operational amplifiers, work by processing continuous signals. They perform functions like amplification, active filtering, demodulation, mixing, etc. Analog ICs ease the burden on circuit designers by having expertly designed analog circuits available instead of designing a difficult analog circuit from scratch.
ICs can also combine analog and digital circuits on a single chip to create functions such as A/D converters and D/A converters. Such circuits offer smaller size and lower cost, but must carefully account for signal interference

Classification of ICs:



Generations

SSI, MSI and LSI

The first integrated circuits contained only a few transistors. Called "Small-Scale Integration" (SSI), digital circuits containing transistors numbering in the tens provided a few logic gates for example, while early linear ICs such as the Plessey SL201 or the Philips TAA320 had as few as two transistors. The term Large Scale Integration was first used by IBM scientist Rolf Landauer when describing the theoretical concept, from there came the terms for SSI, MSI, VLSI, and ULSI. They began to appear in consumer products at the turn of the decade, a typical application being FM inter-carrier sound processing in television receivers.

The next step in the development of integrated circuits, taken in the late 1960s, introduced devices which contained hundreds of transistors on each chip, called "Medium-Scale Integration" (MSI). They were attractive economically because while they cost little more to produce than SSI devices, they allowed more complex systems to be produced using smaller circuit boards, less assembly work (because of fewer separate components), and a number of other advantages.

VLSI

The final step in the development process, starting in the 1980s and continuing through the present, was "very large-scale integration" (VLSI). The development started with hundreds of thousands of transistors in the early 1980s, and continues beyond several billion transistors as of 2007.

In 1986 the first one megabit RAM chips were introduced, which contained more than one million transistors. Microprocessor chips passed the million transistor mark in 1989 and the billion transistor mark in 2005

ULSI, WSI, SOC and 3D-IC

To reflect further growth of the complexity, the term ULSI that stands for "Ultra-Large Scale Integration" was proposed for chips of complexity of more than 1 million transistors.

Wafer-scale integration (WSI) is a system of building very-large integrated circuits that uses an entire silicon wafer to produce a single "super-chip". Through a combination of large size and reduced packaging, WSI could lead to dramatically reduced costs for some systems, notably

massively parallel supercomputers. The name is taken from the term Very-Large-Scale Integration, the current state of the art when WSI was being developed.

System-on-a-Chip (SoC or SOC) is an integrated circuit in which all the components needed for a computer or other system are included on a single chip. The design of such a device can be complex and costly, and building disparate components on a single piece of silicon may compromise the efficiency of some elements.

However, these drawbacks are offset by lower manufacturing and assembly costs and by a greatly reduced power budget: because signals among the components are kept on-die, much less power is require. Three Dimensional Integrated Circuit (3D-IC) has two or more layers of active electronic components that are integrated both vertically and horizontally into a single circuit. Communication between layers uses on-die signaling, so power consumption is much lower than in equivalent separate circuits. Judicious use of short vertical wires can substantially reduce overall wire length for faster operation.

Construction of a Monolithic Bipolar Transistor:

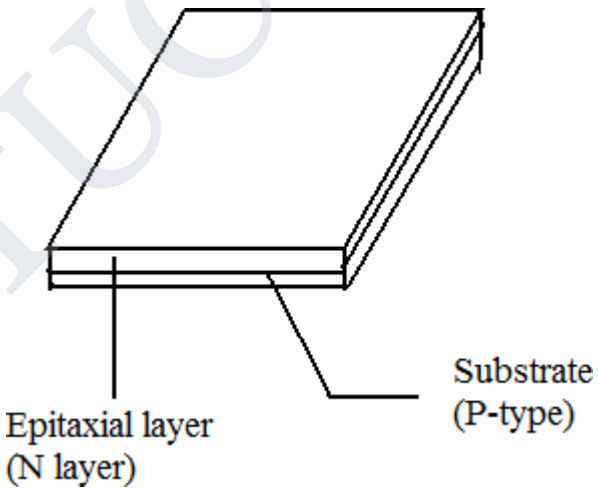
The fabrication of a monolithic transistor includes the following steps.

1. Epitaxial growth
2. Oxidation
3. Photolithography
4. Isolation diffusion
5. Base diffusion
6. Emitter diffusion
7. Contact mask
8. Aluminium metallization
9. Passivation

The letters P and N in the figures refer to type of doping, and a minus (-) or plus (+) with P and N indicates lighter or heavier doping respectively.

1. Epitaxial growth:

The first step in transistor fabrication is creation of the collector region. We normally require a low resistivity path for the collector current. This is due to the fact that, the collector contact is normally taken at the top, thus increasing the collector series resistance and the $V_{CE(Sat)}$ of the device.



The higher collector resistance is reduced by a process called buried layer as shown in figure. In this arrangement, a heavily doped _N' region is sandwiched between the N-type epitaxial layer and

P – type substrate. This buried N^+ layer provides a low resistance path in the active collector region to the collector contact C. In effect, the buried layer provides a low resistance shunt path for the flow of current.

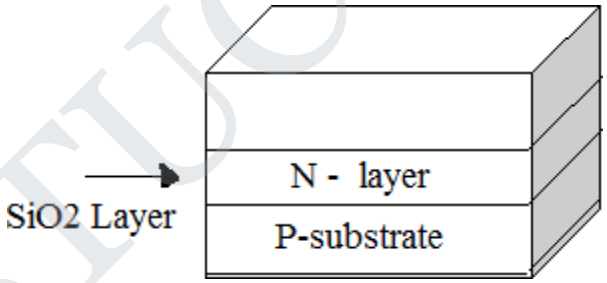
For fabricating an NPN transistor, we begin with a P-type silicon substrate having a resistivity of typically 1Ω-cm, corresponding to an acceptor ion concentration of $1.4 * 10^{15}$ atoms/cm^3 . An oxide mask with the necessary pattern for buried layer diffusion is prepared. This is followed by masking and etching the oxide in the buried layer mask.

The N-type buried layer is now diffused into the substrate. A slow-diffusing material such as arsenic or antimony us used, so that the buried layer will stay-put during subsequent diffusions. The junction depth is typically a few microns, with sheet resistivity of around 20Ω per square.

Then, an epitaxial layer of lightly doped N-silicon is grown on the P-type substrate by placing the wafer in the furnace at 1200^0 C and introducing a gas containing phosphorus (donor impurity). The resulting structure is shown in figure.

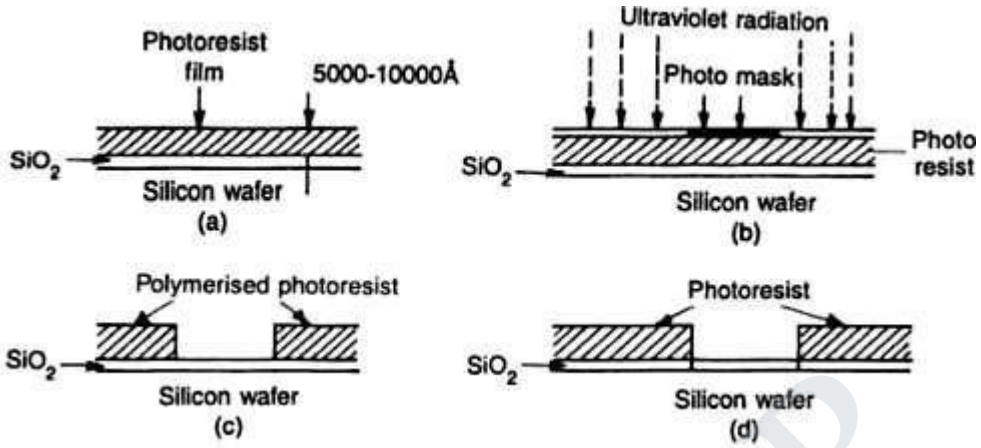
The subsequent diffusions are done in this epitaxial layer. All active and passive components are formed on the thin N-layer epitaxial layer grown over the P-type substrate. Obtaining an epitaxial layer of the proper thickness and doping with high crystal quality is perhaps the most formidable challenge in bipolar device processing.

2. Oxidation:



As shown in figure, a thin layer of silicon dioxide (SiO_2) is grown over the N-type layer by exposing the silicon wafer to an oxygen atmosphere at about 1000^0 C.

3. Photolithography:



The prime use of photolithography in IC manufacturing is to selectively etch or remove the SiO_2 layer. As shown in figure, the surface of the oxide is first covered with a thin uniform layer of photosensitive emulsion (Photo resist). The mask, a black and white negative of the requied pattern, is placed over the structure. When exposed to ultraviolet light, the photo resist under the transparent region of the mask becomes poly-merized. The mask is then removed and the wafer is treated chemically that removes the unexposed portions of the photoresist film. The polymerized region is cured so that it becomes resistant to corrosion. Then the chip is dipped in an etching solution of hydrofluoric acid which removes the oxide layer not protected by the polymerized photoresist. This creates openings in the SiO_2 layer through which P-type or N-type impurities can be diffused using the isolation diffusion process as shown in figure. After diffusion of impurities, the polymerized photoresist is removed with sulphuric acid and by a mechanical abrasion process.

4. Isolation Diffusion:

The integrated circuit contains many devices. Since a number of devices are to be fabricated on the same IC chip, it becomes necessary to provide good isolation between various components and their interconnections.

The most important techniques for isolation are:

1. PN junction Isolation
2. Dielectric Isolation

In PN junction isolation technique, the P^+ type impurities are selectively diffused into the N-type epitaxial layer so that it touches the P-type substrate at the bottom. This method generated N-type isolation regions surrounded by P-type moats. If the P-substrate is held at the most negative potential, the diodes will become reverse-biased, thus providing isolation between these islands.

The individual components are fabricated inside these islands. This method is very economical, and is the most commonly used isolation method for general purpose integrated circuits.

In dielectric isolation method, a layer of solid dielectric such as silicon dioxide or ruby surrounds each component and this dielectric provides isolation. The isolation is both physical and electrical. This method is very expensive due to additional processing steps needed and this is mostly used for fabricating IC's required for special application in military and aerospace.

The PN junction isolation diffusion method is shown in figure. The process take place in a furnace using boron source. The diffusion depth must be atleast equal to the epitaxial thickness in order to obtain complete isolation. Poor isolation results in device failures as all transistors might get shorted together. The N-type island shown in figure forms the collector region of the NPN transistor. The heavily doped P-type regions marked P^+ are the isolation regions for the active and passive components that will be formed in the various N-type islands of the epitaxial layer.

5 Base diffusion:

Formation of the base is a critical step in the construction of a bipolar transistor. The base must be aligned, so that, during diffusion, it does not come into contact with either the isolation region or the buried layer. Frequently, the base diffusion step is also used in parallel to fabricate diffused resistors for the circuit. The value of these resistors depends on the diffusion conditions and the width of the opening made during etching. The base width influences the transistor parameters very strongly. Therefore, the base junction depth and resistivity must be tightly controlled. The base sheet resistivity should be fairly high (200- 500Ω per square) so that the base does not inject carriers into the emitter. For NPN transistor, the base is diffused in a furnace using a boron source. The diffusion process is done in two steps, pre deposition of dopants at 900^0 C and driving them in at about 1200^0 C. The drive-in is done in an oxidizing ambience, so that oxide is grown over the base region for subsequent fabrication steps. Figure shows that P-type base region of the transistor diffused in the N-type island (collector region) using photolithography and isolation diffusion processes.

6. Emitter Diffusion:

Emitter Diffusion is the final step in the fabrication of the transistor. The emitter opening must lie wholly within the base. Emitter masking not only opens windows for the emitter, but also for the contact point, which provides a low resistivity ohmic contact path for the emitter terminal.

The emitter diffusion is normally a heavy N-type diffusion, producing low-resistivity layer that can inject charge easily into the base. A Phosphorus source is commonly used so that the diffusion time id shortened and the previous layers do not diffuse further. The emitter is diffused into the base, so that the emitter junction depth very closely approaches the base junction depth. The active base is then a P-region between these two junctions which can be made very narrow by adjusting the emitter diffusion time. Various diffusion and drive in cycles can be used to fabricate the emitter. The Resistivity of the emitter is usually not too critical.

The N-type emitter region of the transistor diffused into the P-type base region is shown below. However, this is not needed to fabricate a resistor where the resistivity of the P-type base region itself will serve the purpose. In this way, an NPN transistor and a resistor are fabricated simultaneously.

7. Contact Mask:

After the fabrication of emitter, windows are etched into the N-type regions where contacts are to be made for collector and emitter terminals. Heavily concentrated phosphorus N^+ dopant is diffused into these regions simultaneously.

The reasons for the use of heavy N^+ diffusion is explained as follows: Aluminium, being a good conductor used for interconnection, is a P-type of impurity when used with silicon. Therefore, it can produce an unwanted diode or rectifying contact with the lightly doped N-material. Introducing a high concentration of N^+ dopant caused the Si lattice at the surface semi-metallic. Thus the N^+ layer makes a very good ohmic contact with the Aluminium layer. This is done by the oxidation, photolithography and isolation diffusion processes.

8. Metallization:

The IC chip is now complete with the active and passive devices, and the metal leads are to be formed for making connections with the terminals of the devices. Aluminium is deposited over the entire wafer by vacuum deposition. The thickness for single layer metal is 1μ m. Metallization is carried out by evaporating aluminium over the entire surface and then selectively etching away aluminium to leave behind the desired interconnection and bonding pads as shown in figure.

Metallization is done for making interconnection between the various components fabricated in an IC and providing bonding pads around the circumference of the IC chip for later connection of wires

9. Passivation/ Assembly and Packaging:

Metallization is followed by passivation, in which an insulating and protective layer is deposited over the whole device. This protects it against mechanical and chemical damage during subsequent processing steps. Doped or undoped silicon oxide or silicon nitride, or some combination of them, are usually chosen for passivation of layers. The layer is deposited by chemical vapour deposition (CVD) technique at a temperature low enough not to harm the metallization.

Transistor Fabrication:

PNP Transistor:

The integrated PNP transistors are fabricated in one of the following three structures.

1. Substrate or Vertical PNP
2. Lateral or horizontal PNP and
3. Triple diffused PNP

Substrate or Vertical PNP:

The P-substrate of the IC is used as the collector, the N-epitaxial layer is used as the base and the next P-diffusion is used as the emitter region of the PNP transistor. The structure of a vertical monolithic PNP transistor Q_1 is shown in figure. The base region of an NPN transistor structure is formed in parallel with the emitter region of the PNP transistor.

The method of fabrication has the disadvantage of having its collector held at a fixed negative potential. This is due to the fact that the P-substrate of the IC is always held at a negative potential normally for providing good isolation between the circuit components and the substrate.

Triple diffused PNP:

This type of PNP transistor is formed by including an additional diffusion process over the standard NPN transistor processing steps. This is called a triple diffusion process, because it involves an additional diffusion of P-region in the second N-diffusion region of a NPN transistor. The structure of the triple diffused monolithic PNP transistor Q_2 is also shown in the below figure.

This has the limitations of requiring additional fabrication steps and sophisticated fabrication assemblies.

Lateral or Horizontal PNP:

This is the most commonly used form of integrated PNP transistor fabrication method. This has the advantage that it can be fabricated simultaneously with the processing steps of an NPN transistor and therefore it requires as the base of the PNP transistor. During the P-type base diffusion process of NPN transistor, two parallel P-regions are formed which make the emitter and collector regions of the horizontal PNP transistor.

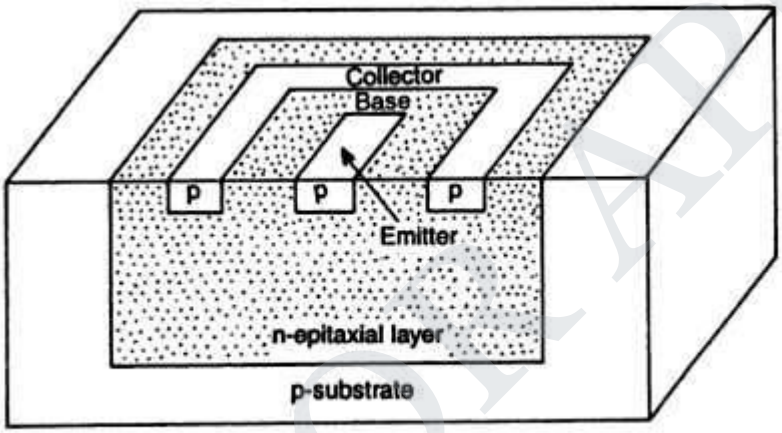


Fig. 1.17 A *pnp* lateral transistor

Comparison of monolithic NPN and PNP transistor:

Normally, the NPN transistor is preferred in monolithic circuits due to the following reasons:

1. The vertical PNP transistor must have his collector held at a fixed negative voltage.

2. The lateral PNP transistor has very wide base region and has the limitation due to the lateral diffusion of P-type impurities into the N-type base region. This makes the photographic mask making, alignment and etching processes very difficult. This reduces the current gain of lateral PNP transistors as low as 1.5 to 30 as against 50 to 300 for a monolithic NPN transistor.

3. The collector region is formed prior to the formation of base and emitter diffusion. During the later diffusion steps, the collector impurities diffuse on either side of the defined collector junction. Since the N-type impurities have smaller diffusion constant compared to P-type impurities the N-

type collector performs better than the P-type collector. This makes the NPN transistor preferable for monolithic fabrication due to the easier process control.

Transistor with multiple emitters: The applications such as transistor- transistor logic (TTL) require multiple emitters. The below figure shows the circuit sectional view of three N-emitter regions diffused in three places inside the P-type base. This arrangement saves the chip area and enhances the component density of the IC.

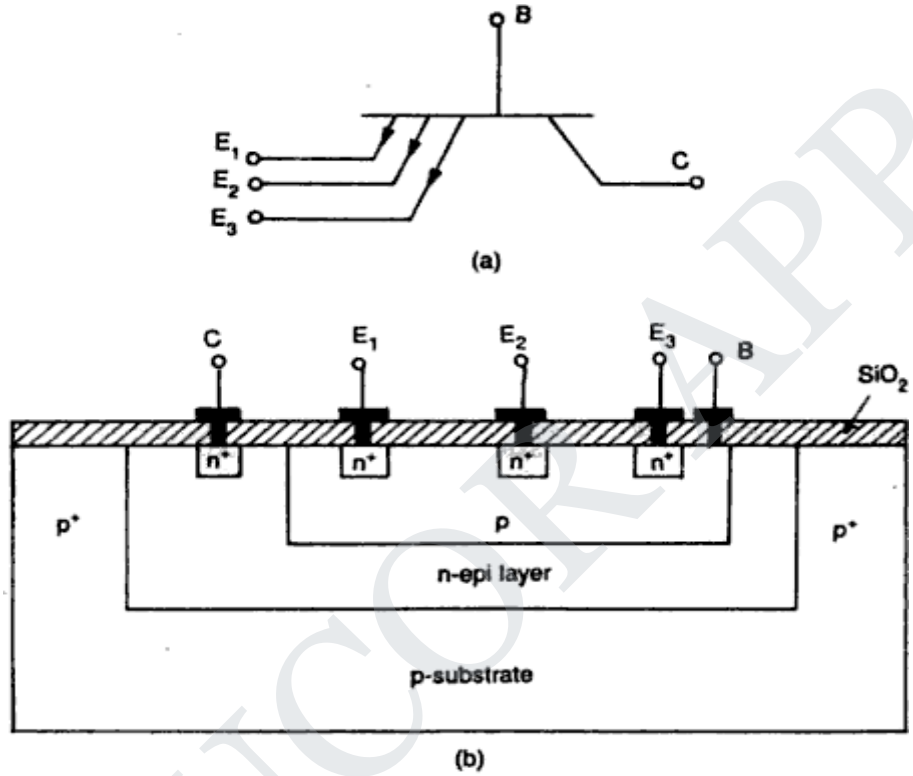


Fig. 1.18 (a) Multi-emitter transistor, (b) Cross-sectional view of a multi-emitter transistor

Schottky Barrier Diode:

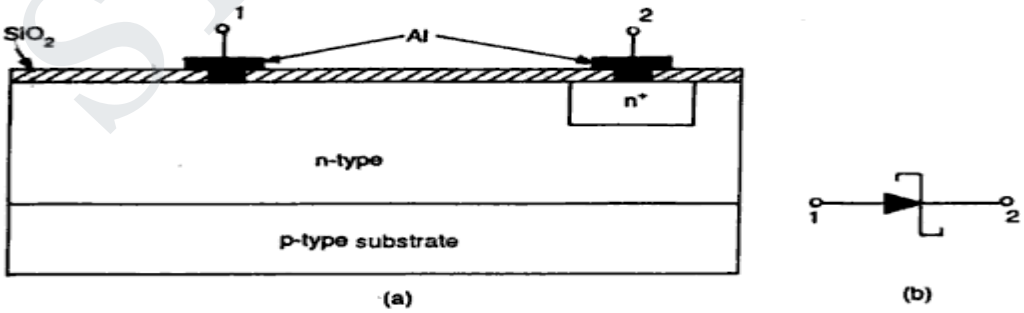


Fig. 1.21 (a) A Schottky diode, (b) Symbol for metal semiconductor diode

The metal contacts are required to be ohmic and no PN junctions to be formed between the metal and silicon layers. The N^+ diffusion region serves the purpose of generating ohmic contacts. On the other hand, if aluminium is deposited directly on the N-type silicon, then a metal semiconductor diode can be said to be formed. Such a metal semiconductor diode junction exhibits the same type of V-I Characteristics as that of an ordinary PN junction.

The cross sectional view and symbol of a Schottky barrier diode as shown in figure. Contact 1 shown in figure is a Schottky barrier and the contact 2 is an ohmic contact. The contact potential between the semiconductor and the metal generated a barrier for the flow of conducting electrons from semiconductor to metal. When the junction is forward biased this barrier is lowered and the electron flow is allowed from semiconductor to metal, where the electrons are in large quantities.

The minority carriers carry the conduction current in the Schottky diode whereas in the PN junction diode, minority carriers carry the conduction current and it incurs an appreciable time delay from ON state to OFF state. This is due to the fact that the minority carriers stored in the junction have to be totally removed. This characteristic puts the Schottky barrier diode at an advantage since it exhibits negligible time to flow the electron from N-type silicon into aluminum almost right at the contact surface, where they mix with the free electrons. The other advantage of this diode is that it has less forward voltage (approximately 0.4V). Thus it can be used for clamping and detection in high frequency applications and microwave integrated circuits.

Schottky transistor:

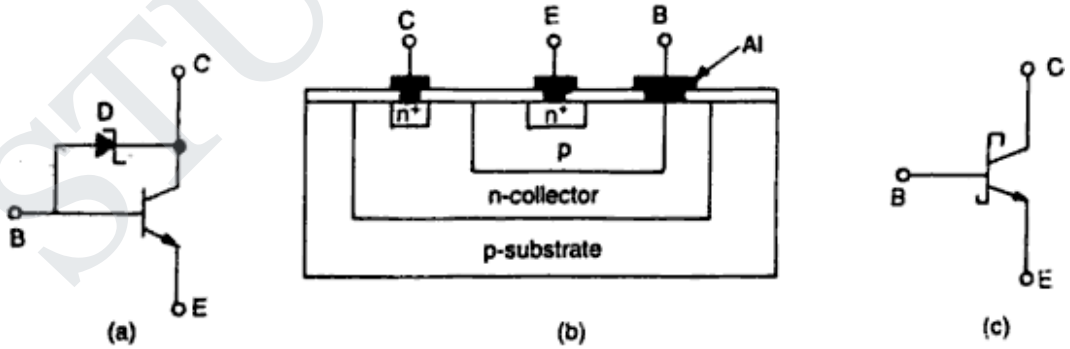


Fig. 1.19 (a) A transistor with a Schottky-barrier diode clamped between base and collector to prevent saturation, (b) Cross-section of a Schottky-barrier transistor, (c) Symbolic representation

The cross-sectional view of a transistor employing a Schottky barrier diode clamped between its base and collector regions is shown in figure. The equivalent circuit and the symbolic representation of the Schottky transistor are shown in figure. The Schottky diode is formed by allowing aluminium metallization for the base lead which makes contact with the N-type collector region also as shown in figure.

When the base current is increased to saturate the transistor, the voltage at the collector C reduces and this makes the diode Ds conduct. The base to collector voltage reduces to 0.4V, which is less the cut-in-voltage of a silicon base-collector junction. Therefore, the transistor does not get saturated.

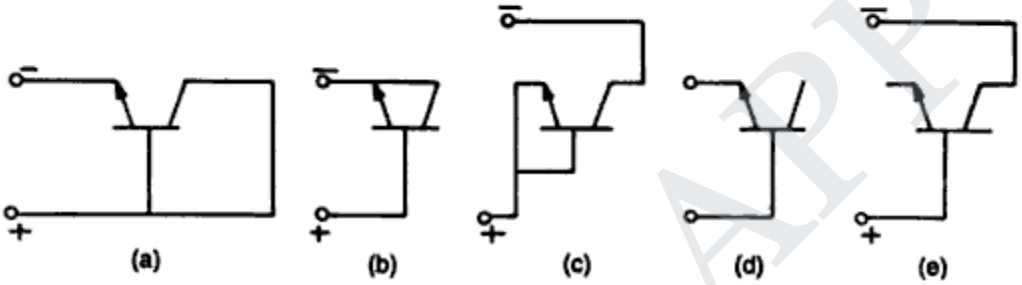
Monolithic diodes:

The diode used in integrated circuits are made using transistor structures in one of the five possible connections. The three most popular structures are shown in figure. The diode is obtained from a transistor structure using one of the following structures.

1. The emitter-base diode, with collector short circuited to the base.
2. The emitter-base diode with the collector open and
3. The collector –base diode, with the emitter open-circuited.

The choice of the diode structure depends on the performance and application desired. Collector-base diodes have higher collector-base arrays breaking rating, and they are suitable for common-cathode diode arrays diffused within a single isolation island. The emitter-base diffusion is very popular for the fabrication of diodes, provided the reverse-voltage requirement of the circuit does not exceed the lower base-emitter breakdown voltage.

Characteristic	(a) $V_{CB} = 0$	(b) $V_{CE} = 0$	(c) $V_{EB} = 0$	(d) $I_C = 0$	(e) $I_E = 0$
Breakdown voltage in volts	7	7	55	7	55
Storage time, n sec	9	100	53	56	85
Forward voltage in volts	.85	.92	.94	.96	.95



Integrated Resistors:

A resistor in a monolithic integrated circuit is obtained by utilizing the bulk resistivity of the diffused volume of semiconductor region. The commonly used methods for fabricating integrated resistors are 1. Diffused 2. epitaxial 3. Pinched and 4. Thin film techniques.

Diffused Resistor:

The diffused resistor is formed in any one of the isolated regions of epitaxial layer during base or emitter diffusion processes. This type of resistor fabrication is very economical as it runs in parallel to the bipolar transistor fabrication. The N-type emitter diffusion and P-type base diffusion are commonly used to realize the monolithic resistor.

The diffused resistor has a severe limitation in that, only small valued resistors can be fabricated. The surface geometry such as the length, width and the diffused impurity profile determine the resistance value. The commonly used parameter for defining this resistance is called the sheet resistance. It is defined as the resistance in ohms/square offered by the diffused area.

In the monolithic resistor, the resistance value is expressed by

$R = R_s\ 1/w$ where R= resistance offered (in ohms)

R_s = sheet resistance of the particular fabrication process involved (in ohms/square)
l = length of the diffused area and

w = width of the diffused area.

The sheet resistance of the base and emitter diffusion in 200Ω/Square and 2.2Ω/square respectively. For example, an emitter-diffused strip of 2mil wide and 20 mil long will offer a resistance of 22Ω. For higher values of resistance, the diffusion region can be formed in a zig-zag fashion resulting in larger effective length. The poly silicon layer can also be used for resistor realization.

Epitaxial Resistor:

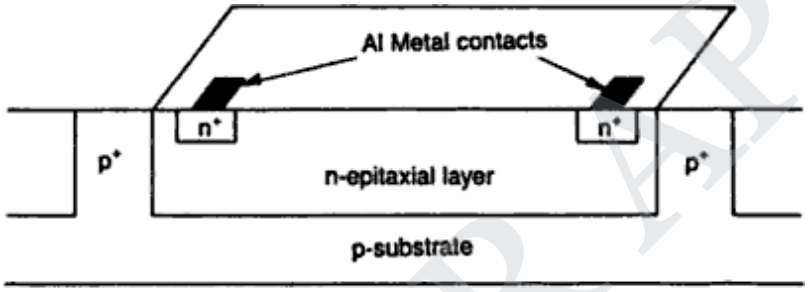


Fig. 1.23 (a) Epitaxial resistor

The N-epitaxial layer can be used for realizing large resistance values. The figure shows the cross-sectional view of the epitaxial resistor formed in the epitaxial layer between the two N^+ aluminium metal contacts.

Pinched resistor:

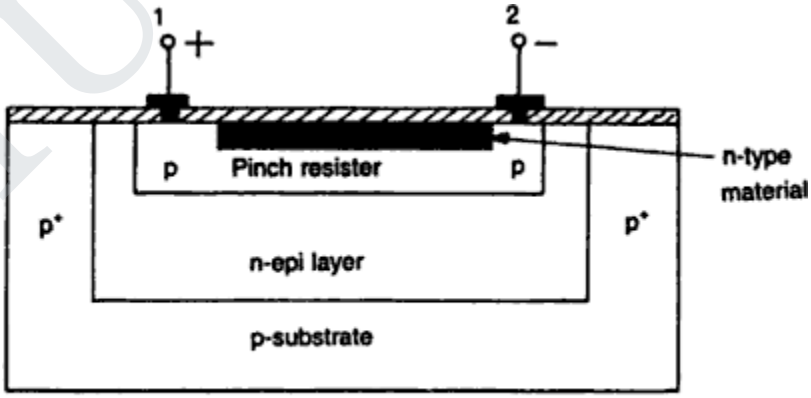


Fig. 1.23 (b) Cross-sectional view of a pinch resistor

The sheet resistance offered by the diffusion regions can be increased by narrowing down its cross-sectional area. This type of resistance is normally achieved in the base region. Figure shows a pinched base diffused resistor. It can offer resistance of the order of mega ohms in a

comparatively smaller area. In the structure shown, no current can flow in the N-type material since the diode realized at contact 2 is biased in reversed direction. Only very small reverse saturation current can flow in conduction path for the current has been reduced or pinched. Therefore, the resistance between the contact 1 and 2 increases as the width narrows down and hence it acts as a pinched resistor.

Thin film resistor:

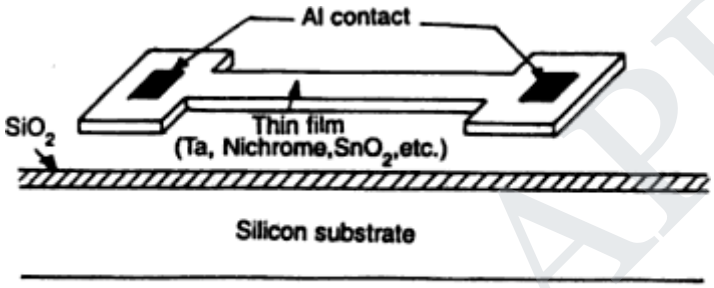


Fig. 1.23 (c) Cross-section of a thin film resistor

The thin film deposition technique can also be used for the fabrication of monolithic resistors. A very thin metallic film of thickness less than 1µm is deposited on the silicon dioxide layer by vapour deposition techniques. Normally, Nichrome (NiCr) is used for this process. Desired geometry is achieved using masked etching processes to obtain suitable value of resistors. Ohmic contacts are made using aluminium metallization as discussed in earlier sections.

The cross-sectional view of a thin film resistor as shown in figure. Sheet resistances of 40 to 400Ω/ square can be easily obtained in this method and thus 20kΩ to 50kΩ values are very practical.

The advantages of thin film resistors are as follows:

1. They have smaller parasitic components which makes their high frequency behaviour good.
2. The thin film resistor values can be very minutely controlled using laser trimming.
3. They have low temperature coefficient of resistance and this makes them more stable.

The thin film resistor can be obtained by the use of tantalum deposited over silicon dioxide layer. The main disadvantage of thin film resistor is that its fabrication requires additional processing steps.

Monolithic Capacitors:

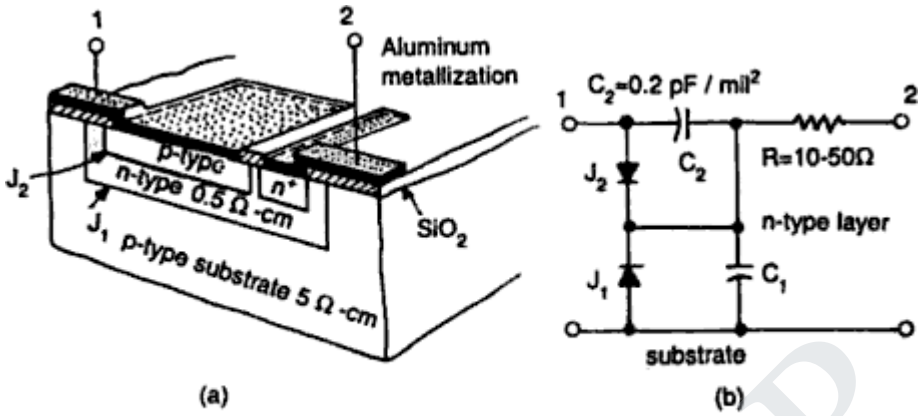


Fig. 1.24 (a) Junction-type IC capacitor, (b) Equivalent circuit

Monolithic capacitors are not frequently used in integrated circuits since they are limited in the range of values obtained and their performance. There are, however, two types available, the junction capacitor is a reverse biased PN junction formed by the collector-base or emitter-base diffusion of the transistor. The capacitance is proportional to the area of the junction and inversely proportional to the depletion thickness.

C α A, where a is the area of the junction and

C α T , where t is the thickness of the depletion layer.

The capacitance value thus obtainable can be around 1.2nF/mm^2 .

The thin film or metal oxide silicon capacitor uses a thin layer of silicon dioxide as the dielectric. One plate is the connecting metal and the other is a heavily doped layer of silicon, which is formed during the emitter diffusion. This capacitor has a lower leakage current and is non-directional, since emitter plate can be biased positively. The capacitance value of this method can be varied between 0.3 and 0.8nF/mm^2 .

Inductors:

No satisfactory integrated inductors exist. If high Q inductors with inductance of values larger than 5μH are required, they are usually supplied by a wound inductor which is connected externally to the chip. Therefore, the use of inductors is normally avoided when integrated circuits are used.

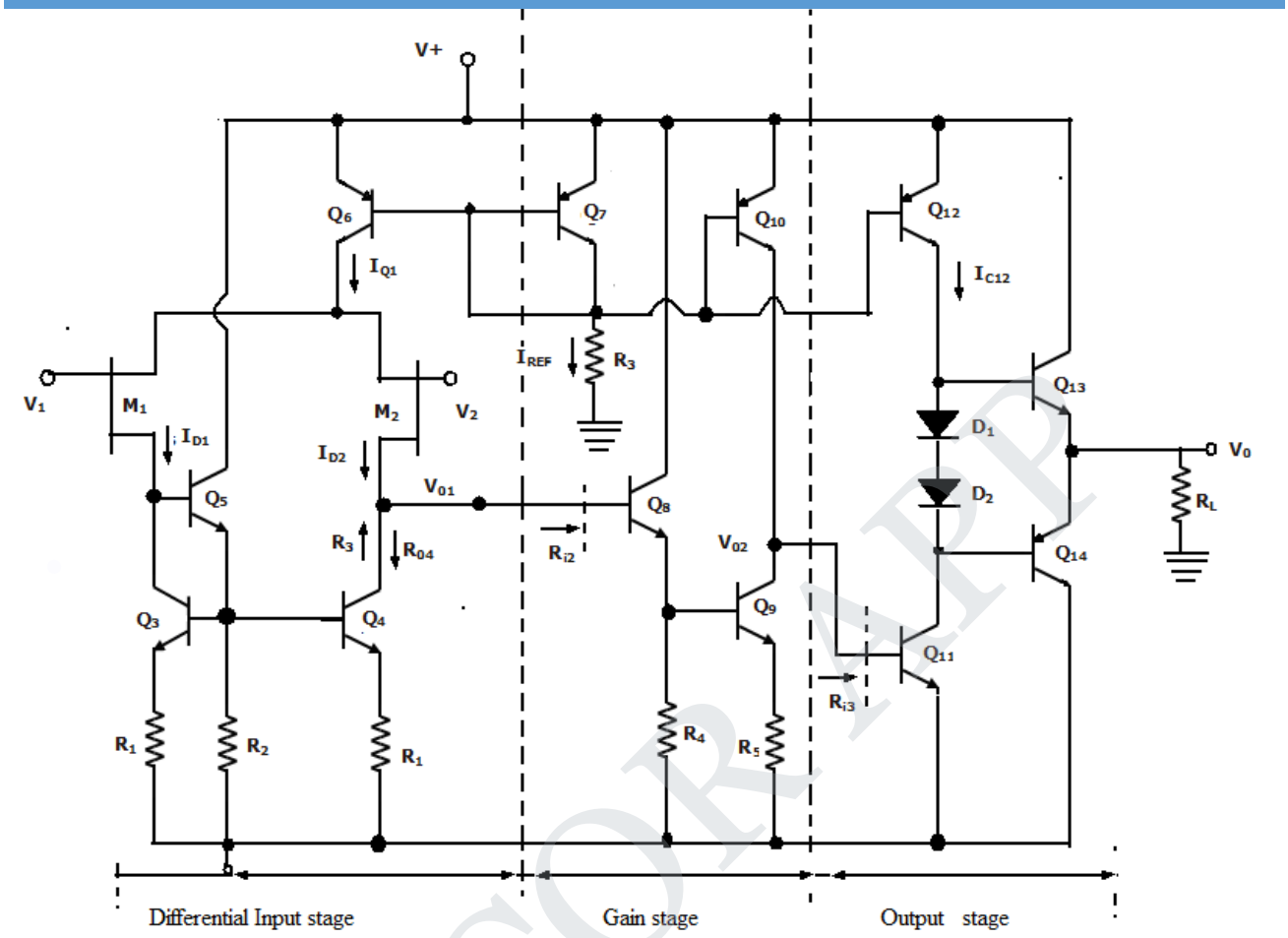
UNIT II

CHARACTERISTICS OF OPAMP

General Operational Amplifier:

An operational amplifier generally consists of three stages, anmely,1. a differential amplifier 2. additional amplifier stages to provide the required voltage gain and dc level shifting 3. an emitter-follower or source follower output stage to provide current gain and low output resistance.

A low-frequency or dc gain of approximately 10^4 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp. The output voltage is required to be at ground, when the differential input voltages is zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of picoamperes, an FET input stage is normally preferred. The figure shows a general op-amp circuit using JFET input devices.



Input stage:

The input differential amplifier stage uses p-channel JFETs M_1 and M_2. It employs a three-transistor active load formed by Q_3 , Q_4 , and Q_5 . the bias current for the stage is provided by a two-transistor current source using PNP transistors Q_6 and Q_7. Resistor R_1 increases the output resistance seen looking into the collector of Q_4 as indicated by R_{04}. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R_2 establishes a definite bias current through Q_5 . A single ended output is taken out at the collector of Q_4 .

MOSFET‘s are used in place of JFETs with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

Gain stage:

The second stage or the gain stage uses Darlington transistor pair formed by Q_8 and Q_9 as shown in figure. The transistor Q_8 is connected as an emitter follower, providing large input resistance.Therefore, it minimizes the loading effect on the input differential amplifier stage. The

transistor Q_9 provides an additional gain and Q_{10} acts as an active load for this stage. The current mirror formed by Q_7 and Q_{10} establishes the bias current for Q_9 . The V_{BE} drop across Q_9 and drop across R_5 constitute the voltage drop across R_4 , and this voltage sets the current through Q_8 . It can be set to a small value, such that the base current of Q_8 also is very less.

Output stage:

The final stage of the op-amp is a class AB complementary push-pull output stage. Q_{11} is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q_{11} is provided by the current mirror formed by Q_7 and $Q_{12,}$ through Q_{13} and Q_{14} for minimizing the cross over distortion. Transistors can also be used in place of the two diodes.

The overall voltage gain A_V of the op-amp is the product of voltage gain of each stage as given by

$A_V = |A_d ||A_2||A_3|$

Where A_d is the gain of the differential amplifier stage, A_2 is the gain of the second gain stage and A_3 is the gain of the output stage.

IC 741 Bipolar operational amplifier:

The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure shows that equivalent circuit of the 741 op-amp, divided into various individual stages. The op-amp circuit consists of three stages.

1. the input differential amplifier
2. The gain stage
3. the output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the IC. The op-amp is supplied with positive and negative supply voltages of value ± 15V, and the supply voltages as low as ±5V can also be used.

Bias Circuit:

The reference bias current I_{REF} for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q_{11} and Q_{12} and resistor $R_{5.}$ The widlar current source formed by Q_{11} , Q_{10} and R_4 provide bias current for the differential amplifier stage at the collector of $Q_{10.}$

Transistors Q_8 and Q_9 form another current mirror providing bias current for the differential

amplifier. The reference bias current I_{REF} also provides mirrored and proportional current at the collector of the double –collector lateral PNP transistor $Q_{13.}$ The transistor Q_{13} and Q_{12} thus form a two-output current mirror with Q_{13A} providing bias current for output stage and Q_{13B} providing bias current for $Q_{17.}$ The transistor Q_{18} and Q_{19} provide dc bias for the output stage. Formed by Q_{14} and Q_{20} and they establish two V_{BE} drops of potential difference between the bases of Q_{14} and Q_{18} .

Input stage:

The input differential amplifier stage consists of transistors Q_1 through Q_7 with biasing provided by Q_8 through $Q_{12.}$ The transistor Q_1 and Q_2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q_3 and Q_4 which offers a large voltage gain.

The transistors Q5, Q6 and Q7 along with resistors $R_{1,}$ R_2 and R_3 from the active load for input stage. The single-ended output is available at the collector of $Q_{6.}$ the two null terminals in the input stage facilitate the null adjustment. The lateral PNP transistors Q_3 and Q_4 provide additional protection against voltage breakdown conditions. The emitter-base junction Q_3 and Q_4 have higher emitter-base breakdown voltages of about 50V. Therefore, placing PNP transistors in series with NPN transistors provide protection against accidental shorting of supply to the input terminals.

Gain Stage:

The Second or the gain stage consists of transistors Q_{16} and $Q_{17,}$ with Q_{16} acting as an emitter – follower for achieving high input resistance. The transistor Q_{17} operates in common emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage.

Internal compensation through Miller compensation technique is achieved using the feedback capacitor C_1 connected between the output and input terminals of the gain stage.

Output stage:

The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q_{14} and Q_{20} . Hence, they provide an effective loss output resistance and current gain.

The output of the gain stage is connected at the base of Q_{22} , which is connected as an emitter – follower providing a very high input resistance, and it offers no appreciable loading effect on the gain stage. It is biased by transistor Q_{13A} which also drives Q_{18} and $Q_{19,}$ that are used for

establishing a quiescent bias current in the output transistors Q_{14} and Q_{20}.

Ideal op-amp characteristics:

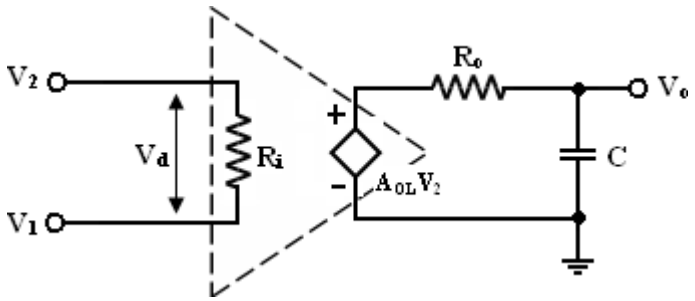
1. Infinite voltage gain A.
2. Infinite input resistance R_i, so that almost any signal source can drive it and there is no loading of the proceeding stage.
3. Zero output resistance R_o, so that the output can drive an infinite number of other devices.
4. Zero output voltage, when input voltage is zero.
5. Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified with out attenuation.
6. Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.
7. Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

AC Characteristics:

For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

Frequency Response:

The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth Bw =∞ (i.e) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the o/p.

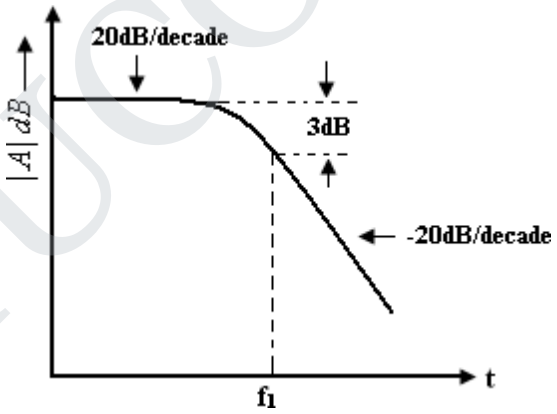


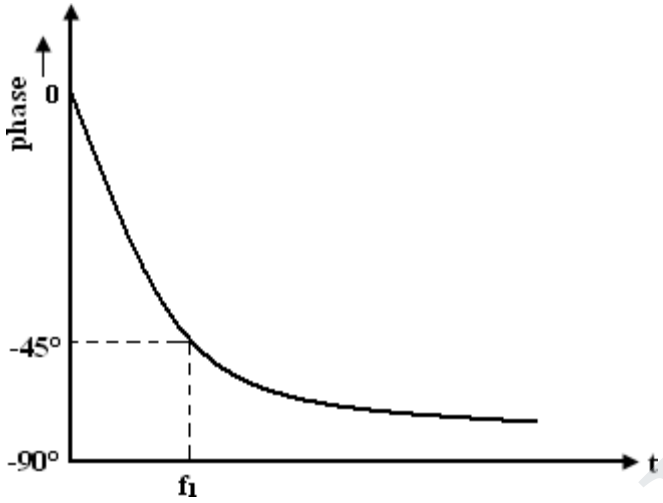
There is one pole due to R_0 C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig.

f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are fu of frequency can be written as,

The magnitude and phase angle characteristics from eqn (29) and (30)

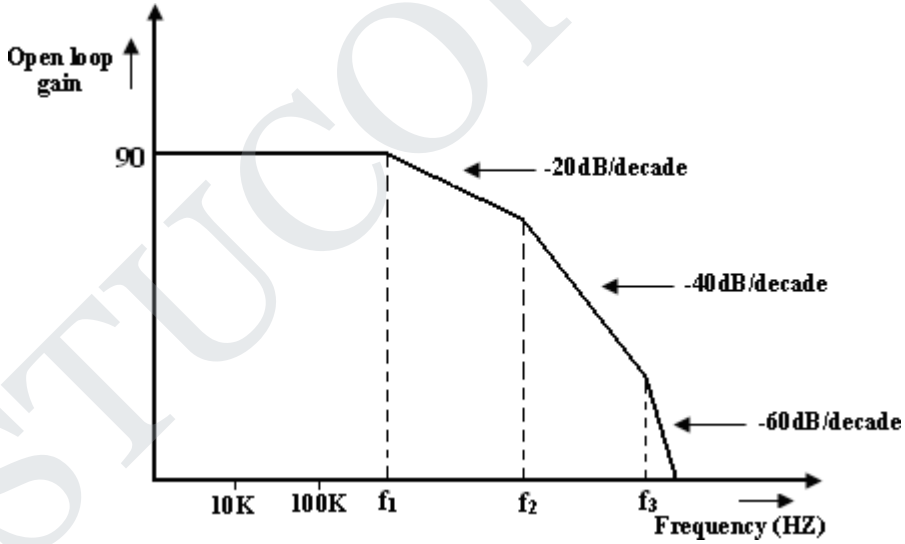
1. For frequency f<< f_1 the magnitude of the gain is 20 log A_{OL} in dB.
2. At frequency f = f_1 the gain in 3 dB down from the dc value of A_{OL} in dB. This frequency f_1 is called corner frequency.
3. For f>> f_1 the fain roll-off at the rate off -20dB/decade or -6dB/decade.





From the phase characteristics that the phase angle is zero at frequency f =0.

At the corner frequency f_1 the phase angle is -45^0 (lagging and a infinite frequency the phase angle is -90^0 . It shows that a maximum of 90^0 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as te decade below the corner frequency and infinite frequency is one decade above the corner frequency.

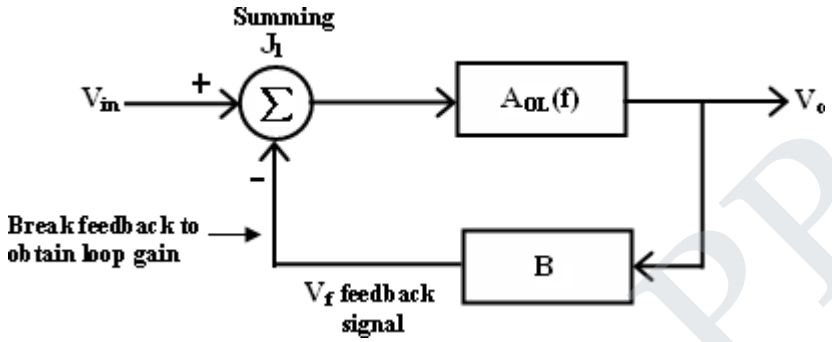


Circuit Stability:

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on increasing until the system break down. The unstable system are impractical and need be made stable. The

criterian gn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability , ex: Bode plots.

Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.



The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred -Transfer frequency' From fig we represented it by $A_{OL}(f)$ which is given by

$A_{OL}(f) = V_0 / Vin$ if $V_f = 0$ ----- (1)

where $A_{OL}(f)$ = open loop volt gain. The closed loop gain A_f is given by

$A_F = V_0 / Vin$

$A_F = A_{OL} / (1+(A_{OL})(B)$ ----- (2)

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components. Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

1. Method:1:

Determine the phase angle when the magnitude of $(A_{OL})(B)$ is 0dB (or) 1. If phase angle is > .-180^0 , the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

2. Method 2:

Determine the phase angle when the magnitude of $(A_{OL})(B)$ is 0dB (or) 1. If phase angle is > .-180^0 , If the magnitude is –ve decibels then the system is stable. However, the some systems the

phase angle of a system may reach -180^0 , under such conditions method 1 must be used to determine the system stability.

Slew Rate:

Another important frequency related parameter of an op-amp is the slew rate. (Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs).

Reason for Slew rate:

There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by

$$dVc/dt = I/C \text{ ----------(1)}$$

I -> Maximum amount furnished by the op-amp to capacitor C. Op-amp should have the either a higher current or small compensating capacitors.

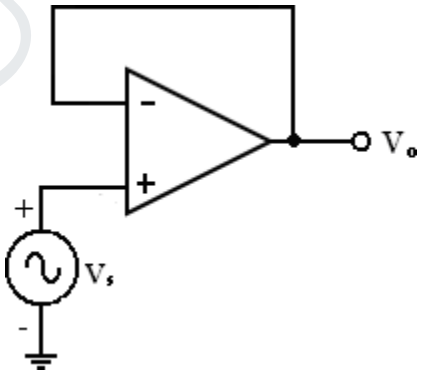
For 741 IC, the maximum internal capacitor charging current is limited to about 15μA. So the slew rate of 741 IC is

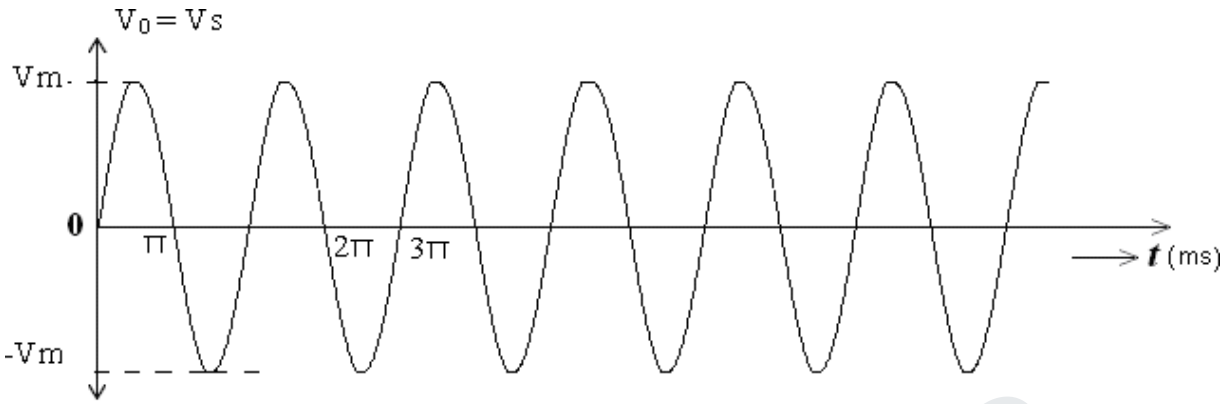
$$SR = dVc/dt\,|max = Imax/C .$$

For a sine wave input, the effect of slew rate can be calculated as consider volt follower -> The input is large amp, high frequency sine wave .

If Vs = Vm Sinwt then output V_0 = Vm sinwt . The rate of change of output is given by

$$dV_0/dt = Vm\ w\ coswt.$$





Input and Output Waveforms

The max rate of change of output across when coswt =1

(i.e) SR = $dV_0/dt|max = wVm.$

SR = 2∏fVm V/s = 2∏fVm v/ms.

Thus the maximum frequency fmax at which we can obtain an undistorted output volt of peak value Vm is given by

fmax (Hz) = Slew rate/6.28 * Vm .

called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

DC Characteristics of op-amp:

Current is taken from the source into the op-amp inputs respond differently to current and voltage due to mismatch in transistor.

DC output voltages are,

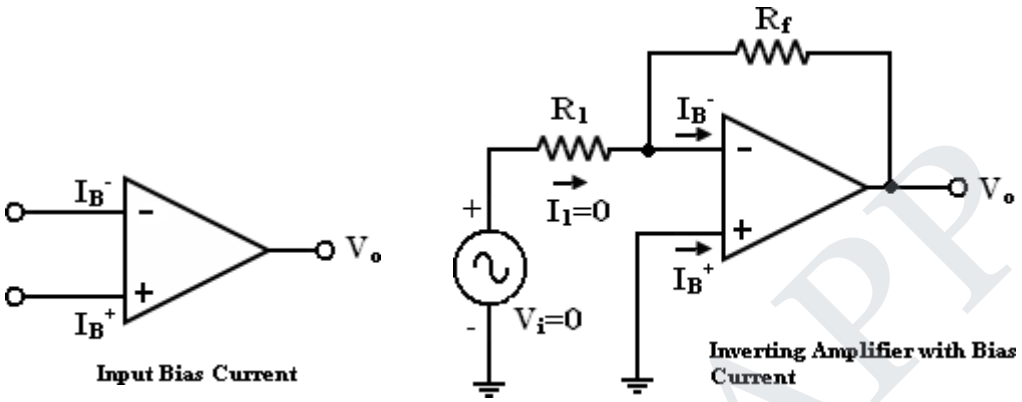
1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift

Input bias current:

The op-amp's input is differential amplifier, which may be made of BJT or FET.

- In an ideal op-amp, we assumed that no current is drawn from the input terminals.
- The base currents entering into the inverting and non-inverting terminals

- Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalance between the two inputs.
- Manufacturers specify the input bias current I_B



So, $I_B = \frac{I_B^+ + I_B^-}{2}$ (1a)

If input voltage $V_i = 0V$. The output Voltage V_o should also be ($V_o = 0$)

$I_B = 500nA$

We find that the output voltage is offset by,

$$V_o = I_B R_f \quad (2b)$$

Op-amp with a 1M feedback resistor

$V_o = 5000nA \times 1M = 500mV$

The output is driven to 500mV with zero input, because of the bias currents.

In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated. Where a compensation resistor R_{comp} has been added between the non-inverting input terminal and ground as shown in the figure below.

Current I_B^+ flowing through the compensating resistor R_{comp}, then by KVL we get,

$$-V_1+0+V_2-V_o = 0 \text{ (or)}$$

$$V_o = V_2 - V_1 \quad \text{——>(3)}$$

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the $V_o = 0$. The value of R_{comp} is derived a

$$V_1 = I_B^+ R_{comp} \text{ (or)}$$

$$I_B^+ = V_1/R_{comp} \text{ ——>(4)}$$

The node _a' is at voltage $(-V_1)$. Because the voltage at the non-inverting input terminal is $(-V_1)$. So with $V_i = 0$ we get,

$$I_1 = V_1/R_1 \text{ ——>(5)}$$

$$I_2 = V_2/R_f \text{ ——>(6)}$$

For compensation, V_o should equal to zero ($V_o = 0$, $V_i = 0$). i.e. from equation (3) $V_2 = V_1$. So that,

$$I_2 = V_1/R_f \text{ ——>(7)}$$

KCL at node _a' gives,

$$I_B^- = I_2 + I_1$$

$$I_B \square \quad R_f \quad \square \quad R_1$$

Assume $I_B^- = I_B^+$ and using equation (4) & (8) we get

$$R_{comp} \square \quad R_1 \square R_f$$

$$R_{comp} = R_1 \| R_f \quad \text{———>(9)}$$

i.e. to compensate for bias current, the compensating resistor, R_{comp} should be equal to the parallel combination of resistor R_1 and R_f.

Input offset current:

- Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal.
- Since the input transistor cannot be made identical. There will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current

$$|I_{os}| = I_B^+ - I_B^- \quad \text{——>(10)}$$

Offset current I_{os} for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when $V_i = 0$.

$$V_1 = I_B^+ R_{comp} \quad \text{——>(11)}$$

And $I_1 = V_1/R_1 \quad \text{——>(12)}$

KCL at node _a' gives,

Again

$$V_0 = I_2 R_f - V_1$$
$$V_o = I_2 R_f - I_B^+ R_{comp}$$

$$V_o = 1M\,\Omega \text{ X } 200nA$$
$$V_o = 200mV \text{ with } V_i = 0$$

Equation (16) the offset current can be minimized by keeping feedback resistance small.

- Unfortunately to obtain high input impedance, R_1 must be kept large.
- R_1 large, the feedback resistor R_f must also be high. So as to obtain reasonable gain.

The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).

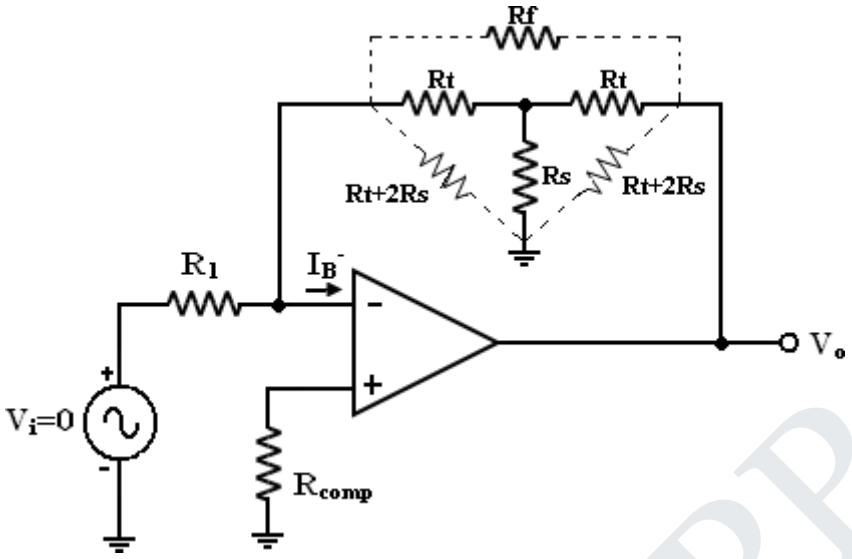
- The T-network provides a feedback signal as if the network were a single feedback resistor.

By T to Π conversion,

To design T- network first pick $R_t << R_f/2$ ——>(18)

Then calculate R_s □

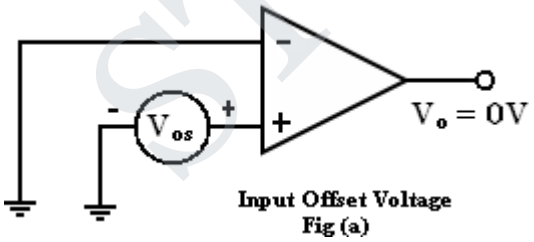
$$R_f \; 2R_t$$



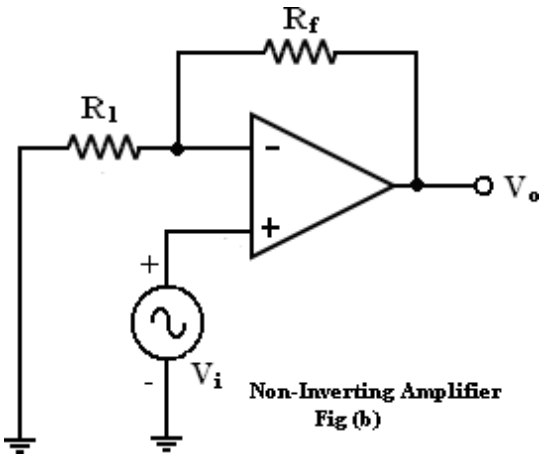
Input offset voltage:

Inspite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [$V_o \neq 0$ with $V_i = 0$]. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (V_o) = 0.

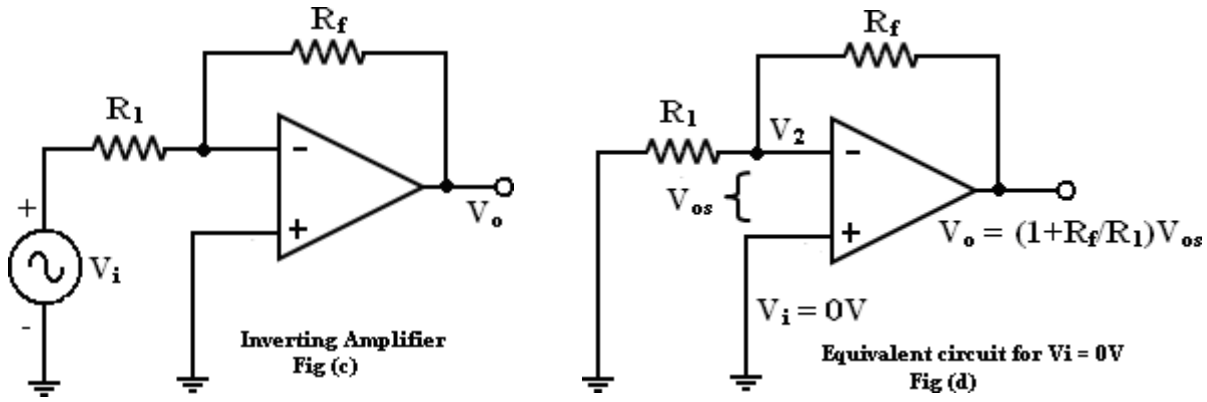
This voltage is called input offset voltage V_{os}. This is the voltage required to be applied at the input for making output voltage to zero ($V_o = 0$).



Input Offset Voltage
Fig (a)



Non-Inverting Amplifier
Fig (b)



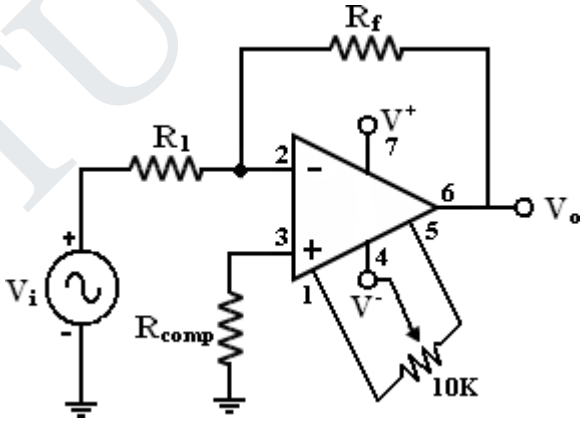
Let us determine the V_{os} on the output of inverting and non-inverting amplifier. If $V_i = 0$ (Fig (b) and (c)) become the same as in figure (d).

Total output offset voltage:

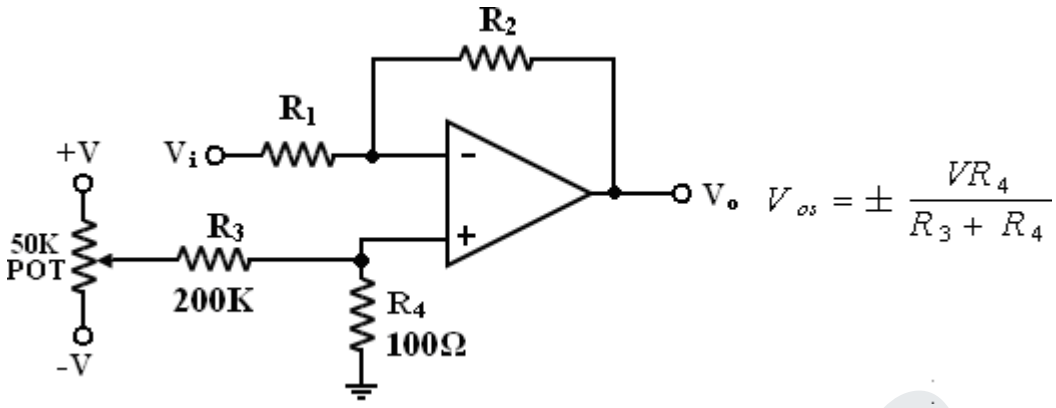
The total output offset voltage V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current (I_B) or input offset voltage alone(V_{os}).

This is because I_B and V_{os} could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non-inverting amplifier (figure b, c) without any compensation technique used is given by many op-amp provide offset compensation pins to nullify the offset voltage.

- 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4.
- The position of the wipes is adjusted to nullify the offset voltage.

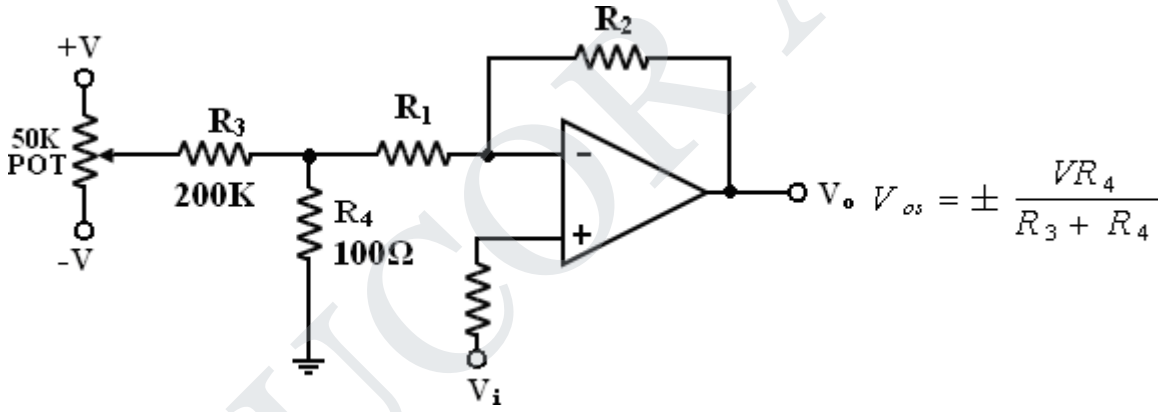


When the given (below) op-amps does not have these offset null pins, external balancing techniques are used.



$$V_{os} = \pm \frac{VR_4}{R_3 + R_4}$$

Non-inverting amplifier:



$$V_{os} = \pm \frac{VR_4}{R_3 + R_4}$$

Thermal drift:

- Bias current, offset current, and offset voltage change with temperature.

- A circuit carefully nulled at 25ºC may not remain. So when the temperature rises to 35ºC. This is called drift.
- Offset current drift is expressed in nA/ºC.
- These indicate the change in offset for each degree Celsius change in temperature.

Open – loop op-amp Configuration:

The term open-loop indicates that no feedback in any form is fed to the input from the output. When connected in open – loop, the op-amp functions as a very high gain amplifier. There are three open – loop configurations of op-amp namely,

1. differential amplifier
2. Inverting amplifier
3. Non-inverting amplifier

The above classification is made based on the number of inputs used and the terminal to which the input is applied. The op-amp amplifies both ac and dc input signals. Thus, the input signals can be either ac or dc voltage.

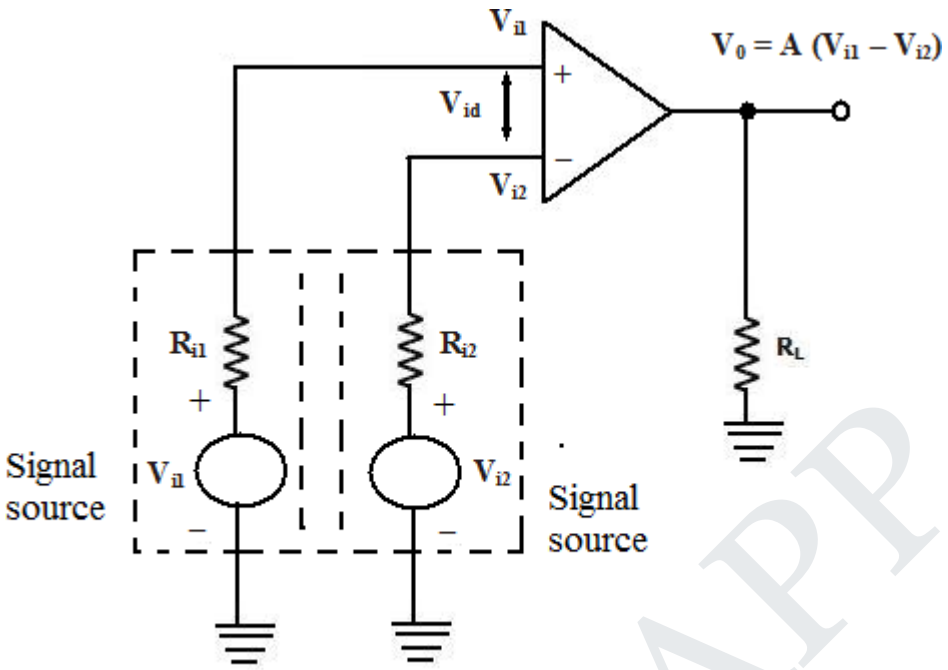
Open – loop Differential Amplifier:

In this configuration, the inputs are applied to both the inverting and the non-inverting input terminals of the op-amp and it amplifies the difference between the two input voltages. Figure shows the open-loop differential amplifier configuration.

The input voltages are represented by V_{i1} and $V_{i2.}$ The source resistance R_{i1} and R_{i2} are negligibly small in comparison with the very high input resistance offered by the op-amp, and thus the voltage drop across these source resistances is assumed to be zero. The output voltage V_0 is given by

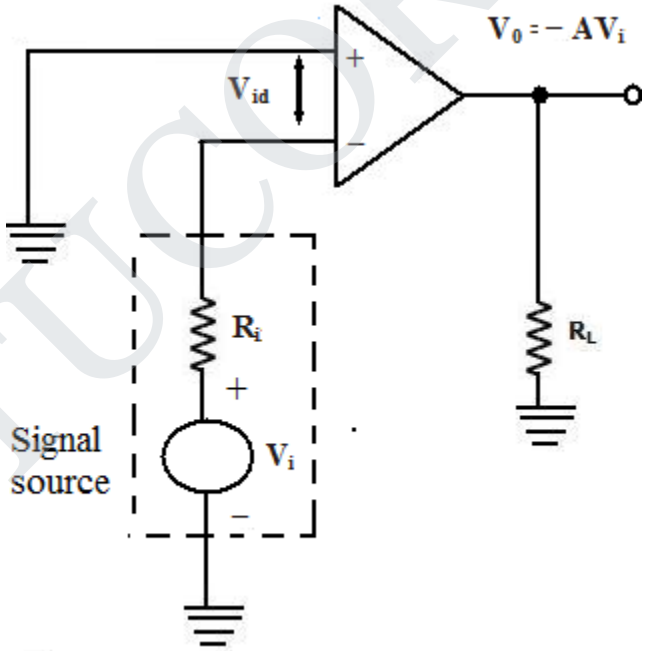
$V_0 = A(V_{i1} – V_{i2})$

where A is the large signal voltage gain. Thus the output voltage is equal to the voltage gain A times the difference between the two input voltages. This is the reason why this configuration is called a differential amplifier. In open – loop configurations, the large signal voltage gain A is also called open-loop gain A.



Open - loop Differential Amplifier

Inverting amplifier:



Open - loop Inverting Amplifier

In this configuration the input signal is applied to the inverting input terminal of the op-amp and the non-inverting input terminal is connected to the ground. Figure shows the circuit of an

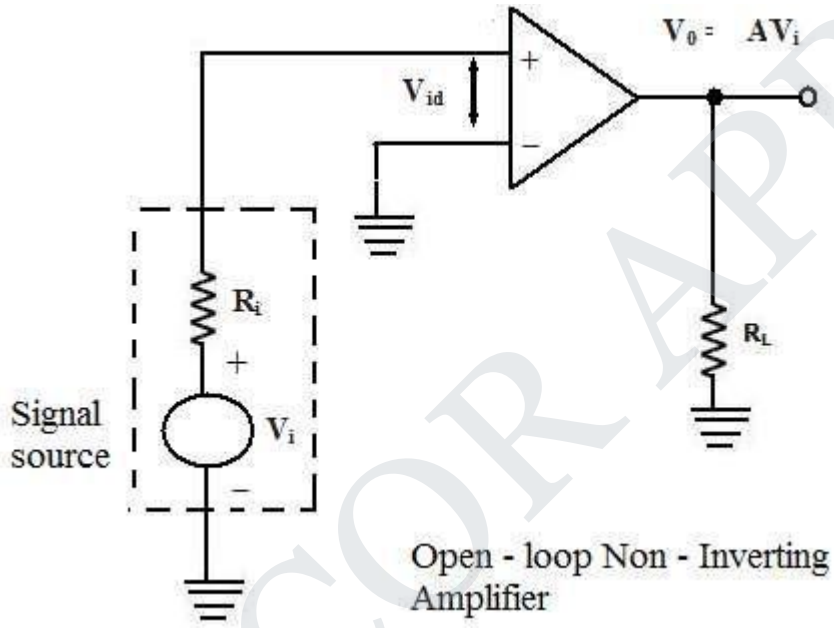
open – loop inverting amplifier.

The output voltage is 180^0 out of phase with respect to the input and hence, the output voltage V_0 is given by,

$V_0 = -AV_i$

Thus, in an inverting amplifier, the input signal is amplified by the open-loop gain A and in phase – shifted by 180^0.

Non-inverting Amplifier:



Open - loop Non - Inverting Amplifier

Figure shows the open – loop non- inverting amplifier. The input signal is applied to the non-inverting input terminal of the op-amp and the inverting input terminal is connected to the ground.

The input signal is amplified by the open – loop gain A and the output is in-phase with input signal.

$V_0 = AV_i$

In all the above open-loop configurations, only very small values of input voltages can be applied. Even for voltages levels slightly greater than zero, the output is driven into saturation, which is observed from the ideal transfer characteristics of op-amp shown in figure. Thus, when operated in the open-loop configuration, the output of the op-amp is either in negative or positive saturation, or switches between positive and negative saturation levels. This prevents the use of open – loop configuration of op-amps in linear applications.

Limitations of Open – loop Op – amp configuration:

Firstly, in the open – loop configurations, clipping of the output waveform can occur when the output voltage exceeds the saturation level of op-amp. This is due to the very high open – loop gain of the op-amp. This feature actually makes it possible to amplify very low frequency signal of the order of microvolt or even less, and the amplification can be achieved accurately without any distortion. However, signals of such magnitudes are susceptible to noise and the amplification for those application is almost impossible to obtain in the laboratory.

Secondly, the open – loop gain of the op – amp is not a constant and it varies with changing temperature and variations in power supply. Also, the bandwidth of most of the open- loop op amps is negligibly small. This makes the open – loop configuration of op-amp unsuitable for ac applications. The open – loop bandwidth of the widely used 741 IC is approximately 5Hz. But in almost all ac applications, the bandwidth requirement is much larger than this.

For the reason stated, the open – loop op-amp is generally not used in linear applications. However, the open – loop op amp configurations find use in certain non – linear applications such as comparators, square wave generators and astable multivibrators.

Closed – loop op-amp configuration:

The op-amp can be effectively utilized in linear applications by providing a feedback from the output to the input, either directly or through another network. If the signal feedback is out- of-phase by 180^0 with respect to the input, then the feedback is referred to as negative feedback or degenerative feedback. Conversely, if the feedback signal is in phase with that at the input, then the feedback is referred to as positive feedback or regenerative feedback.

An op – amp that uses feedback is called a closed – loop amplifier. The most commonly used closed – loop amplifier configurations are 1. Inverting amplifier (Voltage shunt amplifier) 2. Non-Inverting amplifier (Voltage – series Amplifier)

Inverting Amplifier:

The inverting amplifier is shown in figure and its alternate circuit arrangement is shown in figure, with the circuit redrawn in a different way to illustrate how the voltage shunt feedback is achieved. The input signal drives the inverting input of the op – amp through resistor R_1 .

The op – amp has an open – loop gain of A, so that the output signal is much larger than the error voltage. Because of the phase inversion, the output signal is 180^0 out – of – phase with the input signal. This means that the feedback signal opposes the input signal and the feedback is negative or degenerative.

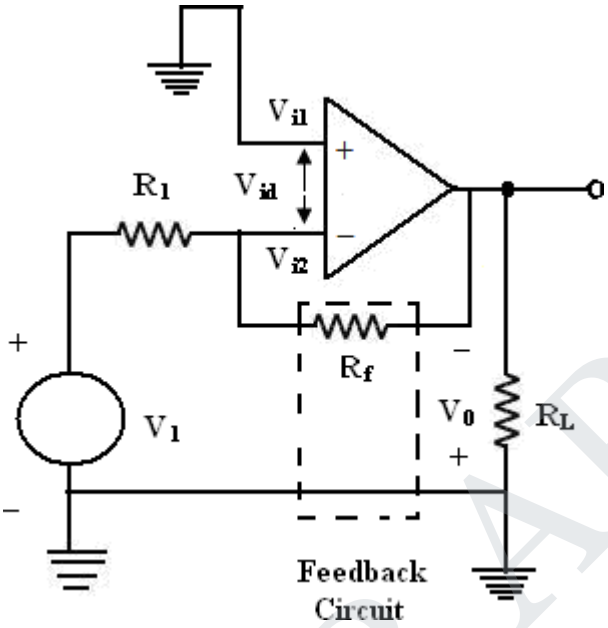
Virtual Ground:

A virtual ground is a ground which acts like a ground . It may not have physical connection to ground. This property of an ideal op – amp indicates that the inverting and non – inverting terminals of the op –amp are at the same potential. The non – inverting input is grounded for the inverting amplifier circuit. This means that the inverting input of the op –amp is also at ground potential. Therefore, a virtual ground is a point that is at the fixed ground potential (0V), though it is not practically connected to the actual ground or common terminal of the circuit.

The open – loop gain of an op – amp is extremely high, typically 200,000 for a 741. For ex, when the output voltage is 10V, the input differential voltage V_{id} is given by

Further more, the open – loop input impedance of a 741 is around 2MΩ. Therefore, for an input differential voltage of 0.05mV, the input current is only

Since the input current is so small compared to all other signal currents, it can be approximated as zero. For any input voltage applied at the inverting input, the input differential voltage V_{id} is negligibly small and the input current is ideally zero. Hence, the inverting input acts as a virtual ground. The term virtual ground signifies a point whose voltage with respect to ground is zero, and yet no current can



The expression for the closed – loop voltage gain of an inverting amplifier can be obtained from figure. Since the inverting input is at virtual ground, the input impedance is the resistance between the inverting input terminal and the ground. That is, $Z_i = R_1$. Therefore, all of the input voltage appears across R_1 and it sets up a current through R_1 that equals . The current must flowthrough R_f because the virtual ground accepts negligible current. The left end of R_f is ideally grounded, and hence the output voltageappears wholly across it. Therefore,

The input impedance can be set by selecting the input resistor R_1 . Moreover, the above equation shows that the gain of the inverting amplifier is set by selecting a ratio of feedback resistor R_f to the input resistor R_1 . The ratio R_f / R_1 can be set to any value less than or greater than unity. This feature of the gain equation makes the inverting amplifier with feedback very popular and it lends this configuration to a majority of applications.

Practical Considerations:

1. Setting the input impedance R_1 to be too high will pose problems for the bias current, and it is usually restricted to 10KΩ.
2. The gain cannot be set very high due to the upper limit set by the fain – bandwidth (GBW = A_v * f) product. The A_v is normally below 100.
3. The peak output of the op – amp is limited by the power supply voltages, and it is about 2V less than supply, beyond which, the op – amp enters into saturation.
4. The output current may not be short – circuit limited, and heavy loads may damage the op – amp. When short – circuit protection is provided, a heavy load may drastically distort the output voltage.

Practical Inverting amplifier:

The practical inverting amplifier has finite value of input resistance and input current, its open voltage gain A_0 is less than infinity and its output resistance R_0 is not zero, as against the ideal inverting amplifier with finite input resistance, infinite open – loop voltage gain and zero output resistance respectively.

Figure shows the low frequency equivalent circuit model of a practical inverting amplifier. This circuit can be simplified using the Thevenin's equivalent circuit shown in figure. The signal source Vi and the resistors R_1 and R_i are replaced by their Thevenin's equivalent values. The closed – loop gain A_V and the input impedance R_{if} are calculated as follows.

The input impedance of the op- amp is normally much larger than the input resistance R_1. Therefore, we can assume $V_{eq} \approx V_i$ and $R_{eq} \approx R_1$. From the figure we get,

$$V_0 = IR_0 = AV_{id}$$

and $V_{id} = IR_f + V_0 = 0$

Substituting the value of V_{id} *from above eqn , we get,*

$$V_0 \left(1 + \frac{R_0}{AR_f}\right) = IR_0$$

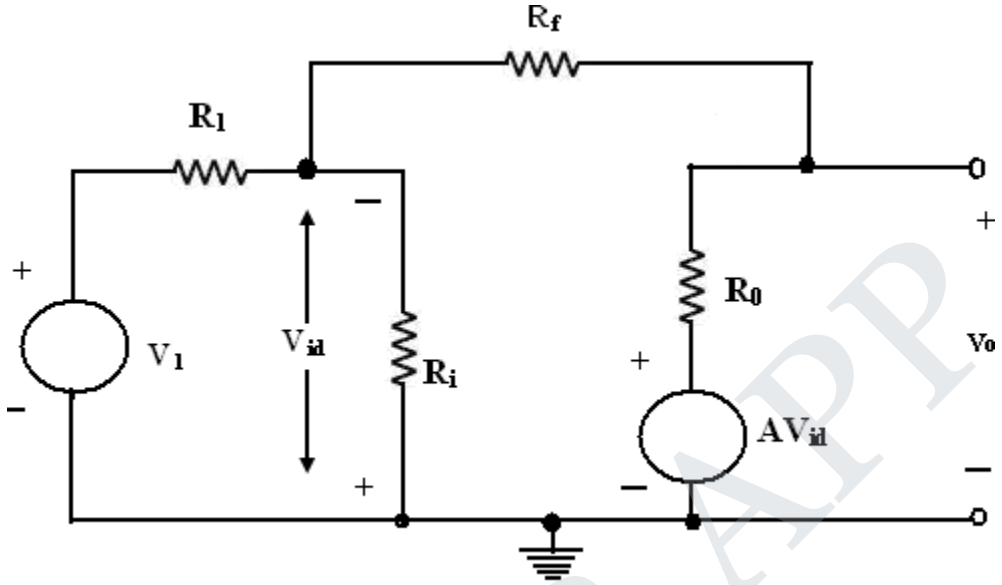
Also using the KVL , we get

$$V_i = IR_1 + IR_f + V_0$$

Substituting the value of I derived from above eqn and obtaining the closed loop gain A_v*, we get*

It can be observed from above eqn that when A>> 1, R_0 is negligibly small and the product AR_1 >> R_0 +R_f , the closed loop gain is given by

Which is as the same form as given in above eqn for an ideal inverter.



Equivalent Circuit of a Practical Inerting Amplifier

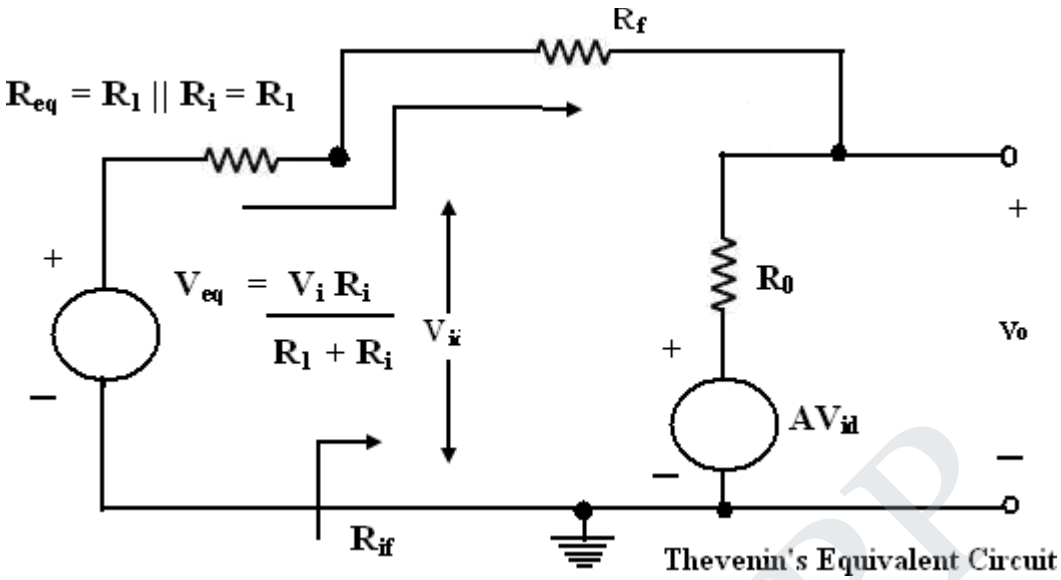
Input Resistance:

From figure we get,

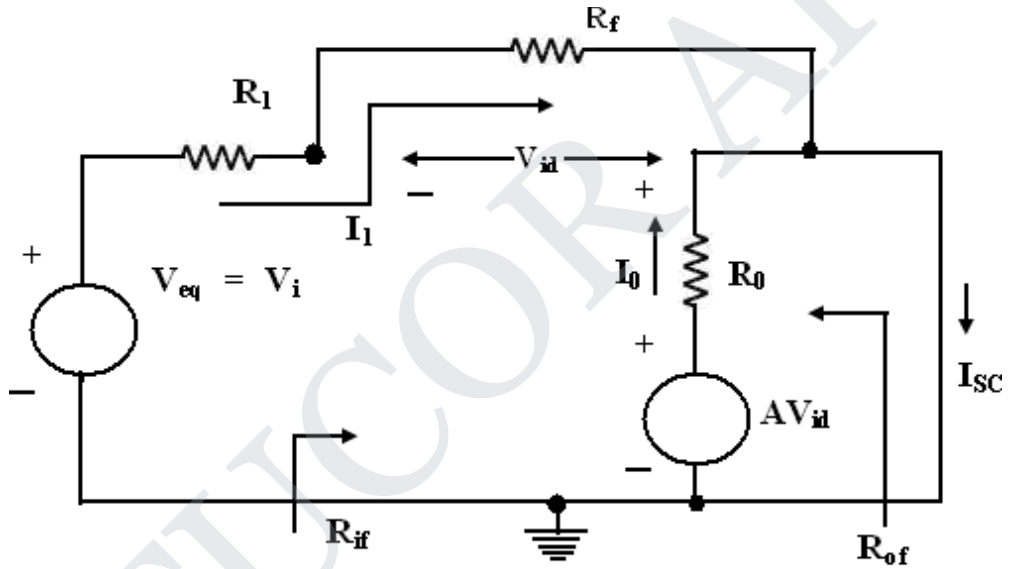
Using KVL, weget,

$$V_{id} - I_1 R_f - R_0 - AV_{id} - 0$$

which can be simplified for R_{if} *as*



Output Resistance:



Equivalent circuit to determine Rof

Figure shows the equivalent circuit to determine R_{of} . The output impedance R_{of} without the load resistance factor R_L is calculated from the open circuit output voltage V_{oc} and the short circuit output current I_{SC} .

Non –Inverting Amplifier:

The non – inverting Amplifier with negative feedback is shown in figure. The input signal drives the non – inverting input of op-amp. The op-amp provides an internal gain A. The external resistors R_1 and R_f form the feedback voltage divider circuit with an attenuation factor of β. Since

the feedback voltage is at the inverting input, it opposes the input voltage at the non – inverting input terminals, and hence the feedback is negative or degenerative.

The differential voltage V_{id} at the input of the op-amp is zero, because node a is at the same voltage as that of the non- inverting input terminal. As shown in figure, R_f and R_1 form a potential divider. Therefore,

$$V$$

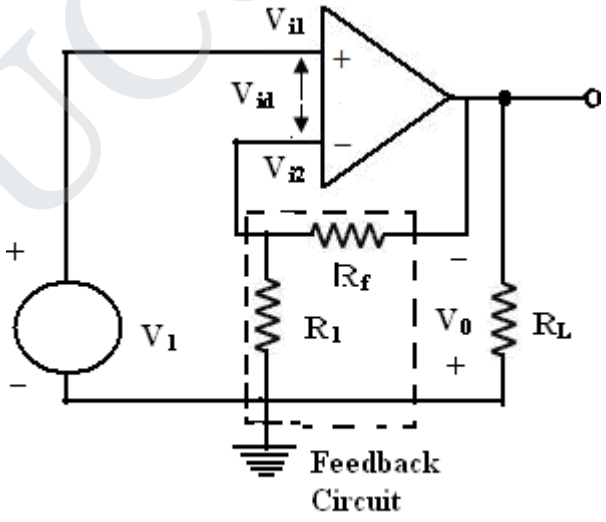
Since no current flows into the op-amp.

Eqn can be written as

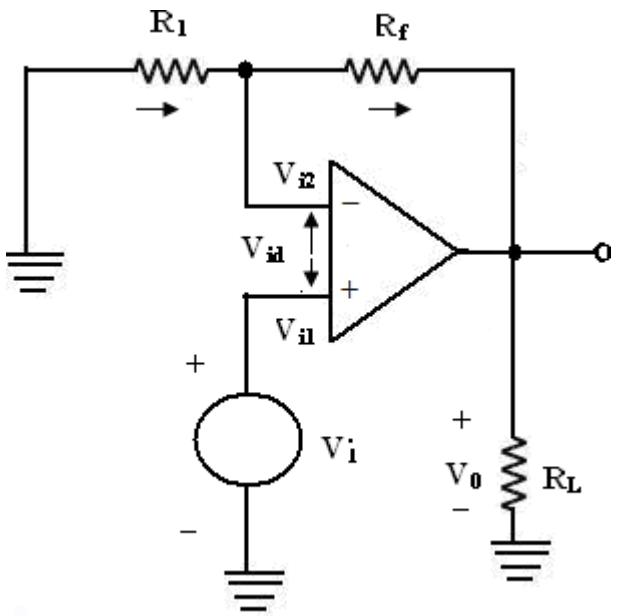
Hence, the voltage gain for the non – inverting amplifier is given by

Using the alternate circuit arrangement shown in figure, the feedback factor of the feedback voltage divider network is

From the above eqn, it can be observed that the closed – loop gain is always greater than one and it depends on the ratio of the feedback resistors. If precision resistors are used in the feedback network, a precise value of closed – loop gain can be achieved. The closed – loop gain does not drift with temperature changes or op – amp replacements.



Its alternate Circuit Arrangement

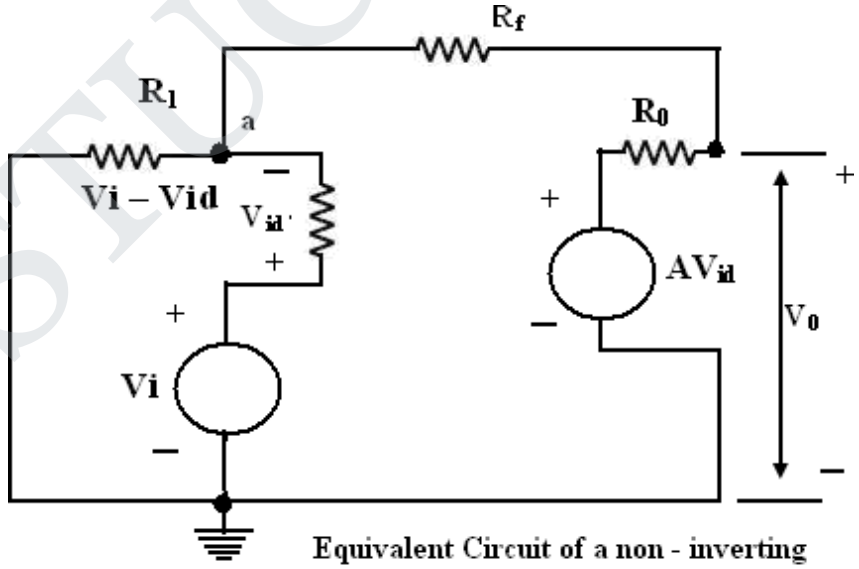


Closed Loop Non – Inverting Amplifier

The input resistance of the op – amp is extremely large (approximately infinity,) since the op – *amp draws negligible current from the input signal.*

Practical Non –inverting amplifier:

The equivalent circuit of a non- inverting amplifier using the low frequency model is shown below in figure. Using Kirchoff's current law at node a,



Equivalent Circuit of a non - inverting Amplifier using low frequency

Feedback amplifier:

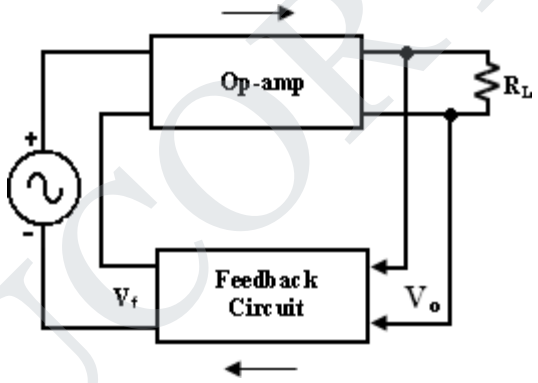
An op-amp that was feedback is called as feedback amplifier. A feedback amplifier is sometimes referred to as closed loop amplifier because the feedback forms a closed loop between the input and output. A closed loop amplifier can be represented by using 2 blocks.

1. One for an op-amp
2. another for an feedback circuit.

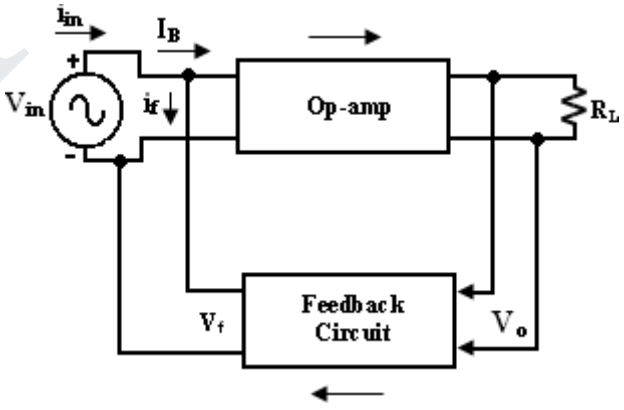
There are 4 ways to connect these 2 blocks according to whether volt or current.

1. Voltage Series Feedback
2. Voltage Shunt feedback
3. Current Series Feedback
4. Current shunt Feedback

Voltage series and voltage shunt are important because they are most commonly used.

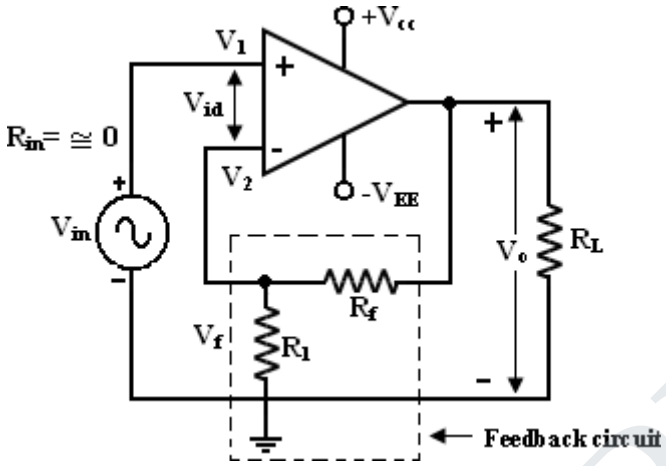


Voltage Series Feedback Amplifier



Voltage shunt feedback Amplifier

Voltage Series Feedback Amplifier:



Before Proceeding, it is necessary to define some terms.

Voltage gain of the op-amp with a without feedback:

Gain of the feedback circuit are defined as open loop volt gain (or gain without feedback) $A = V_0 / Vid$

Closed loop volt gain (or gain with feedback) $A_F = V_0 / Vin$

Gain of the feedback circuit => $B = V_F / V_0$.

1. Negative feedback:

KVL equation for the input loop is,

$Vid = Vin - V_f$ ---------- (1)

Vin = input voltage.

V_f = feedback voltage.

Vid = difference input voltage.

The difference volt is equal to the input volt minus the f/b volt. (or) The feedback volt always opposes the input volt (or out of phase by 180^0 with respect to the input voltage) hence the feedback is said to be negative.

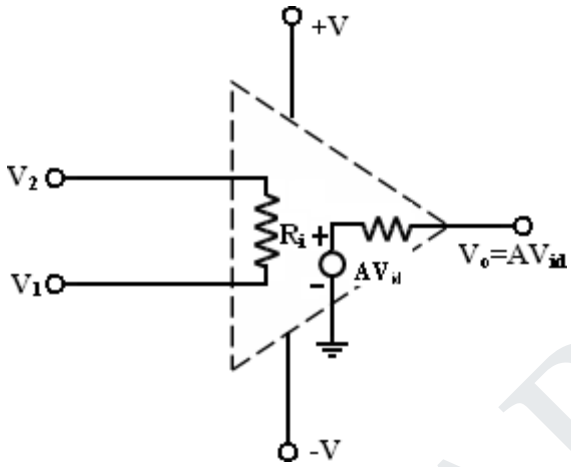
It will be performed by computing

1. Closed loop volt gain
2. Input and output resistance
3. Bandwidth

1. Closed loop volt gain:

The closed loop volt gain is $A_F = V_0 / Vin$

$V_0 = Avid = A(V_1 - V_2)$



A = large signal voltage gain.

From the above eqn, $V_0 = A(V_1 - V_2)$

Refer fig, we see that, $V_1 = Vin$

$V_2 = V_f = R_1 V_0$

$$\frac{}{R_1 + R_f}$$

Since $Ri >> R_1$

$$V_0 = AVin - \frac{R_1 V_0}{R_1 + R_f}$$

$$V_0 + \frac{A R_1 V_0}{R_1 + R_f} = AVin$$

3. Difference input voltage ideally zero (Vid)

Reconsider eqn $V_0 = A\ Vid$

$Vid = V_0 / A$

Since A is very large (ideally α)

Vid t 0 ---(7.a)

(i.e) V_1 t V_2 --(7.b)

Eqn (7.b) says that the volt at the Non-inverting input terminal of an op-amp is approximately equal to that at the inverting input terminal provided that A, is vey large.

From the circuit diagram,

$V_1 = Vin$

$V_2 = V_F = R_1 V_0 / R_1 + R_F$

Sub these values of V_1 and V_2 in eqn (7.b) we get

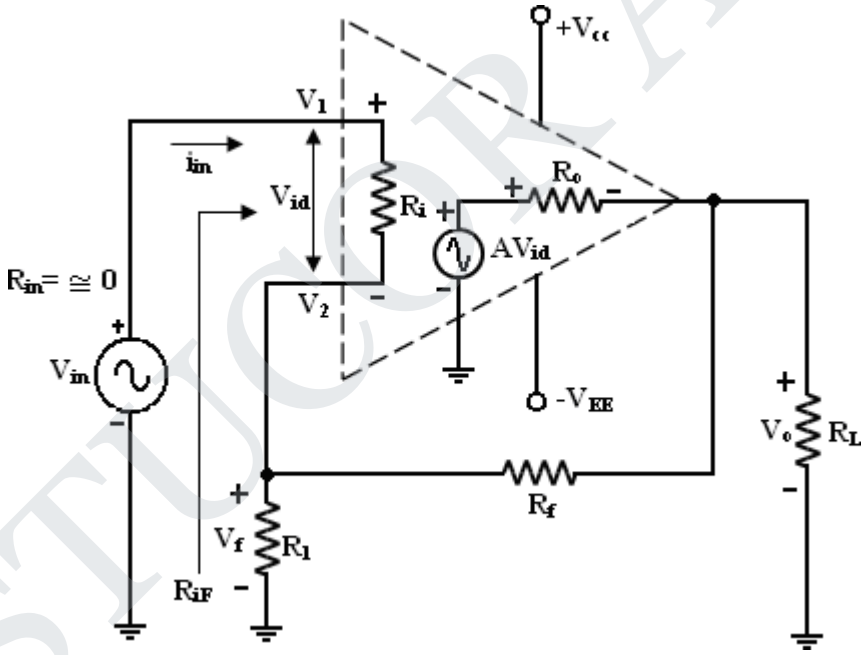
$Vin = R_1 V_0 / R_1 + R_F$ (i.e) $A_F = V_0 / Vin = 1 + R_F / R_1$

4. Input Resistance with feedback:

From the below circuit diagram Ri -> input resistance

Rif -> input resistance of an op-amp with feedback

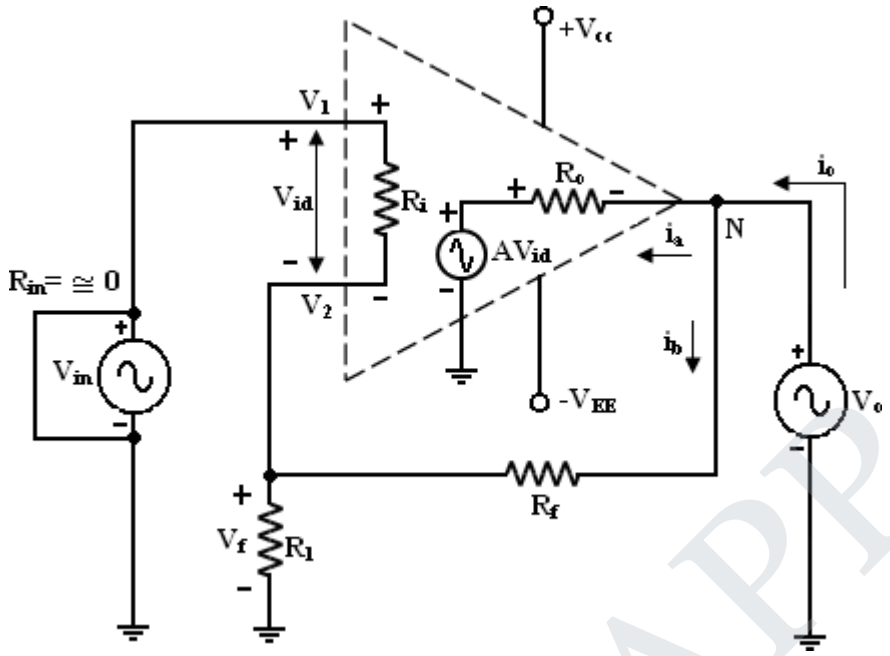
Derivation of input resistance with Feedback:



The input resistance with feedback is defined as,

This means that the input resistance of the op-amp with feedback is (i+AB) times that without feedback.

5. Output Resistance with feedback:



This resistance can be obtained by using Thevenin's theorem. To find out o/p resistance with feedback R_{OF} reduce independent source Vin to zero, apply an external voltage V_0 , and calculate the resulting current i_0 .

The R_{OF} is defined as follows,

$R_{OF} = V_0 / i_0$ ---(9.a)

KCL at o/p node _N' we get,

$i_0 = i_a + i_b$

Since $((R_F + R_1) \| R_i >> R_0$ and $i_0 >> i_b$

. i_0 t i_a

The current i_0 can be found by writing KVL eqn for the o/p loop

$V_0 - R_0 i_0 - AVid = 0$

$i_0 = V_0 - AVid$

R_0

$Vid = V_1 - V_2$

$= 0 - V_F$

This result shows that the output resistance of the voltage series feedback amplifier is 1/(1+AB) the output resistance of R_0 the op-amp. (i.e) The output resistance of the op-amp with feedback is much smaller than the output resistance without feedback.

6. Bandwidth with feedback:

The bandwidth of the amplifier is defined as the band (range of frequency) for which the gain remains constant. The Frequency at which the gain equals 1 is known as unity gain bandwidth (UGB). The relationship between the breakfrequency f_0 , open loop volt gain A, bandwidth with feedback f_F and closed loop gain A_F .

For an op-amp with a single break frequency f_0 , the gain bandwidth product is constant and equal to the unity-gain bandwidth. (UGB).

UGB = (A) (f_0) (10.a)

A = open loop volt gain

f_0 = break frequency of an op-amp ((or) only for a single break frequency op-amp UGB = A_F f_F ---- (10.b)

A_F = closed loop volt gain

f_F = bandwidth with feedback.

Equating eqn 10.a and 10.b

$Af_0 = A_F f_F$

$f_F = Af_0 / A_F$-------- (10.c)

For the non-inverting amplifier with feedback

$A_F = A/(1+AB)$

Sub the value of A_F in eqn 10.c, we get

$f_F = Af_0 / A/(1+AB)$

$f_F = (1+AB) f_0$---- (10.d)

eqn 10.d -> bandwidth of the non-inverting amplifier with feedback is = bandwidth of the with feedback f_0 times (1+AB)

7. Total o/p offset voltage with feedback (Vout)

In an open loop op-amp the total o/p offset voltage is equal to either the +ve or –ve saturation volt.

Vout = +ve (or) –ve saturation volt.

With feedback the gain of the Non-inverting amplifier changes from A to A/(1+AB), the total output offset voltage with feedback must also be 1/(1+AB) times the voltage without feedback. (i.e)

Total o/p offset Vout with feedback = Total o/p offset volt without feedback

---

1+AB

Vout = ±Vsat

1+AB ----(11)

1/(1+AB) is < I and ±Vsat = Saturation voltages. The maximum voltages the output of an op-amp can reach.

Note:

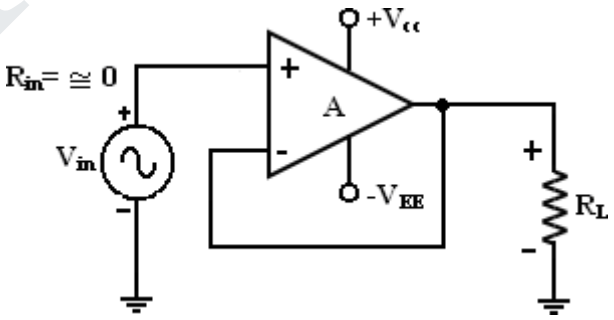
Open-loop even a very small volt at the input of an op-amps can cause to reach maximum value (+ Vsat)because of its very high volt gain. According to eqn for a gain op-amp circuit the Vout is either +ve or –ve volt because Vsat can be either +ve or –ve.

Conclusion of Non-Inverting Amplifier with feedback:

The char of the perfect volt Amplifier:

1. It has very high input resistamce.
2. Very low output resistance
3. Stable volt gain
4. large bandwidth

8. Voltage Follower: [Non-Inverting Buffer]



The lowest gain that can be obtained from a non-inverting amplifier feedback is 1.

When the Non-Inverting amplifier is designed for unity and it is called a voltage follower, because the output voltage is equal to and inphase with the input or in volt follower the output follows the input.

It is similar to discrete emitter follower, the volt follower is preferred, because it had much higher input resistance and output amplitude is exactly equal to input.

To obtain the voltage follower, from this circuit simply open R_1 and short R_F .

In this figure all the output volt is fed back into the inverting terminal of the op-amp.

The gain of the feedback circuit is 1 ($B = A_F = 1$)

$A_F = 1$

$R_{iF} =$

AR_i

$R_{OF} = R_0 / A$

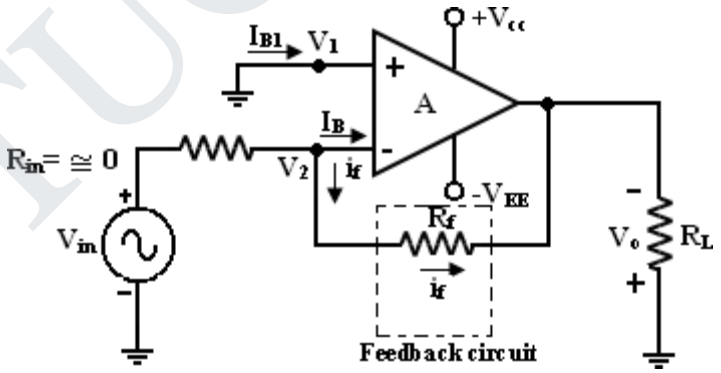
$f_F = Af_0$

$V_{out} = \pm V_{sat}$

$$\frac{\text{---------}}{A}$$

Since $1 + A \approx A$.

Voltage Shunt Feedback Amplifier:[Inverting Amplifier]



The input voltage drives the inverting terminal, and amplified as well as inverted output signal also applied to the inverting input via feedback resistor R_F .

Note:

Non-inverting terminal is grounded and feedback circuit has R_F and extra resistor R_1 is connected in series with the input signal source Vin.

We derive the formula for

1. Voltage gain
2. Input and output resistance
3. Bandwidth
4. Total output offset voltage.

1. Closed – loop voltage gain A_F :

A_F of volt shunt feedback amplifier can be obtained by writhing KCL eqn at the input node V_2 .

$i_{in} = i_F + I_B$ ----- (12.a)

Since R_i is very large, the input bias current is negligibly small.

i_{in} t i_F

(i.e) $\frac{Vin - V_2}{R_i} = \frac{V_2 - V_0}{R_F}$ ---------- (12.b)

Consider, from eqn,

$V_1 - V_2 = - V_0 / A$

Since $V_1 = 0V$

$V_2 = -V_0 / A$

Sub this value of V_2 in eqn (12.b) and rearranging,

$\frac{Vin + V_0/A}{R_i} = \frac{-(V/A) - V_0}{R_F}$

$A_F = \frac{V_0}{Vin} = -\frac{AR_F}{R_1 + R_F + AR_1}$ (exact) -------- (13)

The –ve sign indicates that the input and output signals are out of phase 180^0 . (or opposite polarities).

Because of this phase inversion the diagram is known as Inverting amplifier with feedback. Since the internal gain A of the op-amp is very large (α) , $AR_1 >> R_1 + R_F$, (i.e) eqn (13)

$A_F = V_0 / Vin = -R_F / R_1$ (Ideal)

To express eqn (13) in terms of eqn(6). To begin with, we divide both numerator and denominator of eqn (13) by $(R_1 + R_F)$

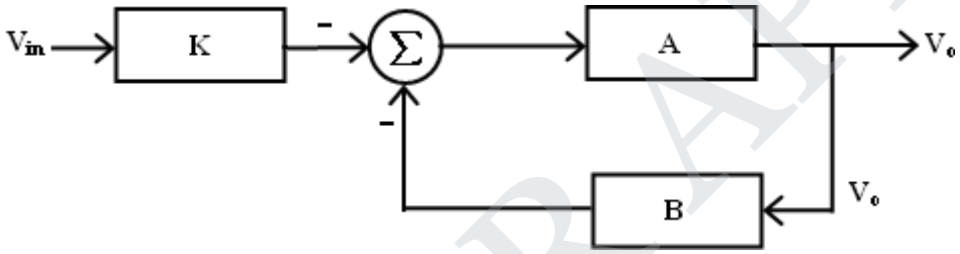
$$A_F = AR_F / R_1 + R_F$$

$$\frac{}{1+ AR_1 (R_1 + R_F)} \quad ---(15)$$

$$A_F = - AR/ 1+AB)$$

Where $K = R_F /(R_1 + R_F)$

$B = R_1 /(R_1 + R_F)$ Gain of feedback.



The comparison of eqn (15) with feedback (6) indicates that in addition to the phase inversion (- sign), the closed loop gain of the inverting amplifier in K times the closed loop gain of the Non-inverting amplifier where K< 1. To derive a ideal closed loop gain, we can use Eqn 15 as follows,

If AB >> 1, then (1+AB) = AB and $A_F = K/B = -R_F /R_1$ ----(16)

2. Input Resistance with feedback:

Easiest method of finding the input resistance is to millerize the feedback resistor R_F . (i.e) Split R_F in to its 2 Miller components as shown in fig.

In this circuit, the input resistance with feedback Rif is then

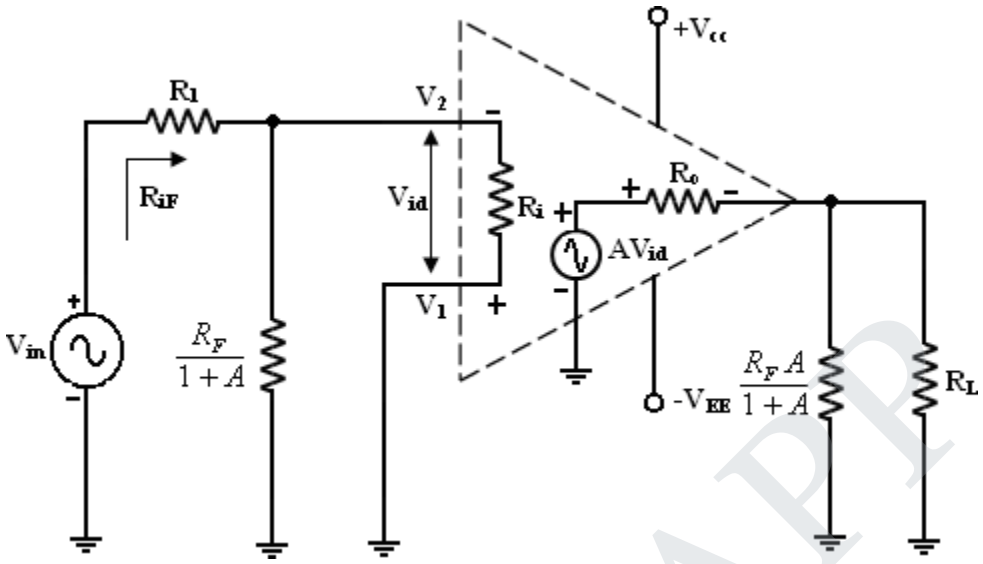
$$Rif = R_1 + R_F$$

$$\frac{}{1+A} \quad \| \quad (Ri) \text{ --------(18)}$$

Since Ri and A are very large.

$$R_1 + R_F$$

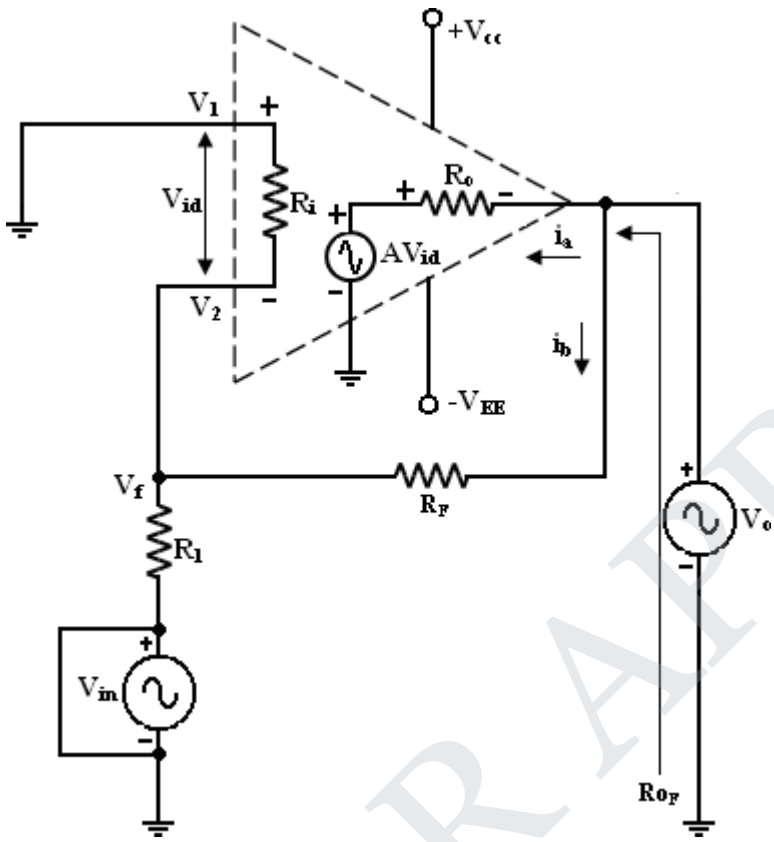
----- || (R_1) t 0Ω



1+A

3. Output Resistance with feedback:

The output resistance with feedback R_{OF} is the resistance measured at the output terminal of the feedback amplifier. Thevenin's circuit is exactly for the same as that of Non-inverting amplifier because the output resistance R_{OF} of the inverting amplifier must be identical to that of non – inverting amplifier.



R_0 = Output Resistance of the op-amp

A = Open loop volt gain of the op-amp

B = Gain of the feedback circuit.

4. Bandwidth with Feedback:

The gain Bandwidth product of a single break frequency op-amp is always constant.

Gain of the amplifier with feedback < gain without feedback

The bandwidth of amplifier with feedback f_F must be larger than that without feedback.

$f_F = f_0 (1+AB)$ ----------(21.a)

f_0 = Break frequency of the op-amp

= unity gain Bandwidth = UGB

Open- loop voltage gain A

Sub this value of f_0 in eqn (21.a)

$$f_F = \frac{UGB}{A} = \frac{UGB}{(1+AB)}$$

$$f_F = \frac{UGB\,(K)}{A_F} \quad \text{-----(21.b)}$$

Where $K = R_F/(R_1 + R_F)$; $A_F = AK/1+AB$

Eqn 10.b and 21.b => same for the bandwidth.

Same closed loop gain the closed loop bandwidth for the inverting amplifier is < that of Non – inverting amplifier by a factor of K(<1)

5. Total output offset voltage with feedback:

When the temp & power supply are fixed, the output offset voltage is a function of the gain of an op-amp.

Gain of the feedback < gain without feedback.

The output offset volt with feedback < without feedback.

Total Output offset Voltage with f/b =Total output offset volt without f/b

$$\frac{\text{Total output offset volt without f/b}}{1+AB}$$

$$V_{out} = \frac{\pm V_{sat}}{1+AB} \quad \text{----(22)}$$

$\pm V_{sat}$ = Saturation Voltage

A = open-loop volt gain of the op-amp

B = Gain of the f/b circuit

$B = R_1/(R_1 + R_F)$

In addition, because of the –ve f/b,

1. Effect of noise
2. Variations in supply voltages
3. Changes in temperature on the output voltage of inverting amplifier are reduced.

Differential amplifier:

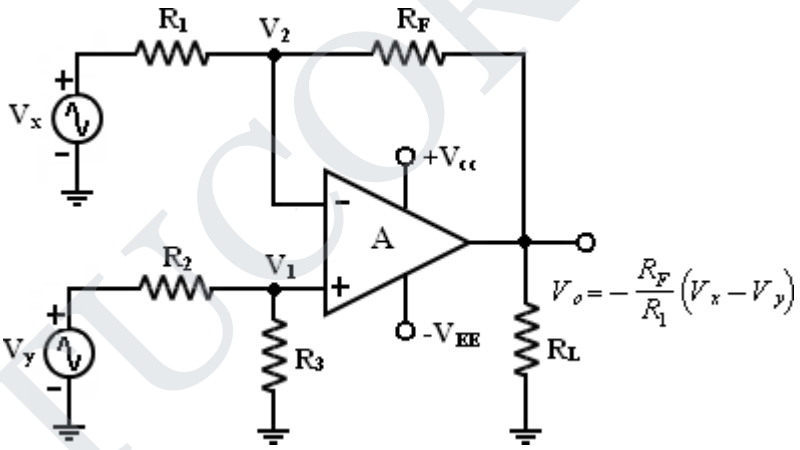
We will evaluate 2 different arrangements of the differential amplifier with -ve feedback. Classify these arrangements according to the number of op-amps used. i.e

1. Differential amplifier with one op-amp
2. Differential amplifier with two op-amps.

Differential amplifier are used in instrumentation and industrial applications to amplify differences between 2 input signals such as output of the wheat stone bridge circuit.

Differential amplifier preferred to these application because they are better able to reject common mode (noise) voltages than single input circuit such as inverting and non-inverting amplifier.

1. Differential Amplifier with one op-amp:



To analyse this circuit by deriving voltage gain and input resistance. This circuit is a combination of inverting and non-inverting amplifier. (i.e) When V_x is reduced to zero the circuit is non-inverting amplifier and when V_y is reduced to zero the circuit is invertingamplifier.

Voltage Gain:

The circuit has 2 inputs V_x and V_y . Use superposition theorem, when V_y = 0V, becomes inverting amplifier. Hence the o/p due to V_x only is

$V_{ox} = -R_F (V_x)$

---------- -----(24.a)

R_1

Similarly, when $V_x = 0V$, becomes Non-inverting amplifier having a voltage divider network composed of R_2 and R_3 at the Non – inverting input.

Note : the gain of the differential amplifier is same as that of inverting amplifier.

Input Resistance:

The input resistance R_{if} of the differential amplifier is resistance determined looking into either one of the 2 input terminals with the other grounded,

With $V_y = 0V$,

Inverting amplifier, the input resistance which is,

$RiFx \approx R_1$ ----------

(26.a) Similarly, , $V_x = 0V$,

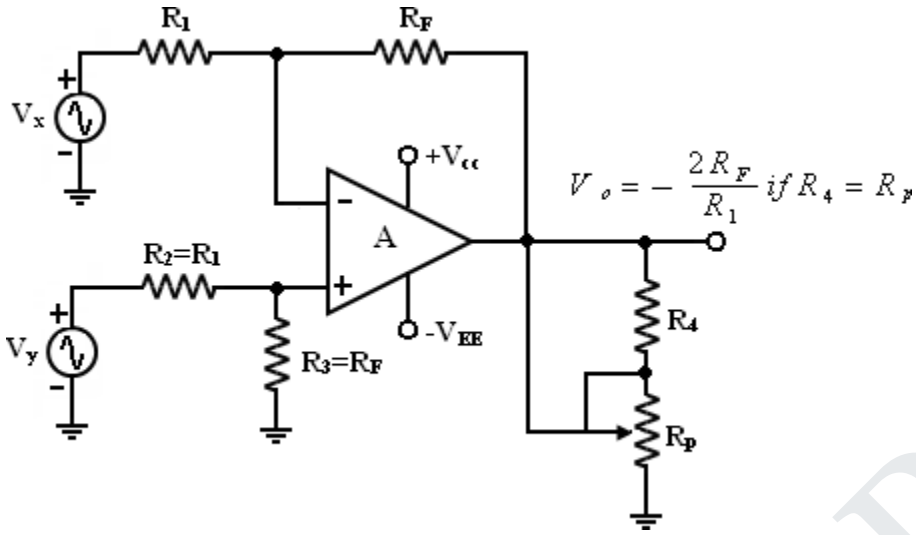
Non-inverting amplifier, the input resistance which is,

$RiFy \approx (R_2 + R_3)$ ------ (26.b)

V_x and V_y are not the same. Both the input resistance can be made equal, if we modify the basic differential amplifier. Both R_1 and $(R_2 + R_3)$ can be made much larger than the source resistances. So that the loading of the signal sources does not occur.

Note: If we need a variable gain, we can use the differential amplifier. In this circuit $R_1 = R_2$, $R_F = R_3$ and the potentiometer $R_p = R_4$.

Depending on the position of the wiper in R voltage can be varied from the closed loop gain of $-2R_F/R_1$ to the open loop gain of A.



$$V_o = -\frac{2R_F}{R_1} \; if \; R_4 = R_p$$

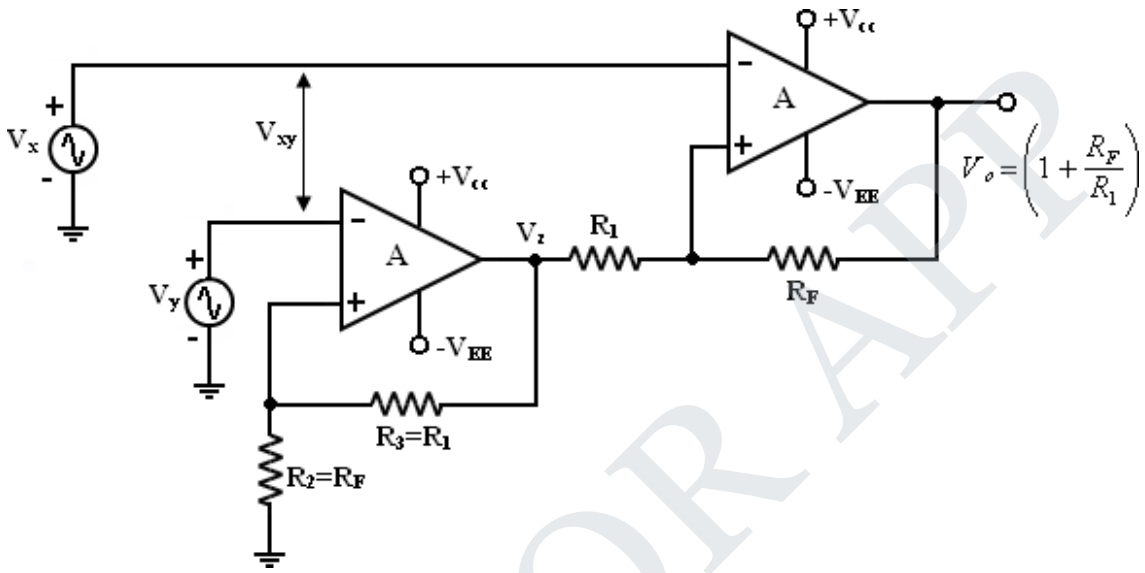
2. Differential Amplifier with 2 op-amps:

We can increase the gain of the differential amplifier and also increase the input resistance R_{if} if we use 2 op-amps.

Voltage gain:

It is compares of 2 stages 1. Non-inverting

. Differential amplifier with gain.



By finding the gain of these 2 stages, we can obtain the overall gain of the circuit, The o/p

$$V_2 = \left(1 + \frac{R_f}{R_2}\right)$$

Input Resistance:

The input resistance Rif of the differential amplifier is the resistance determined from either one of the two non-inverting terminals with the other grounded. The first stage A_1 is the non-inverting amplifier, its input resistance is

RiFy = Ri (1+AB) --------- (29. a)

Where Ri = open loop input resistance of the op-amp. B =
$R_2 / R_2 + R_3$

Similarly, with V_y shorted to ground (V_y = 0 V), the 2nd stage (A_2) also becomes non-inverting amplifier, whose input resistance is

RiFx = Ri (1+AB) --------- (29. b)

Where Ri = open loop input resistance of the op-amp B =

$R_1 /(R_1 + R_F)$

Since $R_1 = R_3$ and $R_F = R_2$, the Rify ≠ RiFx because the loading of the input sources V_x and V_y may occur. (Or)

The output signal may be smaller in amplitude than expected. This possible reduction in the amplitude of the output signal is drawback of differential amplifier.

To overcome this:

With proper selection of components, both RiFy and RiFx can be made much larger than the sources resistance so that the loading of the input sources does not occur.

Output resistance and Bandwidth of differential amplifier with feedback:

The output resistance of the differential amplifier should be the same as that of the non-inverting amplifier expect that $B = 1/A_D$ (i.e)

$R_{OF} = R_0 /(1+A/A_D)$ -------- (30)

A_D = closed loop gain of the differential amplifier R_0 = output resistance of the op-amp

A = open – loop volt gain of the op-amp

Remember that A_D is different for differential amplifier.

In the case of Inverting and Non-inverting amplifier, the bandwidth of the differential amplifier also depends on the closed loop gain of the amplifier and is given by,

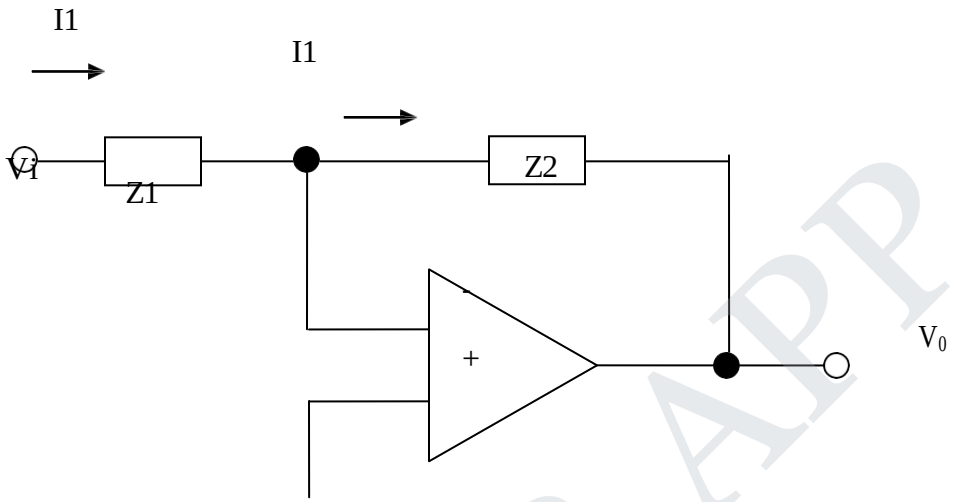
f_F = Unity gain Bandwidth closed loop gain A_D (or)

$f_F = (A) (f_0)$

UNIT – III

APPLICATIONS OF OPERATIONAL AMPLIFIER

SIGN CHANGER (PHASE INVERTER)



The basic inverting amplifier configuration using an op-amp with input impedance Z_1 and feedback impedance Z_f.

If the impedance Z_1 and Z_f are equal in magnitude and phase, then the closed loop voltage gain is -1,and the input signal will undergo a 180^0 phase shift at the output. Hence, such circuit is also called phase inverter. If two such amplifiers are connected in cascade, then the output from the second stage is the same as the input signal without any change of sign.

Hence, the outputs from the two stages are equal in magnitude but opposite in phase and such a system is an excellent paraphase amplifier.

Scale Changer:

Referring the above diagram, if the ratio $Z_f / Z_1 = k$, a real constant, then the closed loop gain is –k, and the input voltage is multiplied by a factor –k and the scaled output is available at the output. Usually, in such applications, Z_f and Z_1 are selected as precision resistors for obtaining precise and scaled value of input voltage.

PHASE SHIFT CIRCUITS

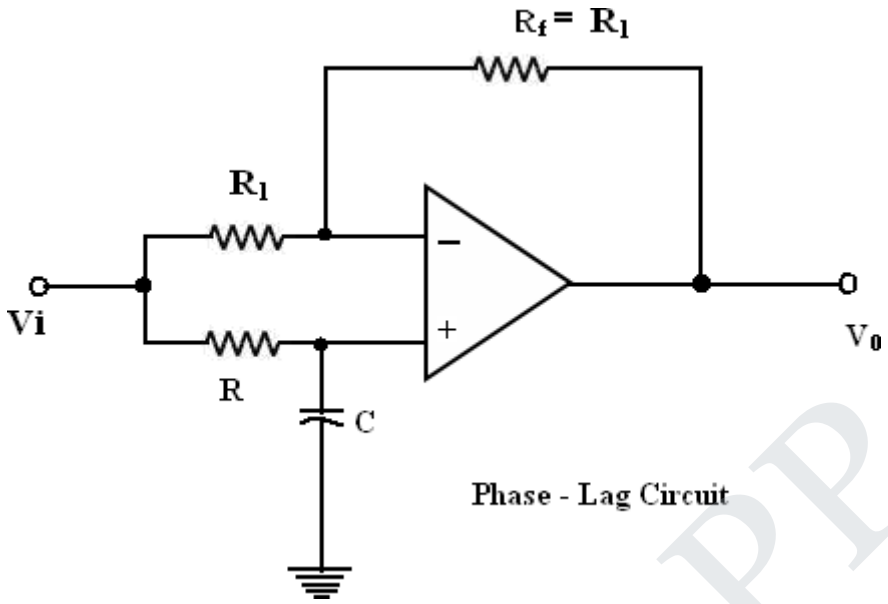
The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called constant-delay filters or all-pass filters. That constant delay refers to the fact the time difference between input and output remains constant when frequency is changed over a range of operating frequencies.

This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles.

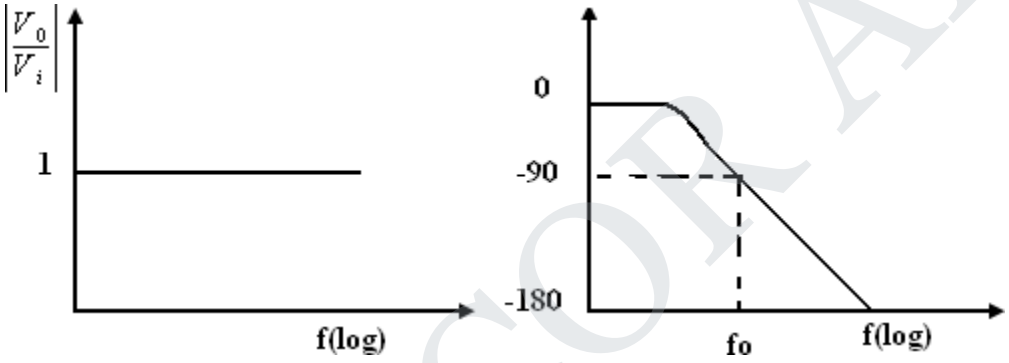
Phase-lag circuit:

Phase log circuit is constructed using an op-amp, connected in both inverting and non inverting modes. To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at(-)terminal of op-amp and a non inverting amplifier with a low-pass filter.

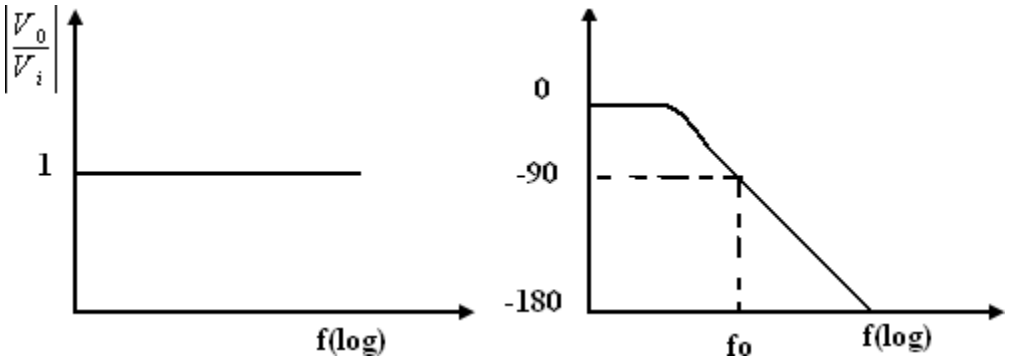
It is also assumed that inverting gain is -1 and non-inverting gain after the low-pass circuit is $1 + \frac{R_f}{R_1}$ =1+1=2, Since $R_f = R_1$



Phase - Lag Circuit



The relationship is complex as defined above equation and it shows that it has both magnitude and phase. Since the numerator and denominator are complex conjugates, their



Voltage follower:

If $R_1=\infty$ and Rf=0 in the non inverting amplifier configuration .

The amplifier act as a unity-gain amplifier or voltage follower.

That is

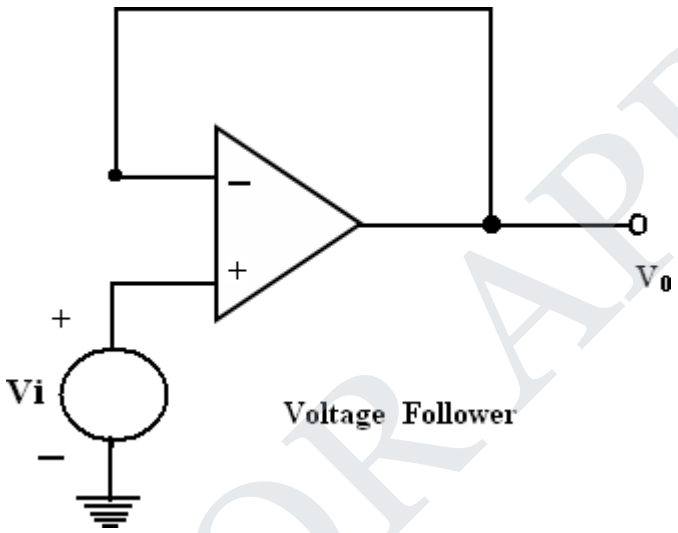
$$A_v = 1 + \frac{R_f}{R}$$

Since $\frac{R_f}{R_1} = 0 \quad A_v = 1$

The circuit consist of an op-amp and a wire connecting the output voltage to the input ,i.e the output voltage is equal to the input voltage, both in magnitude and phase. $V_0=V_i$

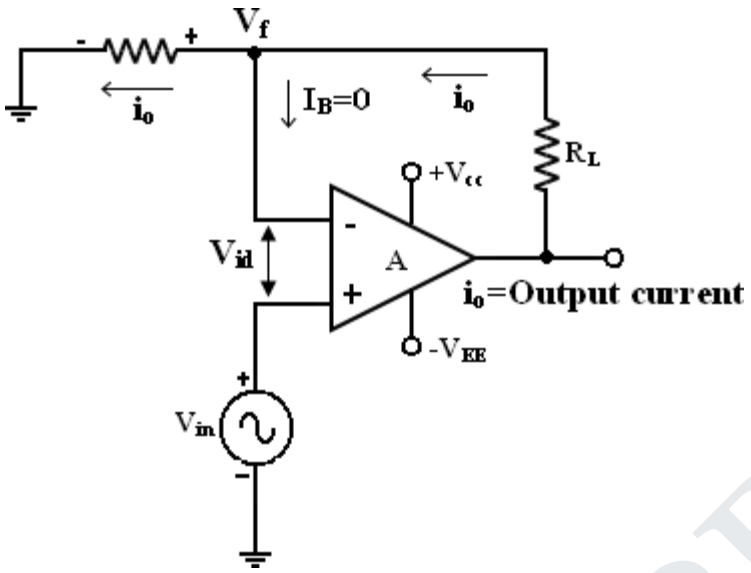
Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower. It offers very high input impedance of the order of MΩ and very low output impedance.

Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.



Voltage to Current Converter with floating loads (V/I):

1. Voltage to current converter in which load resistor R_L is floating (not connected to ground).
2. Vin is applied to the non inverting input terminal, and the feedback voltage across R_1 devices the inverting input terminal.
3. This circuit is also called as a current – series negative feedback amplifier.
4. Because the feedback voltage across R_1 (applied Non-inverting terminal) depends on the output current i_0 and is in series with the input difference voltage V_{id}.



Writing KVL for the input loop,

$$Vin \square V_{id} \square V_f$$

$$V_{id} \text{ t } 0v \text{ , since A is very large A}$$

$$Vin \square V_f$$

$$Vin \square R_1 \quad \text{`or}^{a}$$

$$i_0$$

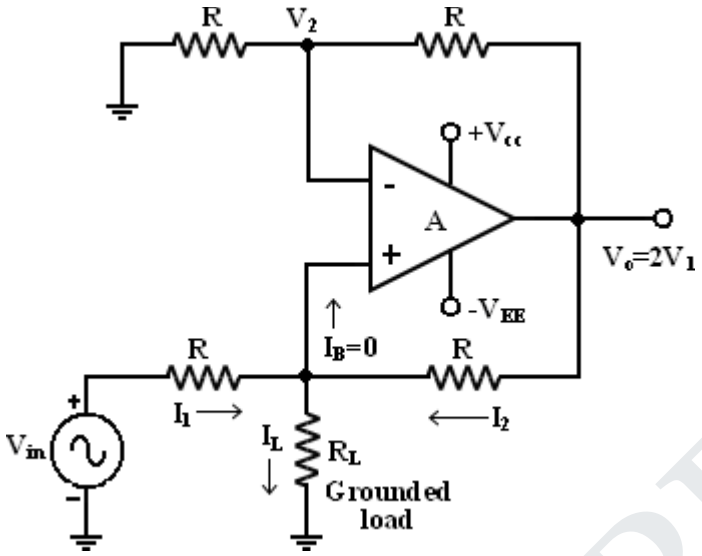
From the fig input voltage Vin is converted into output current of Vin/R_1 [Vin -> i_0] . In other words, input volt appears across R_1. If R_1 is a precision resistor, the output current (i_0 = Vin/R_1) will be precisely fixed.

Applications:

1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED
4. Zener diode testers.

Voltage – to current converter with Grounded load:

This is the other type V – I converter, in which one terminal of the load is connected to ground.



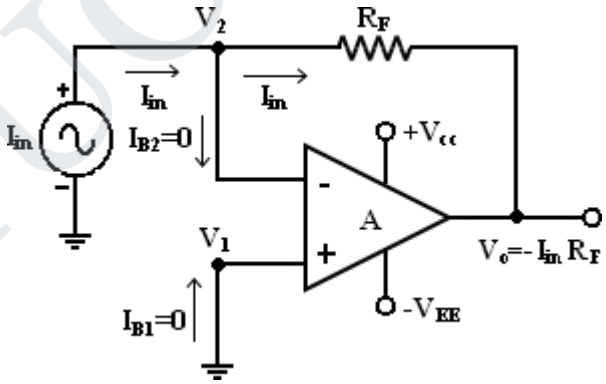
Analysis of the circuit:

The analysis of the circuit can be done by following 2 steps.

1. To determine the voltage V_1 at the non-inverting (+) terminals and
2. To establish relationship between V_1 and the load current I_L.

Applying KCL at node V_1 we can write that,

Current to Voltage Converter (I –V):

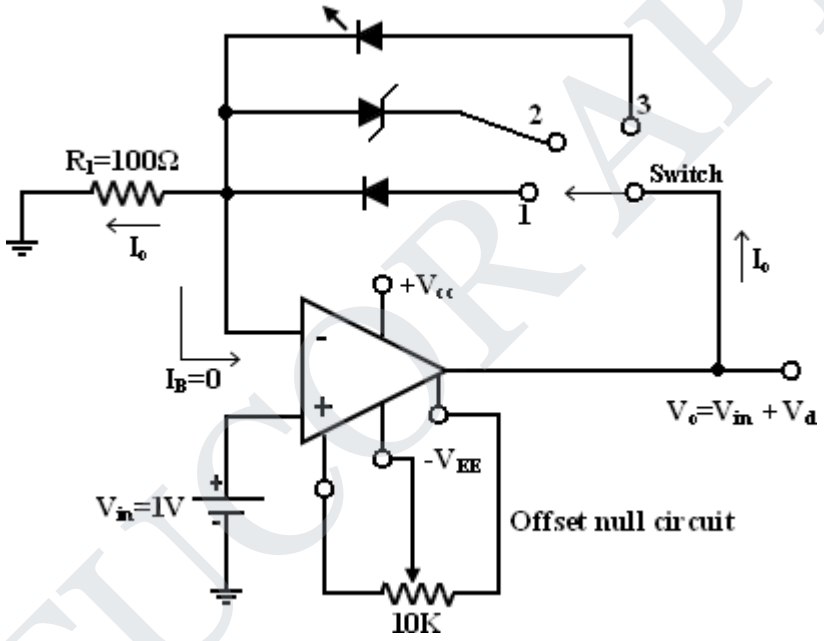


Sensitivity of the I – V converter:

1. The output voltage $V_0 = -R_F I_{in}$.
2. Hence the gain of this converter is equal to $-R_F$. The magnitude of the gain (i.e) is also called as sensitivity of I to V converter.
3. The amount of change in output volt ΔV_0 for a given change in the input current ΔIin is decide by the sensitivity of I-V converter.
4. By keeping R_F variable, it is possible to vary the sensitivity as per the requirements.

Applications of V-I converter with Floating Load:

1. Diode Match finder:



In some applications, it is necessary to have matched diodes with equal voltage drops at a particular value of diode current. The circuit can be used in finding matched diodes and is obtained from fig (V-I converter with floating load) by replacing R_L with a diode. When the switch is in position 1: (Diode Match Finder) Rectifierr diode (IN 4001) is placed in the f/b loop, the current through this loop is set by input voltage Vin and Resistor R_1 . For Vin = 1V and $R_1 = 100\Omega$, the current through this

$I_0 = Vin/R_1 = 1/100 = 10mA.$

As long as V_0 and R_1 constant, I_0 will be constant. The Voltage drop across the diode can be found either by measuring the volt across it or o/p voltage. The output voltage is equal to (Vin + V_D) V_0

= Vin + V_D . To avoid an error in output voltage the op-amp should be initially nulled. Thus the matched diodes can be found by connecting diodes one after another in the feedback path and measuring voltage across them.

2. Zener diode Tester:

(When the switch position 2)

when the switch is in position 2, the circuit becomes a zener diode tester. The circuit can be used to find the breakdown voltage of zener diodes. The zener current is set at a constant value by Vin and R_1. If this current is larger than the knee current (I_{ZK}) of the zener, the zenerr blocks (V_z) volts.

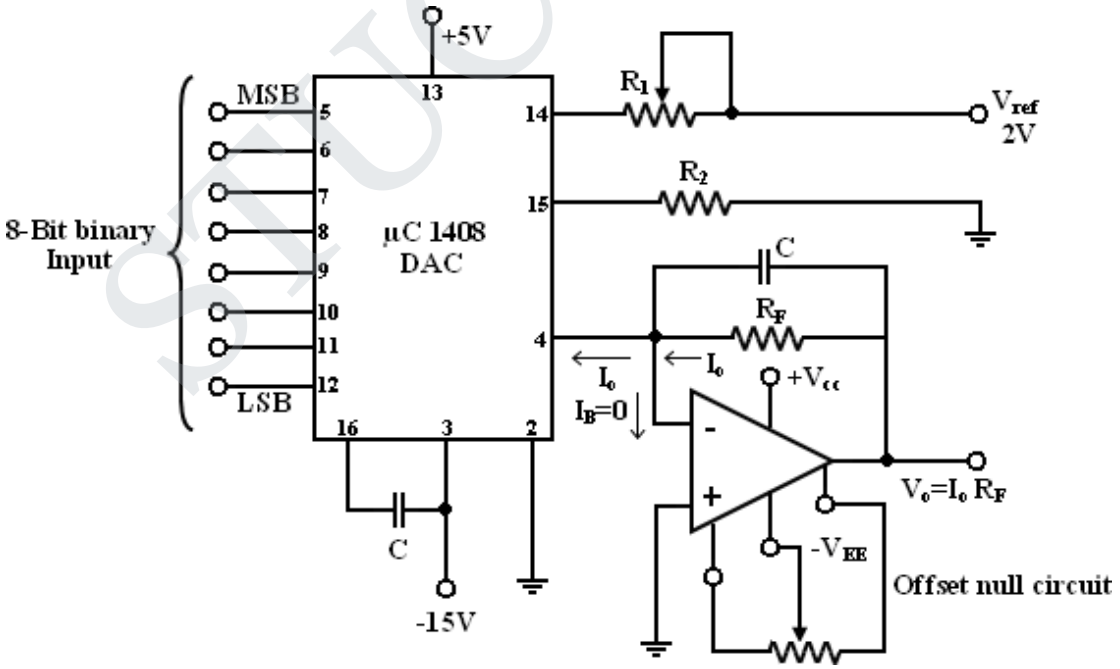
For Ex:

I_{ZK} = 1mA , V_Z = 6.2V, Vin = 1v , R_1 = 100Ω Since the current through the zener is , I_0 = Vin/R_1 = 1/100 =10mA > I_{ZK} the voltage across the zener will be approximately equal to 6.2V.

3. When the switch is in position 3: (LED)

The circuit becomes a LED when the switch is in position 3. LED current is set at a constant value by Vin and R_1. LEDs can be tested for brightness one after another at this current. Matched LEDs with equal brightness at a specific value of current are useful as indicates and display devices in digital applications.

Applications of I – V Converter:



One of the most common use of the current to voltage converter is

1. Digital to analog Converter (DAC)
2. Sensing current through Photodetector. Such as photocell, photodiodes and photovoltaic cells.

Photoconductive devices produce a current that is proportional to an incident energy or light (i.e) It can be used to detect the light.

1. DAC using I – V converter:

It shows a combination of a DAC and current to voltage converter. The 8 digit binary signal is the input to the DAC and V_0 is the corresponding analog output of the current to voltage converter. The outputu of the DAC is current I_0, the value of which depends on the logic state (0 or 1), of the binary inputs as indicated by the following eqn.

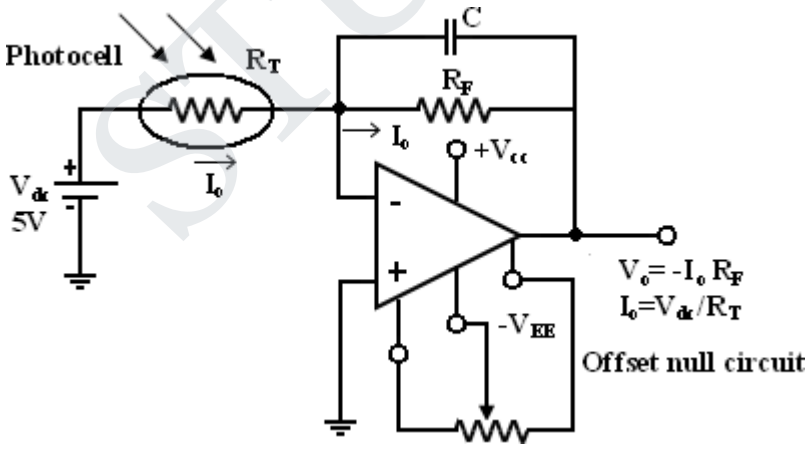
This means I_0 is zero when all inputs are logic 0.

I_0 is max when all inputs are logic 1.

The variations in I_0 can be converted into a desired o/p voltage range by selecting a proper value for R_F. since, $V_0 = I_0 R_F$

Where I_0 is given by eqn (1). It is common to parallel R_F with capacitance C to minimize the overshoot. In the fig the o/p voltage of the current to voltage converter is positive because the direction of input current I_0 is opposite to that in the basic I – V Converter.

2. Detecting current through photosensitive devices:



Photocells, photodiodes, photovoltaic cells give an output curren that depends on the intensity of light and independent of the load. The current through this devices can be converted to voltage by I – V converter and it can be used as a measure of the amount of light. In this fig photocell is connected to the I – V Converter. Photocell is a passive transducer, it requires an external dc voltage(Vdc). The dc voltage can be eliminated if a photovoltaic cell is used instead of a photocell. The Photovoltaic Cell is a semiconductor device that converts the radiant energy to electrical power. It is a self generating circuit because it doesnot require dc voltage externally. Ex of Photovoltaic Cell : used in space applications and watches.

Summing Amplifier:

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer.

An inverting summer or a non-inverting summer may be discussed now.

Inverting Summing Amplifier:

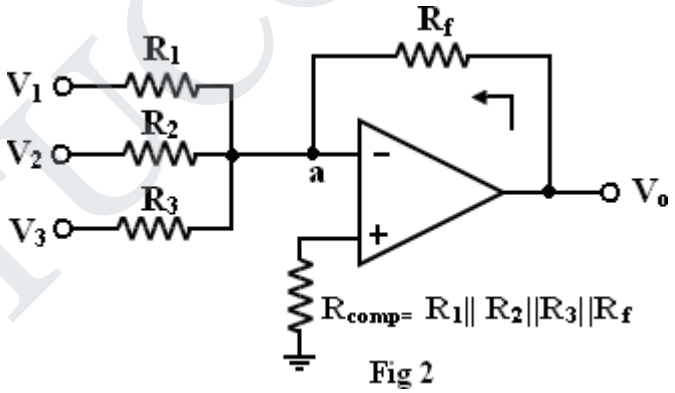


Fig 2

A typical summing amplifier with three input voltages V_1, V_2 and V_3 three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in figure 2.

The following analysis is carried out assuming that the op-amp is an ideal one, that is, $A_{OL} = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$. So the effective input resistance $R_i = R_1 \parallel R_2 \parallel R_3$. Therefore, $R_{comp} = R_i \parallel R_f = R_1 \parallel R_2 \parallel R_3 \parallel R_f$.

Non-Inverting Summing Amplifier:

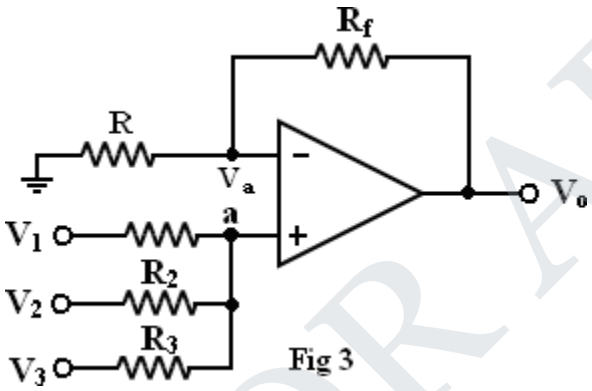


Fig 3

A summer that gives a non-inverted sum is the non-inverting summing amplifier of figure **3.** Let the voltage at the (-) input teriminal be V_a.

which is a non-inverting weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then $V_o = V_1+V_2+V_3$

Subtractor:

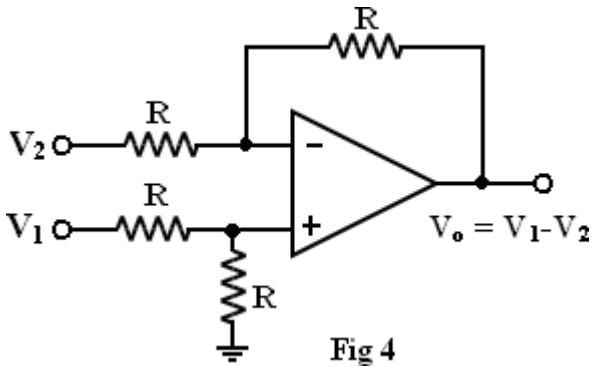


Fig 4

A basic differential amplifier can be used as a subtractor as shown in the above figure. If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

To find the output V_{01} due to V_1 alone, make $V_2 = 0$.

Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

$$V_{01} = \frac{V_1}{2}\left(1 + \frac{R_f}{R}\right) = V_1$$

Similarly the output V_{02} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$$V_{02} = -V_2$$

Thus the output voltage V_o due to both the inputs can be written as

$$V_o = V_{01} + V_{02} = V_1 - V_2$$

Adder/Subtractor:

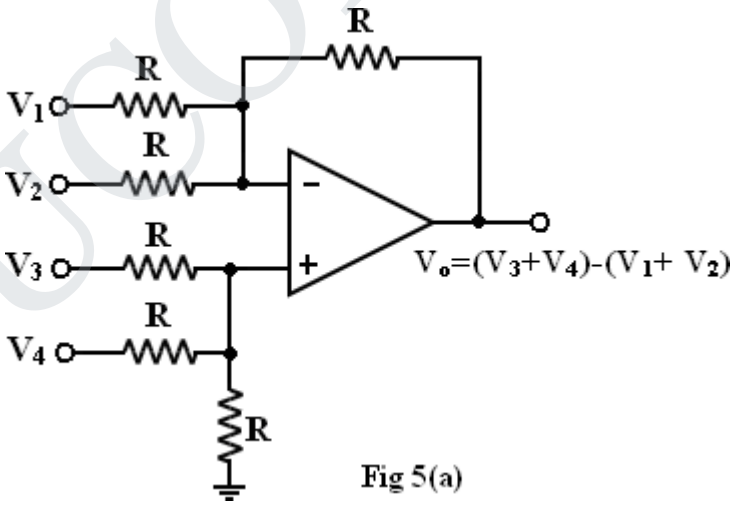


Fig 5(a)

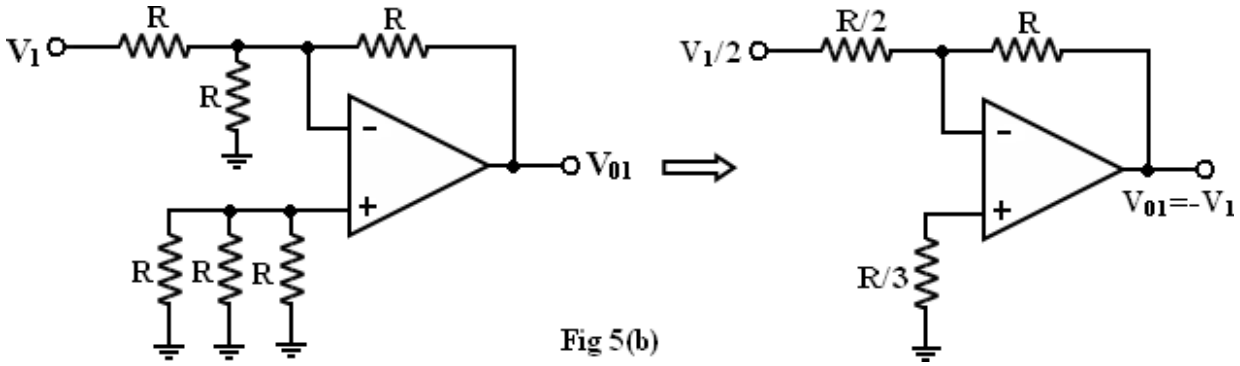


Fig 5(b)

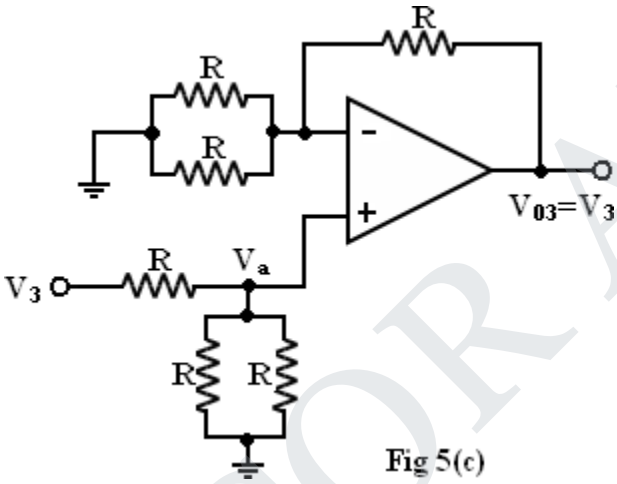


Fig 5(c)

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in figure 5(a).

The output voltage V_o can be obtained by using superposition theorem. To find output voltage V_{01} due to V_1 alone, make all other input voltages V_2, V_3 and V_4 equal to zero.

The simplified circuit is shown in figure 5(b). This is the circuit of an inverting amplifier and its output voltage is,

(by Thevenin‘s equivalent circuit at inverting input terminal).

Similarly, the output voltage V_{02} due to V_2 alone is,

V_{02} □@V v tage to the input voltage signal V_3
2 o V_{03} alone applied at the (+)
l due

Now, the output

input terminal can be found by setting V_1, V_2 and V_4 equal to zero.

The circuit now becomes a non-inverting amplifier as shown in figure 5(c). The voltage V_a at the non-inverting terminal is

Similarly, it can be shown that the output voltage V_{04} due to V_4 alone is

$$V_{04} = V_4$$

Thus, the output voltage V_o due to all four input voltages is given by

$$V_o = V_{01} + V_{02} + V_{03} + V_{04}$$

$$V_o = \left(1 + \frac{R_b}{R_c}\right) V_1 + \left(1 + \frac{R_b}{R_c}\right) V_2 + V_3 + V_4$$

$$V_o = V_3 + V_4 + \left(1 + \frac{R_b}{R_c}\right)(V_1 + V_2)$$

So, the circuit is an adder-subtractor.

Instrumentation Amplifier:

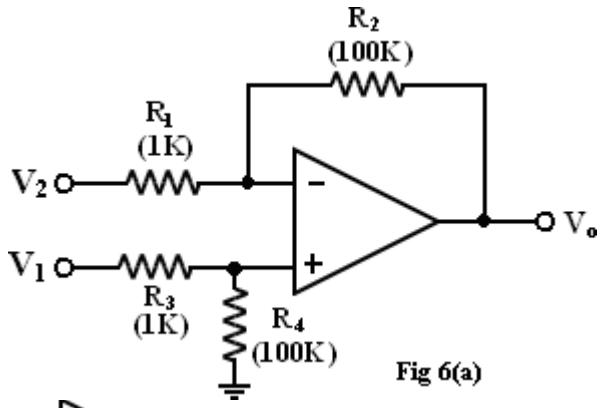


Fig 6(a)

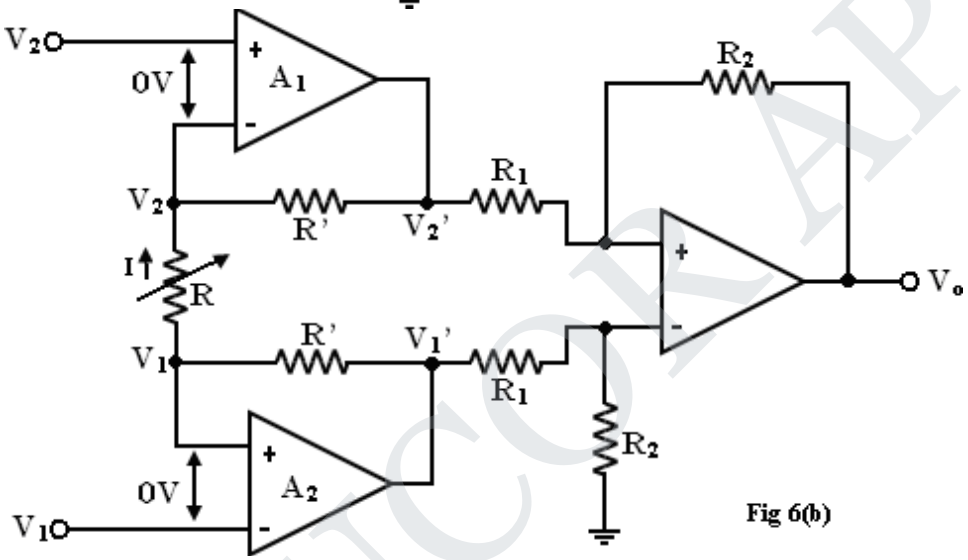


Fig 6(b)

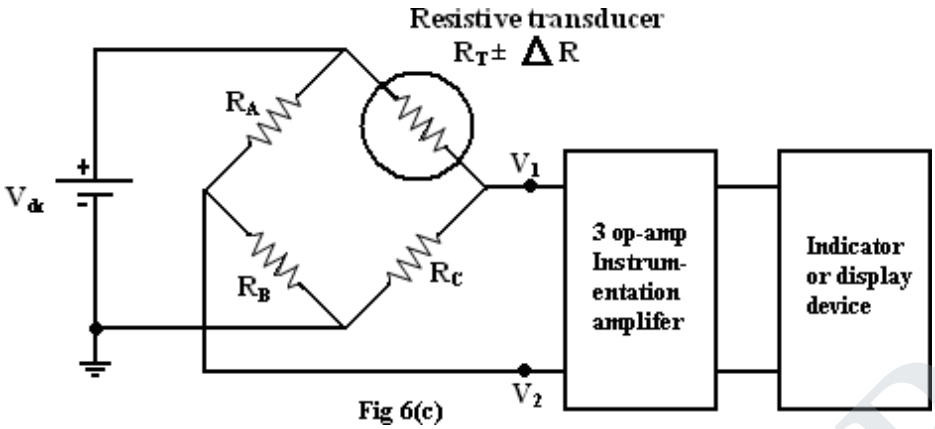


Fig 6(c)

In a number of industrial and consumer applications, one is required to measure and control physical quantities.

Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. these physical quantities are usually measured with help of transducers.

The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are

1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature coefficient
4. low output impedance

There are specially designed op-amps such as µA725 to meet the above stated requirements of a good instrumentation amplifier. Monolithic (single chip) instrumentation amplifier are also available commercially such as AD521, AD524, AD620, AD624 by Analog Devices, LM363.XX (XX -->10,100,500) by National Semiconductor and INA101, 104, 3626, 3629 by Burr Brown.

In the circuit of figure 6(a), source V_1 sees an input impedance = R_3+R_4 (=101K) and the impedance seen by source V_2 is only R_1 (1K). This low impedance may load the signal source heavily.

Therefore, high resistance buffer is used preceding each input to avoid this loading effect as shown in figure 6(b).

The op-amp A_1 and A_2 have differential input voltage as zero. For $V_1=V_2$, that is, under common mode condition, the voltage across R will be zero. As no current flows through R and R‘ the non-inverting amplifier.

A_1 acts as voltage follower, so its output $V_2‘=V_2$. Similarly op-amp A_2 acts as voltage follower having output $V_1‘=V_1$. However, if $V_1\neq V_2$, current flows in R and R‘, and $(V_2‘-V_1‘)>(V_2-V_1)$. Therefore, this circuit has differential gain and CMRR more compared to the single op-amp circuit of figure 6(a).

The difference gain of this instrumentation amplifier R, however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.

Figure 6(c) shows a differential instrumentation amplifier using Transducer Bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured.

The bridge is initially balanced by a dc supply voltage V_{dc} so that $V_1=V_2$. As the physical quantity changes, the resistance R_T of the transducer also changes, causing an unbalance in the bridge ($V_1 \neq V_2$). This differential voltage now gets amplified by the three op-amp differential instrumentation amplifier.

There are number differential applications of instrumentation amplifier with the transducer bridge, such as temperature indicator, temperature controller, and light intensity meter to name a few.

Differentiator:

One of the simplest of the op-amp circuits that contains capacitor in the differentiating amplifier.

Differentiator:

As the name implies, the circuit performs the mathematical operation of differentiation (i.e) the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1 .

The expression for the output voltage can be obtained KCL eqn written at node V_2 as follows,

Since the differentiator performs the reverse of the integrator function.

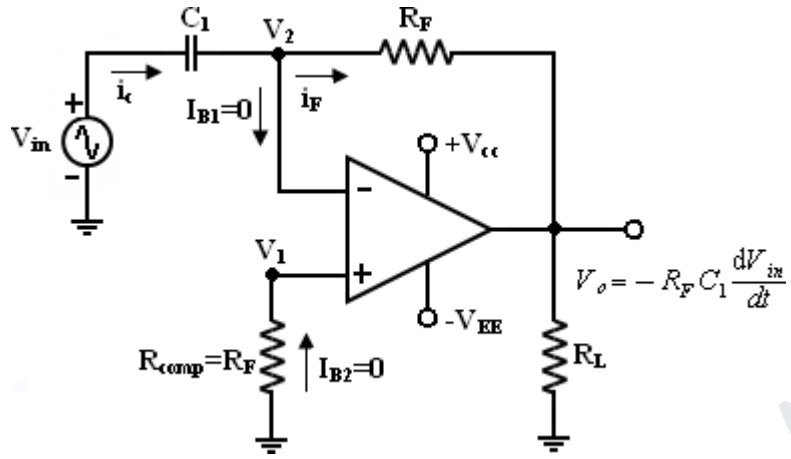
Thus the output V_0 is equal to $R_F C_1$ times the negative rate of change of the input voltage Vin with time.

The –sign => indicates a 180^0 phase shift of the output waveform V_0 with respect to the input signal.

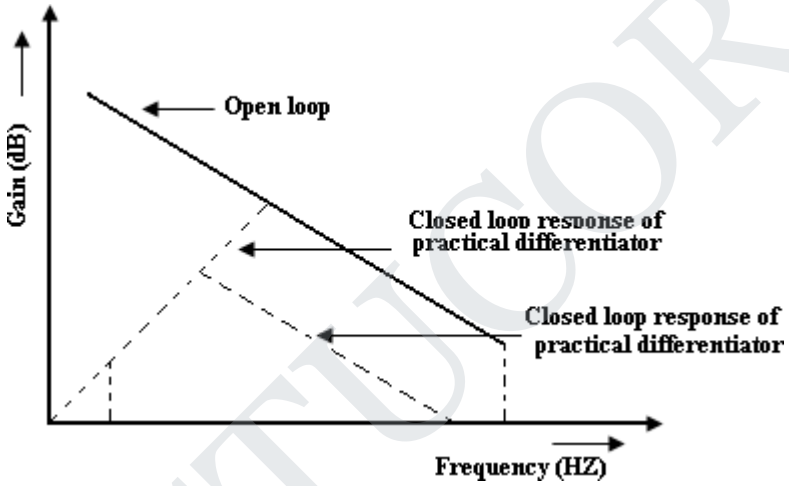
The below circuit will not do this because it has some practical problems.

The gain of the circuit (R_F /XC_1) R with R in frequency at a rate of 20dB/decade. This makes the circuit unstable.

Also input impedance XC_1 Swith Rin frequency which makes the circuit very susceptible to high frequency noise.



Basic Differetntiator



From the above fig, f_a = frequency at which the gain is 0dB and is given by,

Both stability and high frequency noise problems can be corrected by the addition of 2 components. R_1 and C_F . This circuit is a practicaldifferentiator.

From Frequency f to feedback the gain Rsat 20dB/decade after feedback the gain S at 20dB/decade. This 40dB/ decade change in gain is caused by the R_1 C_1 and R_F C_F combinations. The gain limiting frequency f_b is given by,

Where R_1 C_1 = R_F C_F

R_1 C_1 and R_F C_F => helps to reduce the effect of high frequency input, amplifier noise and offsets.

All R_1 C_1 and R_F C_F make the circuit more stable by preventing the Rin gain with frequency.

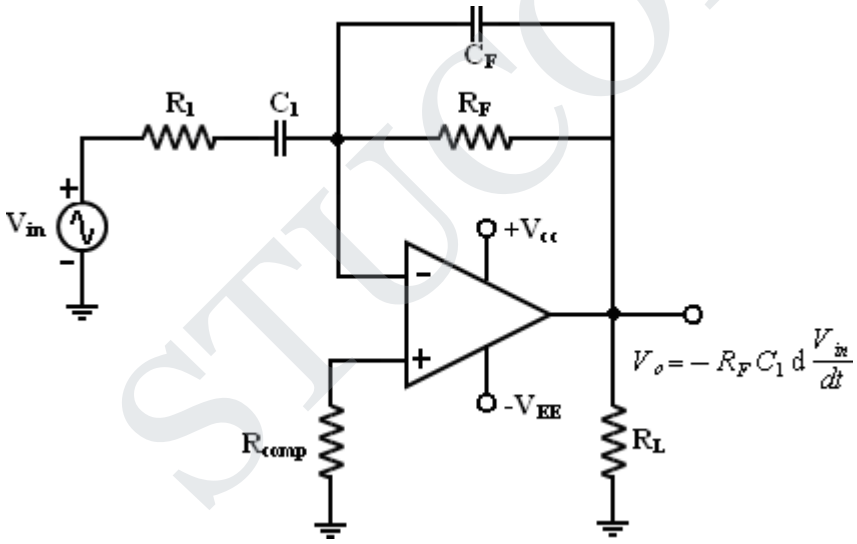
Generally, the value of Feedback and in turn R_1 C_1 and R_F C_F values should be selected such that

$$f_a < f_b < f_C$$

where

f_c □ *unity gain bandwidth*

The input signal will be differentiated properly, if the time period T of the input signal is larger than or equal to R_F C_1 (i.e) T > R_F C_1



Practical Differentiator

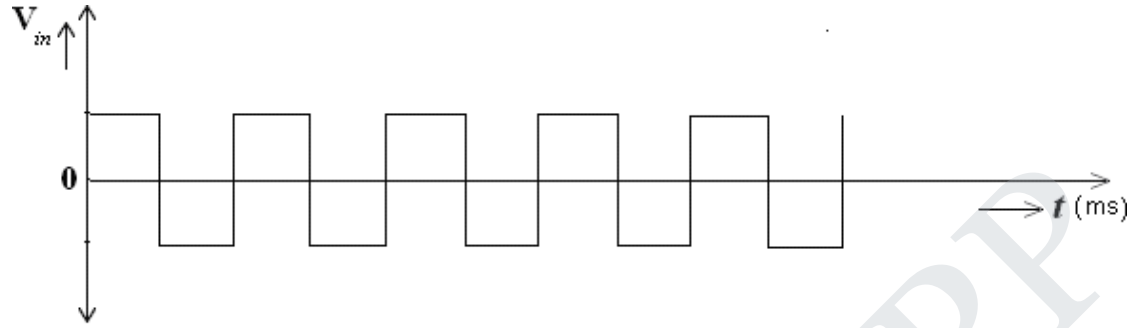
A workable differentiator can be designed by implementing the following steps.

1. Select fa equal to the highest frequency of the input signal to be differentiated then assuming a value of C_1 < 1μf. Calculate the value of R_F .

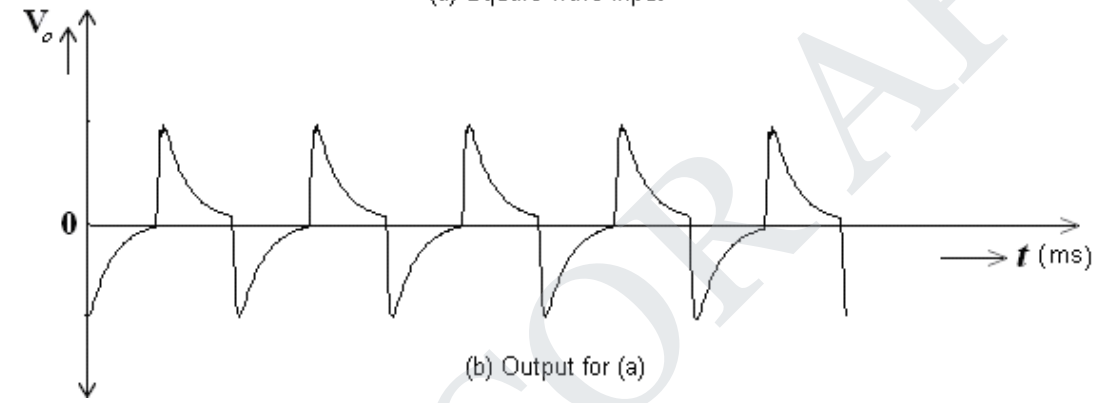
2. Choose fb = 20fa and calculate the values of R_1 and C_F so that R_1 C_1 = R_F C_F .

Uses:

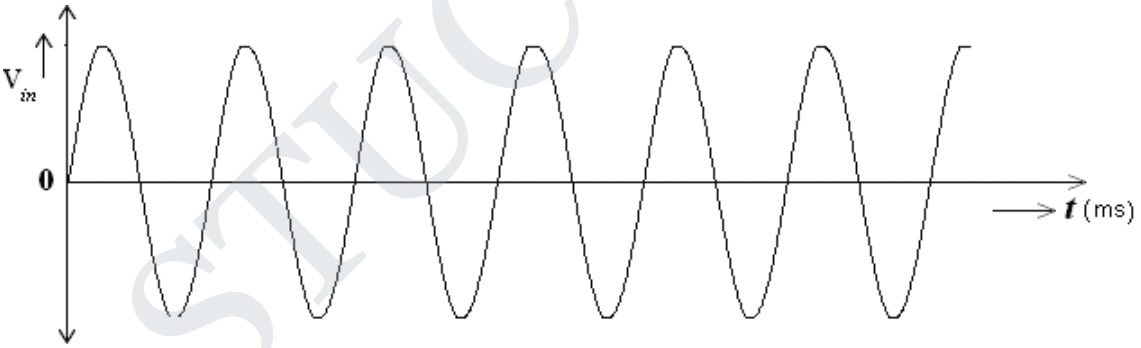
Its used in waveshaping circuits to detect high frequency components in an input signal and also as a rate of change and detector in FM modulators.



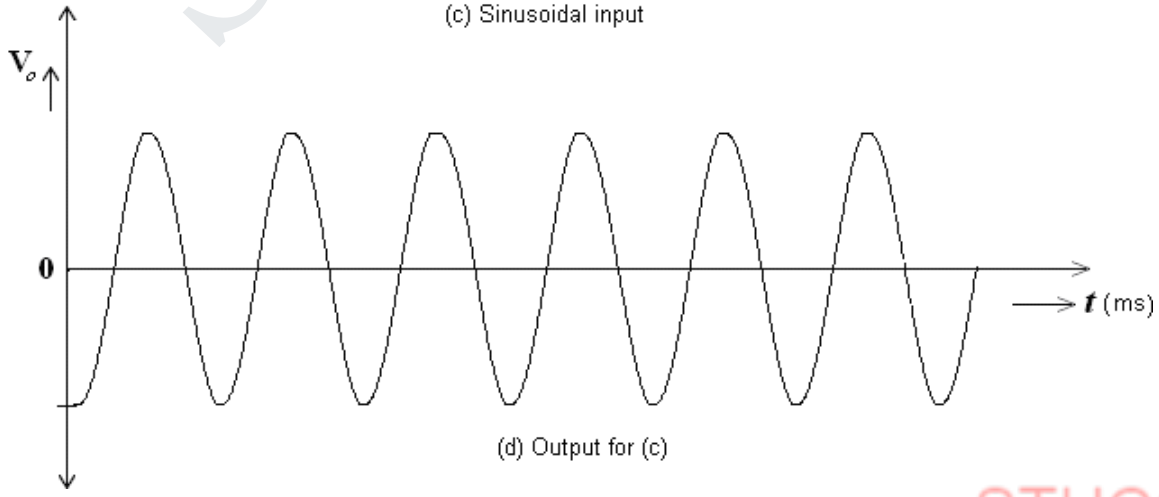
(a) Square wave input



(b) Output for (a)



(c) Sinusoidal input



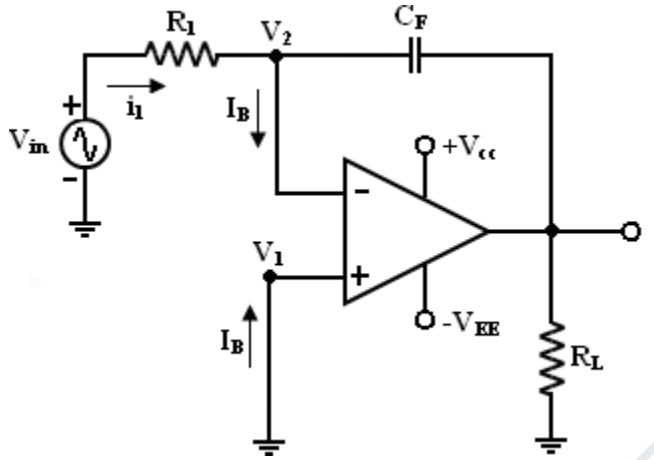
(d) Output for (c)

This o/p for practical differentiator.

Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or Integration Amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C_F .

The expression for the output voltage V_0 can be obtained by KVL eqn at node V_2 .



$$V_o = -\frac{1}{R_1 C_F}\int_0^t V_{in}\,dt + C$$

`

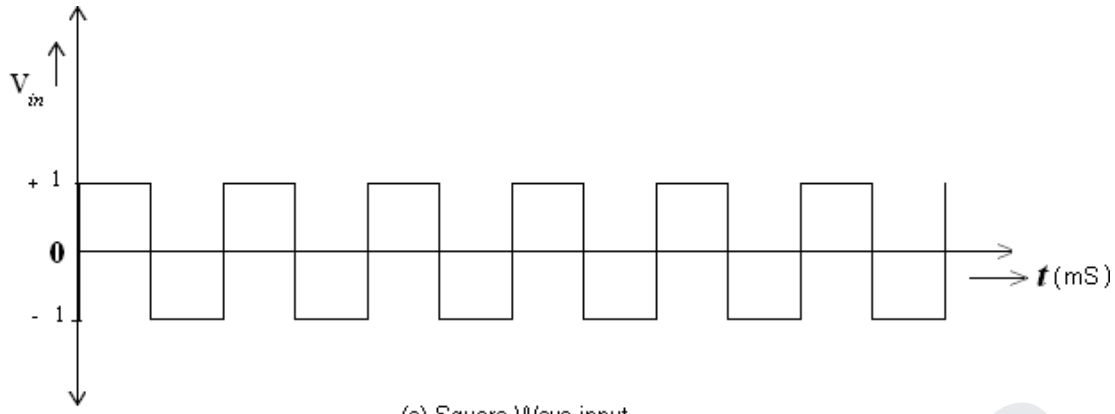
a

where C @integration constant A

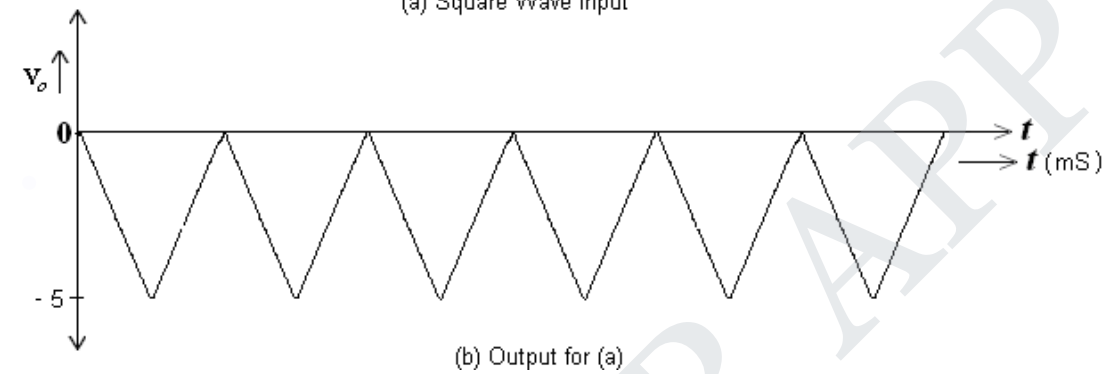
eqn (3) indicates that the output is directly proportional to the negative integral of the input volts and inversely proportional to the time constant $R_1 C_F$.

Ex: If the input is sine wave -> output is cosine wave.

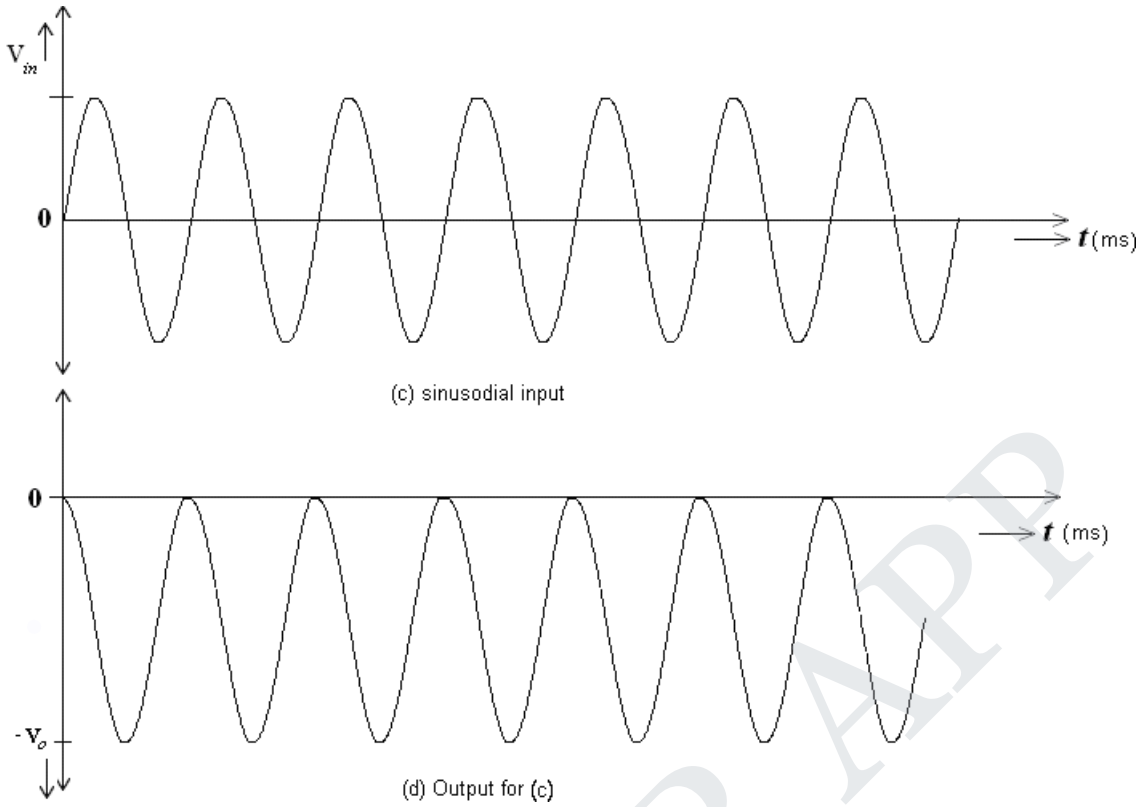
If the input is square wave -> output is triangular wave.



(a) Square Wave input



(b) Output for (a)



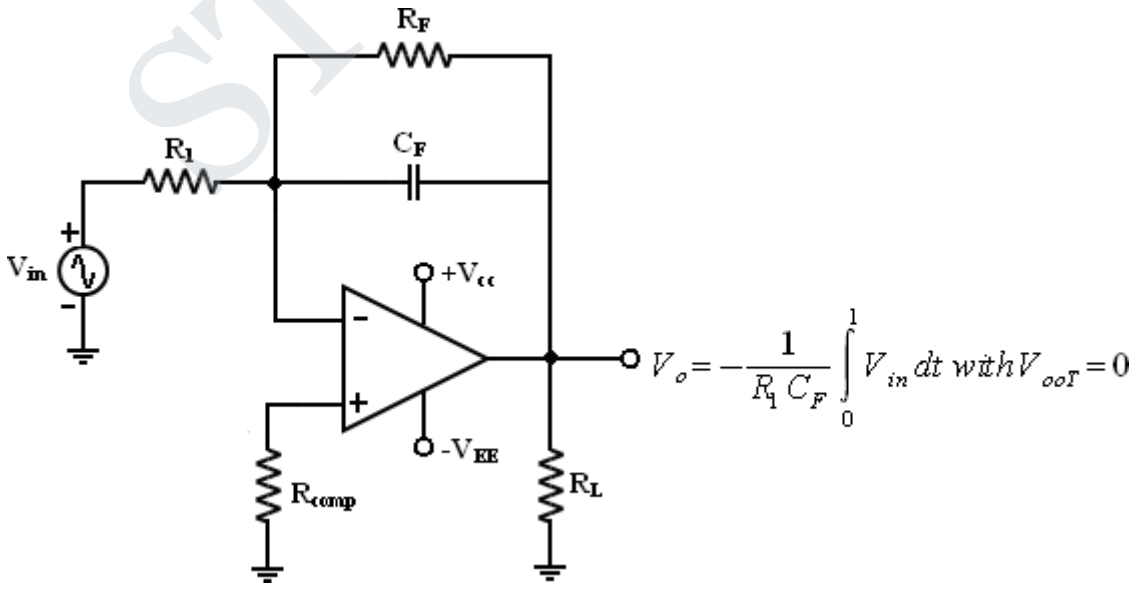
These waveform with assumption of R_1 C_f = 1, Vout =0V (i.e) C =0.

When Vin = 0 the integrator works as an open loop amplifier because the capacitor C_F acts an open circuit to the input offset voltage Vio.

Or

The Input offset voltage Vio and the part of the input are charging capacitor C_F produce the error voltage at the output of the integrator.

Practical Integrator:



Practical Integrator to reduce the error voltage at the output, a resistor R_F is connected across the feedback capacitor C_F .

Thus R_F limits the low frequency gain and hence minimizes the variations in the output voltages. The frequency response of the basic integrator, shown from this fb is the frequency at which the gain is dB and is given by,

Both the stability and low frequency roll-off problems can be corrected by the addition of a resistor R_F in the practical integrator.

Stability -> refers to a constant gain as frequency of an input signal is varied over a certain range.

Low frequency -> refers to the rate of decrease in gain roll off at lower frequencies.

From the fig of practical Integrators,

f is some relative operating frequency and for frequencies f to fa to gain R_F / R_1 is constant. After fa the gain decreases at a rate of 20dB/decade or between fa and fb the circuit act as an integrator.

Generally the value of fa and in turn R_1 C_F and R_F C_F values should be selected such that fa<fb.

In fact, the input signal will be integrated properly if the time period T of the signal is larger than or

equal to R_F C_F, (i.e)

` a

$$T \geq R_F C_F \text{ @@@@6}$$

Uses:

Most commonly used in analog computers.

ADC

Signal wave shaping circuits.

Log and Antilog Amplifier:

There are several applications of log and antilog amplifiers. Antilog computation may require functions such as ln x, log x or Sinhx.

These can be performed continusely with log amps, and also used for direct dB display on a digital Voltmeter and Spectrum analyzer.

Log-amp can also be used to compress the dynamic range of a signal.

Log Amplifier:

The fundamental log amp circuit shown in fig

Fig a. Fundamental log-amp Circuit

Where a grounded base transistor is placed in the feedback path. Since the collector is placed in the feedback path.

Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_C \approx I_s \, e^{\frac{qV_{BE}}{kT}} \text{ ---------- (2)}$$

Is-emitter saturation current $\approx 10^{-13}$A

k=Boltzmann's constant

T=absolute temperature(in ^{o} K)

d [illegible] e

The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (ln),one can find $\log_{10}$, by proper scaling Log10X=0.4343 ln X----------(6) The circuit have one problem.

The emitter saturation current Is varies from transistor to transistor and with temperature. Thus a stable reference voltage V ref cannot be obtained

This is eliminated by the circuit given in fig(b)

The input is applied to one log-amp, while a reference voltage is applied to one log-amp,while a reference voltage is applied to another log-amp.

The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

Fig(b)Log-amp with saturation current and temperature compensation

Assume $I_{S1}=I_{S2}=I_S$----------(7)

Antilog Amplifier

The Circuit is shown in fig .The input Vi for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2 . The output V_o of the antilog- amp is fed back to the inverting input of A_1 through the resistor R_1.

The base to emitter voltage of transistors Q_1 and Q_2 can be written as

Since the base of Q_1 is tied to ground, we get

Or, $kT\ R_2 \square R_{TC}\qquad V_{ref}$

Changing the natural log i.e.,ln to $\log_{10}$ using eqn(6) we get

Hence an increase of input by one volt causes the output to decrease by a decade.

Comparator

To obtain for better performance, we shall also look at integrated designed specifically as comparators and converters. A comparator as its name implies, compares a signal voltage on one input of an op-amp with a known voltage called a reference voltage on the other input. Comparators are used in circuits such as,

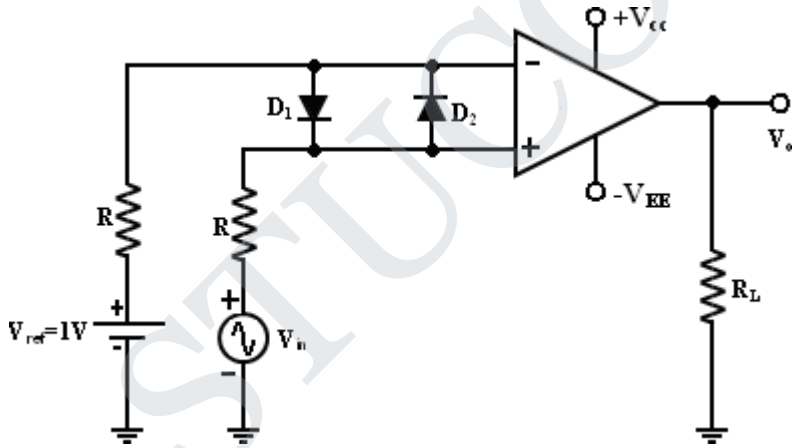
Digital Interfacing

Schmitt Trigger

Discriminator

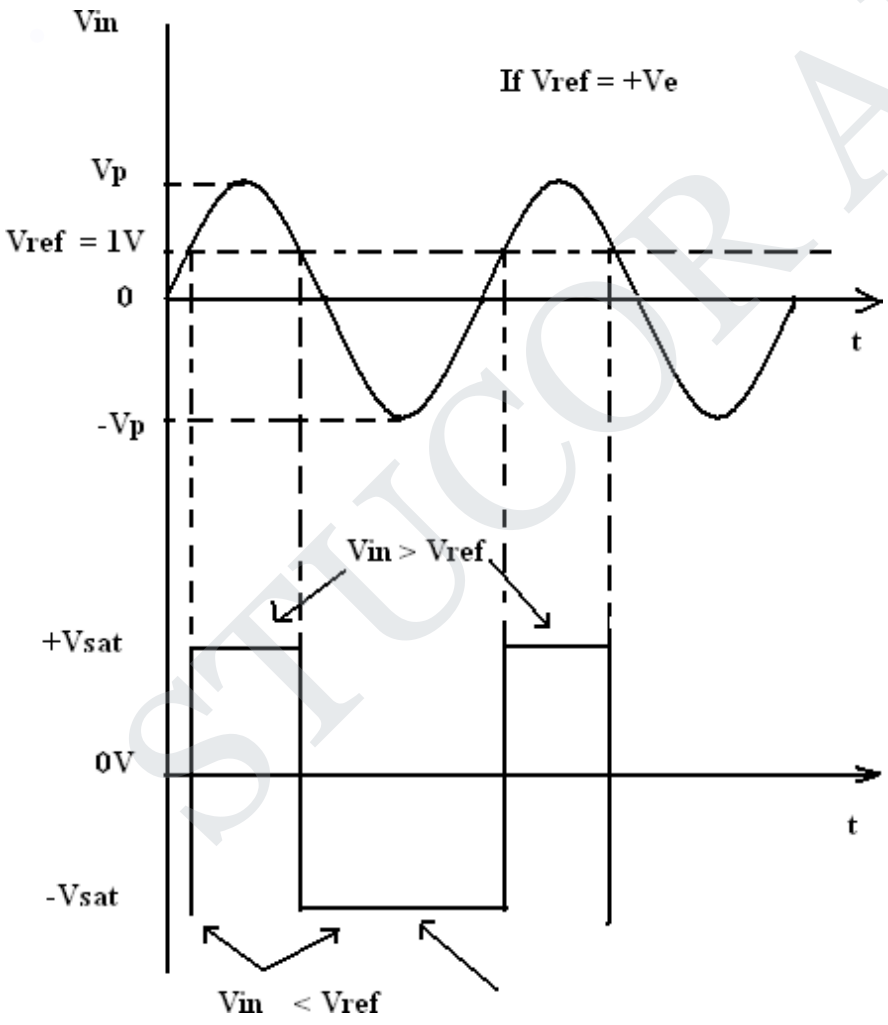
Voltage level detector and oscillators

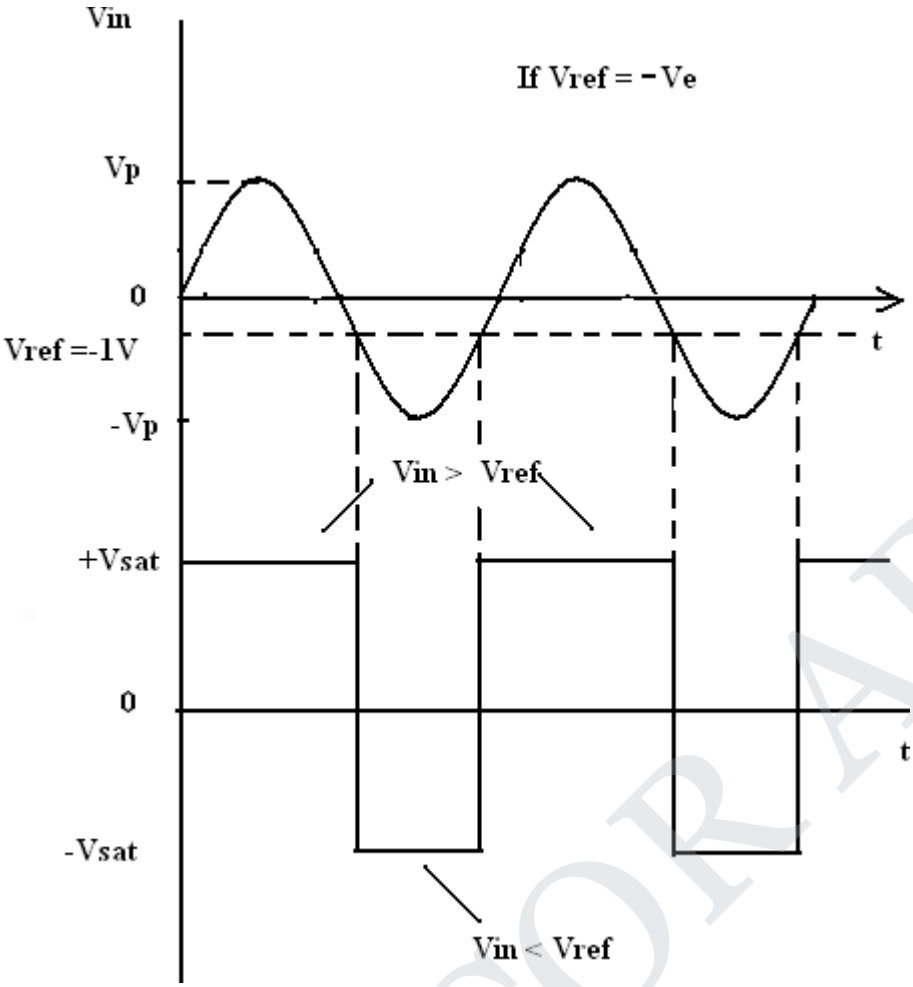
1. Non-inverting Comparator:



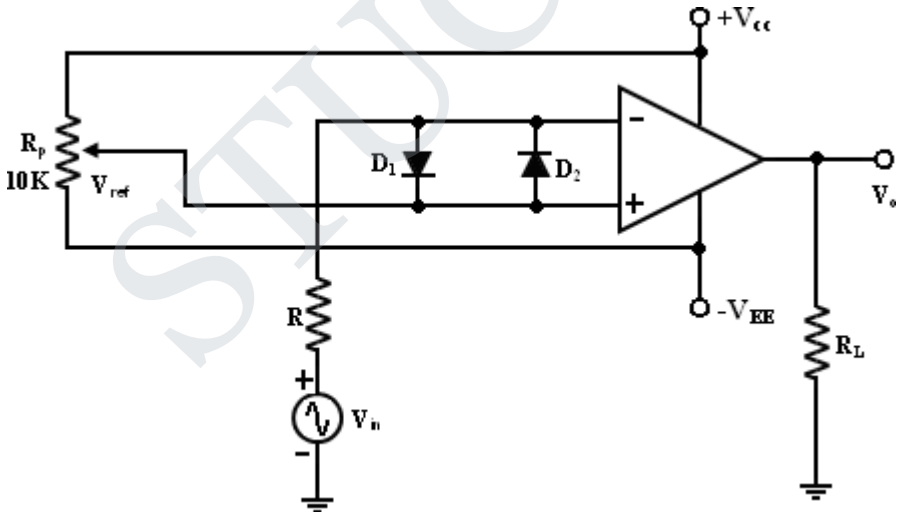
A fixed reference voltage Vref of 1 V is applied to the negative terminal and time varying signal voltage Vin is applied tot the positive terminal.When Vin is less than Vref the output becomes V_0 at –Vsat [Vin < Vref => V_0 (-Vsat)]. When Vin is greater than Vref, the (+) input becomes positive, the V_0 goes to +Vsat. [Vin > Vref => V_0 (+Vsat)]. Thus the V_0 changes from one saturation level to another. The diodes D_1 and D_2 protects the op-amp from damage due to the excessive input voltage Vin. Because of these diodes, the difference input voltage Vid of the op-amp diodes are called clamp diodes. The resistance R in series with Vin is used to limit the current through D_1 and D_2 . To reduce offset problems, a resistance Rcomp = R is connected between the (-ve) input and Vref.

Input and Output Waveforms:



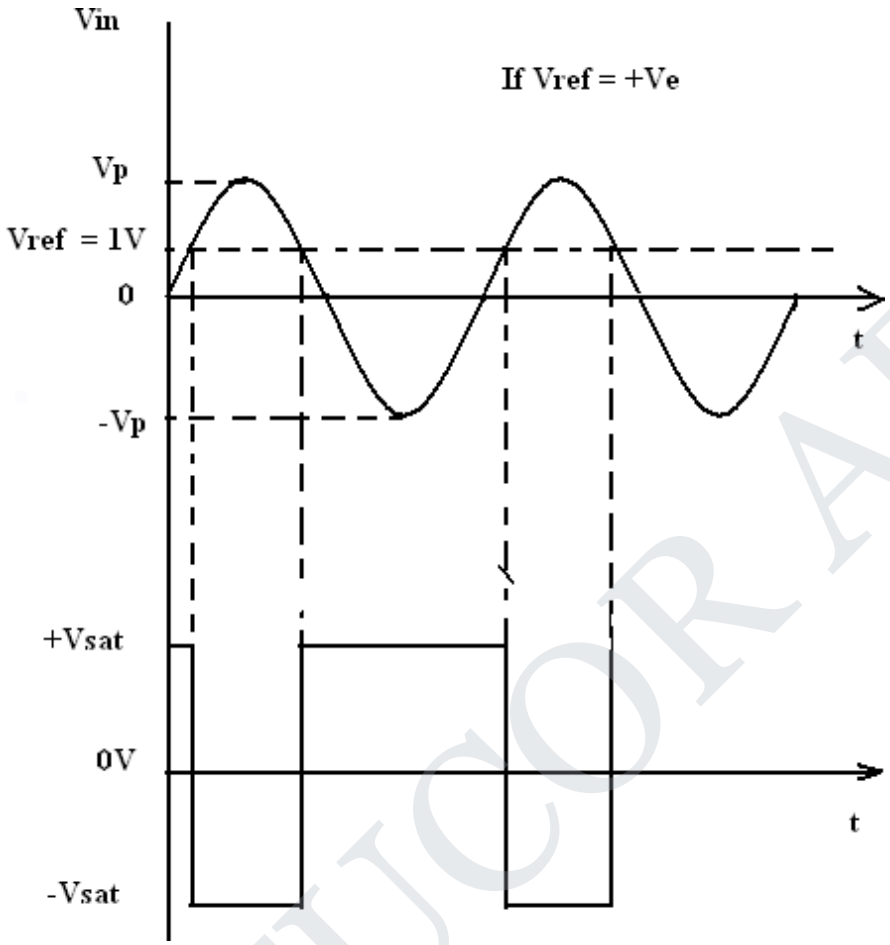


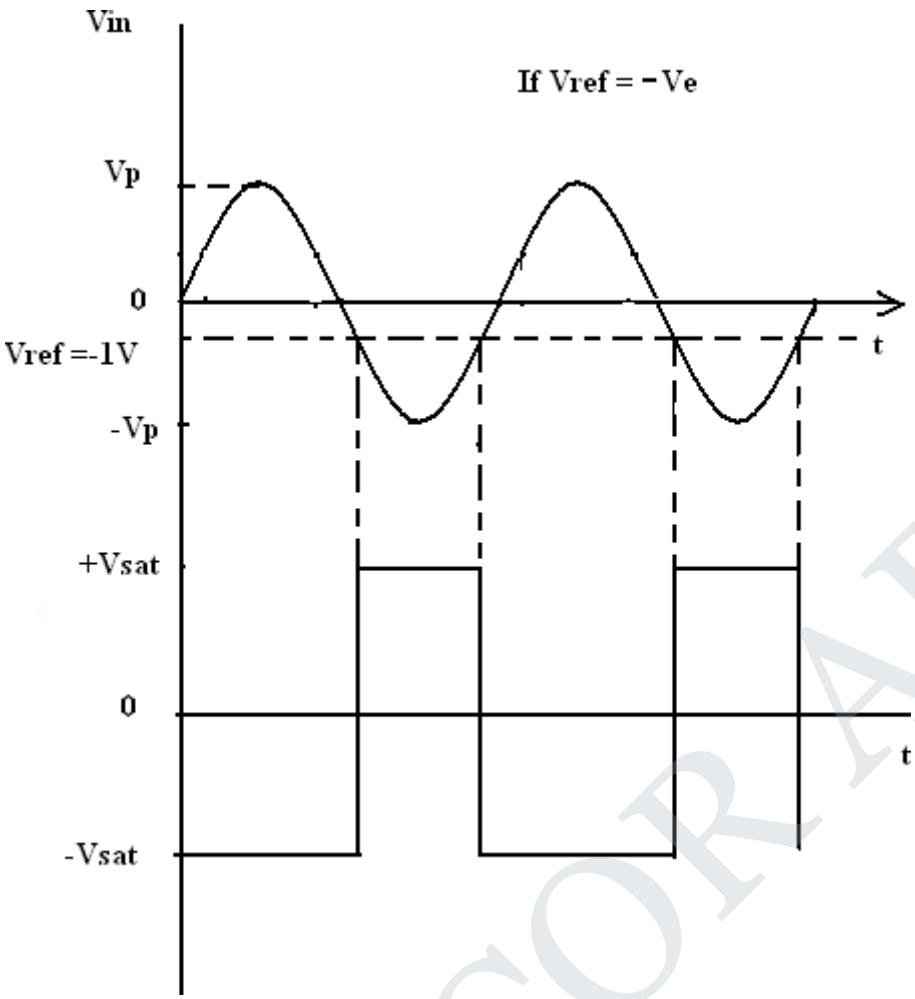
2. Inverting Comparator:



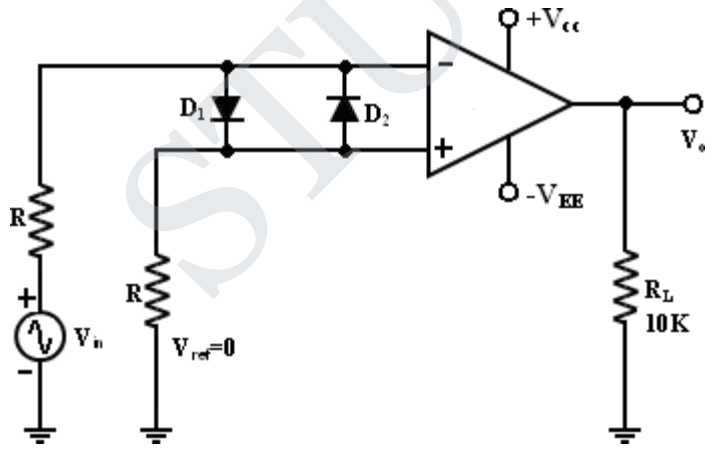
This fig shows an inverting comparator in which the reference voltage Vref is applied to the (+) input terminal and Vin is applied to the (-) input terminal. In this circuit Vref is obtained by using a

10K potentiometer that forms a voltage divider with dc supply volt +Vcc and -1 and the wiper connected to the input. As the wiper is moved towards +Vcc, Vref becomes more positive. Thus a Vref of a desired amplitude and polarity can be obtained by simply adjusting the 10k potentiometer.



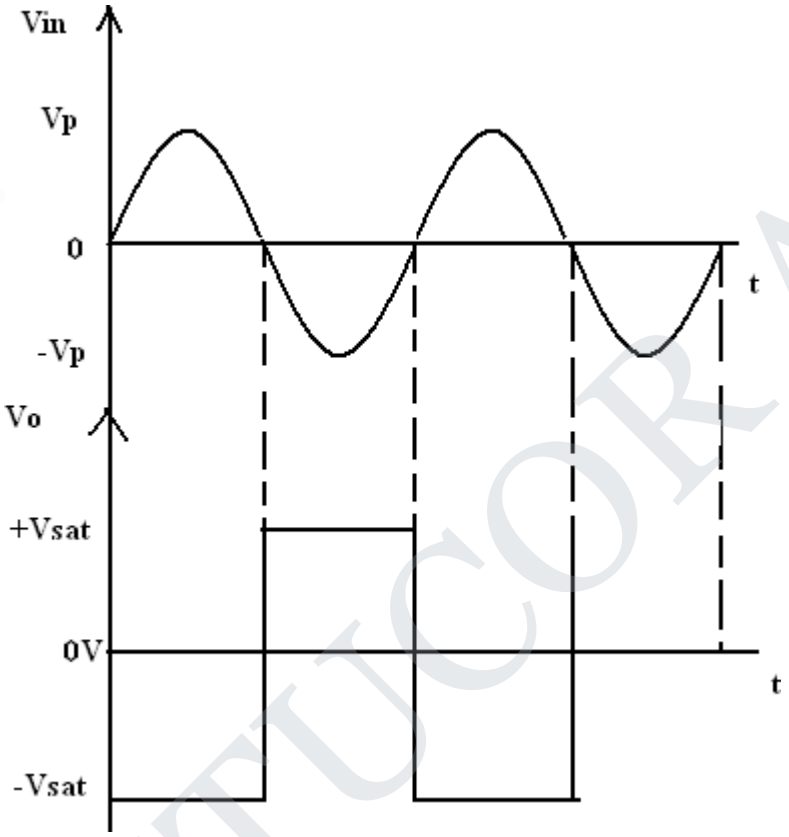


3. Zero Crossing Detector: [Sine wave to Square wave converter]



One of the application of comparator is the zero crossing detector or -sine wave to Square wave Converter‖. The basic comparator can be used as a zero crossing detector by setting Vref is set to Zero. (Vref =0V).

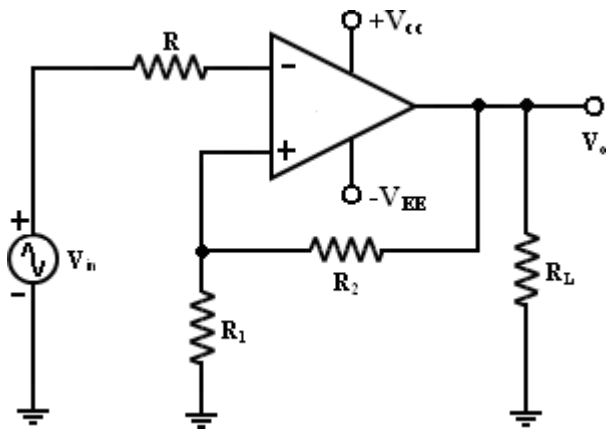
This Fig shows when in what direction an input signal Vin crosses zero volts. (i.e) the o/p V_0 is driven into negative saturation when the input the signal Vin passes through zero in positive direction. Similarly, when Vin passes through Zero in negative direction the output V_0 switches and saturates positively.

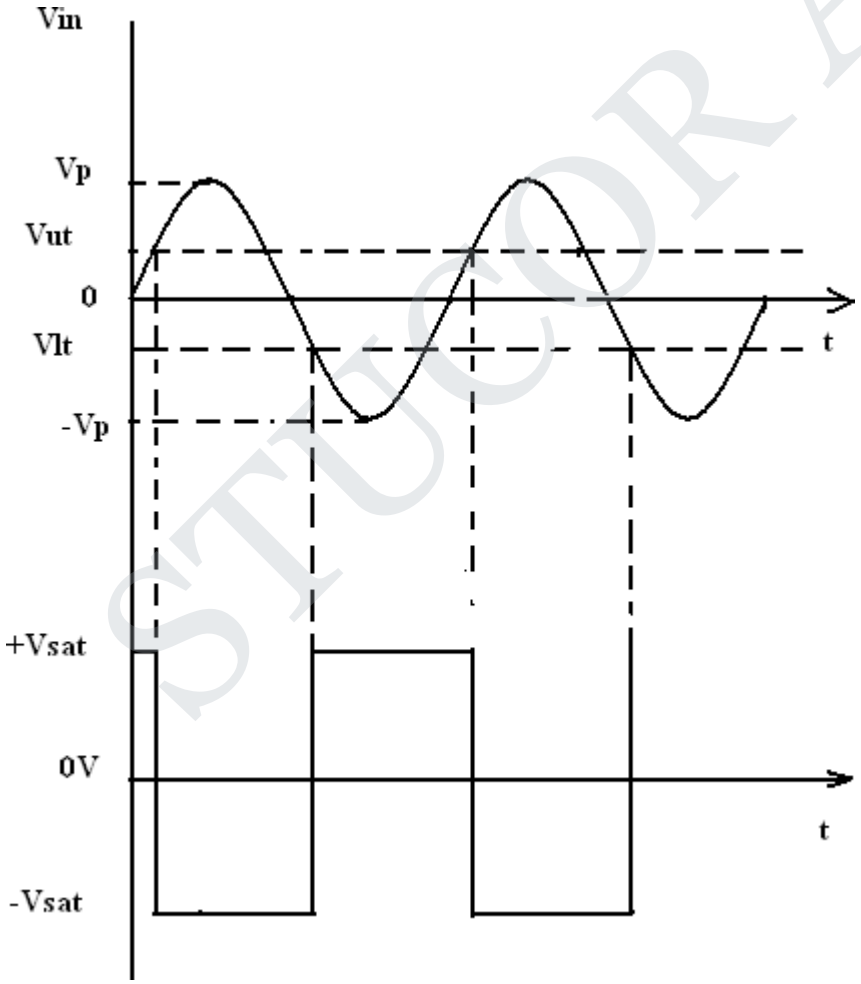


Drawbacks of Zero- crossing detector:

In some applications, the input Vin may be a slowly changing waveform, (i.e) a low frequency signal. It will take Vin more time to cross 0V, therefore V_0 may not switch quickly from one saturation voltage to the other. Because of the noise at the op-amp‘s input terminals the output V_0 may fluctuate between 2 saturations voltages +Vsat and –Vsat. Both of these problems can be cured with the use of regenerative or positive feedback that cause the output V_0 to change faster and eliminate any false output transitions due to noise signals at the input. Inverting comparator with positive feedback . This is known as —Schmitt Trigger‖.

Schmitt Trigger: [Square Circuit]





This circuit converts an irregular shaped waveform to a square wave or pulse. The

circuit is known as Schmitt Trigger or squaring circuit. The input voltage Vin triggers (changes the state of) the o/p V_0 every time it exceeds certain voltage levels called the upper threshold Vut and lower threshold voltage. These threshold voltages are obtained by using theh voltage divider R_1 – R_2, where the voltage across R_1 is feedback to the (+) input. The voltage across R_1 is variable reference threshold voltage that depends on the value of the output voltage. When V_0 = +Vsat, the voltage across R_1 is called -upper threshold‖ voltage Vut. The input voltage Vin must be more positive than Vut in order to cause the output V_0 to switch from +Vsat to –Vsat. As long as Vin < Vut , V_0 is at +Vsat, using voltage divider rule,

Similarly, when V_0 = -Vsat, the voltage across R_1 is called lower threshold voltage V_{lt} . the vin must be more negative than V_{lt} in order to cause V_0 to switch from –Vsat to +Vsat. In other words, for Vin > V_{lt} , V_0 is at –Vsat. V_{lt} is given by the following eqn.

Thus, if the threshold voltages Vut and Vlt are made larger than the input noise voltages, the positive feedback will eliminate the false o/p transitions. Also the positive feedback, because of its regenerative action, will make V_0 switch faster between +Vsat and –Vsat. Resistance Rcomp t $R_1 \parallel R_2$ is used to minimize the offset problems. The comparator with positive feedback is said to exhibit hysteresis, a dead band condition. (i.e) when the input of the comparator exceeds Vut its output switches from +Vsat to –Vsat and reverts to its original state, +Vsat when the input goes below Vlt. The hysteresis voltage is equal to the difference between Vut and Vlt. Therefore

$V_{ref} = V_{ut} - V_{lt}$

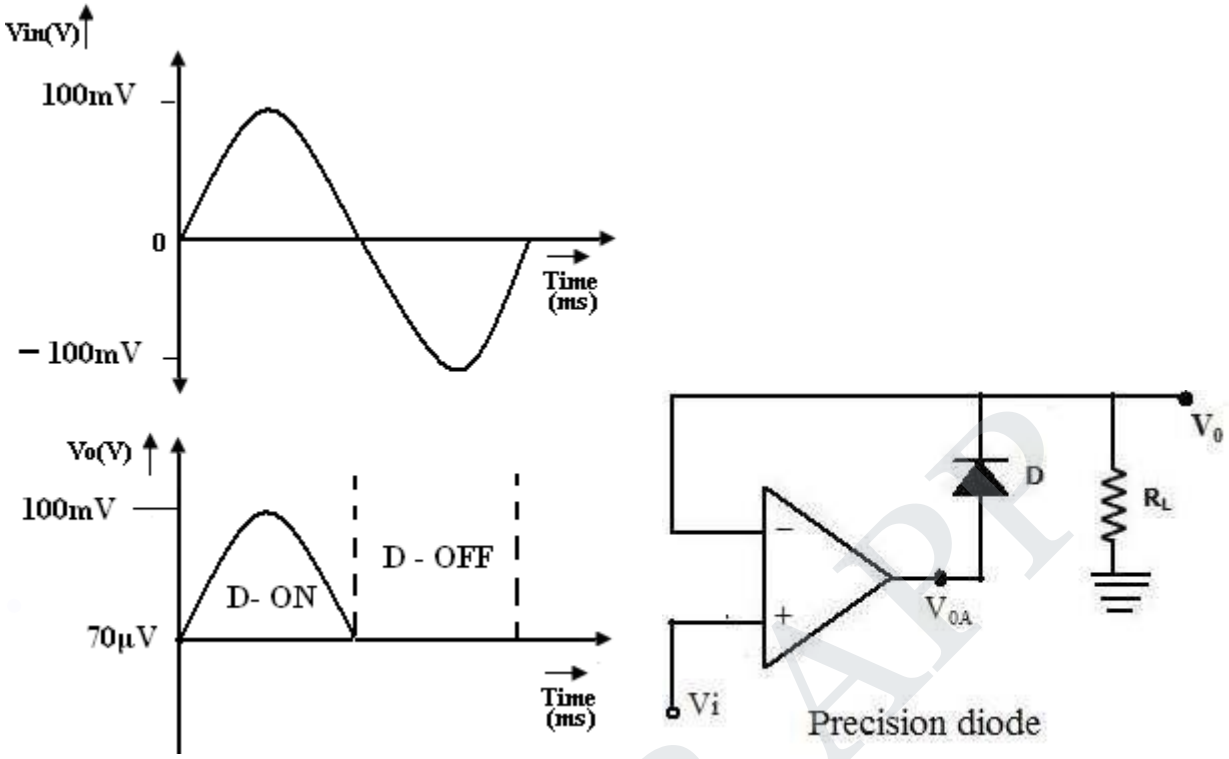
$$V_{ref} = \frac{R_1}{R_1 + R_2} [+V_{sat} - (-V_{sat})]$$

Precision Rectifier:

The signal processing applications with very low voltage, current and power levels require rectifier circuits. The ordinary diodes cannot rectify voltages below the cut-in-voltage of the diode. A circuit which can act as an ideal diode or precision signal – processing rectifier circuit for rectifying voltages which are below the level of cut-in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp.

Precision diodes:

Figure shows the arrangement of a precision diode. It is a single diode arrangement and functions as a non-inverting precision half – wave rectifier circuit. If V_1 in the circuit of figure is positive, the op-amp output V_{OA} also becomes positive. Then the closed loop condition is achieved for the op-amp and the output voltage $V_0 = V_i$. when $V_i < 0$, the voltage V_{0A} becomes negative and the diode is reverse biased. The loop is then broken and the output $V_0 = 0$.



Input and Output Waveform

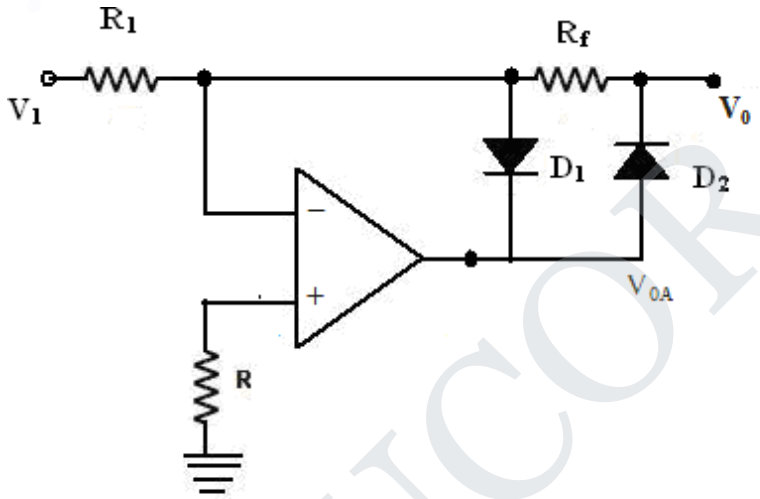
Consider the open loop gain A_{OL} of the op-amp is approximately 10^4 and the cut-in voltage V_γ for silicon diode is ≈ 0.7V. When the input voltage $V_i > V_\gamma / A_{OL}$, the output of the op-amp V_{OA} exceeds V_γ and the diode D conducts. Then the circuit acts like a voltage follower for input voltage level $V_i > V_\gamma / A_{OL}$,(i.e. when $V_i > 0.7/10^4 = 70\mu V$), and the output voltage V_0 follows the input voltage during the positive half cycle for input voltages higher than 70µV as shown in figure. When V_i is negative or less than V_γ / A_{OL} , the output of op-amp V_{OA} becomes negative, and the diode becomes reverse biased. The loop is then broken, and the op-amp swings down to negative saturation. However, the output terminal is now isolated from both the input signal and the output of the op-amp terminal thus $V_0 = 0$. No current is then delivered to the load R_L except for the small bias current of the op-amp and the reverse saturation current of the diode.

This circuit is an example of a non-linear circuit, in which linear operation is achieved over the remaining region ($V_i < 0$). Since the output swings to negative saturation level when $V_i < 0$, the circuit is basically of saturating form. Thus the frequency response is also limited. The precision diodes are used in half wave rectifier, Full-wave rectifier, peak value detector, clipper and clamper circuits.

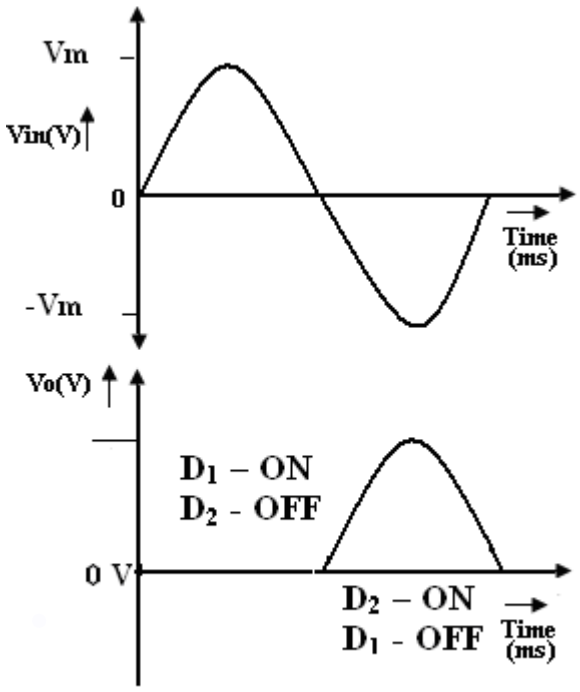
It can be observed that the precision diode as shown in figure operated in the first quadrant with $V_i > 0$ and $V_0 > 0$. The operation in third quadrant can be achieved by connecting the diode in reverse direction.

Half – wave Rectifier:

A non-saturating half wave precision rectifier circuit is shown in figure. When $V_i > 0V$, the voltage at the inverting input becomes positive, forcing the output V_{OA} to go negative. This results in forward biasing the diode D_1 and the op-amp output drops only by ≈ 0.7V below the inverting input voltage. Diode D_2 becomes reverse biased. The output voltage V_0 is zero when the input is positive. When $V_i > 0$, the op-amp output V_{OA} becomes positive, forward biasing the diode D_2 and reverse biasing the diode D_1 . The circuit then acts like an inverting amplifier circuit with a non-linear diode in the forward path. The gain of the circuit is unity when $R_f = R_i$.



Non - Saturating half - wave precision rectifier circuit



Input and Output Waveforms

The circuit operation can mathematically be expressed as

$V_0 = 0 \text{ when } V_i > 0$

and

$V_0 = -\frac{R}{R_i} V_i \text{ for } V_i < 0$

The voltage V_{OA} *at the op @amp output is*

$V_{OA} = -0.7 \text{ for } V_i > 0V$

and

$V_{OA} = V_i + 0.7V \text{ for } V < 0V$

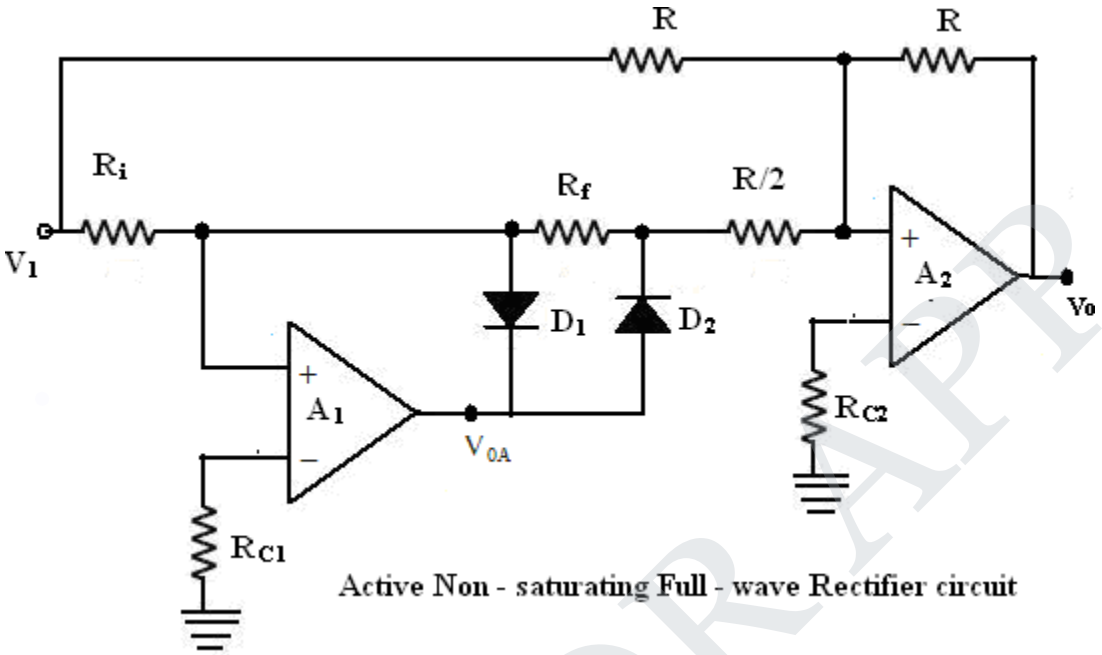
The input and output waveforms are shown in figure. The op-amp shown in the circuit must be a high speed op-amp. This accommodates the abrupt changes in the value of V_{OA} when V_i changes sign and improves the frequency response characteristics of the circuit.

The advantages of half wave rectifier are it is a precision half wave rectifier and it is a non saturating one.

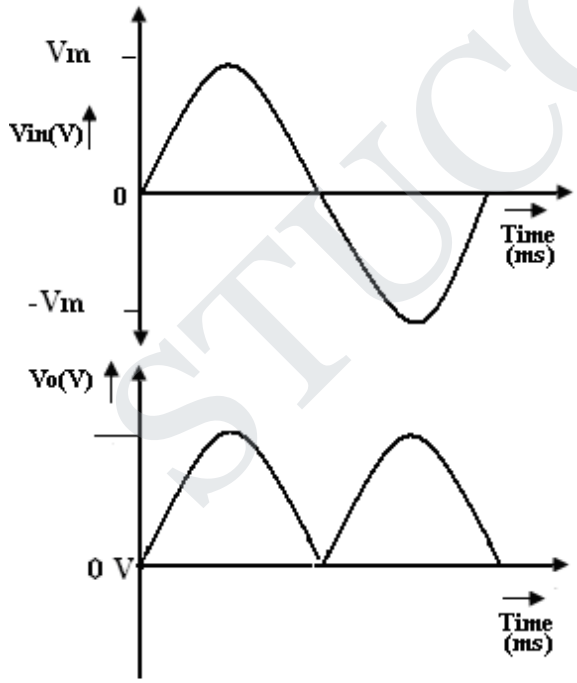
The inverting characteristics of the output V_0 can be circumvented by the use of an additional inversion for achieving a positive output.

Full wave Rectifier:

The Full wave Rectifier circuit commonly used an absolute value circuit is shown in figure. The first part of the total circuit is a half wave rectifier circuit considered earlier in figure. The second part of the circuit is an inverting.



Active Non - saturating Full - wave Rectifier circuit



Input and Output Waveforms

For positive input voltage $V_i > 0V$ and assuming that $R_F = R_i = R$, the output voltage $V_{OA} = V_i$. The voltage V_0 appears as (-) input to the summing op-amp circuit formed by A_2 , The gain for the input V'_0 is R/(R/2), as shown in figure. The input V_i also appears as an input to the summing amplifier. Then, the net output is $V_0 = -V_i - 2V'_0$

$$= -V_i - 2(-V_i) = V_i$$

Since $V_i > 0V$, V'_0 will be positive, with its input output characteristics in first quadrant. For negative input $V_i < 0V$, the output V'_0 of the first part of rectifier circuit is zero. Thus, one input of the summing circuit has a value of zero. However, V_i is also applied as an input to the summer circuit formed by the op-amp A_2 . The gain for this input id (-R/R) = -1, and hence the output is $V_0 = -V_i$. Since V_i is negative, v_0 will be inverted and will thus be positive. This corresponds to the second quadrant of the circuit.

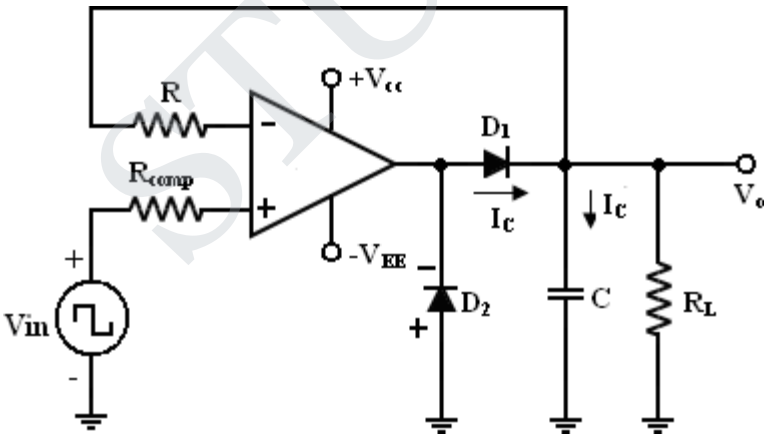
To summarize the operation of the circuit,

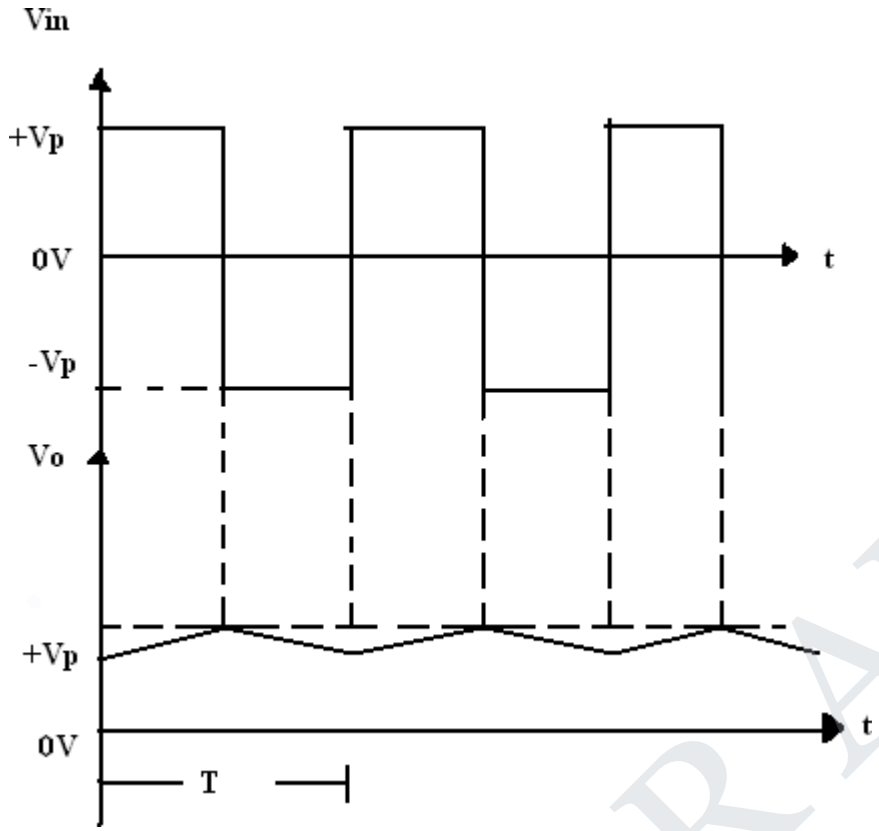
$V_0 = V_i$ when $V_i < 0V$ and $V_0 = V_i$ for $V_i > 0V$, and hence $V_0 = |V_i|$

It can be observed that this circuit is of non-saturating form. The input and output waveforms are shown in the figure.

Peak detector:

Square, Triangular, Sawtooth and pulse waves are typical examples of non-sinusoidal waveforms. A conventional ac voltmeter cannot be used to measure these sinusoidal waveforms because it is designed to measure the rms value of the pure sine wave. One possible solution to this problem is to measure the peak values of the non-sinusoidal waveforms. Peak detector measures the +ve peak value of the square wave input.





i) During the positive half cycle of Vin:

the o/p of the op-amp drives D_1 on. (Forward biased)

Charging capacitor C to the positive peak value V_p of the input volt Vin.

ii) During the negative half cycle of Vin:

D_1 is reverse biased and voltage across C is retained. The only discharge path for C is through $R_{L.}$ since the input bias I_B is negligible.

For proper operation of the circuit, the charging time constant (CR_d) and discharging time constant (CR_L) must satisfy the following condition.

$CR_d <= T/10$ ----------(1)

Where R_d = Resistance of the forward-biased diode.

T = time period of the input waveform.

$CR_L >= 10T$ ----------(2)

Where R_L = load resistor. If R_L is very small so that eqn (2) cannot be satisfied. Use a (buffer) voltage follower circuit between capacitor C and R_L load resistor.

R = is used to protect the op-amp against the excessive discharge currents.

Rcomp = minimizes the offset problems caused by input current

D_2 = conducts during the –ve half cycle of Vin and prevents the op-amp from going into negative saturation.

Note: -ve peak of the input signal can be detected simply by reversing diode D_1 and D_2 .

Clippers and Clampers:

Waveshaping circuits are commonly used in digital computers and communication such as TV and FM receiver. Waveshaping technique include clipping and clamping. In op-amp clipper circuits a rectifier diode may be used to clip off a certain portion of the input signal to obtain a desired o/p waveform. The diode works as an ideal diode (switch) because when on -> the voltage drop across the diode is divided by the open loop gain of the op-amp. When off(reverse biased) -> the diode is an open circuit.

In an op-amp clamper circuits, however a predetermined dc level is deliberately inserted in the o/p volt. For this reason, the clamper is sometimes called a dc inverter.

Positive and Negative Clipper:

Positive Clipper:

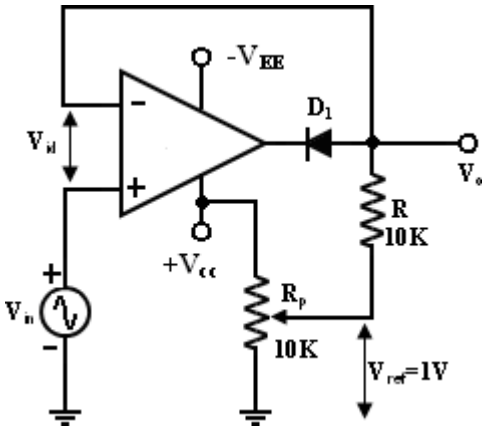
A Circuit that removes positive parts of the input signal can be formed by using an op-amp with a rectifier diode. The clipping level is determined by the reference voltage Vref, which should less than the i/p range of the op-amp (Vref < Vin). The Output voltage has the portions of the positive half cycles above Vref clipped off.

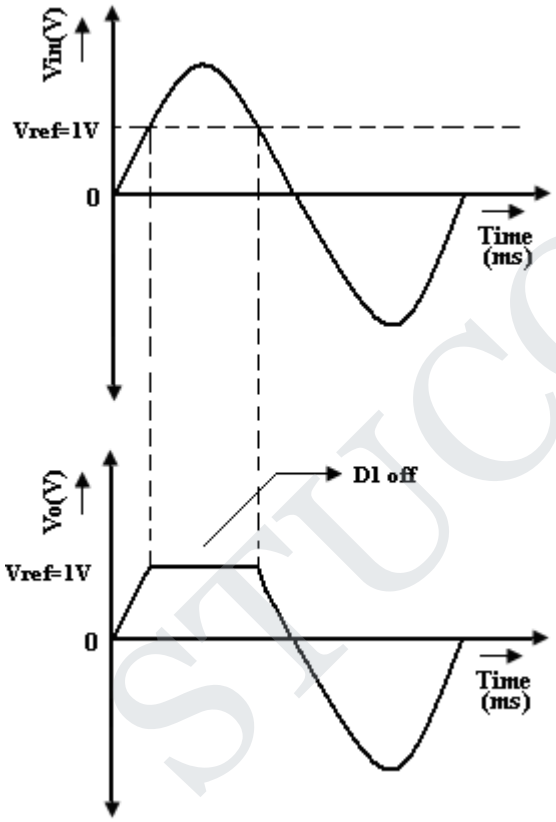
The circuit works as follows:

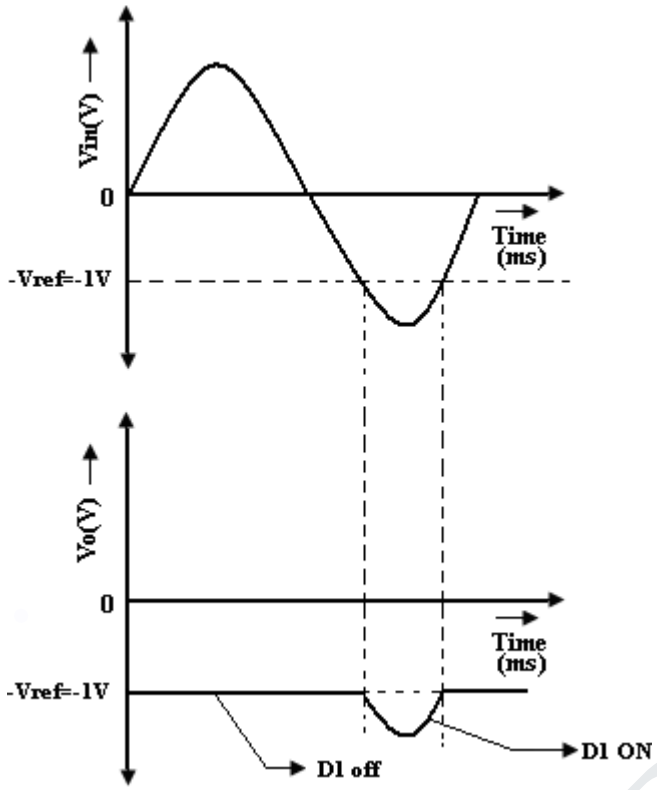
During the positive half cycle of the input, the diode D_1 conducts only until Vin = Vref. This happens because when Vin <Vref, the output volts V_0 _ of the op-amp becomes negative to device D_1 into conduction when D_1 coonducts it closes feedback loop and op-amp operates as a voltage follower. (i.e) Output V_0 follows input until Vin = Vref.

When Vin > Vref => the V'_0 becomes +ve to derive D_1 into off. It open the feedback loop and op-amp operates open loop. When Vin drops below Vref (Vin<Vref) the o/p of the op-amp V'_0 again becomes –ve to device D_1 into conduction. It closed the f/b. (o/p follows the i/p). Thus diode D_1 is

on for vin<Vref (o/p follows the i/p) and D_1 is off for Vin>Vref. The op-amp alternates between open loop (off) and closed loop operation as the D_1 is turned off and on respectively. For this reason the op-amp used must be high speed and preferably compensated for unity gain.

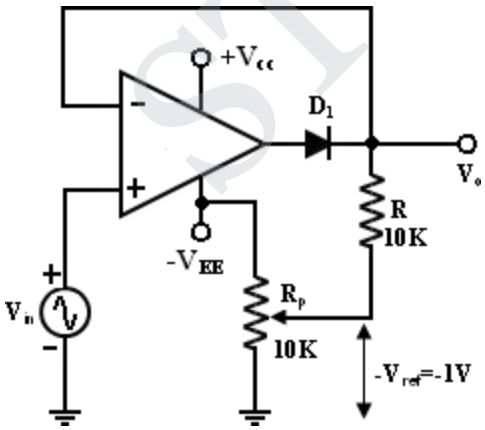


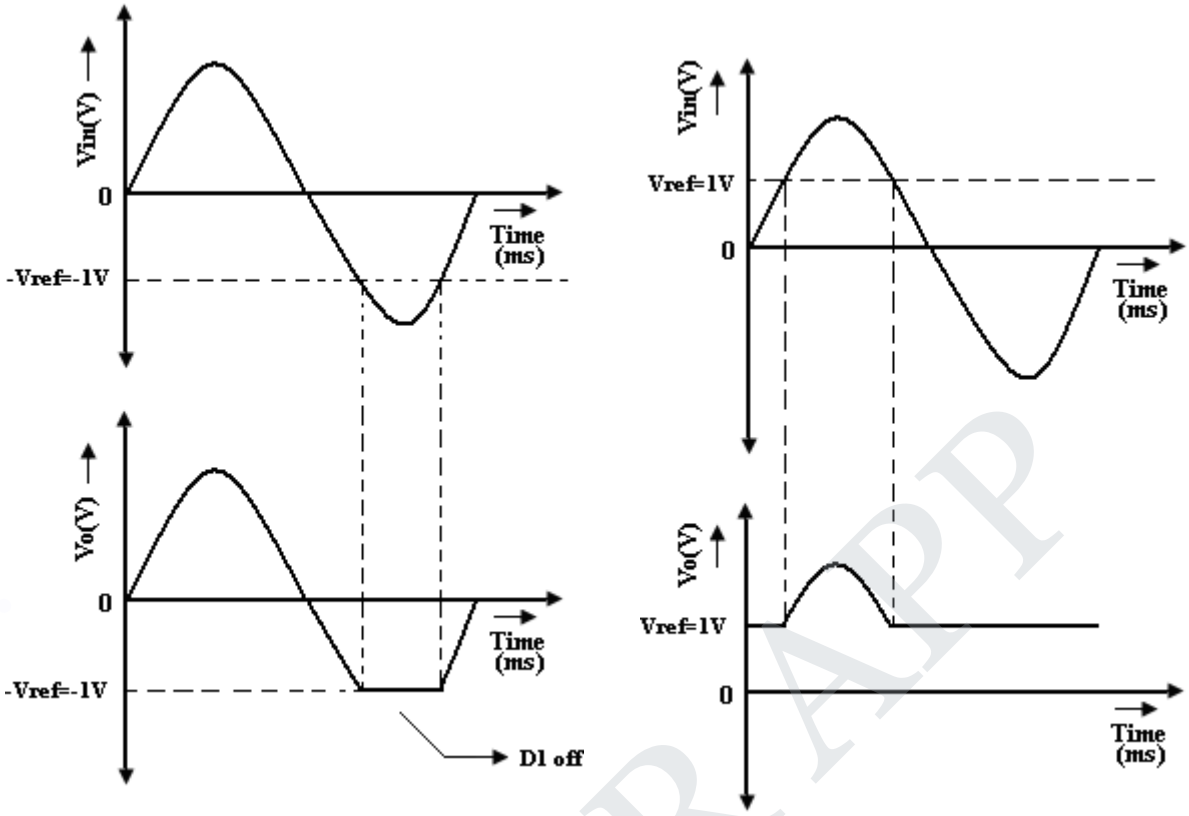




Ex: for high speed op-amp HA 2500, LM310, µA 318. In addition the difference input voltage (Vid=high) is high during the time when the feedback loop is open (D_1 is off) hence an op-amp with a high difference input voltage is necessary to prevent input breakdown. If R_p (pot) is connected to $-V_{EE}$ instead of +Vcc, the ref voltage Vref will be negative (Vref = -ve). This will cause the entire o/p waveform above –Vref to be clipped off.

Negative Clipper:





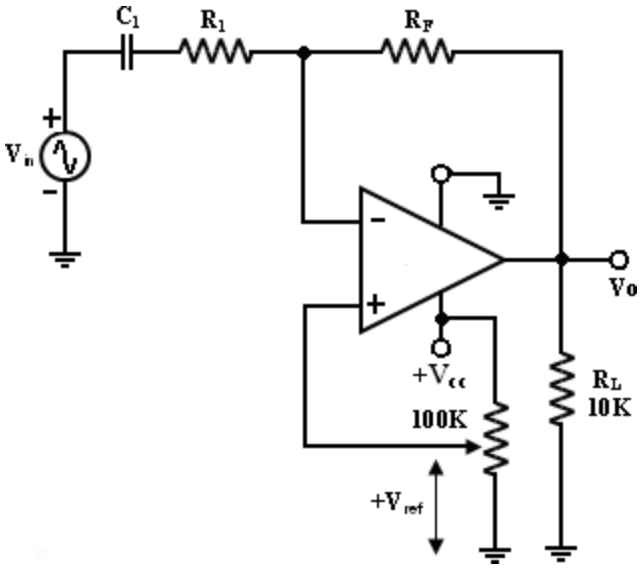
The positive clipper is converted into a –ve clipper by simply reversing diode D_1 and changing the polarity of Vref voltage. The negative clipper -> clips off the –ve parts of the input signal below the reference voltage. Diode D_1 conducts -> when Vin > -Vref and therefore during this period o/p volt V_0 follows the i/p volt Vin. The –Ve portion of the output volt below –Vref is clipped off because (D_1 is off) Vin<-Vref. If –Vref is changed to –Vref by connecting the potentiometer R_p to the +Vcc, the V_0 below +Vref will be clipped off. The diode D_1 must be on for Vin > Vref and off for Vin.

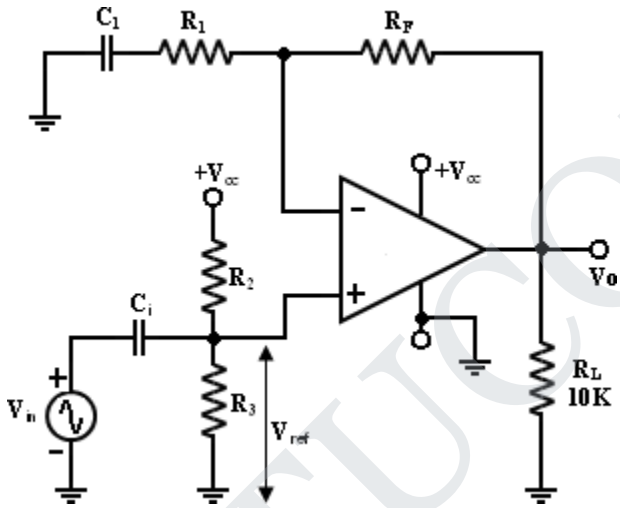
Positive and Negative Clampers:

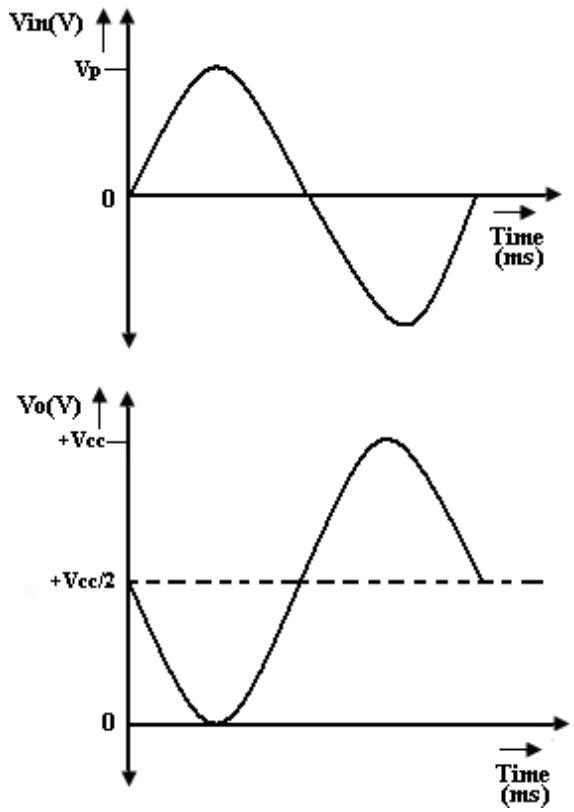
In clamper circuits a predetermined dc level is added to the output voltage. (or) The output is clamped to a desired dc level.

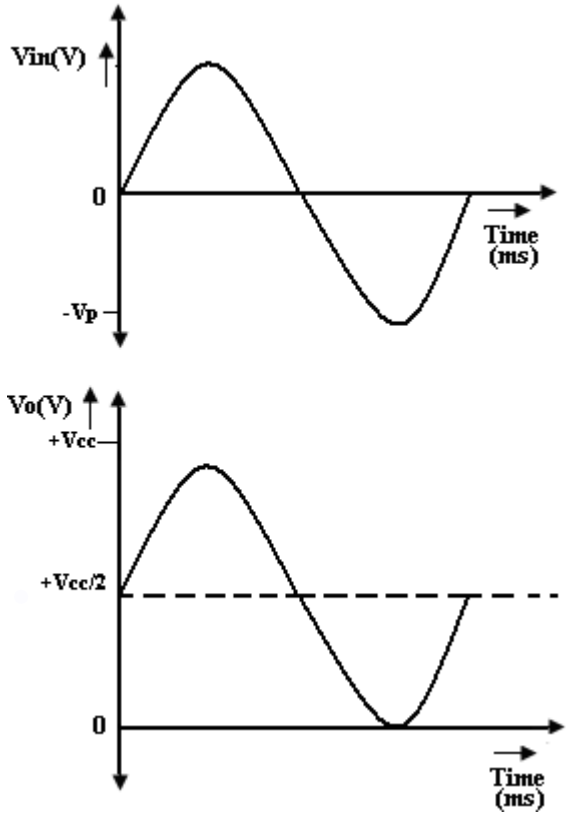
1. If the clamped dc level is +ve, the clamper is positive clamper
2. If the clamped dc level is –ve, the clamper is negative clamper.

Other equivalent terms used for clamper are dc inserter or restorer. Inverting and Non-Inverting that use this technique.









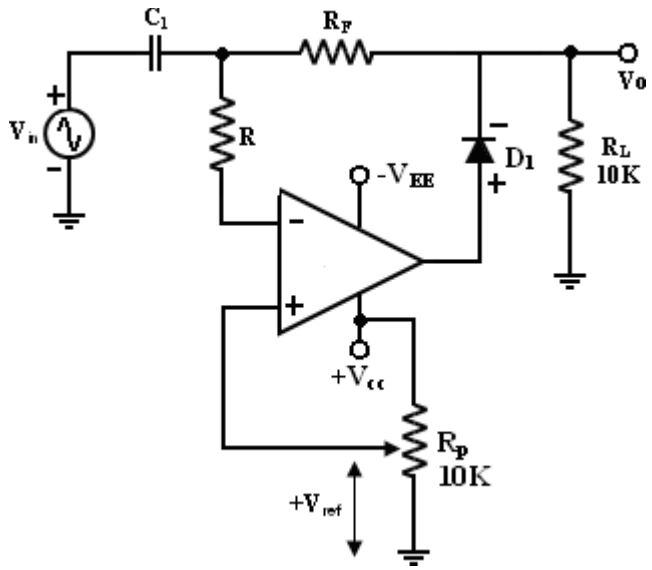
Capacitor:

The Value of the capacitors in these circuits depends on different input rates and pulse widths.

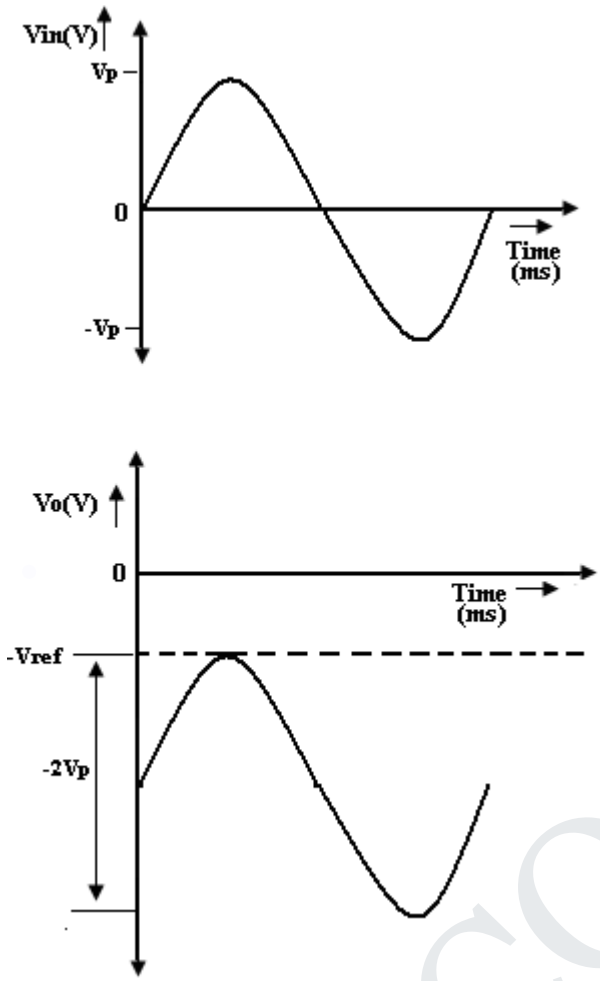
1. In both circuits the dc level added to the o/p voltage is approximately equal to Vcc/2.
2. This +ve fixed dc level is needed to obtain a maximum undistored symmetrical sine wave.

Peak clamper circuit:

Input and output waveform with +Vref:



Input and Output Waveform with –Vref:



In this circuit, the input waveform peak is clamped at Vref. For this reason, the circuit is called the peak clamper.

First consider the input voltage Vref at the (+) input: since this volt is +ve, V'_0 is also +ve which forward biases D_1 . This closed the feedback loop.

Voltage Vin at the (-) input: During its –ve half cycle, diode D_1 conducts, charging c; to the –ve peak value of V_p . During the +ve half cycle, diode D_1 in reverse biased. Since this voltage V_p is in series with the +ve peak volt V_p the o/p volt $V_0 = 2\ V_p$. Thus the nett o/p is Vref plus 2 V_p. so the –ve peak of 2 V_p is at Vref. For precision clamping, $C_iR_d << T/2$

Where R_d = resistance of diode D_1 when it is forward biased.

T = time period of the input waveform.

Resistor r => is used to protect the op-amp against excessive discharge currents from capacitor C_i especially when the dc supply voltages are switched off. A +ve peak clamping is accomplished by reversing D_1 and using –ve reference voltage (-Vref).

Note:

Inv and Non-Inv clamper – Fixed dc level

Peak clamper – Variable dc level

Active filters:

Another important field of application using op-amp.

Filters and Oscillators:

An electric filter is often a frequency selective circuit that passes a specified band of frequencies and blocks or alternates signal and frequencies outside this band.

Filters may be classified as

1. Analog or digital.
2. Active or passive
3. Audio (AF) or Radio Frequency (RF)

1. Analog or digital filters:

Analog filters are designed to process analog signals, while digital filters process analog signals using digital technique.

2. Active or Passive:

Depending on the type of elements used in their construction, filter may be classified as passive or Active elements used in passive filters are Resistors, capacitors, inductors. Elements used in active filters are transistor, or op-amp.

Active filters offers the following advantages over a passive filters:

1. Gain and Frequency adjustment flexibility:

Since the op-amp is capable of providing a gain, the i/p signal is not attenuated as it is in a passive filter. [Active filter is easier to tune or adjust].

2. No loading problem:

Because of the high input resistance and low o/p resistance of the op-amp, the active filter does not cause loading of the source or load.

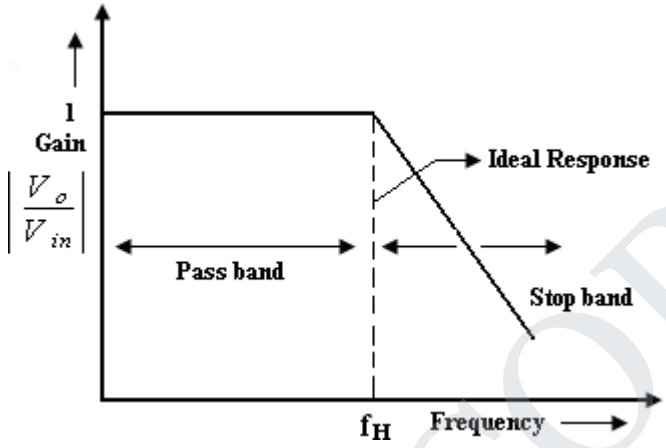
3. Cost:

Active filters are more economical than passive filter. This is because of the variety of cheaper op-amps and the absence of inductors.

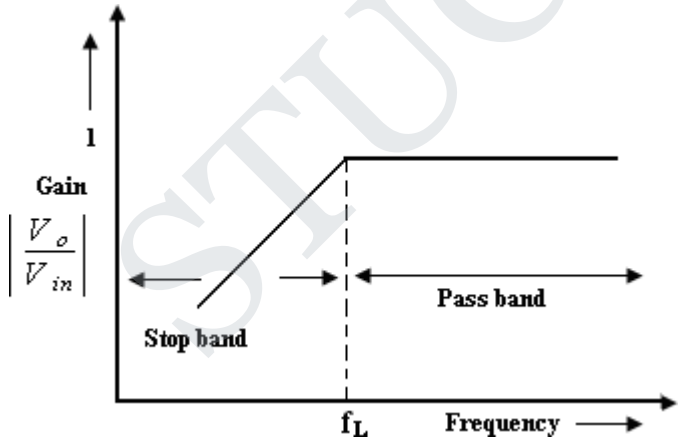
The most commonly used filters are these:

1. Low pass Filters
2. High pass Filters
3. Band pass filters
4. Band –reject filters
5. All pass filters.

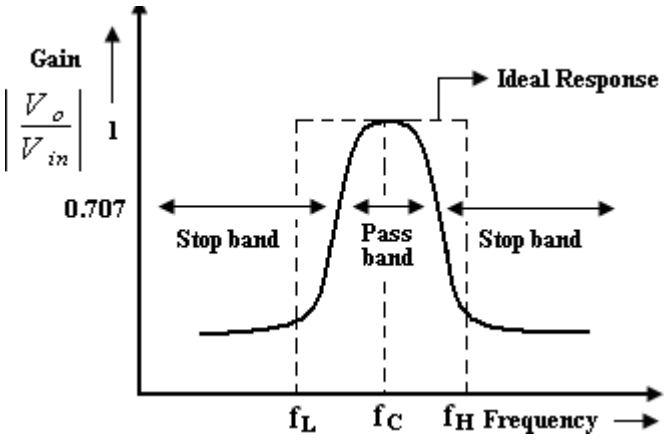
Frequency response of the active filters:



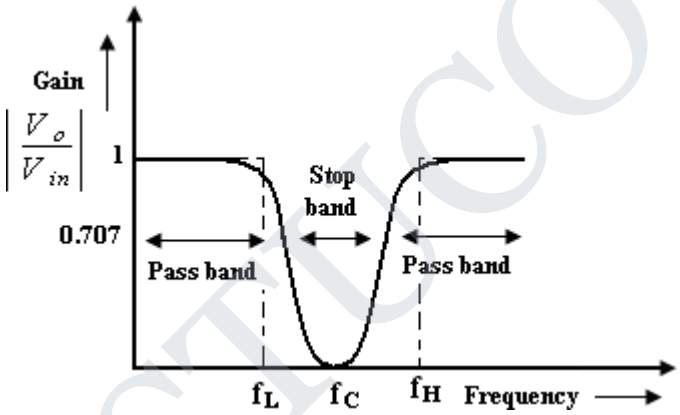
Low pass Filter



High pass Filter



Band Pass Filters



Band Reject

Low pass filters:

1. It has a constant gain from 0 Hz to a high cutoff frequency f_1.
2. At f_H the gain in down by 3db.

3. The frequency between 0hz and f_H are known as the passband frequencies. Where as the range of frequencies those beyond f_H, that are attenuated includes the stopband frequencies.
4. Butterworth, clebyshev and cauer filter are some of the most commonly used practical filters.
5. The key characteristics of the butter worth filter is that it has a flat pass band as well as stop band. For this reason, it is sometimes called a flat-flat filters.
6. Chebyshev filter -> has a ripple pass band & flat stop band.
7. Causer Filter -> has a ripple pass band & ripple stopband. It gives best stopband response among the three.

High pass filter:

High pass filter with a stop band $0<f< f_L$ and a pass band $f> f_L$

f_L -> low cut off frequency

f -> operating frequency.

Band pass filter:

It has a pass band between 2 cut off frequencies f_H and f_L where $f_H > f_L$ and two, stop bands : $0<f< f_L$ and $f > f_H$ between the band pass filter (equal to $f_H - f_L$.

Band –reject filter: (Band stop or Band elimination)

It performs exactly opposite to the band pass. It has a band stop between 2 cut-off frequency f_L and f_H and 2 passbands: $0<f< f_L$ and $f> f_H$

f_C -> center frequency.

Note:

The actual response curves of the filters in the stopband either R or S or both with R in frequencies.

The rate at which the gain of the filter changes in the stopband is determined by the order of the filter.

Ex: 1st order low pass filter the gain rolls off at the rate of 20dB/decade in the stopband. (i.e) for $f > f_H$.

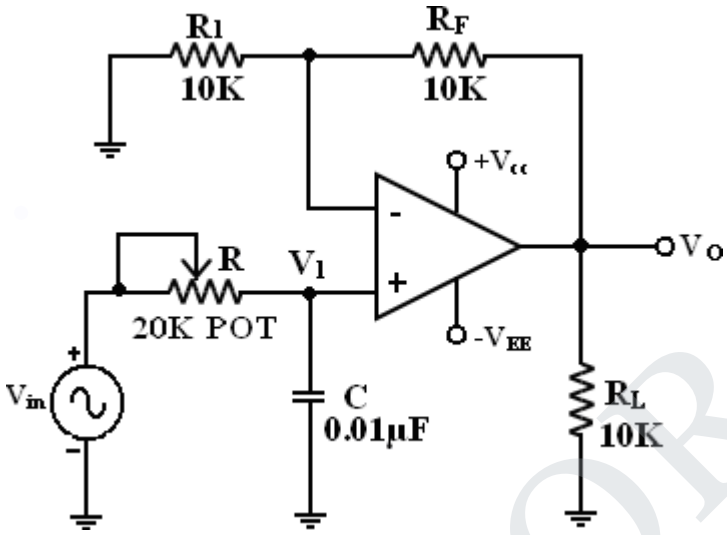
2nd order LPF -> the gain roll off rate is 40dB/decade.

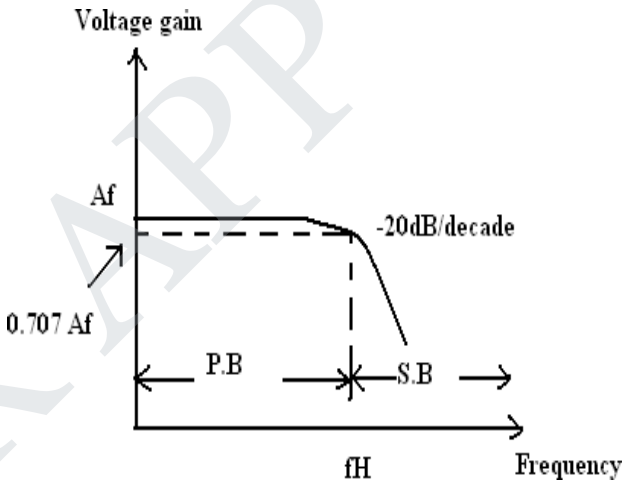
1st order HPF -> the gain Rs at the rate of 20dB (i.e) until f:f_L

2nd order HPF -> the gain Rs at the rate of 40dB/decade

First order LPF Butterworth filter:

First order LPF that uses an RC for filtering op-amp is used in the non inverting configuration. Resistor R1 & R_f determine the gain of the filter. According to the voltage –divider rule, the voltage at the non-inverting terminal (across capacitor) C is,

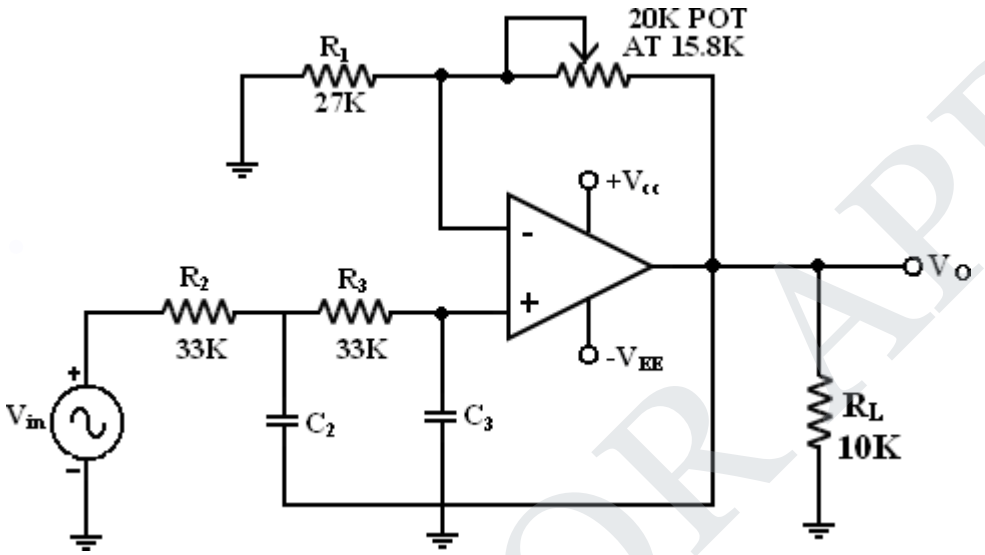


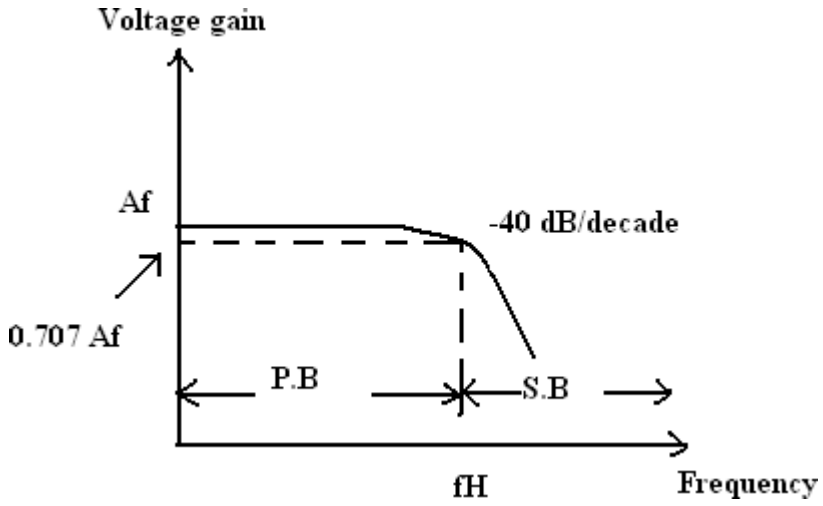


Second order LP Butterworth filter:

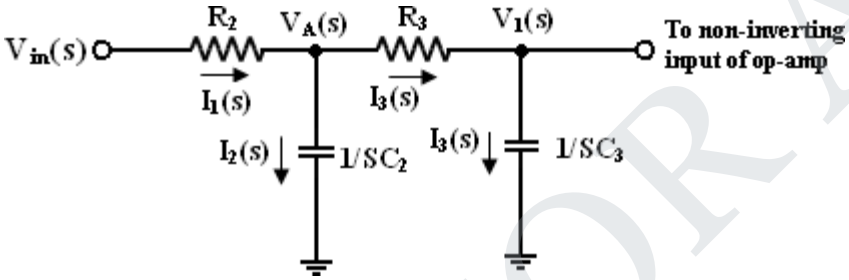
A second order LPF having a gain 40dB/decade in stop band. A First order LPF can be converted into a II order type simply by using an additional RC network.

The gain of the II order filter is set by R1 and R_F, while the high cut off frequency f_H is determined by R2,C2,R3 and C3.





This above fig transferred into S domain.



In this circuit all the components and the circuit parameters are expressed in the S-domain where S = j .

Writing Kirchoff's current law at node V_A (S) .

$$I_1 = I_2 + I_3$$

and solving for V_1 *, we get,*

The denominator quadratic in the gain (V_0/Vin) eqn must have two real and equal roots. This means that

Filter Design:

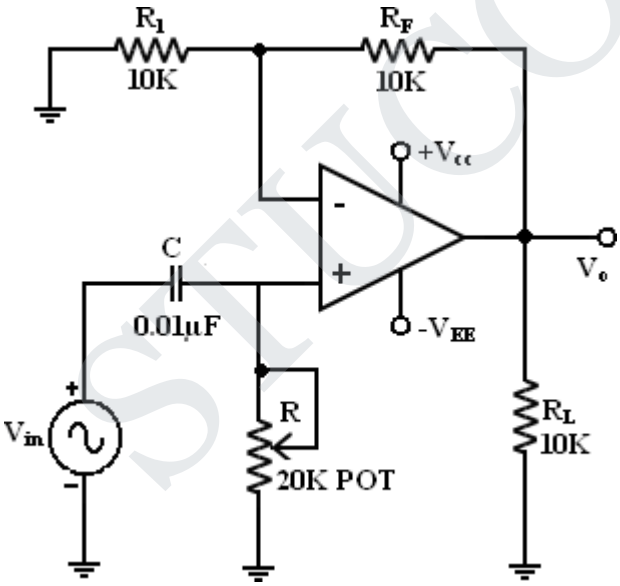
1. Choose a value for a high cut off freq (f_H).
2. To simplify the design calculations, set $R_2 = R_3 = R$ and $C_2 = C_3 = C$ then choose a value of c<=1µf.
4. Finally, because of the equal resistor ($R_2 = R_3$) and capacitor ($C_2 = C_3$) values, the pass band volt gain $A_F = 1 + R_F / R_1$ of the second order had to be = to 1.586. $R_F = 0.586\ R_1$. Hence choose a value of R_1 <=100kΩ and
5. Calculate the value of R_F.

First order HP Butterworth filter:

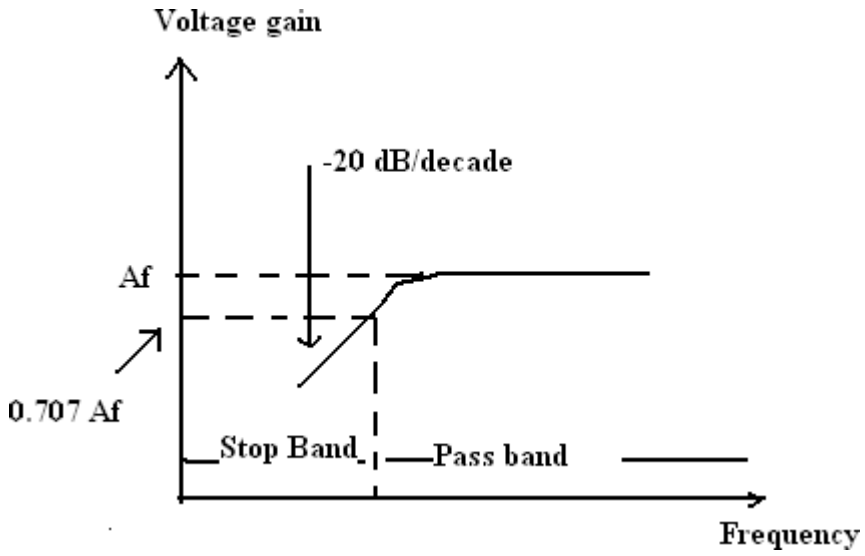
High pass filters are often formed simply by interchanging frequency-determining resistors and capacitors in low-pass filters.

(i.e) I order HPF is formed from a I order LPF by interchanging components R & C.

Similarly II order HPF is formed from a II order LPF by interchanging R & C.



I order HPF

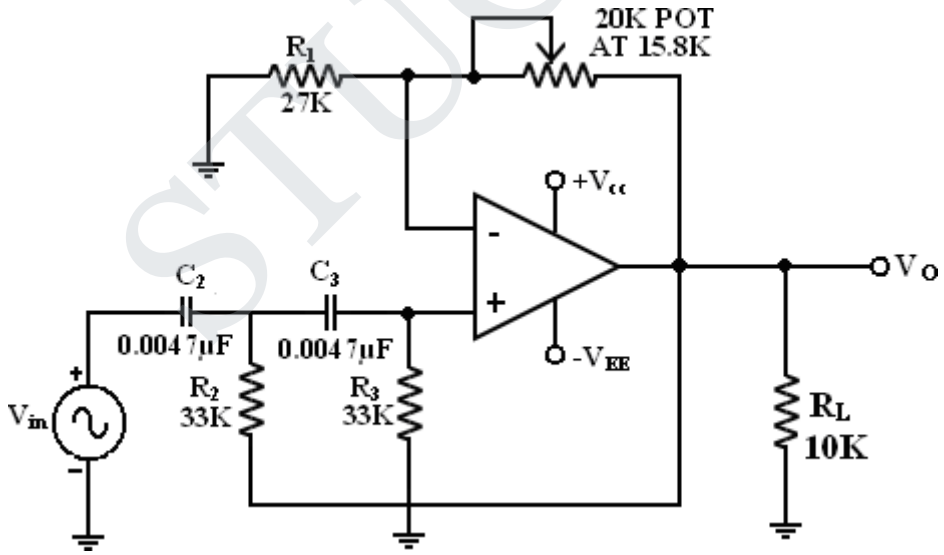


Here I order HPF with a low cut off frequency of f_L. This is the frequency at which the magnitude of the gain is 0.707 times its passband value.

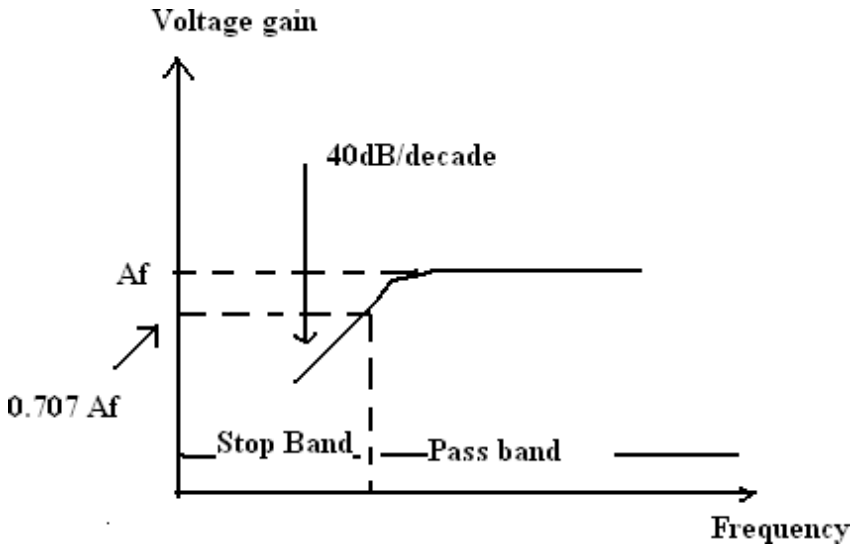
Here all the frequencies higher than f_L are passband frequencies.

Second – order High Pass Butterworth Filter:

I order Filter, II order HPF can be formed from a II order LPF by interchanging the frequency – determine resistors and capacitors.



II order HPF



ANALOG TO DIGITAL & DIGITAL TO ANALOG CONVERTERS

D TO A CONVERTER- SPECIFICATIONS

D/A converters are available with wide range of specifications specified by manufacturer. Some of the important specifications are Resolution, Accuracy, linearity, monotonicity, conversion time, settling time and stability.

Resolution:

Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

Resolution (Volts) = $Vo_{FS} / (2^n - 1)$ = 1 LSB increment

Where _n' is the number of input bits

_Vo_{FS}' is the full scale output voltage.

Example:

Resolution for an 8 – bit DAC for example is said to have

: 8 – bit resolution

: A resolution of 0.392 of full-Scale (1/255)

: A resolution of 1 part in 255.

Thus resolution can be defined in many different ways.

The following table shows the resolution for 6 to 16 bit DACs

S.No.	Bits	Intervals	LSB size (% of full-scale)	LSB size (For a 10 V full-scale)
1.	6	63	1.588	158.8 mV
2.	8	255	0.392	39.2 mV
3.	10	1023	0.0978	9.78 mV
4.	12	4095	0.0244	2.44 mV
5.	14	16383	0.0061	0.61 mV
6.	16	65535	0.0015	0.15 mV

Accuracy:

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. The ideal converter is the one which does not suffer from any problem. Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

The relative accuracy is the maximum deviation after the gain and offset errors have been removed. Accuracy is also given in terms of LSB increments or percentage of full-scale voltage. Normally, the data sheet of a D/A converter specifies the relative accuracy rather than absolute accuracy.

Linearity:

Linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001% of full scale. The linearity of a D/A converter is defined as the precision or exactness with which the digital input is converted into analog output. An ideal D/A converter produces equal increments or step sizes at output for every change in equal increments of binary input.

Monotonicity:

A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristics is essential in control applications. Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition.

When a D/A Converter doesn‘t satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input.

Conversion Time:

It is the time taken for the D/A converter to produce the analog output for the given binary input signal. It depends on the response time of switches and the output of the
Amplifier. D/A converters speed can be defined by this parameter. It is also called as setting time.

Settling time:

It is one of the important dynamic parameter. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (Usually a full-scale change). It depends on the switching time of the logic circuitry due to internal parasitic capacitances and inductances. A typical settling time ranges from 100 ns to 10 μs depending on the word length and type of circuit used.

Stability:

The ability of a DAC to produce a stable output all the time is called as Stability. The performance of a converter changes with drift in temperature, aging and power supply variations. So all the parameters such as offset, gain, linearity error & monotonicity may change from the values specified in the datasheet. Temperature sensitivity defines the stability of a D/A converter.

DIGITAL TO ANALOG CONVERSION

A DAC converts an abstract finite-precision number (usually a fixed-point binary number) into a concrete physical quantity (e.g., a voltage or a pressure). In particular, DACs are often used to convert finite-precision time series data to a continually-varying physical signal.

A typical DAC converts the abstract numbers into a concrete sequence of impulses that are then processed by a reconstruction filter using some form of interpolation to fill in data between the impulses. Other DAC methods (e.g., methods based on Delta-sigma modulation) produce a pulse-density modulated signal that can then be filtered in a similar way to produce a smoothly-varying signal.

By the Nyquist–Shannon sampling theorem, sampled data can be reconstructed perfectly provided that its bandwidth meets certain requirements (e.g., a baseband signal with bandwidth less than the Nyquist frequency). However, even with an ideal reconstruction filter, digital sampling introduces quantization that makes perfect reconstruction practically impossible. Increasing the digital resolution (i.e., increasing the number of bits used in each sample) or introducing sampling dither can reduce this error.

DACs are at the beginning of the analog signal chain, which makes them very important to system performance. The most important characteristics of these devices are:

Resolution: This is the number of possible output levels the DAC is designed to reproduce. This is usually stated as the number of bits it uses, which is the base two logarithm of the number of levels. For instance a 1 bit DAC is designed to reproduce 2 (2^1) levels while an 8 bit DAC is designed for 256 (2^8) levels. Resolution is related to the **effective number of bits**(ENOB) which is a measurement of the actual resolution attained by the DAC.

Maximum sampling frequency: This is a measurement of the maximum speed at which the DACs circuitry can operate and still produce the correct output. As stated in the Nyquist–Shannon sampling theorem, a signal must be sampled at over twice the frequency of the desired signal. For instance, to reproduce signals in all the audible spectrum, which includes frequencies of up to 20 kHz, it is necessary to use DACs that operate at over 40 kHz. The CD standard samples audio at 44.1 kHz, thus DACs of this frequency are often used. A common frequency in cheap computer sound cards is 48 kHz—many work at only this frequency, offering the use of other

sample rates only through (often poor) internal resampling.

Monotonicity: This refers to the ability of a DAC's analog output to move only in the direction that the digital input moves (i.e., if the input increases, the output doesn't dip before asserting the correct output.) This characteristic is very important for DACs used as a low frequency signal source or as a digitally programmable trim element.

THD+N: This is a measurement of the distortion and noise introduced to the signal by the DAC. It is expressed as a percentage of the total power of unwanted harmonic distortion and noise that accompany the desired signal. This is a very important DAC characteristic for dynamic and small signal DAC applications.

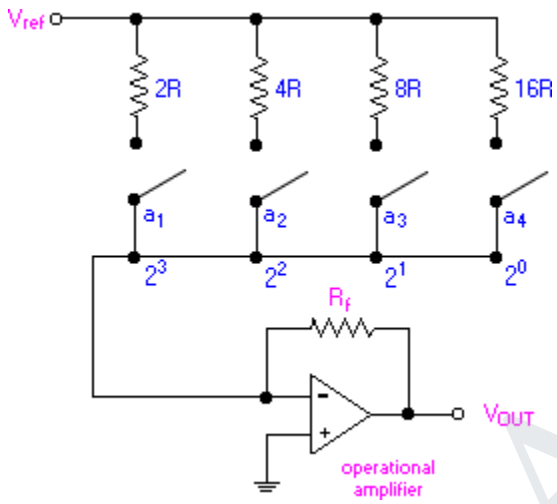
Dynamic range: This is a measurement of the difference between the largest and smallest signals the DAC can reproduce expressed in decibels. This is usually related to DAC resolution and noise floor.

Other measurements, such as phase distortion and sampling period instability, can also be very important for some applications.

BINARY-WEIGHTED RESISTOR DAC

The binary-weighted-resistor DAC employs the characteristics of the inverting summer Op Amp circuit. In this type of DAC, the output voltage is the inverted sum of all the input voltages. If the input resistor values are set to multiples of two: 1R, 2R and 4R, the output voltage would be equal to the sum of V1, V2/2 and V3/4. V1 corresponds to the most significant bit (MSB) while V3 corresponds to the least significant bit (LSB).

The circuit for a 4-bit DAC using binary weighted resistor network is shown below:



The binary inputs, a_i (where i = 1, 2, 3 and 4) have values of either 0 or 1. The value, 0, represents an open switch while 1 represents a closed switch.

The operational amplifier is used as a summing amplifier, which gives a weighted sum of the binary input based on the voltage, V_{ref}.

For a 4-bit DAC, the relationship between V_{out} and the binary input is as follows:

$$
\begin{aligned}
V_{OUT} &= -iR_f \\
&= -\left[V_{ref}\left(\frac{a_1}{2R}+\frac{a_2}{4R}+\frac{a_3}{8R}+\frac{a_4}{16R}\right)\right]R_f \\
&= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2}+\frac{a_2}{4}+\frac{a_3}{8}+\frac{a_4}{16}\right) \\
&= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2^1}+\frac{a_2}{2^2}+\frac{a_3}{2^3}+\frac{a_4}{2^4}\right)
\end{aligned}
$$

The negative sign associated with the analog output is due to the connection to a summing amplifier, which is a polarity-inverting amplifier. When a signal is applied to the latter type of amplifier, the polarity of the signal is reversed (i.e. a + input becomes -, or vice versa).

For a n-bit DAC, the relationship between V_{out} and the binary input is as follows:

$$V_{OUT} = -\frac{V_{ref} R_f}{R} \sum_{i=1}^{n} \frac{a_i}{2^i}$$

Analog Voltage Output: An Example

As an example, consider the following given parameters: V_{ref} = 5 V, R = 0.5 k and R_f = 1 k. The voltage outputs, V_{out}, corresponding to the respective binary inputs are as follows:

Digital Input				V_{OUT} (Volts)
a_1	a_2	a_3	a_4	
0	0	0	0	**0**
0	0	0	1	**- 0.625**
0	0	1	0	**- 1.250**
0	0	1	1	**- 1.875**
0	1	0	0	**- 2.500**
0	1	0	1	**- 3.125**
0	1	1	0	**- 3.750**
0	1	1	1	**- 4.375**
1	0	0	0	**- 5.000**
1	0	0	1	**- 5.625**
1	0	1	0	**- 6.250**

1	0	1	1	**- 6.875**
1	1	0	0	**- 7.500**
1	1	0	1	**- 8.125**
1	1	1	0	**- 8.750**
1	1	1	1	**- 9.375**

Table 1: Voltage Output of 4-bit DAC using Binary Weighted Resistor Network

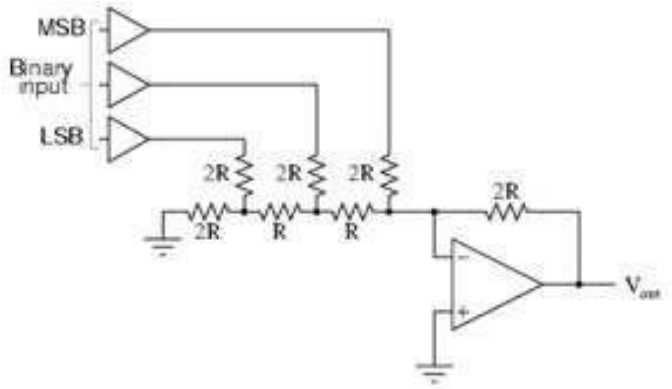
The LSB, which is also the incremental step, has a value of - 0.625 V while the MSB or the full scale has a value of - 9.375 V.

Practical Limitations:

- The most significant problem is the large difference in resistor values required between the LSB and MSB, especially in the case of high resolution DACs (i.e. those that has large number of bits). For example, in the case of a 12-bit DAC, if the MSB is 1 k □, then the LSBis a staggering 2 M□.
- The maintanence of accurate resistances over a large range of values is problematic. With the current IC fabrication technology, it is difficult to manufacture resistors over a wide resistance range that maintain an accurate ratio especially with variations in temperature.

R-2R LADDER DAC

An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin‘s theorem in arriving at the desired output voltages. The R-2R network consists of resistors with only two values - R and 2xR. If each input is supplied either 0 volts or reference voltage, the output voltage will be an analog equivalent of the binary value of the three bits. VS2 corresponds to the most significant bit (MSB) while VS0 corresponds to the least significant bit (LSB).

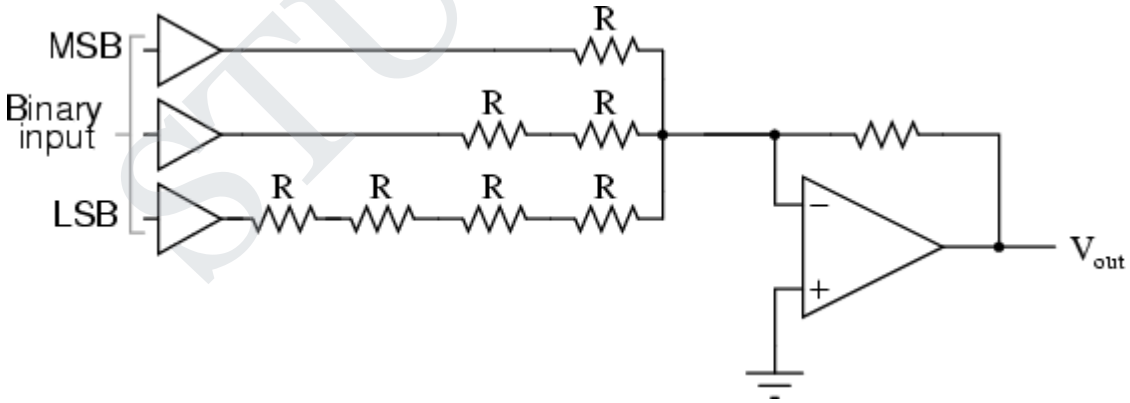


$$Vout = - (VMSB + Vn + VLSB) = - (VRef + VRef/2 + VRef/ 4)$$

The R/2R DAC

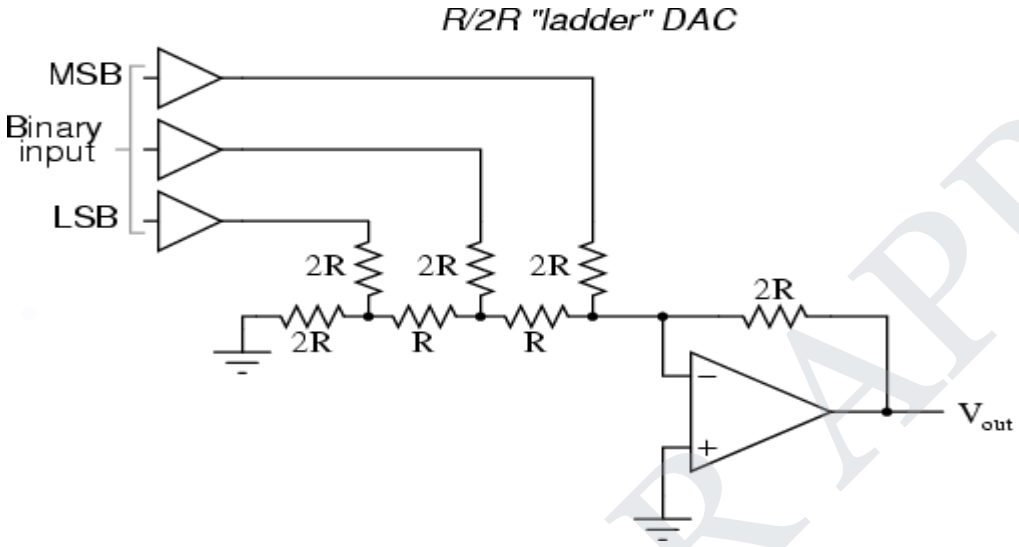
An alternative to the binary-weighted-input DAC is the so-called R/2R DAC, which uses fewer unique resistor values. A disadvantage of the former DAC design was its requirement of several different precise input resistor values: one unique value per binary input bit. Manufacture may be simplified if there are fewer different resistor values to purchase, stock, and sort prior to assembly.

Of course, we could take our last DAC circuit and modify it to use a single input resistance value, by connecting multiple resistors together in series:



Unfortunately, this approach merely substitutes one type of complexity for another: volume of

components over diversity of component values. There is, however, a more efficient design methodology. By constructing a different kind of resistor network on the input of our summing circuit, we can achieve the same kind of binary weighting with only two kinds of resistor values, and with only a modest increase in resistor count. This "ladder" network looks like this:



Mathematically analyzing this ladder network is a bit more complex than for the previous circuit, where each input resistor provided an easily-calculated gain for that bit. For those who are interested in pursuing the intricacies of this circuit further, you may opt to use Thevenin's theorem for each binary input (remember to consider the effects of the *virtual ground*), and/or use a simulation program like SPICE to determine circuit response. Either way, you should obtain the following table of figures:

Binary	Output voltage
000	0.00 V
001	-1.25 V
010	-2.50 V
011	-3.75 V
100	-5.00 V

101	-6.25 V	
110	-7.50 V	
111	-8.75 V	

As was the case with the binary-weighted DAC design, we can modify the value of the feedback resistor to obtain any "span" desired. For example, if we're using +5 volts for a "high" voltage level and 0 volts for a "low" voltage level, we can obtain an analog output directly corresponding to the binary input (011 = -3 volts, 101 = -5 volts, 111 = -7 volts, etc.) by using a feedback resistance with a value of 1.6R instead of 2R.

INVERTED OR CURRENT MODE DAC

As the name implies, Current mode DACs operates based on the ladder currents. The ladder is formed by resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into $i1$, $i2$, $i3$ ..... in in each arm. The currents are either diverted to the ground bus (io) or to the Virtual-ground bus ($\overline{io}$).

The currents are given as

$i1 = VREF/2R = (VREF/R)\ 2^{-1}$, $i2 = (VREF)/2)/2R = (VREF/R)\ 2^{-2}$ ..... $i_n = (VREF/R)\ 2^{-n}$.

And the relationship between the currents are given as

$$i2 = i_1/2$$

$$i3 = i_1/4$$

$$i4 = i_1/8$$

$$in = i_1/2^{n-1}$$

Using the bits to identify the status of the switches, and letting $V_0 = -R_f i_o$ gives

$$V_0 = -(R_f/R)\ V_{REF}\ (b_1 2^{-1} + b_2 2^{-2} + ... + b_n 2^{-n})$$

The two currents *io* and $\overline{io}$ are complementary to each other and the potential of *io* bus must be sufficiently close to that of the $\overline{io}$ bus. Otherwise, linearity errors will occur. The final op-amp is used as current to voltage converter.

Advantages

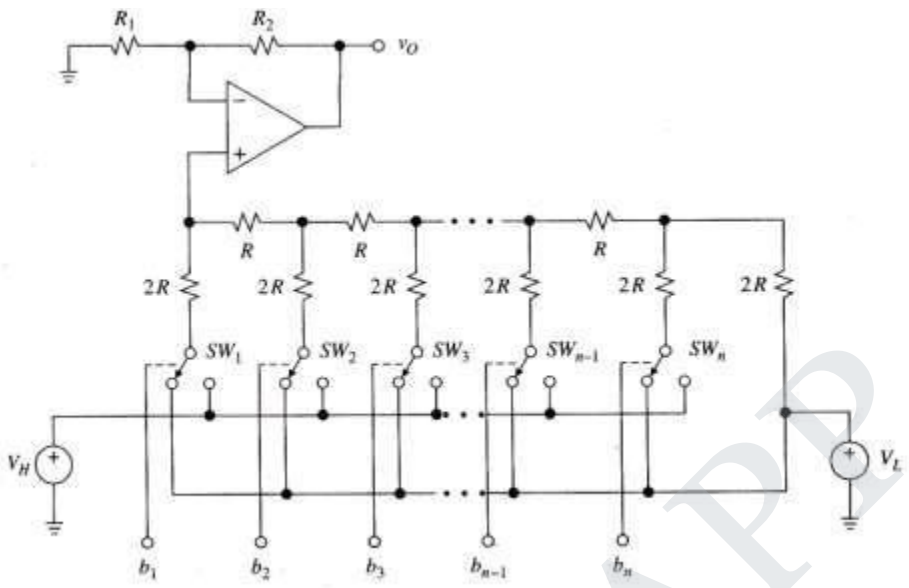
1. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.

2. In Current mode or inverted ladder type DACs, the stray capacitance do not affect the speed of response of the circuit due to constant ladder node voltages. So improved speed performance.

VOLTAGE MODE DAC

This is the alternative mode of DAC and is called so because, the 2R resistance in the shunt path is switched between two voltages named as V_L and V_H. The output of this DAC is obtained from the leftmost ladder node. As the input is sequenced through all the possible binary state starting from All 0s (0…..0) to all 1s (1… 1). The voltage of this node changes in steps of $2^{-n}\ (V_H - V_L)$ from the

minimum voltage of Vo = V_L to the maximum of Vo = V_H - 2^{-n} (V_H - V_L).



The diagram also shows a non-inverting amplifier from which the final output is taken. Due to this buffering with a non- inverting amplifier, a scaling factor defined by K = 1 + (R_2/R_1) results.

Advantages

1. The major advantage of this technique is that it allows us to interpolate between any two voltages, neither of which need not be a zero.
2. More accurate selection and design of resistors R and 2R are possible and simple construction.
3. The binary word length can be easily increased by adding the required number or R-2R sections.

SWITCHES FOR DAC

The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch. Although switches can be made of using diodes, Bipolar junction Transistors, Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs. They are

i) Switches using overdriven Emitter Followers.

ii) Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter Switch.

iii) CMOS switch for Multiplying type DACs .

iv) CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

Switches using overdriven Emitter Followers:

The bipolar transistors have a negligible resistance when they are operated in saturation. The bipolar transistor operating in saturation region indicates a minimum resistance and thus represents ON condition. When they are operating in cut-off region indicates a maximum resistance and thus represents OFF condition.

The circuit shown here is the arrangement of two transistors connected as emitter followers. A silicon transistor operating in saturation will have a offset voltage of 0.2V dropped across them. To have a zero offset voltage condition, the transistors must be overdriven because the saturation factor becomes negative. The two transistors Q_1(NPN) and Q_2(PNP) acts as a double pole switch. The bases of the transistors are driven by +5.75V and -5.75V.

Case 1:

When $V_{B1} = V_{B2} = +5.75V$, Q_1 is in saturation and Q_2 is OFF. And $V_E \approx 5V$ with

$V_{BE1} = V_{BE2} = 0.75V$

Case 2:

When $V_{B1} = V_{B2} = -5.75V$, Q_2 is in saturation and Q_1 is OFF. And $V_E \approx -5V$ with

$V_{BE1} = V_{BE2} = 0.75V$

Thus the terminal B of the resistor R_e is connected to either -5V or +5V depending on the input bit.

Switches using MOS transistor:

i) Totem pole MOSFET Switch:

As shown in the figure, the totem pole MOSFET Switch is connected in series with resistors of R-2R network. The MOSFET driver is connected to the inverting terminal of the summing op-amp. The complementary outputs Q and $\overline{Q}$ drive the gates of the MOSFET M_1 and M_2 respectively. The SR flipflop holds one bit of digital information of the binary word under conversion. Assuming the negative logic (-5V for logic 1 and +5V for logic 0) the operation is given as two cases.

Case 1:

When the bit line is 1 with S=1 and R=0 makes Q=1 and $\overline{Q}$=0. This makes the transistor M_1 ON, thereby connecting the resistor R to reference voltage $-V_R$. The transistor M_2 remains in OFF condition.

Case 2:

When the bit line is 0 with S=0 and R=1 makes Q=0 and $\overline{Q}$=1. This makes the transistor M_2 ON, thereby connecting the resistor R to Ground. The transistor M_1 remains in OFF condition.

ii) CMOS Inverter Switch:

The figure of CMOS inverter is shown here. It consists of a CMOS inverter connected with an op-amp acting as a buffer. The buffer drives the resistor R with a very low output impedance. Assuming positive logic (+5V for logic 1 and 0V for logic 0), the operation can be explained in two cases.

Case1:

When the complement of the bit line Q is low, M_1 becomes ON connecting V_R to the non-inverting input of the op-amp. This drives the resistor R HIGH.

Case2:

When the complement of the bit line $\overline{Q}$ is high, M_2 becomes ON connecting Ground to the non-inverting input of the op-amp. This pulls the resistor R LOW (to ground).

CMOS switch for Multiplying type DACs:

The circuit diagram of CMOS Switch is shown here. The heart of the switching element is formed by transistors M_1 and M_2. The remaining transistors accept TTl or CMOS compatible logic inputs and provides the anti-phase gate drives for the transistors M_1 and M_2. The operation for the two cases is as follows.

Case 1:

When the logic input is 1, M_1 is ON and M_2 is OFF. Thus current I_K is diverted to Io‘ bus.

Case 2:

When the logic input is 0, M_2 is ON and M_1 is OFF. Thus current I_K is diverted to Io bus.

CMOS Transmission gate switches:

The disadvantage of using individual NMOS and PMOS transistors are threshold voltage drop

(NMOS transistor passing only minimum voltage of V_R - V_{TH} and PMOS transistor passing minimum voltage of V_{TH}). This is eliminated by using transmission gates which uses a parallel connection of both NMOS and PMOS. The arrangement shown here can pass voltages from V_R to 0V acting as a ideal switch. The following cases explain the operation.

Case 1:

When the bit-line b_k is HIGH, both transistors M_n and M_p are ON, offering low resistance over the entire range of bit voltages.

Case 2:

When the bit-line b_k is LOW, both the transistors are OFF, and the signal transmission is inhibited (Withdrawn).

Thus the NMOS offers low resistance in the lower portion of the signal and PMOS offers low resistance in the upper portion of the signal. As a combination, they offer a low parallel resistance throughout the operating range of voltage. Wide varieties of these kinds of switches were available. Example: CD4066 and CD4051.

HIGH SPEED SAMPLE AND HOLD CIRCUITS

Introduction:

Sample-and-hold (S/H) is an important analog building block with many applications, ncluding analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1]. The simplest S/H circuit in MOS technology is shown in Figure 1, where *Vin* is the input signal, *M1* is an MOS transistor operating as the sampling switch, *Ch* is the hold capacitor, *ck* is the clock signal, and *Vout* is the resulting sample-and-hold output signal.

Ch

As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever

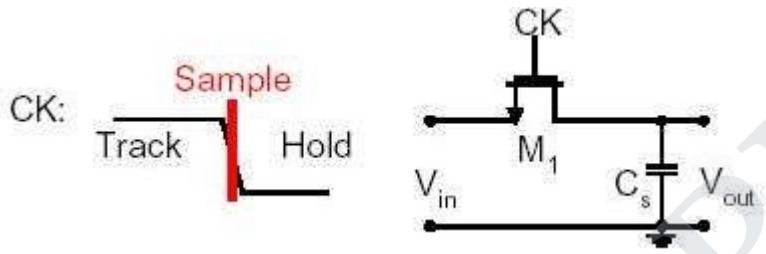


Figure 1: Simplest sample-and-hold circuit in MOS technology.

As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever *ck* is high, the MOS switch is on, which in turn allows *Vout* to track *Vin*. On the other hand, when *ck* is low, the MOS switch is off. During this time, *Ch* will keep *Vout* equal to the value of *Vin* at the instance when *ck* goes low.

Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above. The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

Alternative CMOS Sample-and-Hold Circuits:

This section covers three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feedthrough.

Series Sampling:

The S/H circuit of Figure 1 is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled.

On the other hand, the S/H circuit shown in Figure 2 is referred to as series sampling because the hold capacitor is in series with the signal.

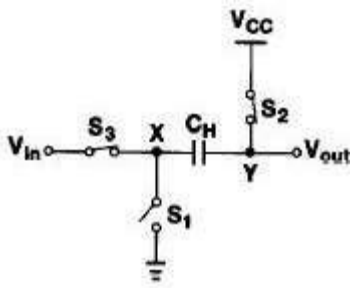


Figure 2: Series sampling.

When the circuit is in sample mode, both switches *S2* and *S3* are on, while *S1* is off. Then,*S2* is turned off first, which means *Vout* is equal to *VCC* (or *VDD* for most circuits) and the voltage drop across *Ch* will be *VCC – Vin*. Subsequently, *S3* is turned off and *S1* is turned on simultaneously. By grounding node *X*, *Vout* is now equal to *VCC – Vin*, and the drop from *VCC* to *VCC – Vin* is equal to the instantaneous value of the input.

As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common-mode levels of the input and the output. This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because *S2* is turned off before *S3*. Thus, the fact that the gate-to-source voltage, *VGS*, of *S2* is constant means that charge injection coming from *S2* is also constant (as opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node *Y*. This parasitic capacitance introduces distortion to the sample-and hold value, thus mandating that *Ch* be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for

series sampling than for parallel sampling. The reason for this is because the value of *Vout* in series sampling is being reset to *VCC* (or *VDD*) for every sample, but this is not the case for parallel sampling.

Switched Op-Amp Based Sample-and-Hold Circuit:

This S/H technique takes advantage of the fact that when a MOS transistor is in the saturation region, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor is connected to the drain of the MOS transistor, charge injection will only go to the source junction, leaving the drain unaffected. Based on this concept, a switched op-amp (SOP) based S/H circuit, as shown in Figure 3.

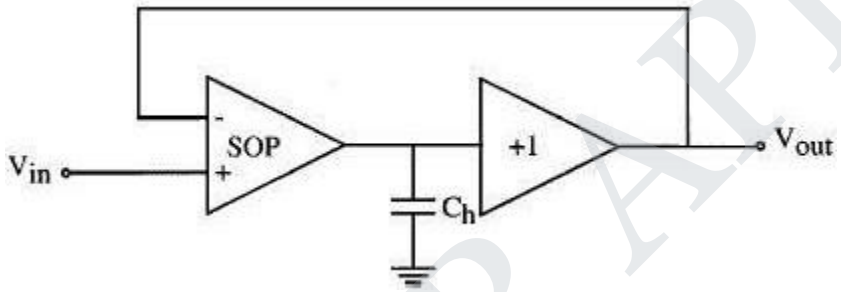


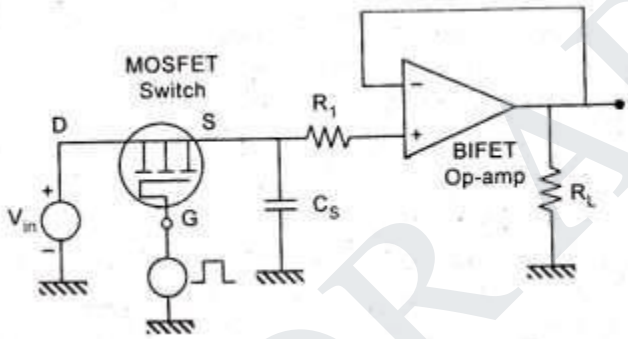
Figure 3: Switched op-amp based sample and hold circuit.

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on *Ch* to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on *Ch* to the output of the S/H circuit.

With the increasing demand for high-resolution and high-speed in date acquisition systems, the performance of the S/H circuits is becoming more and more important. This is especially true in ADCs since the performance of S/H circuits greatly affects the speed and accuracy of ADCs. The fastest S/H circuits operate in open loop, but when such circuits are implemented in CMOS technology, their accuracy is low. S/H circuits

that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed.

At the same time, the employment of low-voltage in VLSI technology requires that the analog circuits be low-voltage as well. As a result of this, new researches in analog circuits are now shifted from voltage-mode to current-mode. The advantages of current mode circuits include low-voltage, low-power, and high-speed. Therefore, future researches of S/H circuit should also shift toward current-mode S/H techniques.

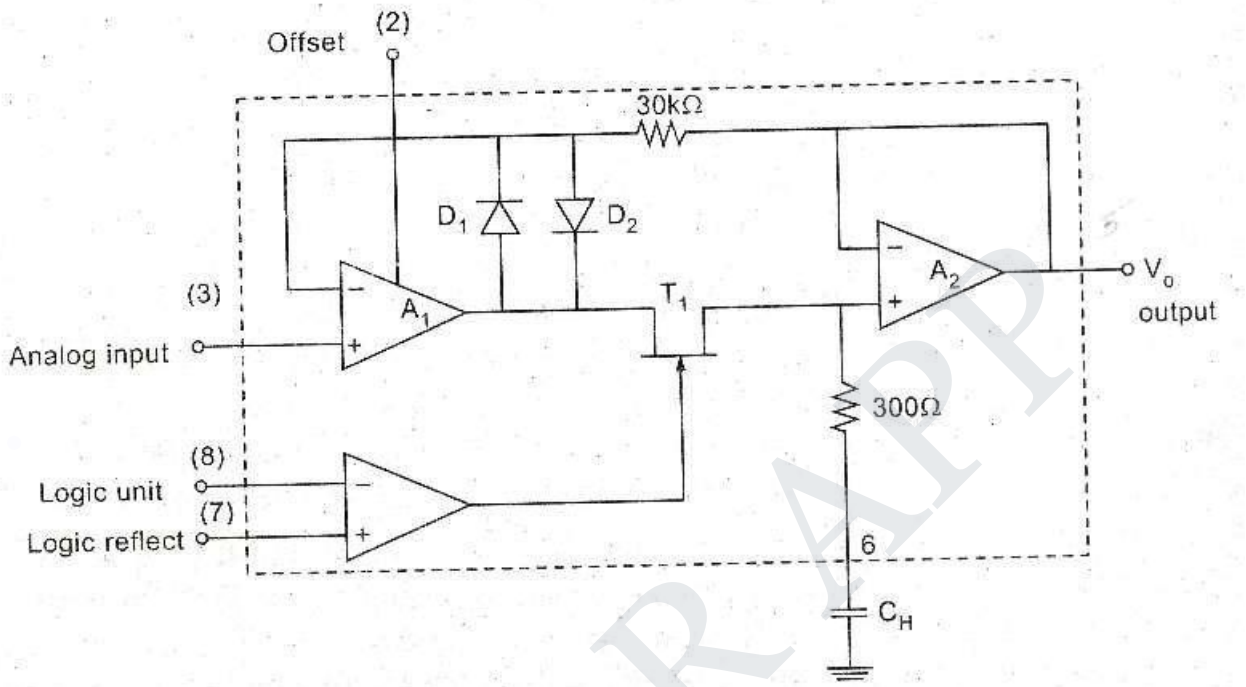


The above figure shows a sample and hold circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor Cs to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

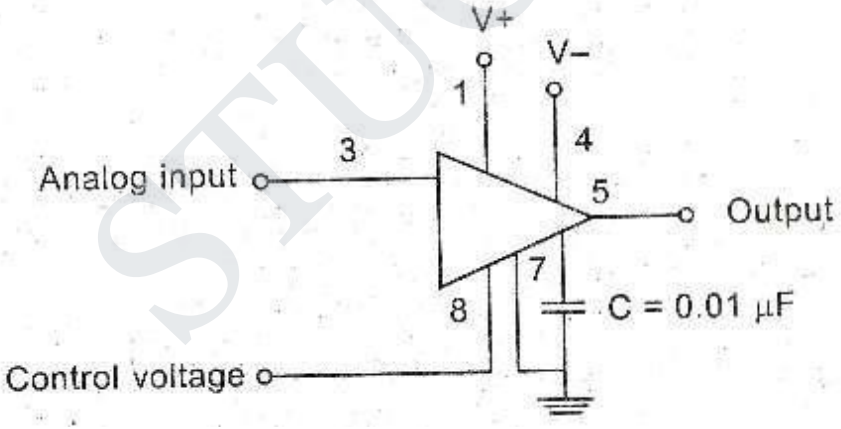
Sample-and-hold (S/H) is an important analog building block that has many applications. The simplest S/H circuit can be constructed using only one MOS transistor and one hold capacitor. However, due to the limitations of the MOS transistor switches, errors due to charge injection and clock feed through restrict the performance of S/H circuits. As a result, different S/H techniques and architectures are developed with the intention to reduce or eliminate these errors. Three of these alternative S/H circuits: series sampling, SOP based S/H circuit, and bottom plate S/H circuit with bootstrapped switch, more new S/H techniques and architectures need to be proposed in order

to meet the increasing demand for high-speed, low-power, and low voltage S/H circuits for data acquisition systems.

LF 398 IC- Functional Diagram



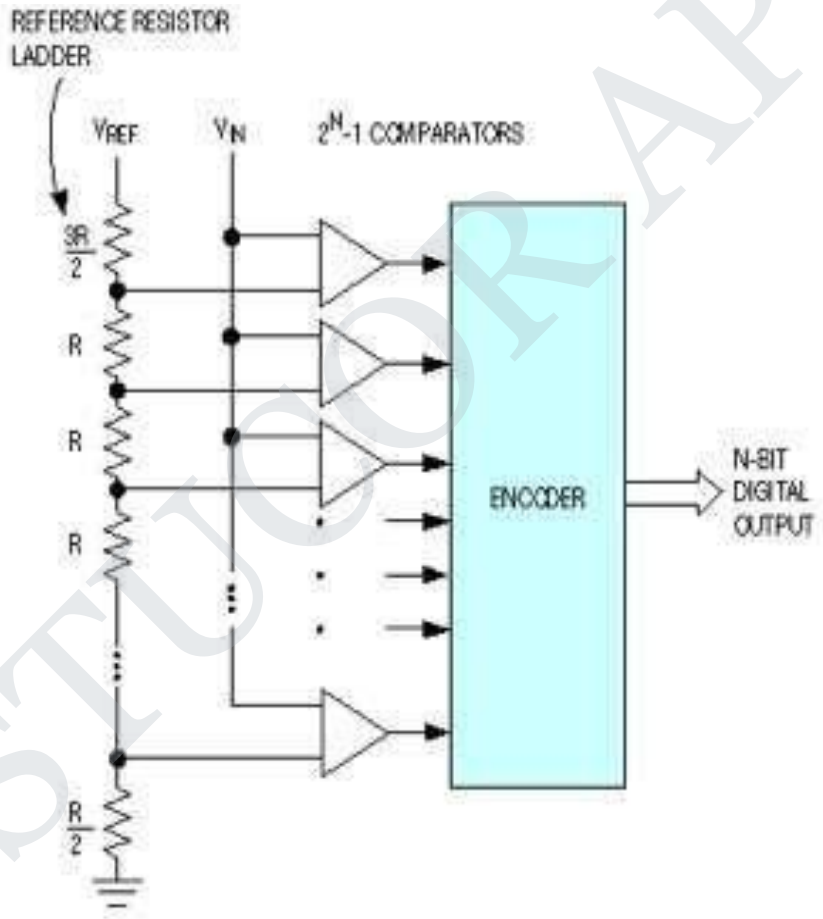
Connection Diagram



Types of ADC

Direct-conversion ADC/Flash type ADC:

This process is extremely fast with a sampling rate of up to 1 GHz. The resolution is however, limited because of the large number of comparators and reference voltages required. The input signal is fed simultaneously to all comparators. A priority encoder then generates a digital output that corresponds with the highest activated comparator.



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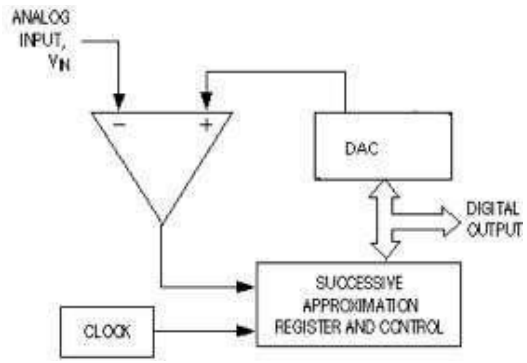
Successive-approximationADCs

Successive-approximation ADC is a conversion technique based on a successive-approximation register (SAR). This is also called bit-weighing conversion that employs a comparator to weigh the applied input voltage against the output of an N-bit digital-to-analog converter (DAC). The final result is obtained as a sum of N weighting steps, in which each step is a single-bit conversion using the DAC output as a reference. SAR converters sample at rates up to 1Mbps, requires a low supply current, and the cheapest in terms of production cost.

A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved. At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons. For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V is compared to 50 V (the reference, divided by two. This is the voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V). At this point the first binary digit (MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V (halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros). The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for '1001' followed by zeros). The result of this would be in the binary form 1001. This is also called *bit-weighting conversion*, and is similar to a binary. The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired. The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required. ADCs of this type have good resolutions and quite wide ranges. They are more

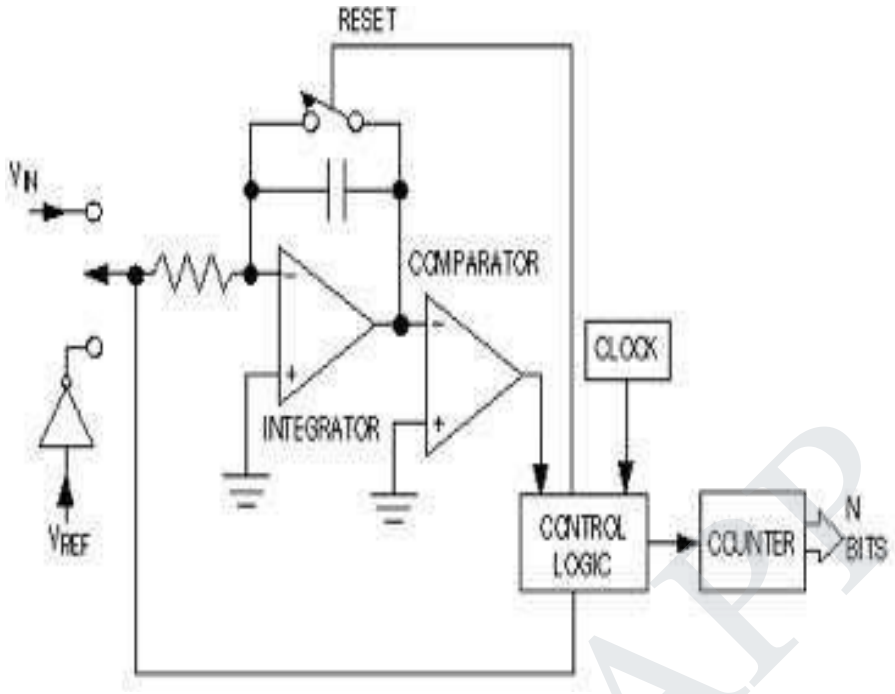
complex than some other designs.



Integrating ADCs

In an integrating ADC, a current, proportional to the input voltage, charges a capacitor for a fixed time interval T charge. At the end of this interval, the device resets its counter and applies an opposite-polarity negative reference voltage to the integrator input. Because of this, the capacitor is discharged by a constant current until the integrator output voltage zero again. The T discharge interval is proportional to the input voltage level and the resultant final count provides the digital output, corresponding to the input signal. This type of ADCs is extremely slow devices with low input bandwidths. Their advantage, however, is their ability to reject high-frequency noise and AC line noise such as 50Hz or 60Hz. This makes them useful in noisy industrial environments and typical application is in multi-meters.

An integrating ADC (also dual-slope or multi-slope ADC) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.



Sigma-delta ADCs/ Over sampling Converters:

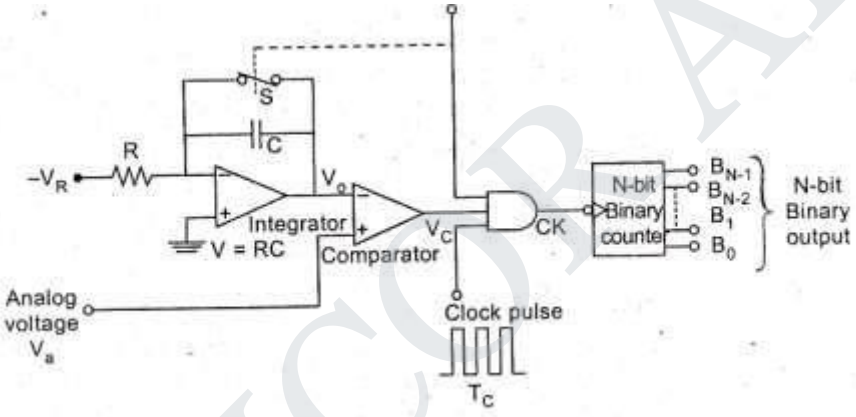
It consist of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transform by the output filter to a sequence of parallel digital words at the sampling rate. The characteristics of sigma-delta converters are high resolution, high accuracy, low noise and low cost. Typical applications are for speech and audio.

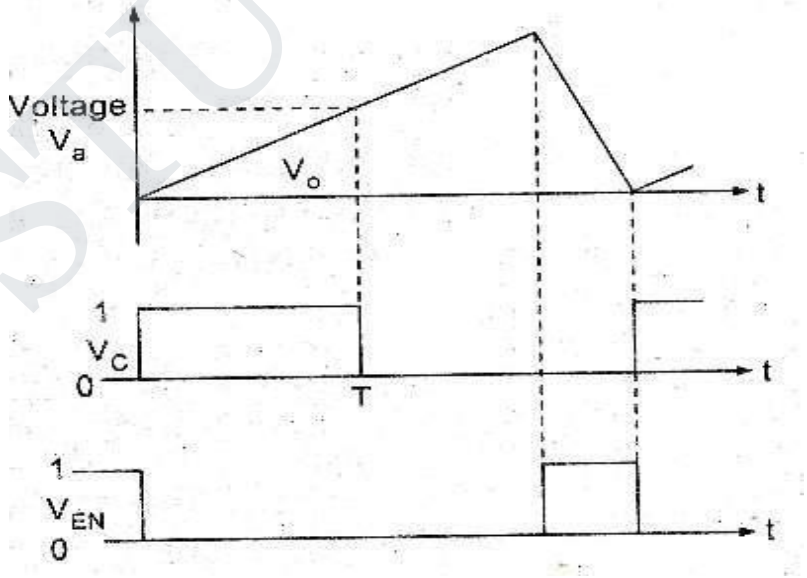
A **Sigma-Delta ADC** (also known as a Delta-Sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally a smaller number of bits than required are converted using a Flash ADC after the Filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies. A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. (sigma-delta modulation, also called delta-sigma modulation)

A/D Using Voltage to time conversion:

The Block diagram shows the basic voltage to time conversion type of A to D converter. Here the cycles of variable frequency source are counted for a fixed period. It is possible to make an A/D converter by counting the cycles of a fixed-frequency source for a variable period. For this, the analog voltage required to be converted to a proportional time period.

As shown in the diagram, A negative reference voltage $-V_R$ is applied to an integrator, whose output is connected to the inverting input of the comparator. The output of the comparator is at 1 as long as the output of the integrator Vo is less than Va. At t = T, Vc goes low and switch S remains open. When V_{EN} goes high, the switch S is closed, thereby discharging the capacitor. Also the NAND gate is disabled. The waveforms are shown here.





UNIT IV – ANALOG MULTIPLIER AND PLL

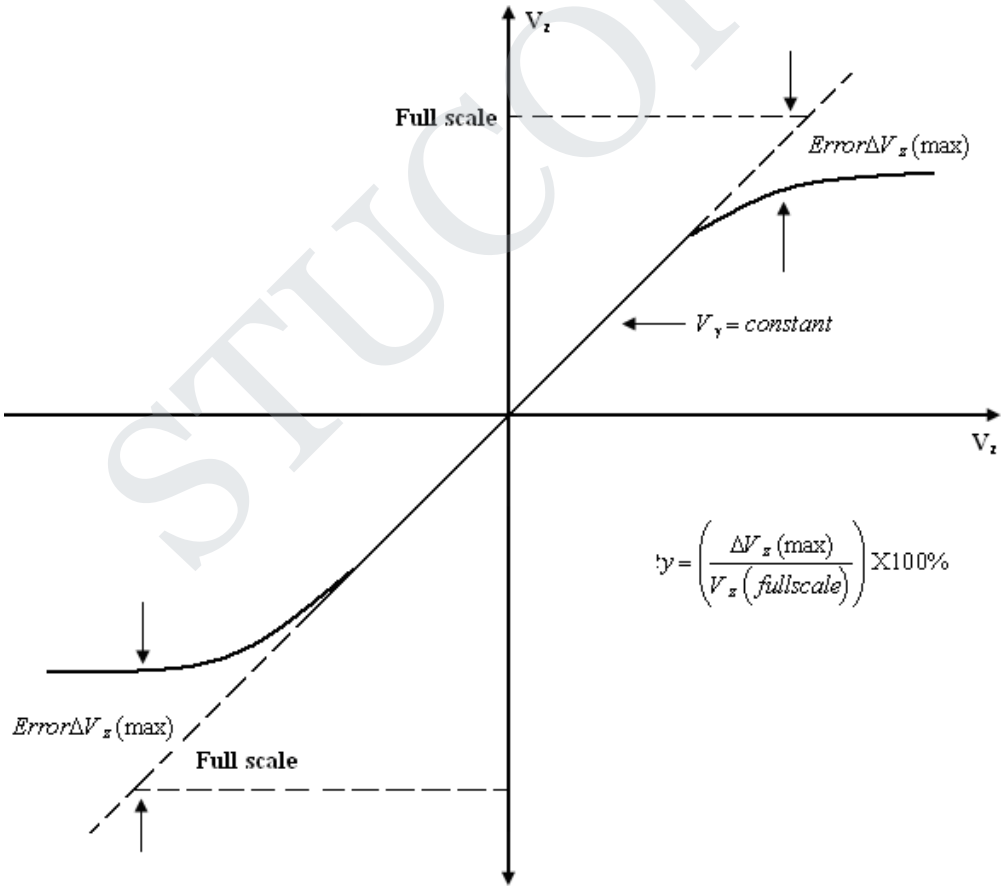
Analog Multipliers:

A multiple produces an output V_0 , which is proportional to the product of two inputs V_x and V_y.

That is, $V_0 = KV_xV_y$ where K is the scaling factor that is usually maintained as (1/10) V^{-1} . There are various methods available for performing analog multiplication. Four of such techniques, namely,

1. Logarithmic summing technique
2. Pulse height/width modulation Technique
3. Variable trans conductance Technique
4. Multiplication using Gilbert cell and
5. Multiplication using variable trans conductance technique.

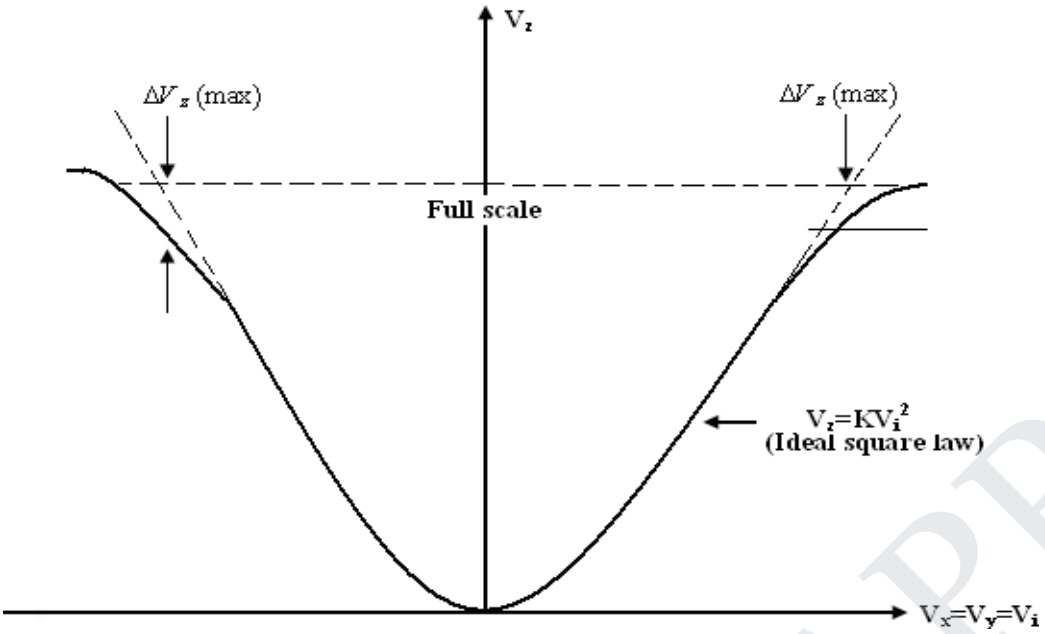
An actual multiplier has its output voltage V_0 defined by



$$\%y = \left(\frac{\Delta V_z(\max)}{V_z(fullscale)}\right) X100\%$$

Squaring Mode Accuracy:

The Square – law curve is obtained with both the X and Y inputs connected together and applied with the same input signal. The maximum derivation of the output voltage from an ideal square – law curve expresses the squaring mode accuracy.



Bandwidth:

The Bandwidth indicates the operating capability of an analog multiplier at higher frequency values. Small signal 3 dB bandwidth defines the frequency f_0 at which the output reduces by 3dB from its low frequency value for a constant input voltage. This is identified individually for the X and Y input channels normally.

The transconductance bandwidth represents the frequency at which the transconductance of the multiplier drops by 3dB of its low frequency value. This characteristics defines the application frequency ranges when used for phase detection or AM detection.

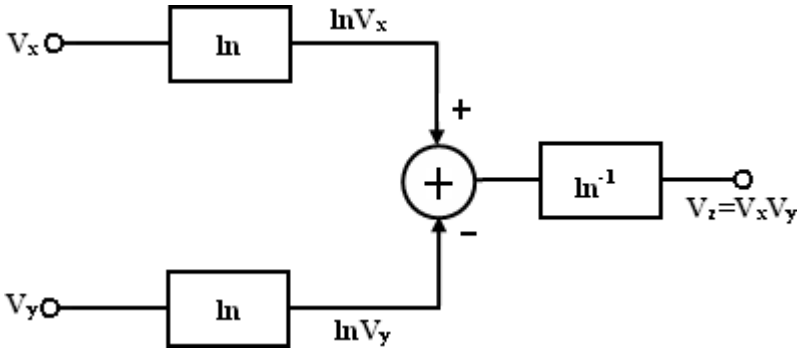
Quadrant:

The quadrant defines the applicability of the circuit for bipolar signals at its inputs. First – quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four quadrant device accepts two bipolar signals.

Logarithmic summing Technique:

This technique uses the relationship

$\ln V_x + \ln V_y = \ln(V_x V_y)$



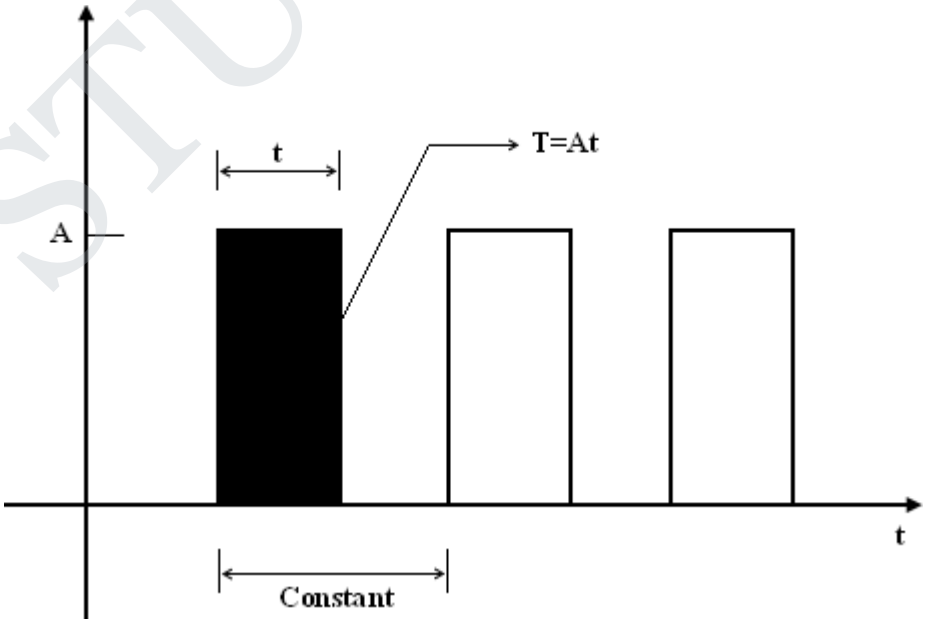
As shown in figure the input voltages V_x and V_y are converted to their logarithmic equivalent, which are then added together by a summer. An antilogarithmic converter produces the output voltage of the summer. The output is given by,

$V_z = \ln^{-1}(\ln(V_x\ V_y)) = V_x\ V_y$ The exponential relationship between the collector current and base

to emitter voltage of bipolar transistor during its active mode of operation could be explained for the logarithmic and anti-logarithmic conversions. The relationship between I_0 and V_{BE} of the transistor is given by

$I_C = I_0 e^{(VBE\ /VT\ )}$ It is found that the transistor follows the relationship very accurately in the range of 10nA to 100mA. Logarithmic multiplier has low accuracy and high temperature instability. This method is applicable only to positive values of V_x and V_y. Therefore, this type of multiplier is restricted to one quadrant operation only.

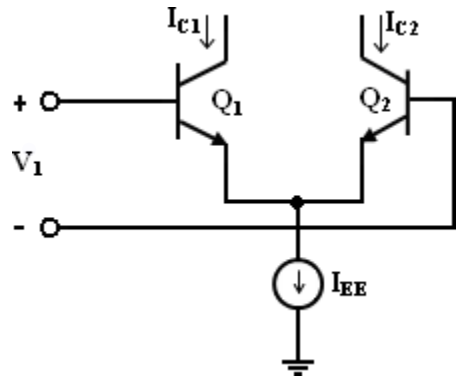
Pulse Height/ Width Modulation Technique:



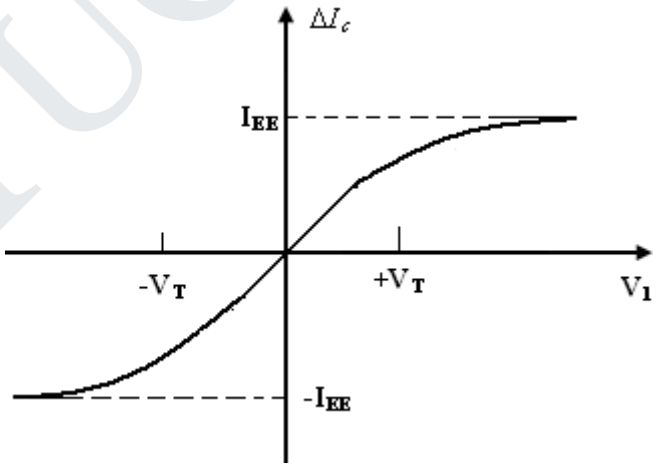
In this method, the pulse width of a pulse train is made proportional to one input voltage and the pulse amplitude is made proportional to the second input voltage. Therefore, $V_x = K_x A$, $V_y = K_y t$, and $V_z = K_z T$ where K_x , K_y , K_z are scaling factors. In figure A is the amplitude of the pulse, t is the pulse width and T is the area of the pulse. Therefore,

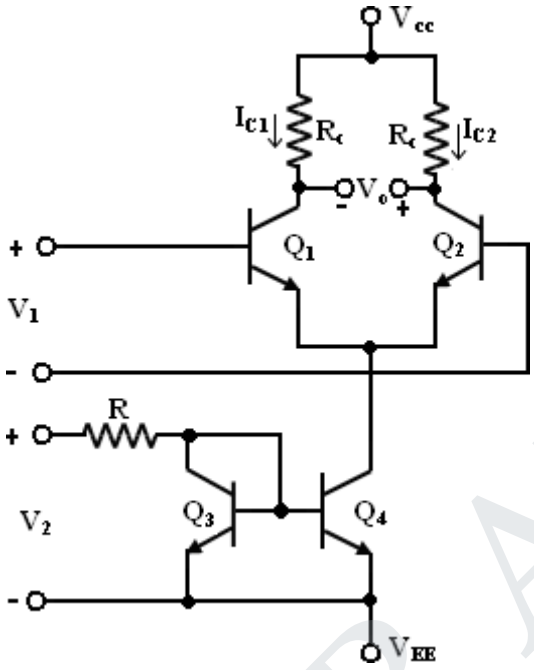
The modulated pulse train is passed through an integrated circuit. Therefore, the input of the integrator is proportional to the area of pulse, which in turn is proportional to the product of two input voltages. K

A simple multiplier using an Emitter coupled Transistor pair:



A circuit using an emitter coupled pair is shown in figure. The output currents I_{C1} and I_{C2} arrelatedto the differential input voltage The dc transfer characteristics of the emitter – coupled pair is shown in figure. It shows that the emitter coupled pair can be used as a simple multiplier using this configuration. When the differential input voltage $V_1 << V_T$, we can appropriate as given by





This arrangement is shown in figure. It is a simple modulator circuit constructed using a differential amplifier. It can be used as a multiplier, provided V_1 is small and much less than 50mV, and V_2 is greater than $V_{BE(on)}$. But, the multiplier circuit shown in figure has several limitations. The first limitation is that V_2 is offset by $V_{BE(on)}$. The second is that V_2 must always be positive which results in only a two-quadrant multiplier operation. The third limitation is that, the tanh (X) is approximately as X, where $X = V_1 /2V_T$. The first two limitations are overcome in the Gilbert cell.

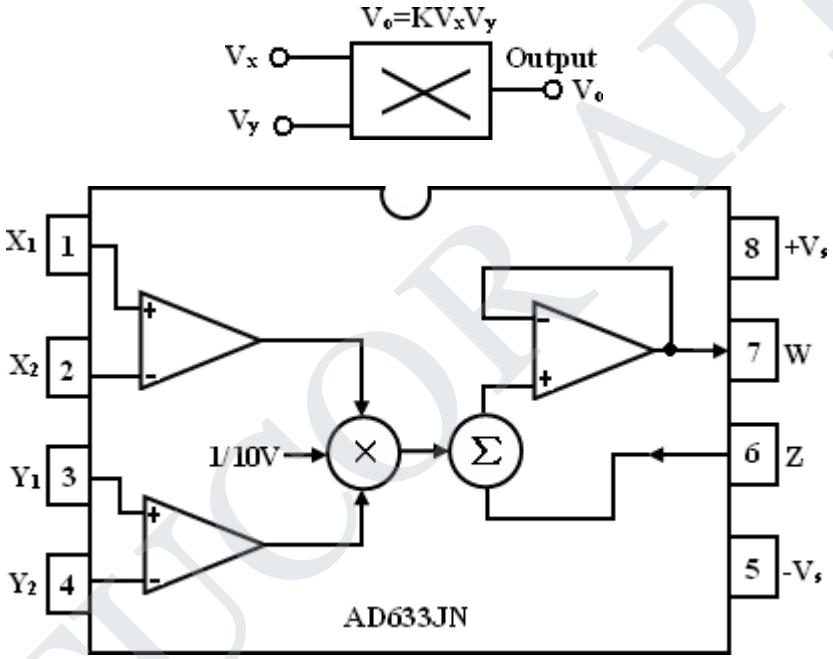
Gilbert Multiplier cell:

The Gilbert multiplier cell is a modification of the emitter coupled cell and this allows four – quadrant multiplication. Therefore, it forms the basis of most of the integrated circuit balanced

multipliers. Two cross- coupled emitter- coupled pairs in series connection with an emitter coupled pair form the structure of the Gilbert multiplier cell.

Analog Multiplier ICs

Analog multiplier is a circuit whose output voltage at any instant is proportional to the product of instantaneous value of two individual input voltages. The important applications of these multipliers are multiplication, division, squaring and square – rooting of signals, modulation and demodulation. These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. The Schematic of a typical analog multiplier, namely, AD633 is shown in figure.



The AD633 multiplier is a four – quadrant analog multiplier. It possesses high input impedance, and this characteristic makes the loading effect on the signal source negligible. It can operate with supply voltages ranging from ±18V. The IC does not require external components. The calibration by user is not necessary. The typical range of the two input signals is ±10V.

Schematic representation of a multiplier:

The schematic representation of an analog multiplier is shown in figure. The output V_0 is the product of the two inputs V_x and V_y is divided by a reference voltage Vref. Normally, the reference voltage Vref is internally set to 10V. Therefore, V_0 =VxVy/10. In other words, the basic input – output relationship can be defined by KV_x V_y when K = 1/10, a constant. Thus for peak input voltages of 10V, the peak magnitude of output voltage is 1/10 *10 *10 =10V. Thus, it can be noted that, as long as V_x < 10V and V_y < 10V, the multiplier output will not saturate.

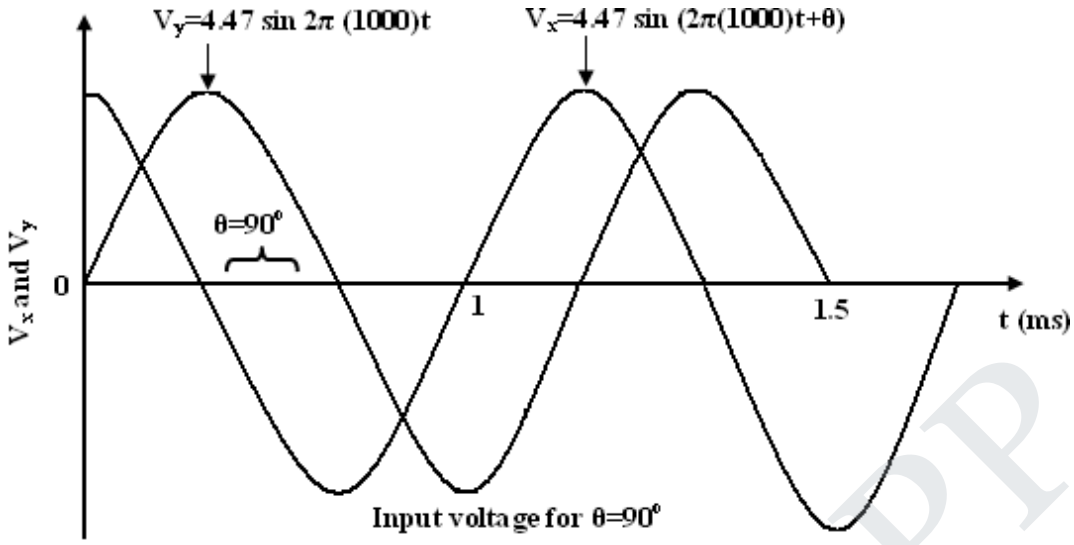
Multiplier quadrants:

The transfer characteristics of a typical four-quadrant multiplier is shown in figure. Both the inputs can be positive or negative to obtain the corresponding output as shown in the transfer characteristics.

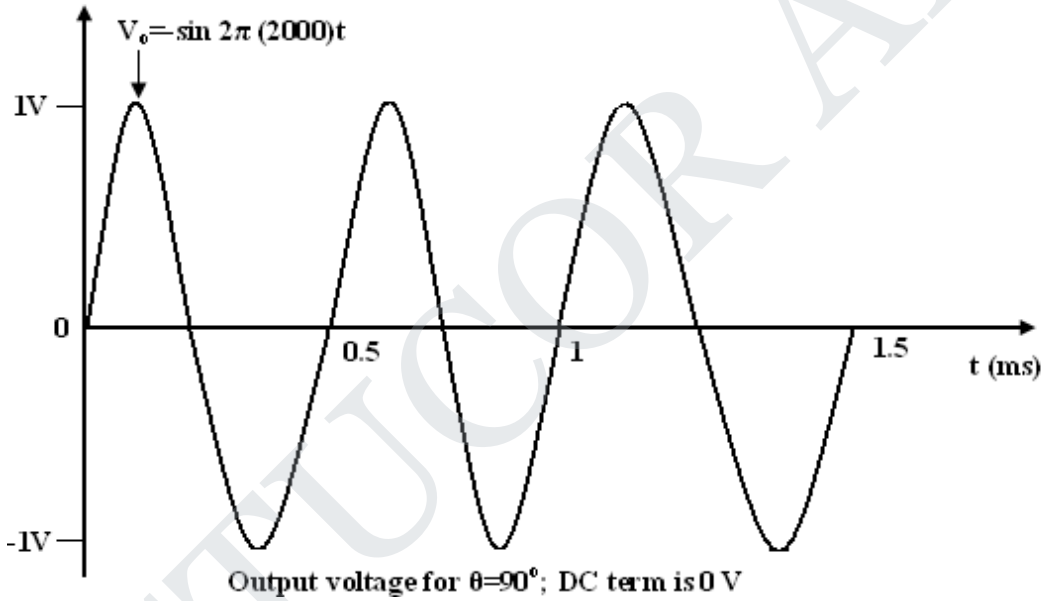
Applications of Multiplier ICs:

The multiplier ICs are used for the following purposes:

1. Voltage Squarer
2. Frequency doubler



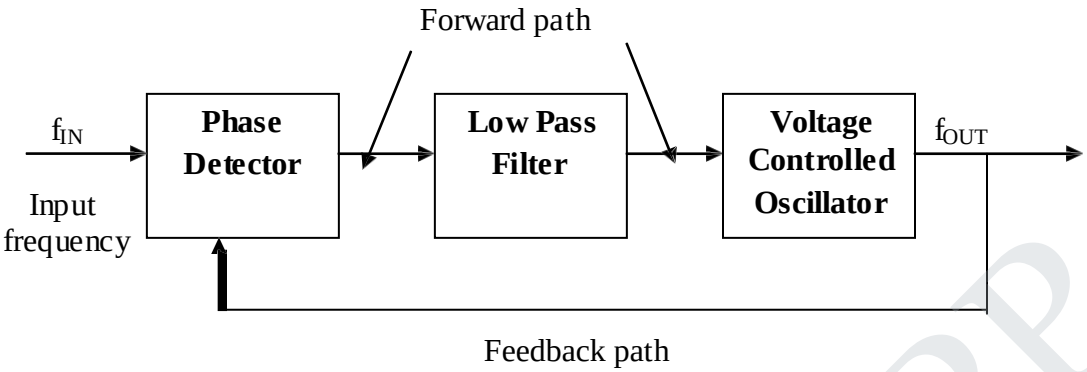
Input voltage for θ=90°



Output voltage for θ=90°; DC term is 0 V

PHASE LOCKED LOOP:

Basic Block Diagram of a PLL



phase locked loop construction and operation:

- The PLL consists of i) Phase detector ii) LPF iii) VCO. The phase detector or comparator compares the input frequency f_{IN} with feedback frequency $f_{OUT.}$
- The output of the phase detector is proportional to the phase difference between f_{IN} & $f_{OUT.}$ The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.
- The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO.
- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.
- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode. When Phase locked, the loop tracks any change in the input frequency through its repetitive action. If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency and/or phase, an error voltage v_e is generated.

The phase detector is basically a multiplier and produces the sum ($f_s + f_o$) and difference ($f_s - f_o$) components at its output. The high frequency component ($f_s + f_o$) is removed by the low pass filter and the difference frequency component is amplified then applied as control voltage v_c to VCO. The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference φ. This phase difference φ generates a corrective control voltage v_c to shift the VCO frequency from f_0 to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Capture range: the range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o.

Pull-in time: the total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

(a) Phase Detector:

Phase detector compares the input frequency and VCO frequency and generates DC voltage i.e., proportional to the phase difference between the two frequencies. Depending on whether the analog/digital phase detector is used, the PLL is called either an analog/digital type respectively. Even though most monolithic PLL integrated circuits use analog phase detectors.

Ex for Analog: Double-balanced mixer

Ex for Digital: Ex-OR, Edge trigger, monolithic Phase detector.

Ex-OR Phase Detector:

This uses an exclusive OR gate. The output of the Ex-OR gate is high only when f_{IN} or f_{OUT} is high.

The DC output voltage of the Ex-OR phase detector is a function of the phase difference between its two outputs. The maximum dc output voltage occurs when the phase difference is Π radians or

180 degrees. The slope of the curve between 0 or Π radians is the conversion gain k_p of the phase detector for eg; if the Ex-OR gate uses a supply voltage Vcc = 5V, the conversion gain K_p is

$$K_P = \frac{5V}{\square} = 1.59V / RAD$$

Edge Triggered Phase Detector:

Advantages of Edge Triggered Phase Detector over Ex-OR are

i) The dc output voltage is linear over 2Π radians or 360 degrees, but in Ex-OR it is Π radians or 180 degrees.

ii) Better Capture, tracking & locking characteristics.

Edge triggered type of phase detector using RS Flip – Flop. It is formed from a pair of cross coupled NOR gates.

RS FF is triggered, i.e, the output of the detector changes its logic state on the positive edge of the inputs f_{IN} & f_{OUT}

Monolithic Phase detector:

- It consists of 2 digital phase detector, a charge pump and an amplifier.
- Phase detector 1 is used in applications that require zero frequency and phase difference at lock.
- Phase detector 2, if quadrature lock is desired, when detector 1 is used in the main loop, detector can also be used to indicate whether the main loop is in lock or out of lock.

  R□ Reference

  V□ Variable or 0feedback input

  PU □ Pump Up signal

  PD□ Pump Down signal

  UF □ Up frequency output signal

  DF □ Down frequency output signal

(b) Low – Pass filter:

The function of the LPF is to remove the high frequency components in the output of the phase detector and to remove the high frequency noise. LPF controls the characteristics of the phase locked loop. i.e, capture range, lock ranges, bandwidth

- Lock range(Tracking range):

  The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency f_{IN}.

- Capture range:

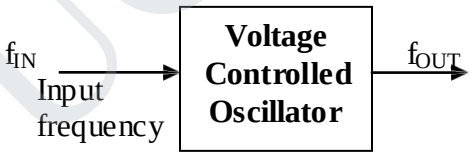
  Capture range is the frequency range in which the PLL acquires phase lock. Capture range is always smaller than the lock range.

- Filter Bandwidth:

  Filter Bandwidth is reduced, its response time increases. However reduced Bandwidth reduces the capture range of the PLL. Reduced Bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes noise.

(c) Voltage Controlled Oscillator (VCO):

The third section of PLL is the VCO; it generates an output frequency that is directly proportional to its input voltage. The maximum output frequency of NE/SE 566 is 500 Khz.



Feedback path and optional divider:

Most PLLs also include a divider between the oscillator and the feedback input to the phase detector to produce a frequency synthesizer. A programmable divider is particularly useful in radio

transmitter applications, since a large number of transmit frequencies can be produced from a single stable, accurate, but expensive, quartz crystal–controlled reference oscillator.

Some PLLs also include a divider between the reference clock and the reference input to the phase detector. If this divider divides by M, it allows the VCO to multiply the reference frequency by N / M. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be constrained by other issues, and then the reference divider is useful. Frequency multiplication in a sense can also be attained by locking the PLL to the 'N'th harmonic of the signal.

Equations:

The equations governing a phase-locked loop with an analog multiplier as the phase detector may be derived as follows. Let the input to the phase detector be $x_c(t)$ and the output of the voltage-controlled oscillator (VCO) is $x_r(t)$ with frequency $\omega_r(t)$, then the output of the phase detector $x_m(t)$ is given by

$$x_m(t) = x_c(t) \cdot x_r(t)$$

the VCO frequency may be written as a function of the VCO input $y(t)$ as

$$\omega_r(t) = \omega_f + g_v y(t)$$

where g_v is the *sensitivity* of the VCO and is expressed in Hz / V.

Hence the VCO output takes the form

$$x_r(t) = A_r \cos\left(\int_0^t \omega_r(\tau)\, d\tau\right) = A_r \cos(\omega_f t + \varphi(t))$$

where

$$\varphi(t) = \int_0^t g_v y(\tau)\, d\tau$$

The loop filter receives this signal as input and produces an output

$$x_f(t) = F_{\text{filter}}(x_m(t))$$

where F_{Filter} is the operator representing the loop filter transformation.

When the loop is closed, the output from the loop filter becomes the input to the VCO thus

$$y(t) = x_f(t) = F_{\text{filter}}(x_m(t))$$

We can deduce how the PLL reacts to a sinusoidal input signal:

$$x_c(t) = A_c \sin(\omega_c t).$$

The output of the phase detector then is:

$$x_m(t) = A_c \sin(\omega_c t) A_r \cos(\omega_f t + \varphi(t)).$$

This can be rewritten into sum and difference components using trigonometric identities:

$$x_m(t) = \frac{A_c A_f}{2} \sin(\omega_c t - \omega_f t - \varphi(t)) + \frac{A_c A_f}{2} \sin(\omega_c t + \omega_f t + \varphi(t))$$

As an approximation to the behaviour of the loop filter we may consider only the difference frequency being passed with no phase change, which enables us to derive a small-signal model of the phase-locked loop. If we can make $\omega_f \approx \omega_c$, then the $\sin(\cdot)$ can be approximated by its argument resulting in: $y(t) = x_f(t) \simeq -A_c A_f \varphi(t)/2$. The phase-locked loop is said to be *locked* if this is the case.

CONTROL SYSTEM ANALYSIS/ CLOSED LOOP ANALYSIS OF PLL

Phase locked loops can also be analyzed as control systems by applying the Laplace transform. The loop response can be written as:

Where

- ζ_o is the output phase in radians
- ζ_i is the input phase in radians
- K_p is the phase detector gain in volts per radian
- K_v is the VCO gain in radians per volt-second
- $F(s)$ is the loop filter transfer function (dimensionless)

The loop characteristics can be controlled by inserting different types of loop filters. The simplest filter is a one-pole RC circuit. The loop transfer function in this case is:

$$F(s) = \frac{1}{1 + sRC}$$

The loop response becomes:

$$\frac{\theta_o}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + \frac{s}{RC} + \frac{K_p K_v}{RC}}$$

This is the form of a classic harmonic oscillator. The denominator can be related to that of a second order system:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

Where

- δ is the damping factor
- ω_n is the natural frequency of the loop

For the one-pole RC filter,

$$\omega_n = \sqrt{\frac{K_p K_v}{RC}}$$

$$\zeta = \frac{1}{2\sqrt{K_p K_v RC}}$$

The loop natural frequency is a measure of the response time of the loop, and the damping factor is a measure of the overshoot and ringing. Ideally, the natural frequency should be high and the damping factor should be near 0.707 (critical damping). With a single pole filter, it is not possible to control the loop frequency and damping factor independently. For the case of critical damping,

$$RC = \frac{1}{2K_p K_v}$$

$$\omega_c = K_p K_v \sqrt{2}$$

A slightly more effective filter, the lag-lead filter includes one pole and one zero. This can be realized with two resistors and one capacitor. The transfer function for this filter is

$$F(s) = \frac{1 + sCR_2}{1 + sC(R_1 + R_2)}$$

This filter has two time constants

$$\tau_1 = C(R_1 + R_2)$$

$$\tau_2 = CR_2$$

Substituting above yields the following natural frequency and damping factor

$$\omega_n = \sqrt{\frac{K_p K_v}{\tau_1}}$$

$$\zeta = \frac{1}{2\omega_n \tau_1} + \frac{\omega_n \tau_2}{2}$$

The loop filter components can be calculated independently for a given natural frequency and damping factor

$$\tau_1 = \frac{K_p K_v}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_p K_v}$$

Real world loop filter design can be much more complex eg using higher order filters to reduce various types or source of phase noise.

Applications of PLL:

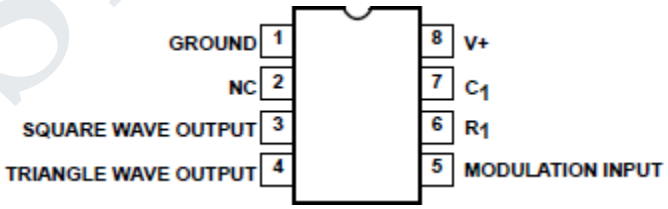
The PLL principle has been used in applications such as FM stereo decoders, motor speed control, tracking filters, FM modulation and demodulation, FSK modulation, Frequency multiplier, Frequency synthesis etc.,

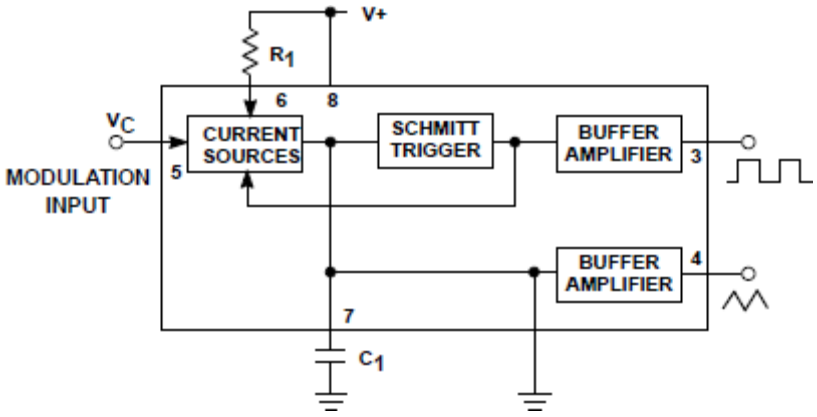
Example PLL ICs:

560 series (560, 561, 562, 564, 565 & 567)

VOLTAGE CONTROLLED OSCILLATOR:

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in figures below.





Referring to the circuit in the above figure, the capacitor c_1 is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_1 external to the IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_1 and thereby decreasing the charging current.

The voltage across the capacitor C_1 is applied to the inverting input terminal of Schmitt trigger via buffer amplifier. The output voltage swing of the Schmitt trigger is designed to V_{cc} and V_{cc}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of Schmitt trigger swings from 0.5 V_{cc} to 0.25 V_{cc}. When the voltage on the capacitor c_1 exceeds 0.5 V_{cc} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{cc}). The capacitor now discharges and when it is at 0.25 V_{cc}, the output of Schmitt trigger goes HIGH (V_{cc}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across c_1 which is also available at pin 4. The square wave output of the Schmitt trigger is inverted by buffer amplifier at pin 3. The output waveforms are shown near the pins 4 and 3.

The output frequency of the VCO can be given as follows:

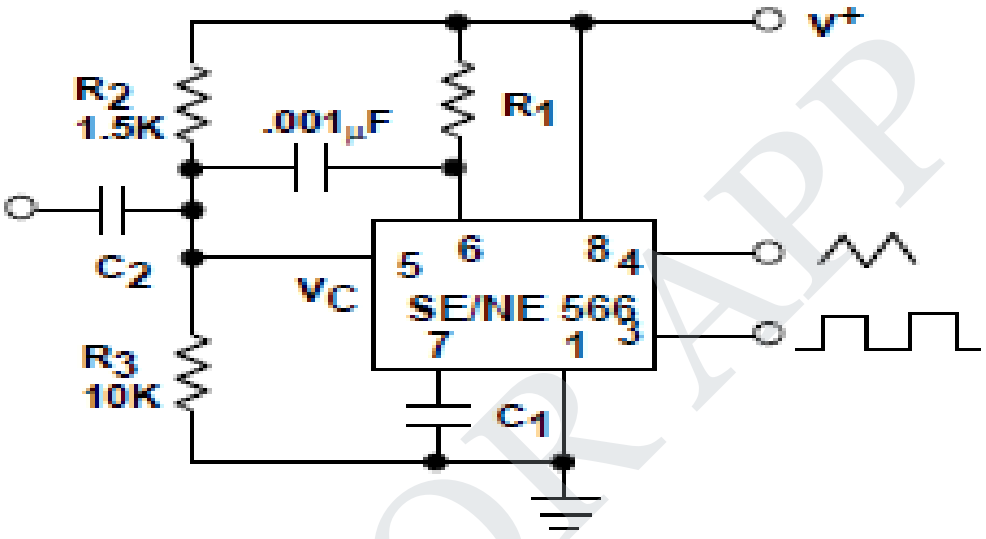
$$f_o = \frac{2\,[(V+) - (V_C)]}{R_1\, C_1\, V+}$$

where V+ is V_{cc}.

The output frequency of the VCO can be changed either by (i) R_1, (ii) c_1 or (iii) the voltage

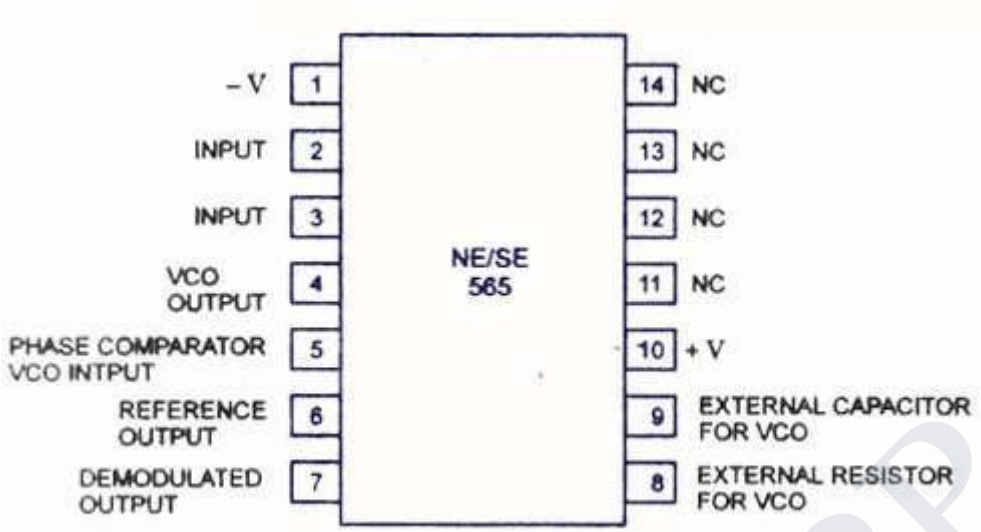
v_c at the modulating input terminal pin 5. The voltage v_c can be varied by connecting a R_1R_2 circuit

as shown in the figure below. The components $R_1$and c_1 are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{cc} to V_{cc} which can produce a frequency variation of about 10 to 1.



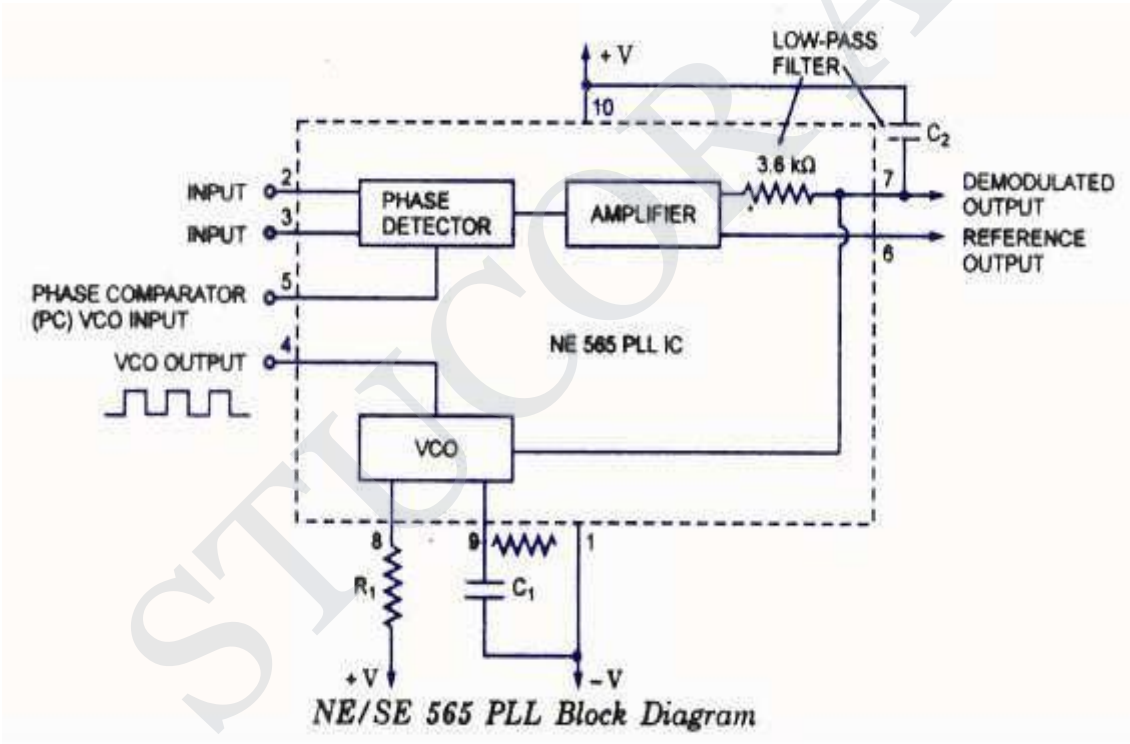
MONOLITHIC PHASE LOCKED LOOPS (PLL IC 565):

Pin Configuration of PLL IC 565:



14-Pin DIP Package

Basic Block Diagram Representation of IC 565



NE/SE 565 PLL Block Diagram

The signetics NE/SE 560 series is monolithic phase locked loops. The SE/NE 560, 561, 562, 564, 565 & 567 differ mainly in operating frequency range, poser supply requirements & frequency & bandwidth adjustment ranges. The important electrical characteristics of the 565 PLL

are,

- Operating frequency range: 0.001Hz to 500 Khz.
- Operating voltage range: ±6 to ±12v
- Input level required for tracking: 10mv rms min to 3 Vpp max
- Input impedance: 10 K ohms typically.
- Output sink current: 1mA
- Output source current: 10 mA

The center frequency of the PLL is determined by the free running frequency of the VCO, which is given by

$$f_{OUT} = \frac{1.2}{4R1C1} \text{ Hz} \text{ ---------- (1)}$$

where R1&C1 are an external resistor & a capacitor connected to pins 8 & 9.

- The VCO free-running frequency f_{OUT} is adjusted externally with R1 & C1 to be at the center of the input frequency range.
- C1 can be any value, R1 must have a value between 2 k ohms and 20 K ohms.
- Capacitor C2 connected between 7 & +V.
- The filter capacitor C2 should be large enough to eliminate variations in the demodulated output voltage in order to stabilize the VCO frequency.
- The lock range f_L & capture range fc of PLL is given by,

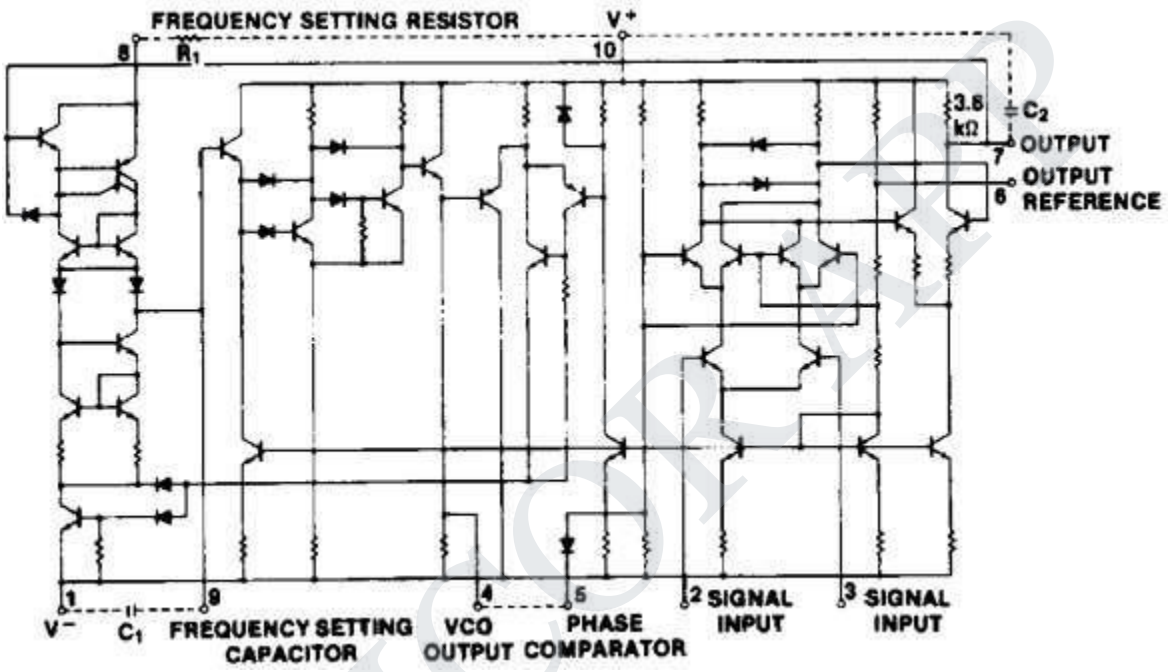
$$f_L = \pm \frac{8 \text{ fout}}{V} \text{ Hz} \text{ ---------- (2)}$$

Where f_{OUT} = free running frequency of VCO (Hz)

V = (+V)-(-V) volts

$$f_C = \pm\left[\frac{f_L}{(2\Pi)(3.6)(10^3)C_2}\right]^{1/2} \quad (3)$$

The circuit diagram of LM565 PLL



Monolithic PLL IC 565 applications:

The output from a PLL system can be obtained either as the voltage signal $v_c(t)$ corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator applications whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

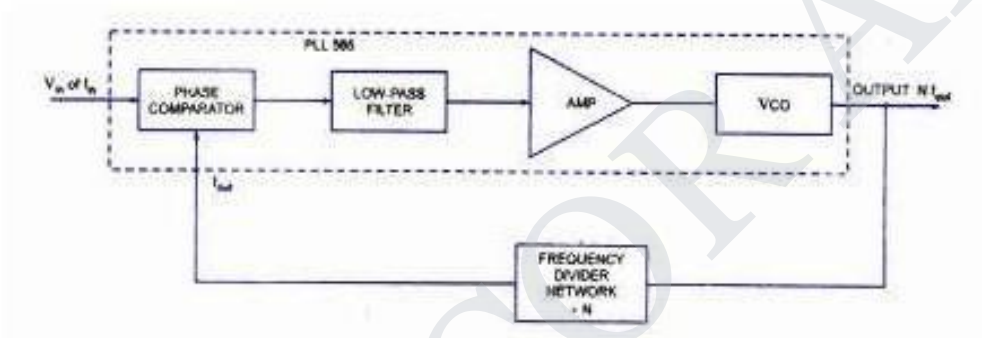
Consider the case of voltage output. When PLL is locked to an input frequency, the error voltage $v_c(t)$ is proportional to (f_s-f_o). If the input frequency is varied as in the case of FM signal, v_c will also vary in order to maintain the lock. Thus the voltage output serves as a frequency discriminator which converts the input frequency changes to voltage changes.

In the case of frequency output, if the input signal is comprised of many frequency components corrupted with noise and other disturbances, the PLL can be made to lock, selectively on one

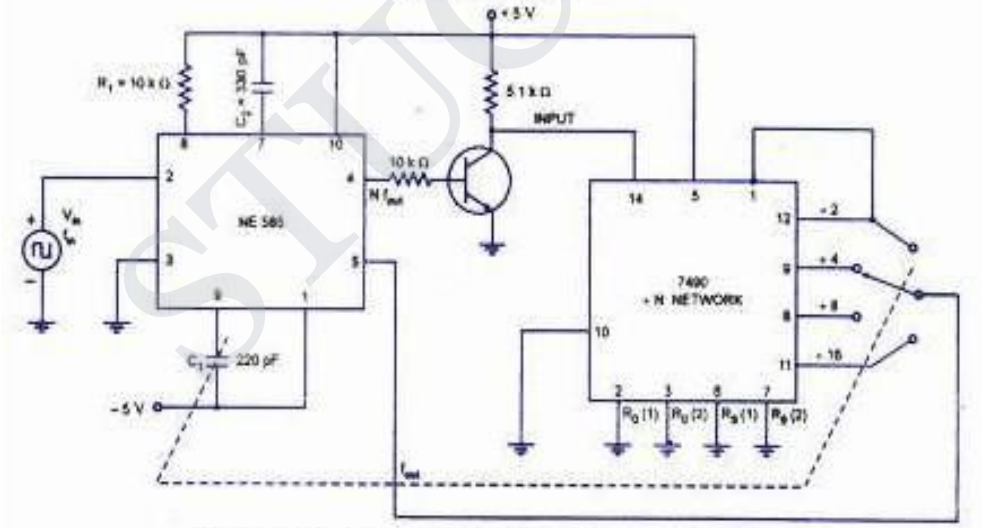
particular frequency component at the input. The output of VCO would then regenerate that particular frequency (because of LPF which gives output for beat frequency) and attenuate heavily other frequencies. VCO output thus can be used for regenerating or reconditioning a desired frequency signal (which is weak and buried in noise) out of many undesirable frequency signals. Some of the typical applications of PLL are discussed below.

(i)Frequency Multiplier:

- Frequency divider is inserted between the VCO & phase comparator. Since the output of the divider is locked to the f_{IN}, VCO is actually running at a multiple of the input frequency.
- The desired amount of multiplication can be obtained by selecting a proper divide-by-N network, where N is an integer.



(a) Block Diagram

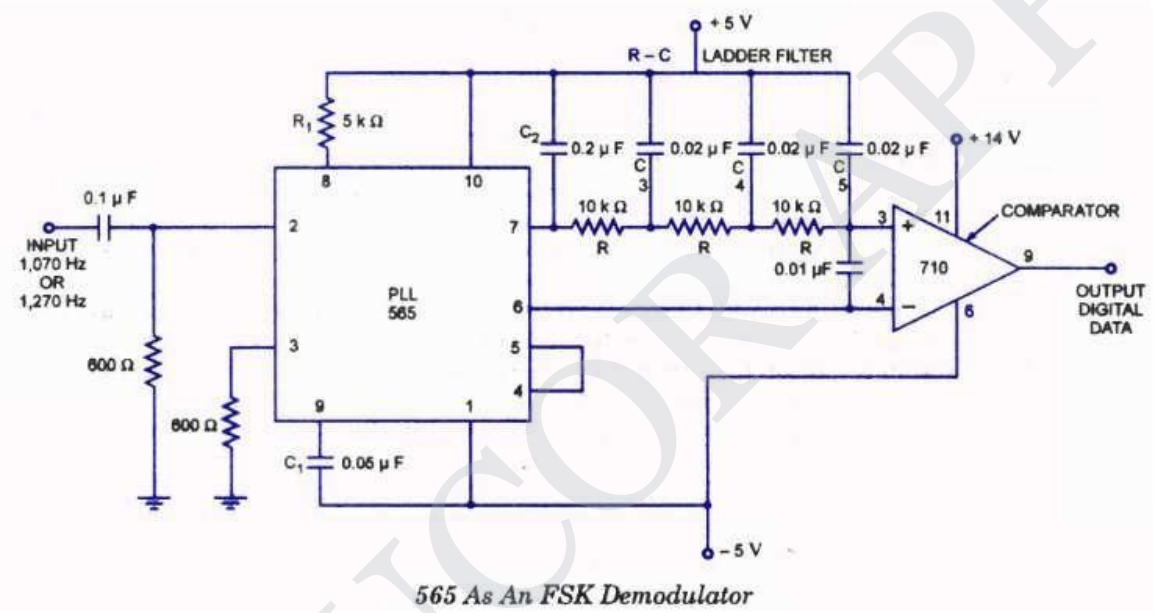


(b) Connection Diagram For Multiple 4 Frequency Multiplier

(ii) Frequency Shift Keying (FSK) demodulator:

In computer peripheral & radio (wireless) communication the binary data or code is transmitted by means of a carrier frequency that is shifted between two preset frequencies. Since a carrier frequency is shifted between two preset frequencies, the data transmission is said to use a FSK. The frequency corresponding to logic 1 & logic 0 states are commonly called the mark & space frequency.

For example, When transmitting teletype writer information using a modulator-demodulator (modem) a 1070-1270 (mark-space) pair represents the originate signal, while a 2025-2225 Hz (mark-space) pair represents the answer signal.



565 As An FSK Demodulator

FSK Generator:

- The FSK generator is formed by using a 555 as an astable multivibrator, whose frequency is controlled by the sate of transistor Q1.
- In other words, the output frequency of the FSK generator depends on the logic state of the digital data input.
- 150 Hz is one the standards frequencies at which the data are commonly transmitted.
- When the input is logic 1, the transistor Q1 is off. Under the condition, 555 timer works in its normal mode as an astable multivibrator i.e., capacitor C charges through R_A & R_B to 2/3 Vcc & discharges through R_B to 1/3 Vcc.

  Thus capacitor C charges & discharges between 2/3 Vcc & 1/3 Vcc as long as the input is logic 1.

- The frequency of the output waveform is given by,

$$fo = \frac{1.45}{(R_A + 2R_B)C} = 1070 \text{ Hz (mark frequency)}$$

- When the input is logic 0, (Q1 is ON saturated) which inturn connects the resistance Rc across R_A. This action reduces the charging time of capacitor C1 increases the output frequency, which is given by,

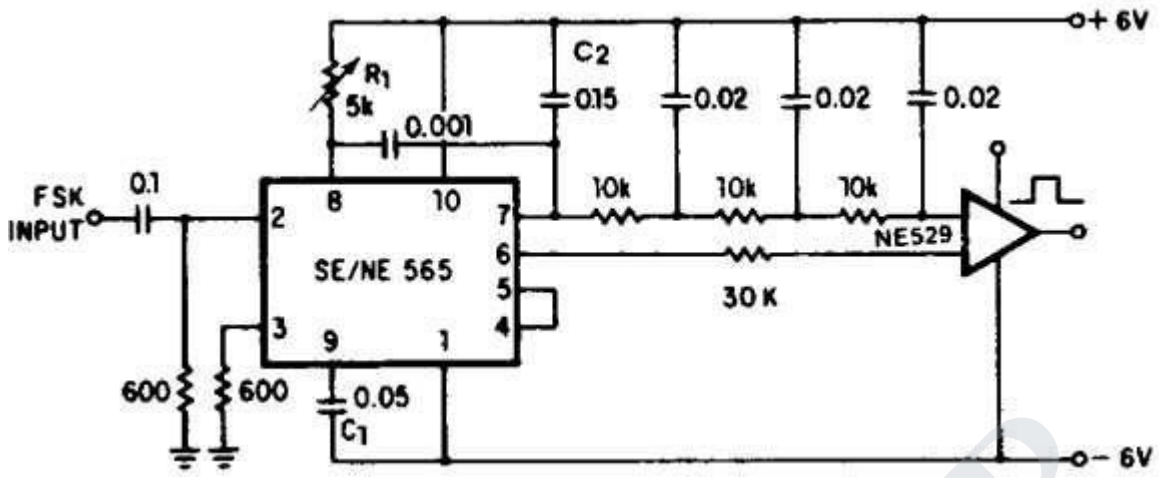
$$fo = \frac{1.45}{(R_A \parallel R_C + 2R_B)C} = 1270 \text{ Hz (space frequency)}$$

- By proper selection of resistance Rc, this frequency is adjusted to equal the space frequency of 1270 Hz. The difference between the FSK signals of 1070 Hz & 1270 Hz is 200 Hz, this difference is called ‐frequency shift‖.
- The output 150 Hz can be made by connecting a voltage comparator between the output of the ladder filter and pin 6 of PLL.
- The VCO frequency is adjusted with R1 so that at f_{IN} = 1070 Hz.

FSK Demodulator:

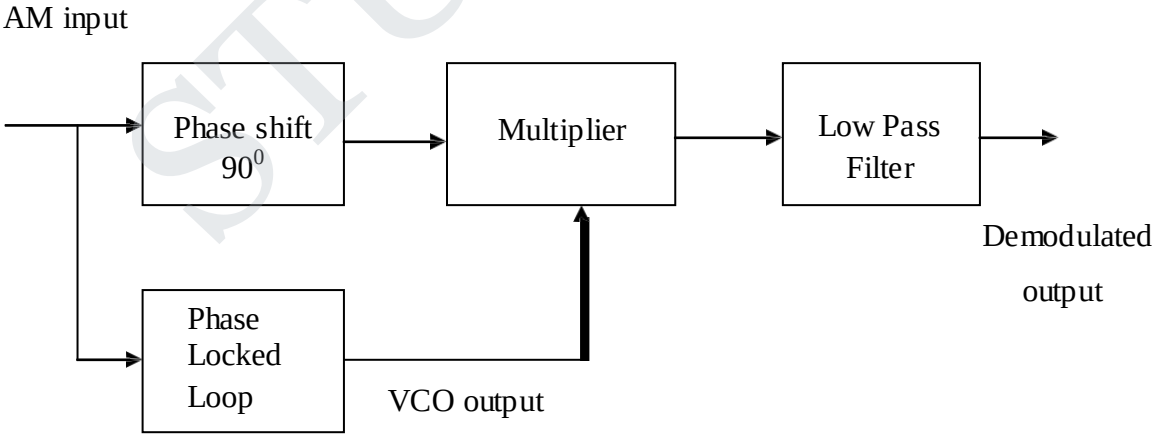
- The output of 555 FSK generator is applied to the 565 FSK demodulator.
- Capacitive coupling is used at the input to remove dc line.
- At the input of 565, the loop locks to the input frequency & tracks it between the 2 frequencies.
- R1 & C1 determine the free running frequency of the VCO, 3 stage RC ladder filter is used to remove the carrier component from the output.

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using FSK demodulator. The figure below shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.



(iii) AM Demodulation:

A PLL may be used to demodulate AM signals as shown in the figure below. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90^0 before being fed to the multiplier. This makes both the signals applied to the multiplier and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.



(iv) FM Demodulation:

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

(v) frequency multiplication/division:

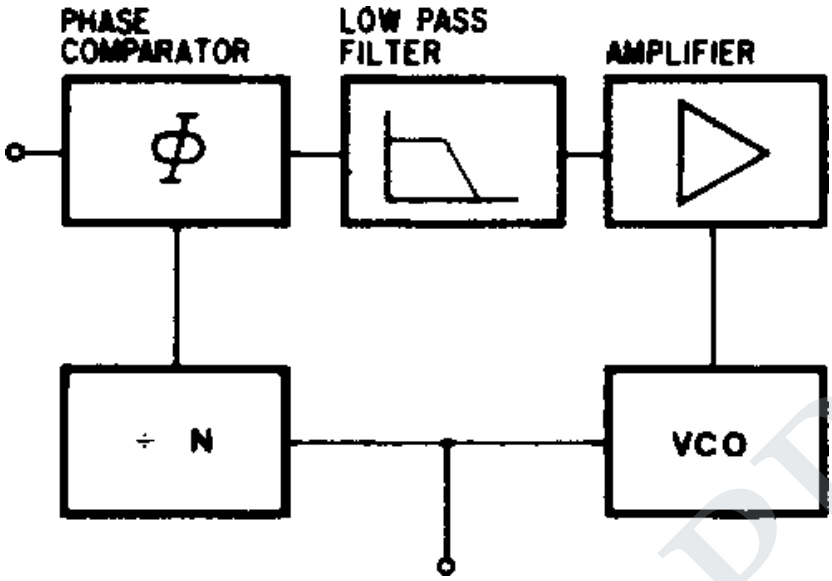
The block diagram shown below shows a frequency multiplier/divider using PLL. A divide by N network is inserter between the VCO output and the phase comparator input. In the locked state, the VCO output frequency f_o is given by

$f_o = Nf_s$. The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics e.g. square wave, pulse train etc., then the VCO can be directly locked to the n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n. Typically n is kept less than 10.

The circuit of the figure above can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output fo of VCO is now given by

$f_o = f_s/m$

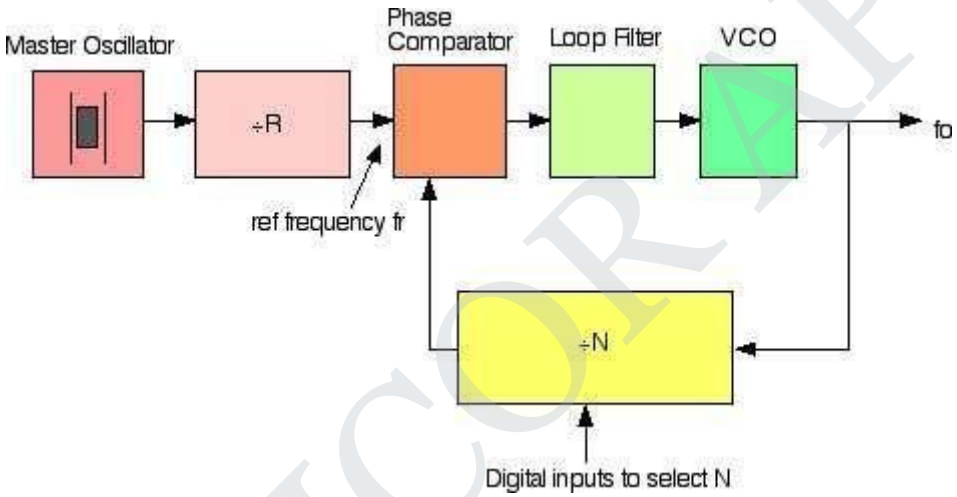


(vi) PLL Frequency Synthesis:

In digital wireless communication systems (GSM, CDMA etc), PLL's are used to provide the Local Oscillator (LO) for up-conversion during transmission, and down-conversion during reception. In most cellular handsets this function has been largely integrated into a single integrated circuit to reduce the cost and size of the handset. However due to the high performance required of base station terminals, the transmission and reception circuits are built with discrete components to achieve the levels of performance required. GSM LO modules are typically built with a Frequency Synthesizer integrated circuit, and discrete resonator VCO's.

Frequency Synthesizer manufacturers include Analog Devices, National Semiconductor and Texas Instruments. VCO manufacturers include Sirenza, Z-Communications, Inc. (Z-COMM) Principle of PLL synthesizers

A phase locked loop does for frequency what the Automatic Gain Control does for voltage. It compares the frequencies of two signals and produces an error signal which is proportional to the difference between the input frequencies. The error signal is then low pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop. If the output frequency drifts, the error signal will increase, driving the frequency in the opposite direction so as to reduce the error. Thus the output is *locked* to the frequency at the other input. This input is called the reference and is derived from a crystal oscillator, which is very stable in frequency. The block diagram below shows the basic elements and arrangement of a PLL based frequency synthesizer.



The key to the ability of a frequency synthesizer to generate multiple frequencies is the divider placed between the output and the feedback input. This is usually in the form of a digital counter, with the output signal acting as a clock signal. The counter is preset to some initial count value, and counts down at each cycle of the clock signal. When it reaches zero, the counter output changes state and the count value is reloaded. This circuit is straightforward to implement using flip-flops, and because it is digital in nature, is very easy to interface to other digital components or a microprocessor. This allows the frequency output by the synthesizer to be easily controlled by a digital system.

Example:

Suppose the reference signal is 100 kHz, and the divider can be preset to any value between 1 and 100. The error signal produced by the comparator will only be zero when the output of the divider is also 100 kHz. For this to be the case, the VCO must run at a frequency which is 100 kHz x the divider count value. Thus it will produce an output of 100 kHz for a count of 1, 200 kHz for a count of 2, 1 MHz for a count of 10 and so on. Note that only whole multiples of the reference frequency can be obtained with the simplest integer N dividers. Fractional N dividers are readily available

Practical considerations:

In practice this type of frequency synthesizer cannot operate over a very wide range of frequencies, because the comparator will have a limited bandwidth and may suffer from aliasing problems. This would lead to false locking situations, or an inability to lock at all. In addition, it is hard to make a high frequency VCO that operates over a very wide range. This is due to several factors, but the primary restriction is the limited capacitance range of varactor diodes. However, in most systems where a synthesiser is used, we are not after a huge range, but rather a finite number over some defined range, such as a number of radio channels in a specific band.

Many radio applications require frequencies that are higher than can be directly input to the digital counter. To overcome this, the entire counter could be constructed using high-speed logic such as ECL, or more commonly, using a fast initial division stage called a *prescaler* which reduces the frequency to a manageable level. Since the prescaler is part of the overall division ratio, a fixed prescaler can cause problems designing a system with narrow channel spacings - typically encountered in radio applications. This can be overcome using a dual-modulus prescaler.[11]

Further practical aspects concern the amount of time the system can switch from channel to channel, time to lock when first switched on, and how much noise there is in the output. All of these are a function of the *loop filter* of the system, which is a low-pass filter placed between the output of the frequency comparator and the input of the VCO. Usually the output of a frequency comparator is in the form of short error pulses, but the input of the VCO must be a smooth noise-

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free DC voltage. (Any noise on this signal naturally causes frequency modulation of the VCO.).

Heavy filtering will make the VCO slow to respond to changes, causing drift and slow response time, but light filtering will produce noise and other problems with harmonics. Thus the design of the filter is critical to the performance of the system and in fact the main area that a designer will concentrate on when building a synthesizer system.

UNIT-V
LINEAR REGULATORS

- All electronic circuits need a dc power supply for their operation. To obtain this dc voltage from 230 V ac mains supply, we need to use rectifier.
- Therefore the filters are used to obtain a -steady‖ dc voltage from the pulsating one.
- The filtered dc voltage is then applied to a regulator which will try to keep the dc output voltage constant in the event of voltage fluctuations or load variation.
- We know the combination of rectifier & filter can produce a dc voltage. But the problem with this type of dc power supply is that its output voltage will not remain constant in the event of fluctuations in an ac input or changes in the load current(I_L).
- The output of unregulated power supply is connected at the input of voltage regulator circuit.
- The voltage regulator is a specially designed circuit to keep the output voltage constant.
- It does not remain exactly constant. It changes slightly due to changes in certain parameters.

Factors affecting the output voltage:

i) I_L (Load Current)

ii) V_{IN} (Input Voltage)

iii) T (Temperature)

IC Voltage Regulators:

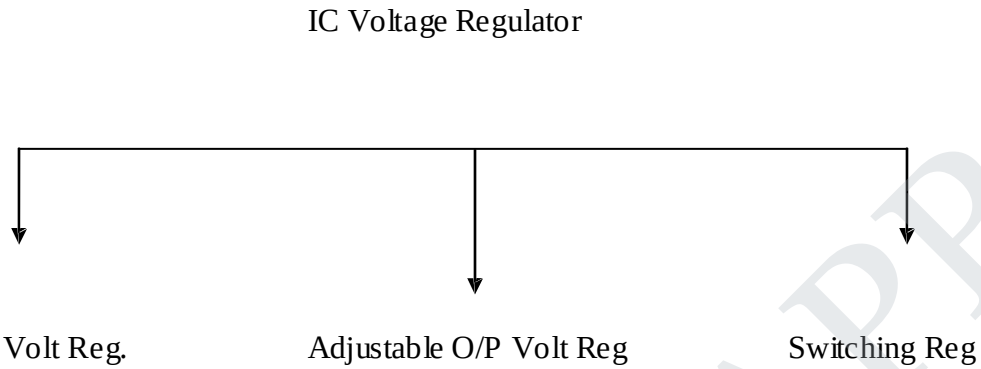
They are basically series regulators with all the basic blocks present inside the IC. Therefore it is easier to use IC voltage regulator instead of discrete voltage regulators.

Important features of IC Regulators:

1. Programmable output
2. Facility to boost the voltage/current
3. Internally provided short circuit current limiting

4. Thermal shutdown
5. Floating operation to facilitate higher voltage output

Classifications of IC voltage regulators:



- Fixed & Adjustable output Voltage Regulators are known as Linear Regulator.
- A series pass transistor is used and it operates always in its active region.

Switching Regulator:

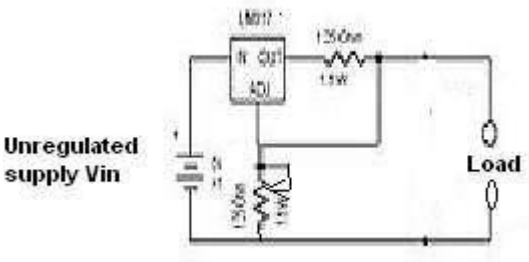
1. Series Pass Transistor acts as a switch.
2. The amount of power dissipation in it decreases considerably.
3. Power saving result is higher efficiency compared to that of linear.

Adjustable Voltage Regulator:

Advantages of Adjustable Voltage Regulator over fixed voltage regulator are,

1. Adjustable output voltage from 1.2v to 57 v
2. Output current 0.10 to 1.5 A
3. Better load & line regulation
4. Improved overload protection
5. Improved reliability under the 100% thermal overloading

Adjustable Positive Voltage Regulator (LM317):



- LM317 series adjustable 3 terminal positive voltage regulator, the three terminals are Vin, Vout & adjustment (ADJ).
- LM317 requires only 2 external resistors to set the output voltage.
- LM317 produces a voltage of 1.25v between its output & adjustment terminals. This voltage is called as Vref.
- Vref (Reference Voltage) is a constant, hence current I1 flows through R1 will also be constant. Because resistor R1 sets current I1. It is called -current set‖ or -program resistor‖.
- Resistor R2 is called as -Output set‖ resistors, hence current through this resistor is the sum of I1 & Iadj
- LM317 is designed in such as that Iadj is very small & constant with changes in line voltage & load current.
- The output voltage Vo is, Vo=R1I1+(I1+Iadj)R2 ----------(1)

Where I1= Vref/R1

Vo =(Vref/R1)R1 + Vref/R1 + Iadj R2

= Vref + (Vref/R1)R2 + Iadj R2

Vo = Vref [1 + R2/R1] + Iadj R2 ----------(2)

R1 = Current (I1) set resistor

R2 = output (Vo) set resistor

Vref = 1.25v which is a constant voltage between output and ADJ terminals.

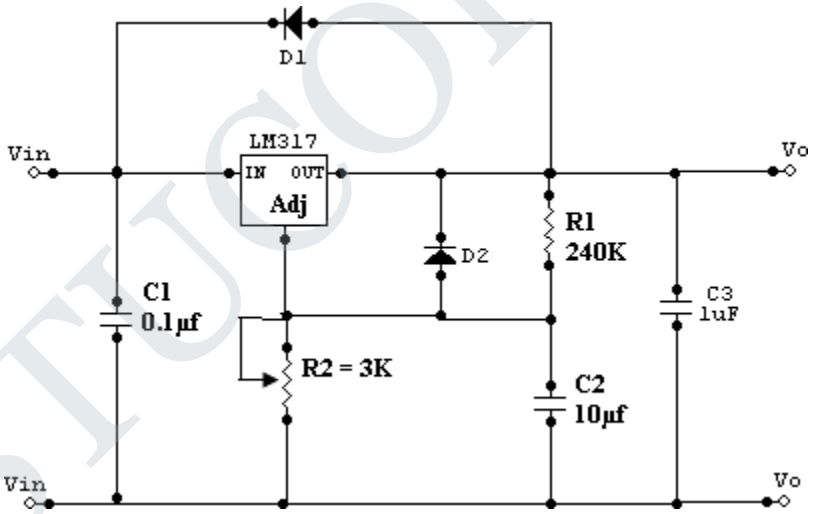
- Current Iadj is very small. Therefore the second term in (2) can be neglected.
- Thus the final expression for the output voltage is given by

$$Vo = 1.25v[1 + R2/R1] \text{ ----------(3)}$$

Eqn (3) indicates that we can vary the output voltage by varying the resistance R2.

The value of R1 is normally kept constant at 240 ohms for all practical applications.

Practical Regulator using LM317:



- If LM317 is far away from the input power supply, then 0.1µf disc type or 1µf tantalum capacitor should be used at the input of LM317.
- The output capacitor Co is optional. Co should be in the range of 1 to 1000µf.

- The adjustment terminal is bypassed with a capacitor C2 this will improve the ripple rejection ratio as high as 80 dB is obtainable at any output level.
- When the filter capacitor is used, it is necessary to use the protective diodes.
- These diodes do not allow the capacitor C2 to discharge through the low current point of the regulator.
- These diodes are required only for high output voltages (above 25v) & for higher values of output capacitance 25µf and above.

IC 723 – GENERAL PURPOSE REGULATOR

Disadvantages of fixed voltage regulator:

1. Do not have the shot circuit protection
2. Output voltage is not adjustable

These limitations can be overcomes in IC723.

Features of IC723:

1. Unregulated dc supply voltage at the input between 9.5V & 40V
2. Adjustable regulated output voltage between 2 to 3V.
3. Maximum load current of 150 mA (I_{Lmax} = 150mA).
4. With the additional transistor used, I_{Lmax} upto 10A is obtainable.
5. Positive or Negative supply operation
6. Internal Power dissipation of 800mW.
7. Built in short circuit protection.
8. Very low temperature drift.
9. High ripple rejection.

The simplified functional block diagram can be divided in to 4 blocks.

1. Reference generating block
2. Error Amplifier
3. Series Pass transistor
4. Circuitry to limit the current

1. Reference Generating block:

The temperature compensated Zener diode, constant current source & voltage reference amplifier together from the reference generating block. The Zener diode is used to generate a fixed reference voltage internally. Constant current source will make the Zener diode to operate at affixed point & it is applied to the Non – inverting terminal of error amplifier. The Unregulated input voltage ±Vcc is applied to the voltage reference amplifier as well as error amplifier.

2. Error Amplifier:

Error amplifier is a high gain differential amplifier with 2 input (inverting & Non-inverting). The Non-inverting terminal is connected to the internally generated reference voltage. The Inverting terminal is connected to the full regulated output voltage.

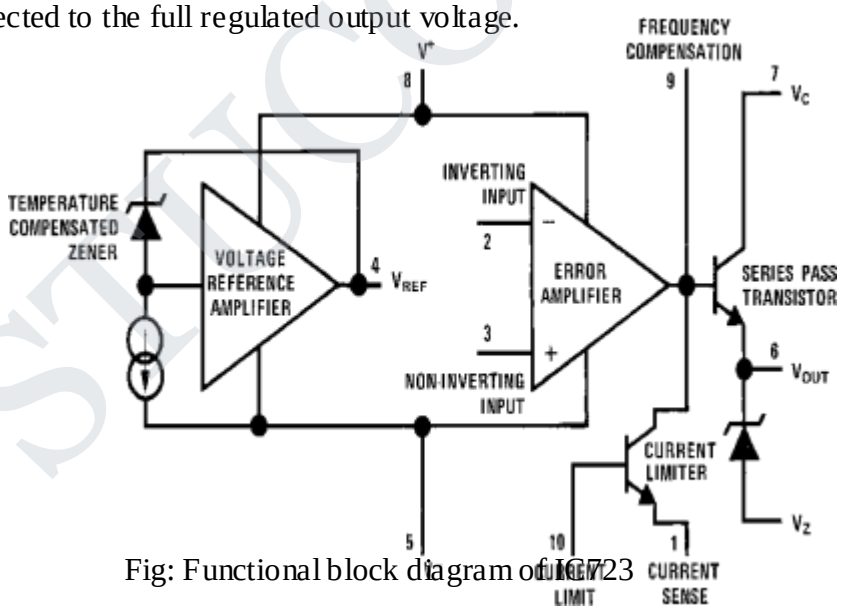


Fig: Functional block diagram of IC723

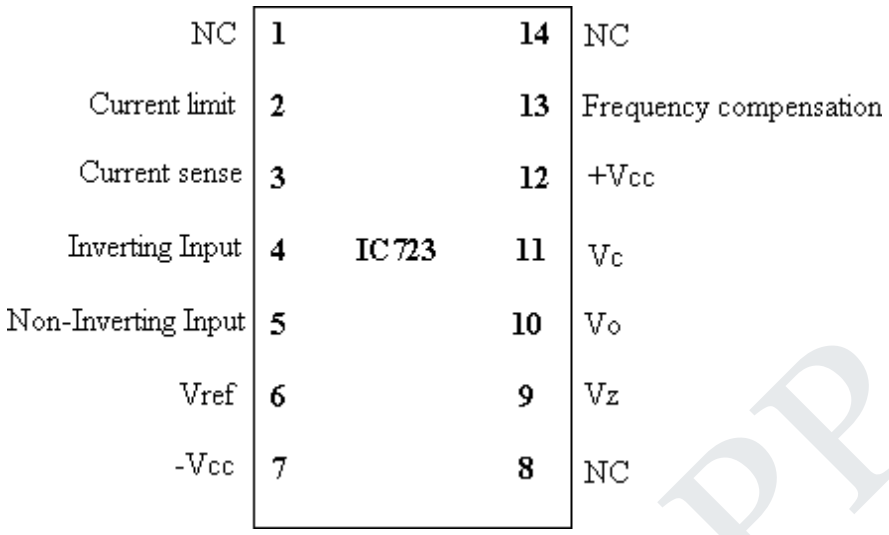


Fig : Pin diagram of IC723

3. Series Pass Transistor:

Q1 is the internal series pass transistor which is driven by the error amplifier. This transistor actually acts as a variable resistor & regulates the output voltage. The collector of transistor Q1 is connected to the Un-regulated power supply. The maximum collector voltage of Q1 is limited to 36Volts. The maximum current which can be supplied by Q1 is 150mA.

4. Circuitry to limit the current:

The internal transistor Q2 is used for current sensing & limiting. Q2 is normally OFF transistor. It turns ON when the I_L exceeds a predetermined limit.

- Low voltage , Low current is capable of supplying load voltage which is equal to or between 2 to 7Volts.

V_{load} = 2 to 7V

I_{load} = 150mA

IC723 as a LOW voltage LOW current :

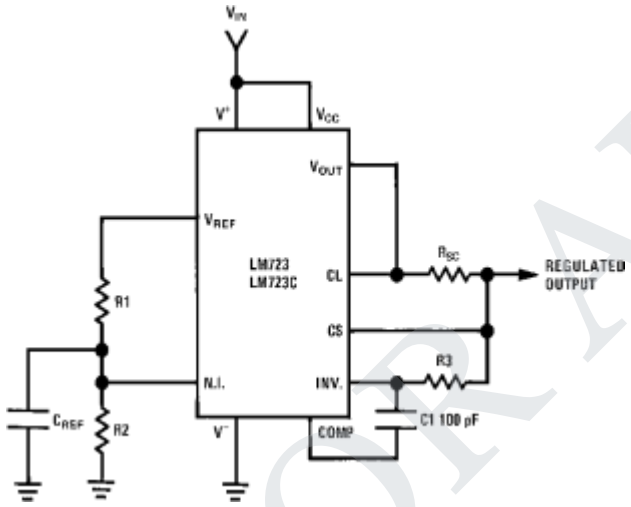


Fig: Typical circuit connection diagram

- R1 & R2 from a potential divider between Vref & Gnd.
- The Voltage across R2 is connected to the Non – inverting terminal of the regulator IC

$$V_{non\text{-}inv} = \frac{R2}{R1 \square R2} \; Vref$$

- Gain of the internal error amplifier is large

$$V_{non\text{-}inv} = V_{in}$$

- Therefore the Vo is connected to the Inverting terminal through R3 & R_{SC} must also be equal to $V_{non\text{-}inv}$

$$V_o = V_{non\text{-}inv} = \frac{R2}{R1 \square R2} \; Vref$$

R1 & R2 can be in the range of 1 KΩ to 10KΩ & value of R3 is given by

$$R3 = R1 \,||\, R2 = \frac{R1R2}{R \square R2}$$

- Rsc (current sensing resistor) is connected between Cs & C_L. The voltage drop across Rsc is proportional to the I_L.
- This resistor supplies the output voltage in the range of 2 to 7 volts, but the load current can be higher than 150mA.
- The current sourcing capacity is increased by including a transistor Q in the circuit.

- The output voltage , $V_o = \frac{R2}{R1 \square R2} \; Vref$

IC723 as a HIGH voltage LOW Current:

- This circuit is capable of supplying a regulated output voltage between the range of 7 to 37 volts with a maximum load current of 150 mA.
- The Non – inverting terminal is now connected to Vref through resistance R3.
- The value of R1 & R2 are adjusted in order to get a voltage of Vref at the inverting terminal at the desired output.

$$Vin = Vref = \frac{R2}{R1 \square R2} Vo$$

$$Vo = \frac{R1 \square R2}{R2} Vref$$

Or

$$Vo = [1 + \frac{R1}{R2}] Vref$$

IC723 as a HIGH voltage HIGH Current:

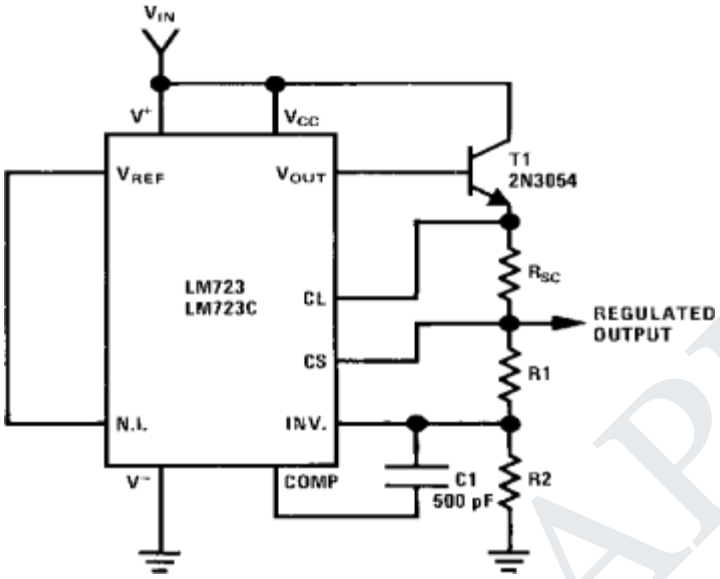


Fig: Typical circuit connection diagram

- An external transistor Q is added in the circuit for high voltage low current regulator to improve its current sourcing capacity.
- For this circuit the output voltage varies between 7 & 37V.
- Transistor Q increase the current sourcing capacity thus $I_{L(MAX)}$ ia greater than 150mA.
- The output voltage Vo is given by,

$$V0=(R2/R1+R2)Vref$$

- The value of Rsc is given by $Rsc = \frac{0.6}{ILimit}$

SWITCHING REGULATOR:

An example of general purpose regulator is Motorola's MC1723. It can be used in many different ways, for example, as a fixed positive or negative output voltage regulator, variable regulator or switching regulator because of its flexibility.

To minimize the power dissipation during switching, the external transistor used must be a switching power transistor.

To improve the efficiency of a regulator, the series pass transistor is used as a switch rather than as a variable resistor as in the linear mode.

- A regulator constructed to operate in this manner is called a series switching regulator. In such regulators the series pass transistor is switched between cut off & saturation at a high frequency which produces a pulse width modulated (PWM) square wave output.
- This output is filtered through a low pass LC filter to produce an average dc output voltage.
    - Thus the output voltage is proportional to the pulse width and frequency.
    - The efficiency of a series switching regulator is independent of the input & output differential & can approach 95%

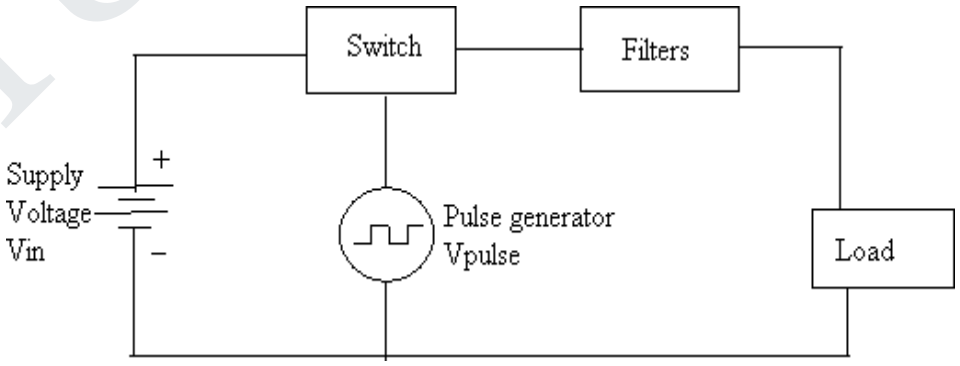


Fig : Basic Switching regulator

A basic switching regulator consists of 4 major components,

1. Voltage source Vin
2. Switch S1
3. Pulse generator Vpulse
4. Filter F1

1. Voltage Source Vin:

It may be any dc supply – a battery or an unregulated or a regulated voltage. The voltage source must satisfy the following requirements.

- It must supply the required output power & the losses associated with the switching regulator.
- It must be large enough to supply sufficient dynamic range for line & load regulations.
- It must be sufficiently high to meet the minimum requirement of the regulator system to be designed.
- It may be required to store energy for a specified amount of time during power failures.

2. Switch S1:

It is typically a transistor or thyristor connected as a power switch & is operated in the saturated mode. The pulse generator output alternately turns the switch ON & OFF

3. Pulse generator Vpulse:

It provides an asymmetrical square wave varying in either frequency or pulse width called frequency modulation or pulse width modulation respectively. The most effective frequency range for the pulse generator for optimum efficiency 20 KHz. This frequency is inaudible to the human ear & also well within the switching speeds of most inexpensive transistors & diodes.

- The duty cucly of the pulse wave form determines the relationship between the input & output voltages. The duty cycle is the ratio of the on time ton, to the period T of the pulse waveform.

$$\text{Duty cycle} = \frac{ton}{ton + toff}$$

- Switching regulator can operate in any of 3 modes

$$= \frac{ton}{T} = \text{ton f.}$$

Where ton = On-time of the pulse waveform
toff=off-time of the pulse wave form

T = time period = ton + toff
= 1/frequency or
T = 1/f

- Typical operating frequencies of switching regulator range from 10 to 50khz.
- Lower operating frequency improve efficiency & reduce electrical noise, but require large filter components (inductors & capacitors).

4. Filter F1:

It converts the pulse waveform from the output of the switch into a dc voltage. Since this switching mechanism allows a conversion similar to transformers, the switching regulator is often referred to as a dc transformer.

The output voltage Vo of the switching regulator is a function of duty cycle & the input voltage Vin.

Vo is expressed as follows,

$$Vo = \frac{ton}{T} Vin$$

- This equation indicates that, if time period T is constant, Vo is directly proportional to the ON-time, ton for a given value of Vin. This method of changing the output voltage by varying ton is referred to as a pulse width modulation.
- Similarly, if ton is held constant, the output voltage Vo is inversely proportional to the period T or directly proportional to the frequency of the pulse waveform. This method of varying the output voltage is referred to as frequency modulation (FM).

i) Step – Down
ii) Step – Up
iii) Polarity inverting

MONOLITHIC SWITCHING REGULATOR [µA78S40]:

The µA78S40 consists of a temperature compensated voltage reference, duty cycle controllable oscillator with an active current limit circuit, a high gain comparator, a high- current, high voltage output switch, a power switching diode & an uncommitted op-amp.

Important features of the µA78S40 switching regulators are:

- Step up, down & Inverting operation
- Operation from 2.5 to 40V input
- 80dB line & load regulations

- Output adjustable from 1.3 to 40V
- Peak current to 1.5A without external resistors
- Variable frequency, variable duty cycle device

The internal switching frequency is set by the timing capacitor C_T, connected between pin12 & ground pin 11. the initial duty cycle is 6:1. The switching frequency & duty cycle can be modified by the current limit circuitry, I_{PK}sense, pin14, 7 the comparator, pin9 & 10.

Comparator:

The comparator modifies the OFF time of the output switch transistor Q1 & Q2. In the step – up & step down modes, the non-inverting input(pin9) of the comparator is connected to the voltage reference of 1.3V (pin8) & the inverting input (pin10) is connected to the output terminal via the voltage divider network.

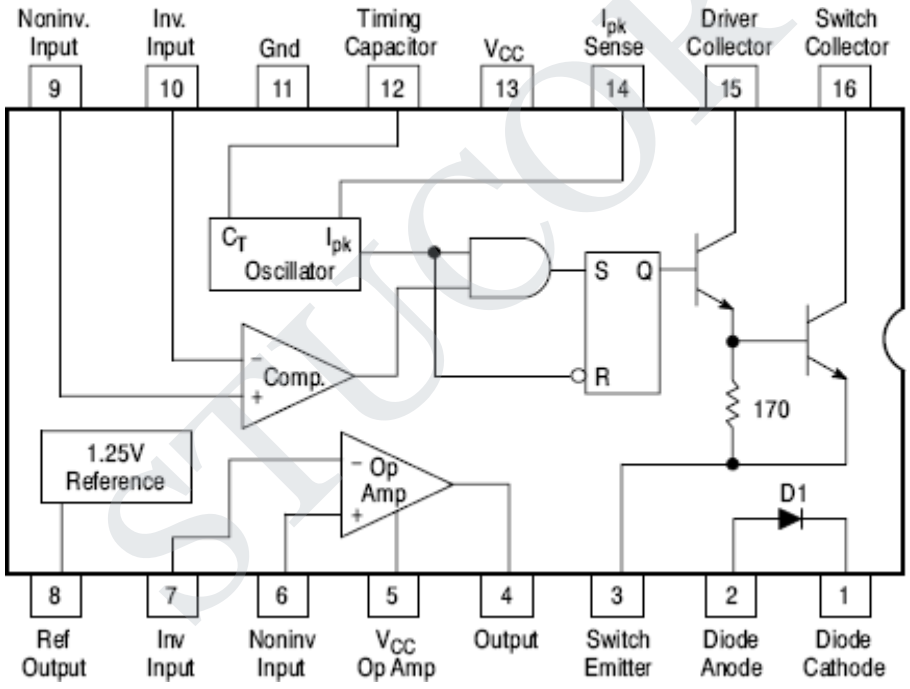
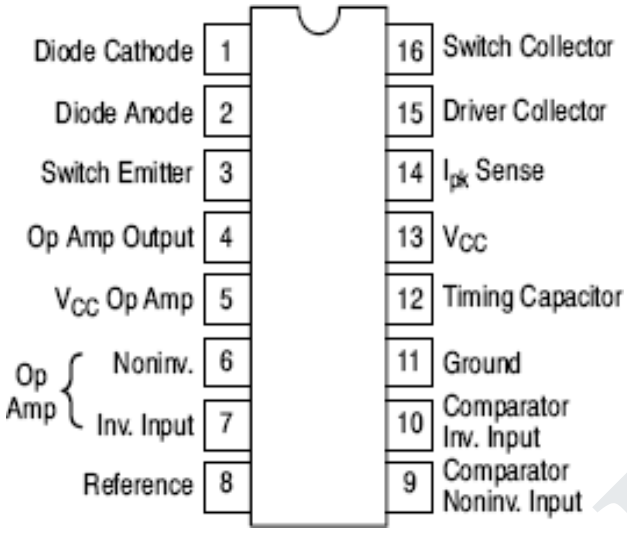


Fig: Functional block diagram of µA78S40



- In the Inverting mode the non – inverting input is connected to both the voltage reference & the output terminal through 2 resistors & the inverting terminal is connected to ground.
- When the output voltage is correct, the comparator output is in high state & has no effect on the circuit operation.
- However, if the output is too high & the voltage at the inverting terminal is higher than that at the non-inverting terminal , then the comparator output goes low.
- In the LOW state the comparator inhibits the turn on of the output switching transistors. This means that, as long as the comparator output is low, the system is in off time.
- As the output current rises or the output voltage falls, the off time of the system decreases.
- Consequently, as the output current nears its maximum Io_{MAX}, the off time approaches its minimum value.

In all 3 modes (Step down, step up, Inverting), the current limit circuit is completed by connecting a sense resistor Rsc, between I_{PK} sense & Vcc.

- The current limit circuit is activated when a 330mV potential appears across Rsc.
- Rsc is selected such that 330mV appears across it when the desired peak current I_{PK},

flows through it.

- When the peak current is reached, the current limit circuit is turned on.
- The forward voltage drop, V_D, across the internal power diode is used to determine the value of inductor L off time & efficiency of the switching regulator.
- Another important quantity used in the design of a switching regulator is the saturation voltage Vs

✓ In the step down mode an -output saturation voltⅱ is 1.1V typical, $1.3V_{MAX}$.

✓ In the step up mode an -Output saturation voltⅱ is 0.45V typical, 0.7 maximum.

$$Rsc = \frac{330mV}{DesiredPeakCurrent}$$

✓ The desired peak current value is reached, the current limiting circuit turns ON & immediately terminates the ON time & starts OFF time.

- As we increase I_L (load current), Vout will decreased, to compensate for this, the ON time of the output is increased automatically.
- If the I_L decreased then Vout increased, to compensate for this, the OFF time of the output is increased automatically.

(i) Step – Down Switching Regulator:

- C_T is the timing capacitor which decides the switching frequency.
- Rsc is the current sensing resistance. Its value is given by

$$Rsc = \frac{330mV}{DesiredPeakCurrent}$$

- The Non-inverting terminal of the internal op-amp(pin9) is connected to the 1.3V reference (pin8).
- Resistances R1 & R2 from a potential divider, across the output voltage Vo. Their value should be such that the potential at the inverting input of the op-amp should be equal to 1.3V ref when Vo is at its desired level.

- $V_{(-)} = 1.3V = \frac{R2}{R1 \square R2} Vo$

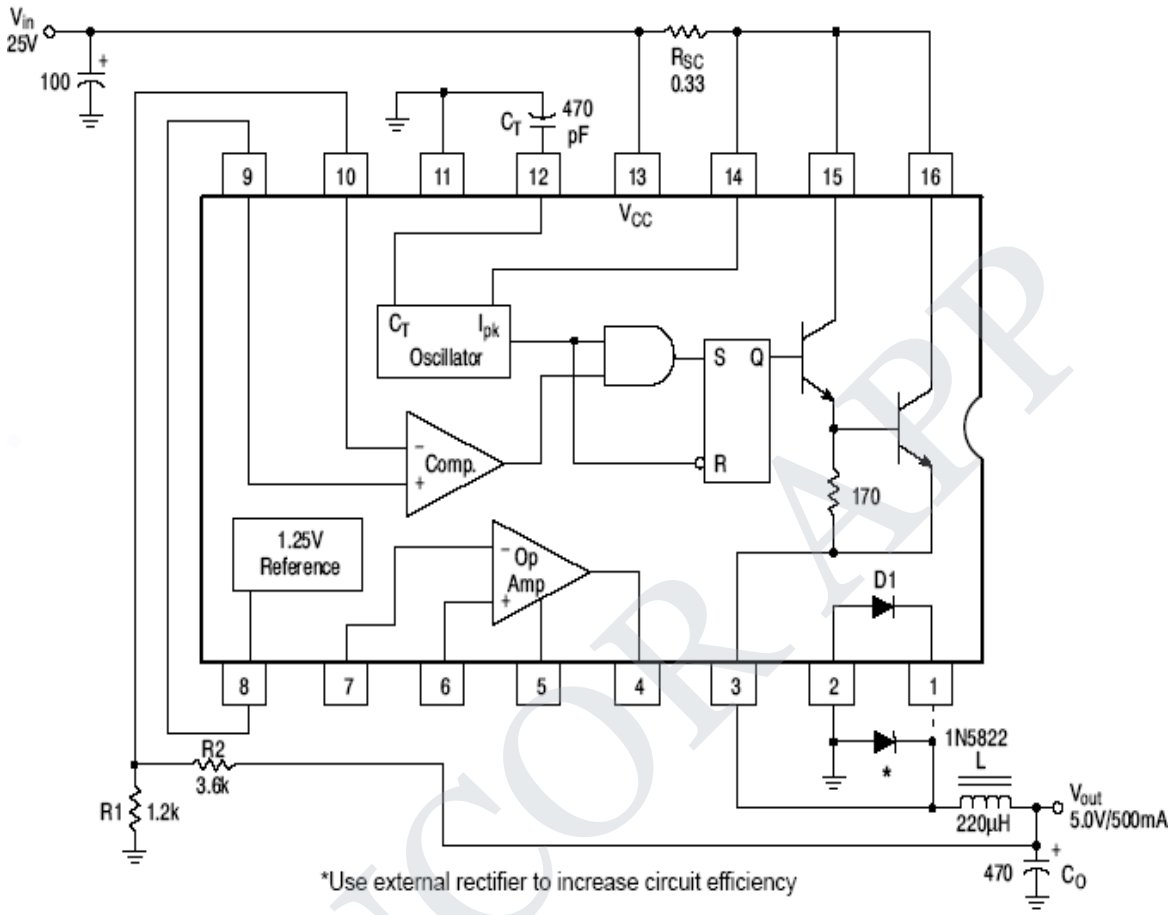


Figure 6. Step–Down Converter

(ii) Step – Up Switching Regulator:

- Note that inductor is connected between the collectors of Q1 & Q2.
- When Q1 is ON, the output is shorted & the collector current of Q1 flows through L.
- The diode D1 is reverse biased & Co supplies the load current.

- The inductor stores the energy. When the Q1 is turned OFF, there is a self induced emf that appears across the inductor with polarities.
- The output voltage is given by,

$$Vo = Vin + V_L$$

- Hence it will be always higher than Vin & step up operation is achieved.

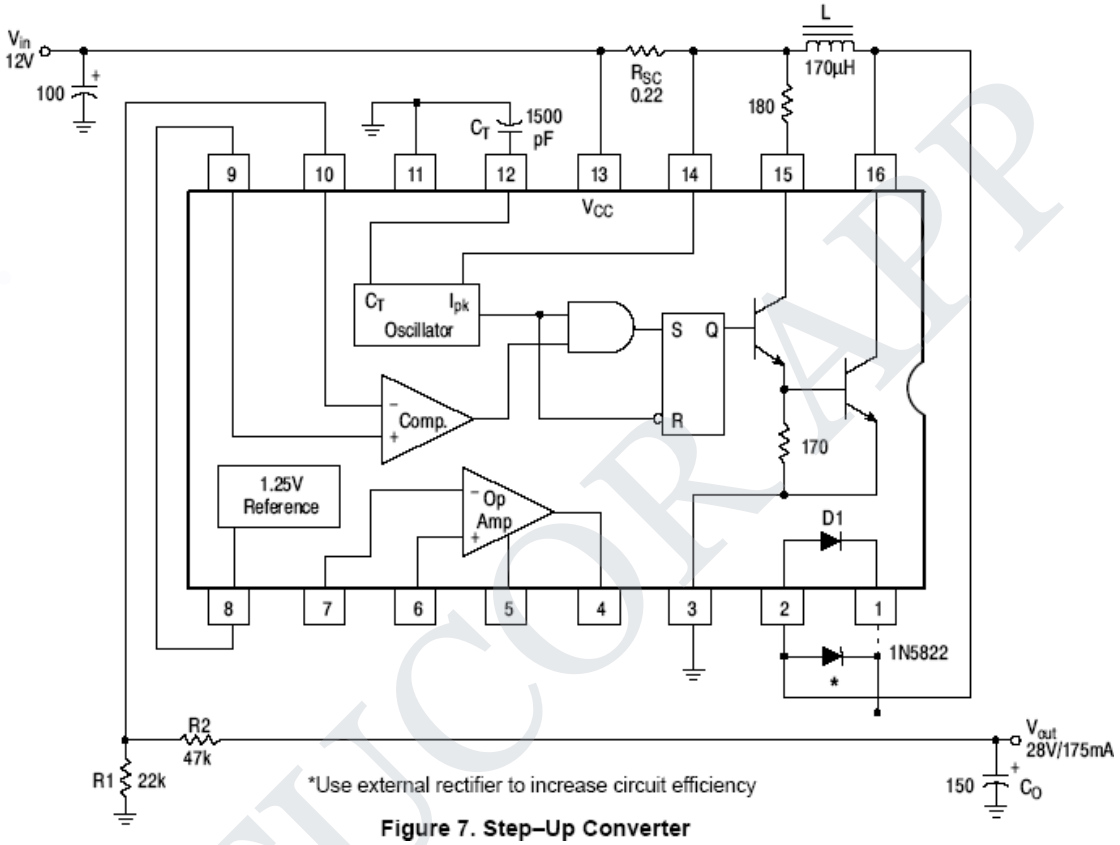
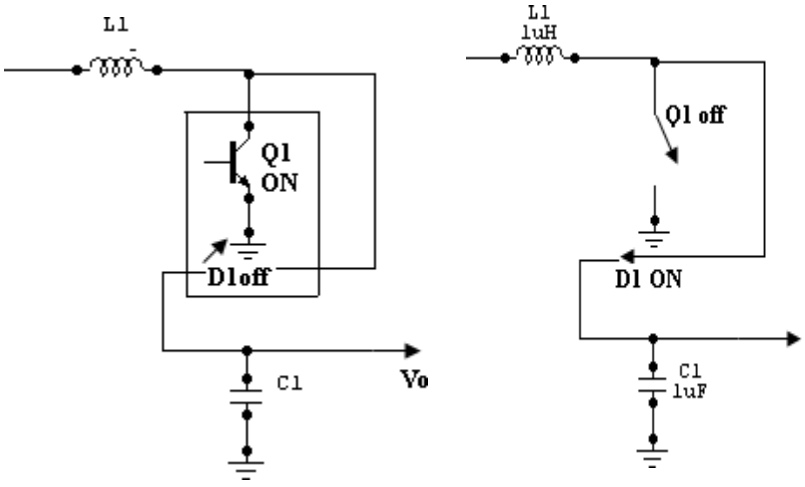


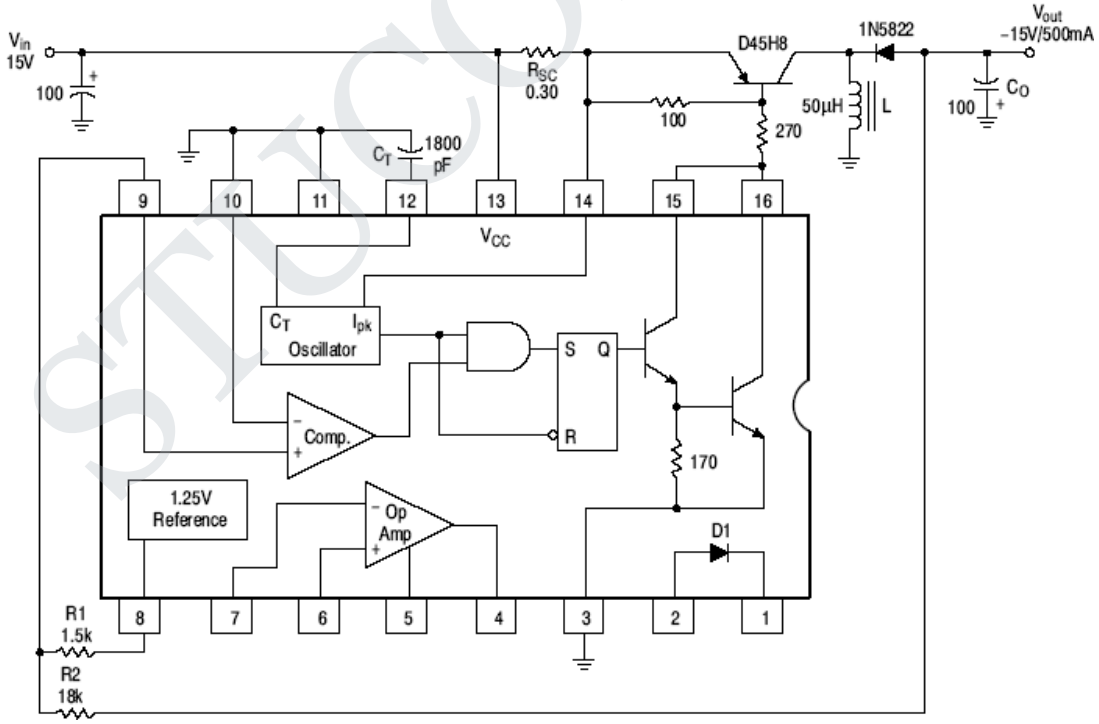
Figure 7. Step–Up Converter



With Q1 ON with Q1 oFF

(iii) Inverting Switching Regulator:

Inverting switching regulator converts a positive input voltage into a negative output voltage which is higher in magnitude.



POWER AUDIO AMPLIFIER IC LM380:

Features of LM380:

1. Internally fixed gain of 50 (34dB)
2. Output is automatically self centring to one half of the supply voltage.
3. Output is short circuit proof with internal thermal limiting.
4. Input stage allows the input to be ground referenced or ac coupled.
5. Wide supply voltage range (5 to 22V).
6. High peak current capability.
7. High impedence.
8. Low total harmonic distortion
9. Bandwidth of 100KHz at Pout = 2W & $R_L = 8\Omega$

Introduction:

Small signal amplifier are essentially voltage amplifier that supply their loads with larger amplifier signal voltage.

On the other hand , large signal or power amplifier supply a large signal current to current operated loads such as speakers & motors.

In audio applications, however, the amplifier called upon to deliver much higher current than that suppkied by general purpose op-amps. This means that loads such as speakers & motors requiring substantial currents cannot be driven directly by the output of general purpose opo-amps.

However there are two possible solutions,

- To use discrete or monolithic power transistors called power boosters at the output of the op-amp
- To use specialized ICs designed as power amplifiers.

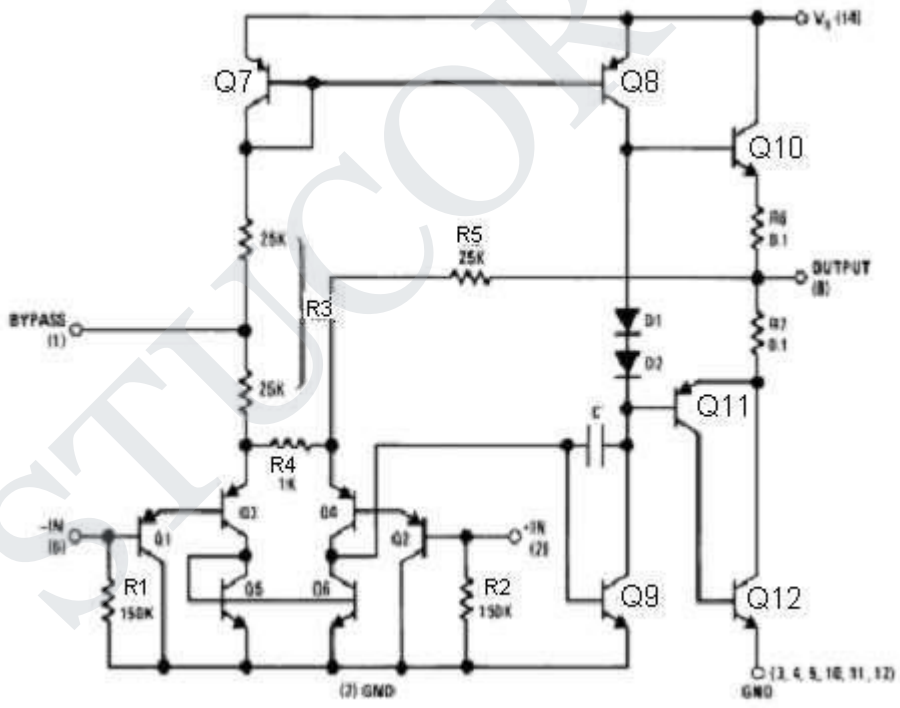


Fig : Functional block diagram of Audio Power Amplifier

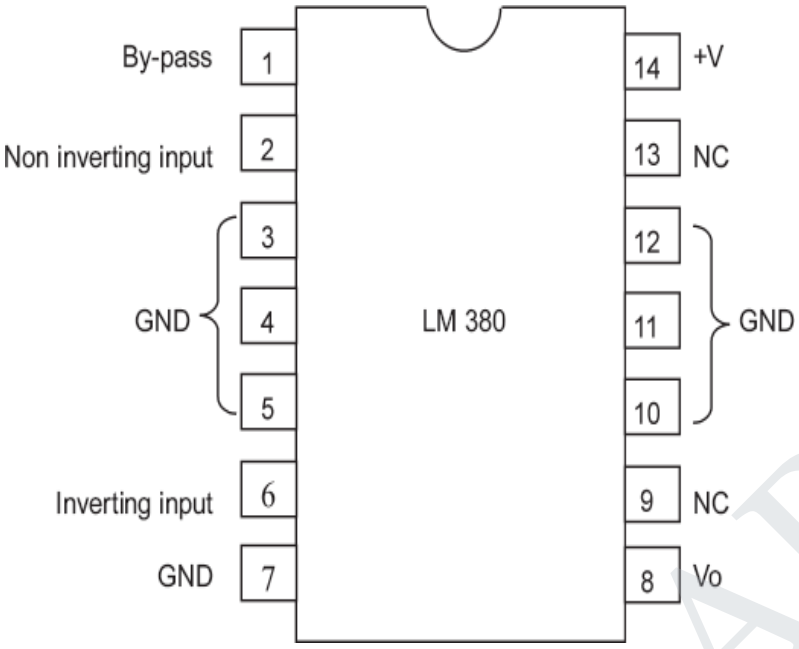


Fig: Pin diagram

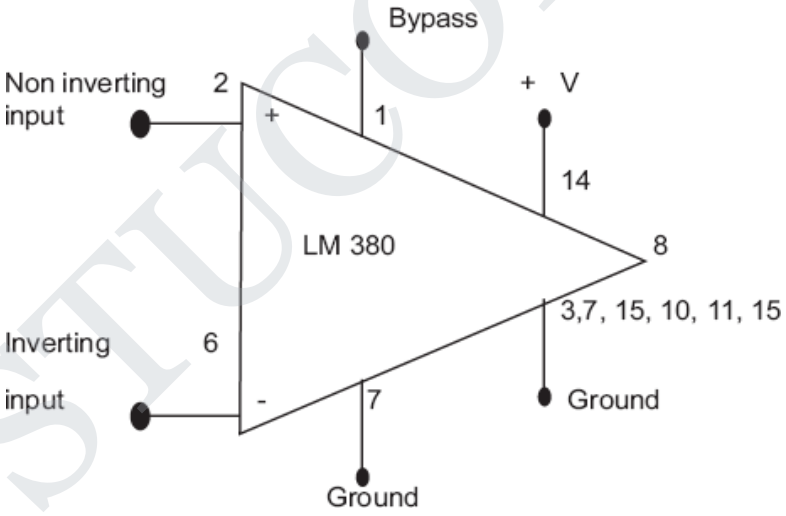


Fig : Block diagram

LM380 circuit description:

It is connected of 4 stages,

(i) PNP emitter follower

(ii) Different amplifier

(iii) Common emitter

(iv) Emitter follower

(i) PNP Emitter follower:

- The input stage is emitter follower composed of PNP transistors Q1 & Q2 which drives the PNP Q3-Q4 differential pair.
- The choice of PNP input transistors Q1 & Q2 allows the input to be referenced to ground i.e., the input can be direct coupled to either the inverting & non-inverting terminals of the amplifier.

(ii) Differential Amplifier:

- The current in the PNP differential pair Q3-Q4 is established by Q7, R3 & +V.
- The current mirror formed by transistor Q7, Q8 & associated resistors then establishes the collector current of Q9.
- Transistor Q5 & Q6 constitute of collector loads for the PNP differential pair.
- The output of the differential amplifier is taken at the junction of Q4 & Q6 transistors & is applied as an input to the common emitter voltage gain.

(iii) Common Emitter:

- Common Emitter amplifier stage is formed by transistor Q9 with D1, D2 & Q8 as a current source load.

- The capacitor C between the base & collector of Q9 provides internal compensation & helps to establish the upper cutoff frequency of 100 KHz.
- Since Q7 & Q8 form a current mirror, the current through D1 & D2 is approximately the same as the current through R3.
- D1 & D2 are temperature compensating diodes for transistors Q10 & Q11 in that D1 & D2 have the same characteristics as the base-emitter junctions of Q11. Therefore the current through Q10 & (Q11-Q12) is approximately equal to the current through diodes D1 & D2.

(iv) (Output stage) - Emitter follower:

- Emitter follower formed by NPN transistor Q10 & Q11. The combination of PNP transistor Q11 & NPN transistor Q12 has the power capability of an NPN transistors but the characteristics of a PNP transistor.
- The negative dc feedback applied through R5 balances the differential amplifier so that the dc output voltage is stabilized at +V/2;
- To decouple the input stage from the supply voltage +V, by pass capacitor in order of micro farad should be connected between the by pass terminal (pin 1) & ground (pin 7).
- The overall internal gain of the amplifier is fixed at 50. However gain can be increased by using positive feedback.

OPTOCOUPLERS/OPTOISOLATORS:

- Optocouplers or Optoisolators is a combination of light source & light detector in the same package.
- They are used to couple signal from one point to other optically, by providing a completer electric isolation between them. This kind of isolation is provided between a low power control circuit & high power output circuit, to protect the control circuit.
- Depending on the type of light source & detector used we can get a variety of optocouplers. They are as follows,

(i) LED – LDR optocoupler

(ii) LED – Photodiode optocoupler

(iii) LED – Phototransistor optocoupler

Characteristics of optocoupler:

(i) Current Transfer Ratio (CTR)

(ii) Isolation Voltage

(iii) Response Time

(iv) Common Mode Rejection

(i) Current Transfer Ratio:

It is defined as the ratio of output collector current (Ic) to the input forward current (If)

$$CTR = Ic/If * 100\%$$

Its value depends on the devices used as source & detector.

(ii) Isolation voltage between input & output:

It is the maximum voltage which can exist differentially between the input & output without affecting the electrical isolation voltage is specified in K Vrms with a relative humidity of 40 to 60%.

(iii) Response Time:

Response time indicates how fast an optocoupler can change its output state. Response time largely depends on the detector transistor, input current & load resistance.

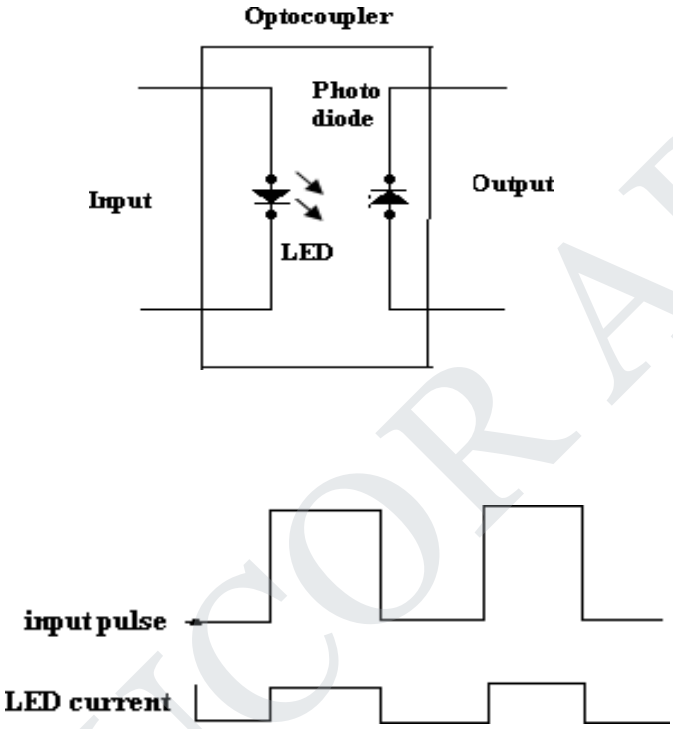
(iv) Common mode Rejection:

Eventhough the optocouplers are electrically isolated for dc & low frequency signals, an impulsive input signal (the signal which changes suddenly) can give rise to a displacement current

Ic= Cf*dv/dt. This current can flow between input & output due to the capacitance Cf existing between input & output. This allow the noise to appear in the output.

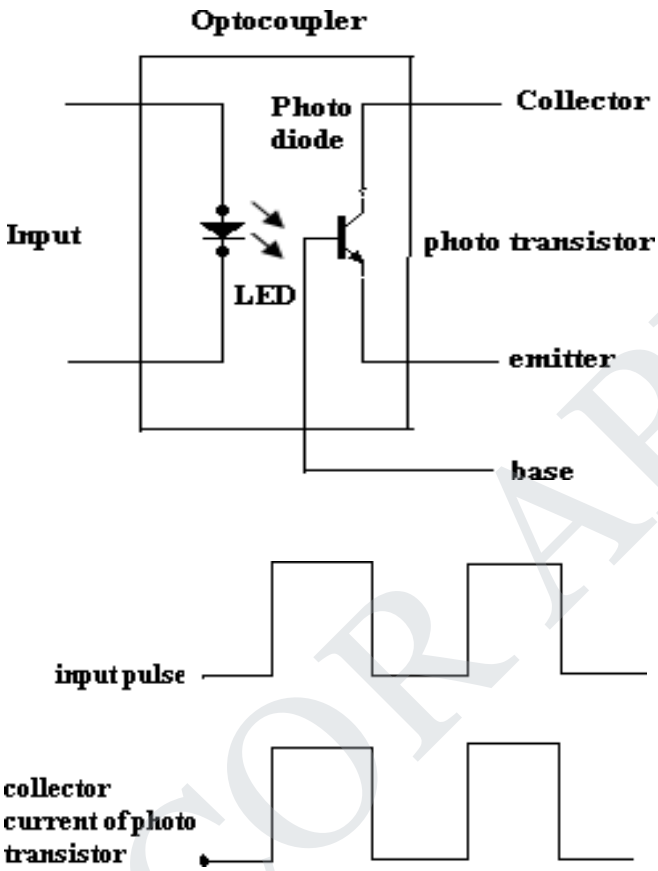
Types of optocoupler:

(i) LED – Photodiode optocoupler:



- LED photodiode shown in figure, here the infrared LED acts as a light source & photodiode is used as a detector.
- The advantage of using the photodiode is its high linearity. When the pulse at the input goes high, the LED turns ON. It emits light. This light is focused on the photodiode.
- In response to this light the photocurrent will start flowing though the photodiode. As soon as the input pulse reduces to zero, the LED turns OFF & the photocurrent through the photodiode reduces to zero. Thus the pulse at the input is coupled to the output side.

(ii) LED – Phototransistor Optocoupler:



- The LED phototransistor optocoupler shown in figure. An infrared LED acts as a light source and the phototransistor acts as a photo detector.
- This is the most popularly used optocoupler, because it does not need any additional amplification.
- When the pulse at the input goes high, the LED turns ON. The light emitted by the LED is focused on the CB junction of the phototransistor.

- In response to this light photocurrent starts flowing which acts as a base current for the phototransistor.
- The collector current of phototransistor starts flowing. As soon as the input pulse reduces to zero, the LED turns OFF & the collector current of phototransistor reduces to zero. Thus the pulse at the input is optically coupled to the output side.

Advantages of Optocoupler:

- Control circuits are well protected due to electrical isolation.
- Wideband signal transmission is possible.
- Due to unidirectional signal transfer, noise from the output side does not get coupled to the input side.
- Interfacing with logic circuits is easily possible.
- It is small size & light weight device.

Disadvantages:

- Slow speed.
- Possibility of signal coupling for high power signals.

Applications:

Optocouplers are used basically to isolate low power circuits from high power circuits.

- At the same time the control signals are coupled from the control circuits to the high power circuits.
- Some of such applications are,
  - (i) AC to DC converters used for DC motor speed control
  - (ii) High power choppers
  - (iii) High power inverters
- One of the most important applications of an optocoupler is to couple the base driving signals to a power transistor connected in a DC-DC chopper.

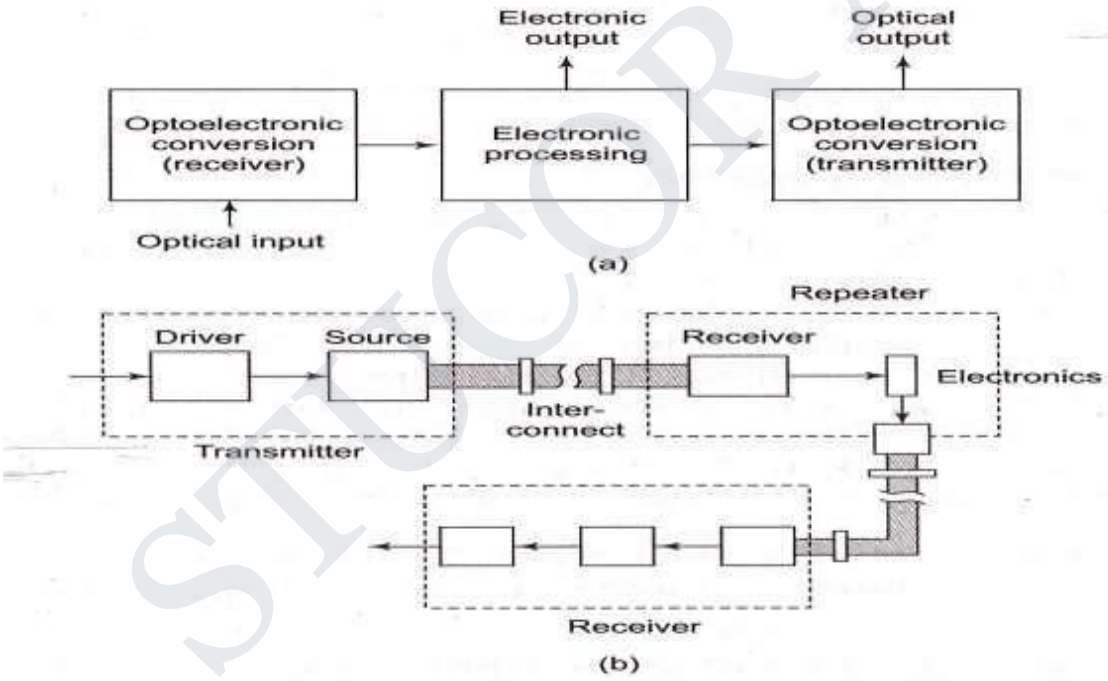
- Note that the input & output waveforms are 180º out of phase as the output is taken at the

collector of the phototransistor.

Optocoupler IC:

The optocouplers are available in the IC form MCT2E is the standard optocoupler IC which is used popularly in many electronic application.

- This input is applied between pin 1& pin 2. An infrared light emitting diode is connected between these pins.
- The infrared radiation from the LED gets focused on the internal phototransistor.
- The base of the phototransistor is generally left open. But sometimes a high value pull down resistance is connected from the Base to ground to improve the sensitivity.
- The block diagram shows the opto-electronic-integrated ciruit (OEIC) and the major components of a fiber-optic communication facility.



FUNCTION GENERATOR IC 8038:

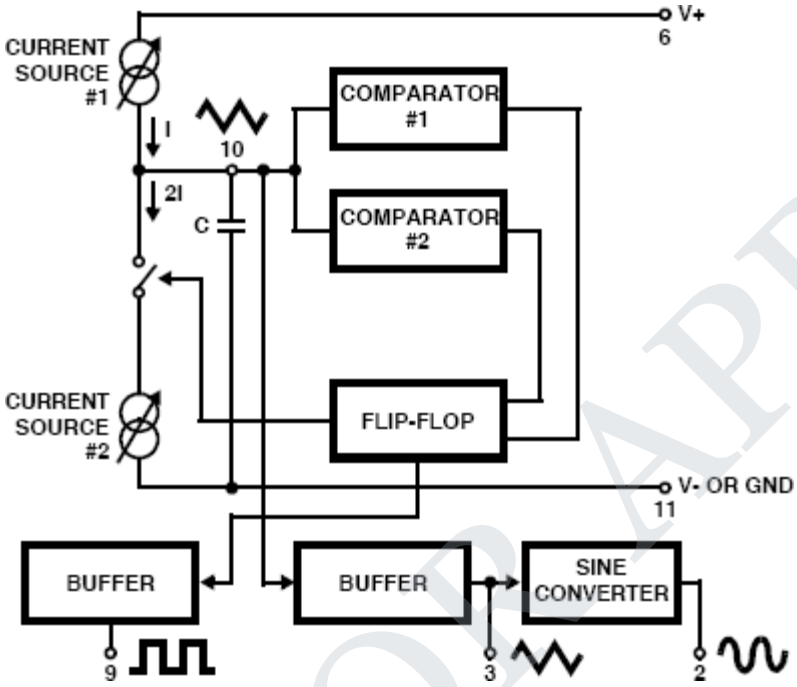
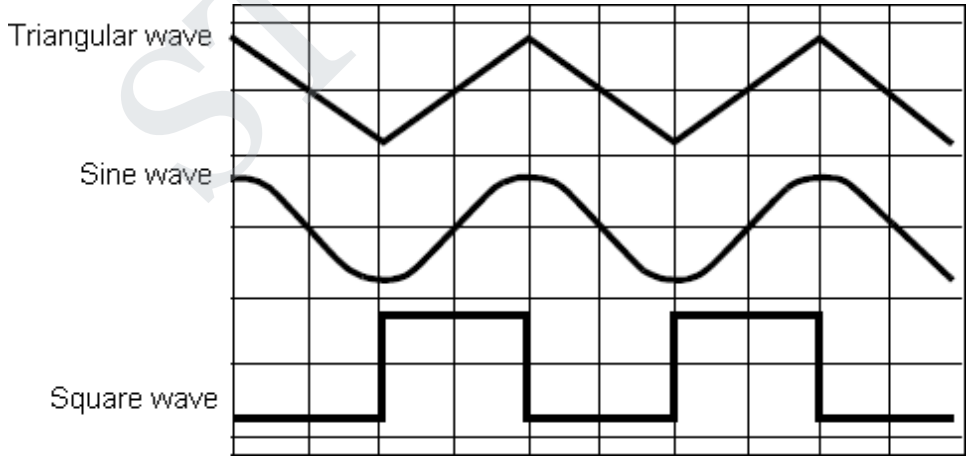


Fig: Functional block diagram of Function generator

Output Waveform:



It consists of two current sources, two comparators, two buffers, one FF and a sine wave converter.

Pin description:

Pin 1 & Pin 12: Sine wave adjusts:

The distortion in the sine wave output can be reduced by adjusting the 100KΩ pots connected between pin12 & pin11 and between pin 1 & 6.

Pin 2 Sine Wave Output:

Sine wave output is available at this pin. The amplitude of this sine wave is 0.22 Vcc.

Where ± 5V ≤ Vcc ≤ ± 15 V.

Pin 3 Triangular Wave output:

Triangular wave is available at this pin. The amplitude of the triangular wave is 0.33Vcc.

Where ± 5V ≤ Vcc ≤ ± 15 V.

Pin 4 & Pin 5 Duty cycle / Frequency adjust:

The symmetry of all the output wave forms & 50% duty cycle for the square wave output is adjusted by the external resistors connected from Vcc to pin 4. These external resistors & capacitors at pin 10 will decide the frequency of the output wave forms.

Pin 6 + Vcc:

Positive supply voltage the value of which is between 10 & 30V is applied to this pin.

Pin 7 : FM Bias:

This pin along with pin no8 is used to TEST the IC 8038.

Pin9 : Square Wave Output:

A square wave output is available at this pin. It is an open collector output so that this pin can be connected through the load to different power supply voltages. This arrangement is very

useful in making the square wave output.

Pin 10 : Timing Capacitors:

The external capacitor C connected to this pin will decide the output frequency along with the resistors connected to pin 4 & 5.

Pin 11 : -V_{EE} or Ground:

If a single polarity supply is to be used then this pin is connected to supply ground & if (±) supply voltages are to be used then (-) supply is connected to this pin.

Pin 13 & Pin 14: NC (No Connection)

Important features of IC 8038:

1. All the outputs are simultaneously available.
2. Frequency range : 0.001Hz to 500kHz
3. Low distortion in the output wave forms.
4. Low frequency drift due to change in temperature.
5. Easy to use.

Parameters:

(i) Frequency of the output wave form:

- The output frequency dependent on the values of resistors R1 & R2 along with the external capacitor C connected at pin 10.
- If $R_A = R_B = R$ & if R_C is adjusted for 50% duty cycle then

$$fo = \frac{0.3}{RC}; \quad R_A = R1,\ R_B = R3,\ R_C = R2$$

(ii) Duty cycle / Frequency Adjust : (Pin 4 & 5):

Duty cycle as well as the frequency of the output wave form can be adjusted by controlling the

values of external resistors at pin 4 & 5.

- The values of resistors R_A & R_B connected between Vcc * pin 4 & 5 respectively along with the capacitor connected at pin 10 decide the frequency of the wave form.
- The values of R_A & R_B should be in the range of 1kΩ to 1MΩ.

(iii) FM Bias:

- The FM Bias input (pin7) corresponds to the junction of resistors R1 & R2.
- The voltage Vin is the voltage between Vcc & pin8 and it decides the output frequency.
- The output frequency is proportional to Vin as given by the following expression

  For $R_A = R_B$ (50% duty cycle).

  $$fo = \frac{1.5Vin}{CRAVcc}$$; where C is the timing capacitor

- With pin 7 & 8 connected to each other the output frequency is given by

  $$fo = \frac{0.3}{RC}$$

  where $R = R_A = R_B$ for 50% duty cycle.

- This is because Vin = $\frac{R1}{R1 \square R2}$ Vcc

(iv) FM Sweep input (pin 8):

- This input should be connected to pin 7, if we want a constant output frequency.
- But if the output frequency is supposed to vary, then a variable dc voltage should be applied to this pin.
- The voltage between Vcc & pin 8 is called Vin and it decides the output frequency as,

$$fo = \frac{1.5\ Vin}{C\ R_A\ Vcc}$$

A potentiometer can be connected to this pin to obtain the required variable voltage required to change the output frequency.

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